On my honor, I have not given, nor received, nor witnessed any unauthorized assistance on this work.

Print name and sign: _____

Question:	1	2	3	4	5	Total
Points:	2	1	12	6	9	30
Score:						

Consider a system with the following specs:

- 128 byte pages
- 1K (1024 byte) virtual address space
- 512 bytes physical memory

1. (2 points) How many bits do we need to represent a virtual address and a physical address?

2. (1 point) Why do we need 3 bits to represent the virtual page number (VPN) and 2 bits to represent the physical frame number (PFN)?

3. Our system has a linear page table which stores an 8-bit PTE in the form:
   `| 1 present bit | 3 RWX bits | 1 valid bit | 1 dirty bit | 2 bit PFN |`
   The page table currently contains:
   `0xCB`
   `0x7E`
   `0x43`
   `0x7D`
   `0xC9`
   `0xEA`
   `0x6C`
   `0xD8`

   Translate the following virtual addresses to physical addresses. Give your answer as either hex or binary.

(a) (4 points) `0x280`

(b) (4 points) `0x05E`

(c) (4 points) `0x3C9`

4. For each of the following virtual addresses, state whether the page is currently in physical memory or in disk swap space. If the page is in physical memory, give its PFN.

(a) (3 points) `0x1EC`

(b) (3 points) `0x235`

5. The TLB has the following contents in each entry: a 3-bit VPN, a 2-bit PFN, and an 3-bit PID field (in that order). This TLB only has four entries, and they look like this:

`0x68`
`0x71`
`0xE0`
`0x9A`

(a) (3 points) If process 0 generates a virtual address with a VPN of 3, is this a TLB hit or miss?

(b) (3 points) If process 2 generates a virtual address with a VPN of 5, is this a TLB hit or miss?

(c) (2 points) Describe what happens when there is a TLB miss in a situation like this (where the TLB is full).

(d) (1 point) Explain why paging-based systems need a TLB to store frequently used translations.