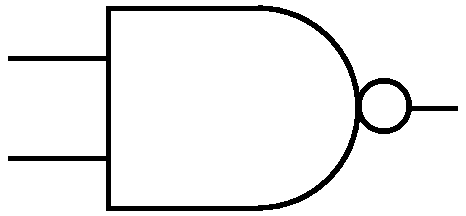
# CMOS 2 Input NAND Gate cmos2nandx



IN1

OUT

IN2

*Description:*

This is an Extrinsic Super Element which models a 2 Input CMOS NAND gate utilizing the EKV model.

*Form:* cmos2nandx:<instance name> *n1 n2 n3 n4 n5*<parameter list>

*n1*is the high voltage source (Vdd) terminal,

*n2*is the first input terminal,

*n3*is the second input terminal,

*n4*  is the output terminal,

*n5* is the ground or Vss terminal

*Parameters:*

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Type | Default Value | Required |
| ln: Channel Length of NMOS (m) | TR\_DOUBLE | 1.0e-6 | No |
| wn: Channel Width of NMOS (m) | TR\_DOUBLE | 1.0e-6 | No |
| lp: Channel Length of PMOS (m) | TR\_DOUBLE | 1.0e-6 | No |
| wp: Channel Width of PMOS (m) | TR\_DOUBLE | 1.0e-6 | No |

*Example:*

cmos2nandx:nand 1 2 3 4 0

*Notes:*

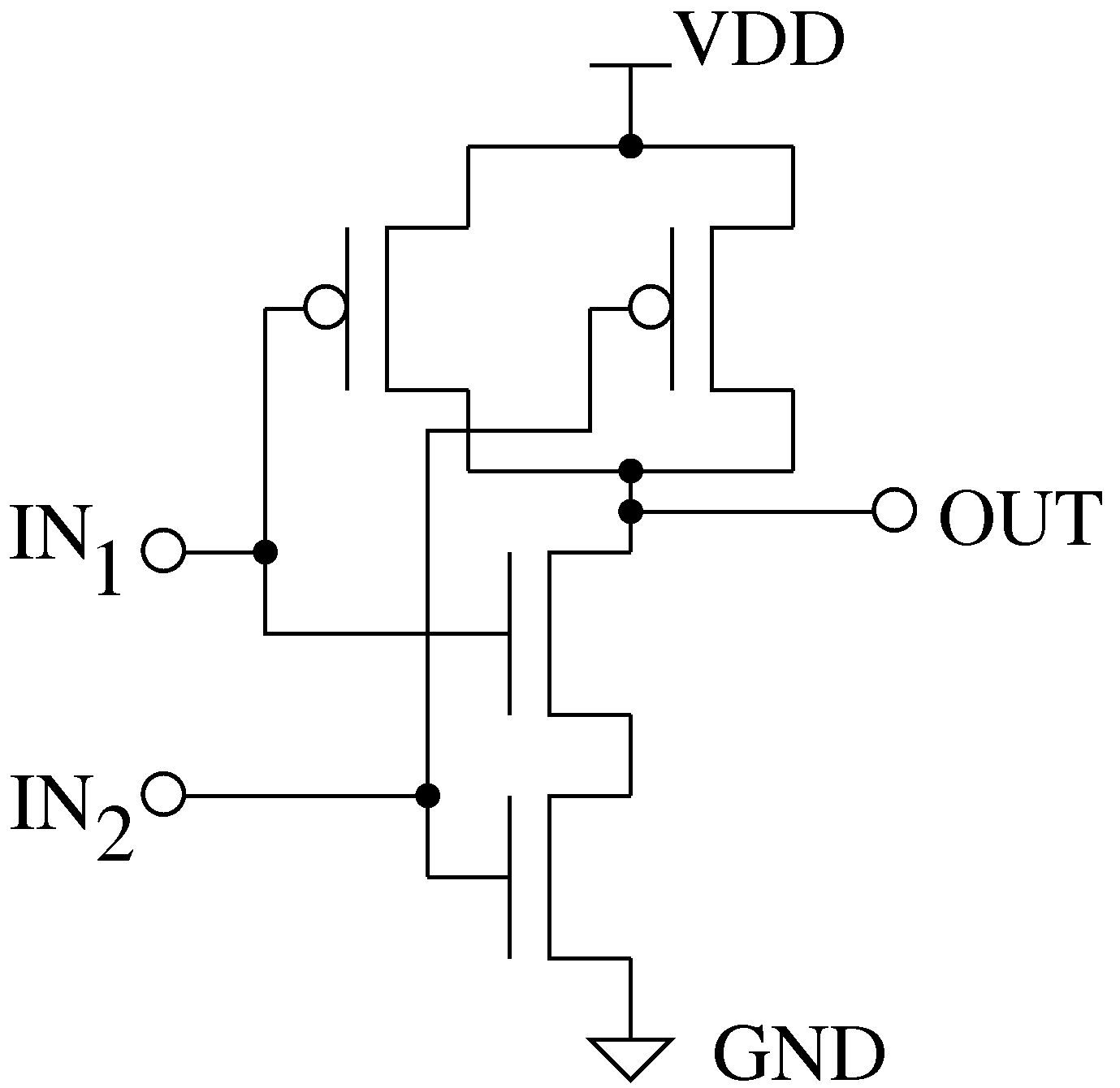
This implementation of cmos nand gate is based on EKV 2.6 [1] mosfet model.

*Known Bugs:*

No known bugs.

**Implementation Details:**

This element is implemented as a fREEDA **Extrinsic Super Element** based on EKV 2.6 MOSFET model [1]. The element has **12 state variables: 3 corresponding to each transistor.** Following is the schematic and truth table of 2-input nand gate:



|  |  |  |
| --- | --- | --- |
| **IN1** | **IN2** | **OUT** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**References:**

**[1]** The EKV 2.6 Documentation: <http://legwww.epfl.ch/ekv/pdf/ekv_v262.pdf>

***Sample Netlist****:*

* **DC Analysis**

The following netlist plots the output voltage of the CMOS gate for an input voltage range of 0 ~ 5V for Vin1 and constant Vin2 = 5V.

\* CMOS Nand DC Analysis

\*\*\*This netlist is for DC Analysis of 2 input Cmos Nand Gate \*\*\*

.dc sweep="vsource:Vin1" start=0 stop=5 step=0.01

\*\*\* DC Sweep First input

vsource:Vin1 22 0

\*\*\* Tie Second input to Vdd

vsource:Vin2 33 0 vdc=5

\*\*\* Vdd connection

vsource:Vdd 1 0 vdc=5

\*\*\*Nand Instantiation

cmos2nandx:nand 1 2 3 4 0

\*\* Source Resistance and Capacitance

r:in2 22 2 r=10

r:in3 33 3 r=10

c:in2 2 0 c=1e-12

c:in3 3 0 c=1e-12

\*\*\*\*Output Resistance and Capacitance

r:R 4 0 r=1000000

c:C 4 0 c=1e-12

.options gnuplot

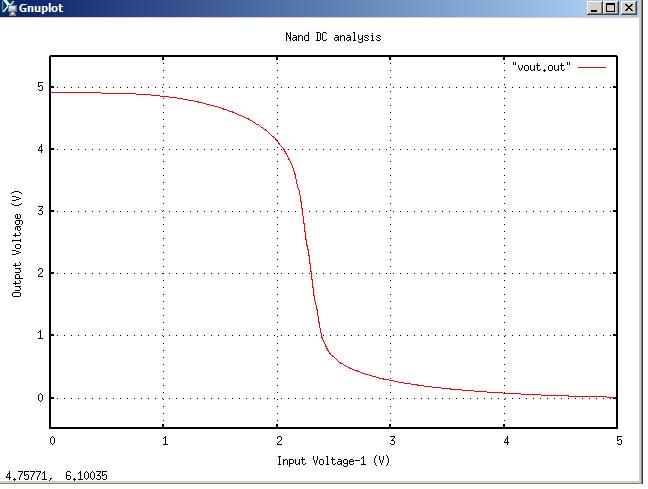
.out plot term 4 vt in "vout.out"

.out plot term 22 vt in "vin1.out"

.out plot term 33 vt in "vin2.out"

.end

*Validation:*

The output graph from the above netlist is shown below:

* **Transient Analysis**

\* CMOS Nand Transient Analysis

\*\*\* This netlist is for Transient analysis of Cmos 2 input Nand Gate\*\*\*

.tran2 tstop=8e-6 tstep=1e-9 out\_steps=1

vpulse:Vin2 22 0 v1=0 v2=5 td=1e-6 per=4e-6 pw=2e-6 tr=0.002e-6 tf=0.002e-6

vpulse:Vin3 33 0 v1=0 v2=5 per=4e-6 pw=2e-6 tr=0.002e-6 tf=0.002e-6

\*\*\*\* Vdd connection

vsource:Vdd 1 0 vdc=5

\*\*\*\*\* Nand instantiation

cmos2nandx:nand 1 2 3 4 0

\*\* Source Resistance and Capacitance

r:in2 22 2 r=10

r:in3 33 3 r=10

c:in2 2 0 c=1e-12

c:in3 3 0 c=1e-12

\*\*\* Load Resistance and Capacitance

r:R 4 0 r=1000000

c:C 4 0 c=1e-12

.options gnuplot

.out plot term 4 vt in "vout.out"

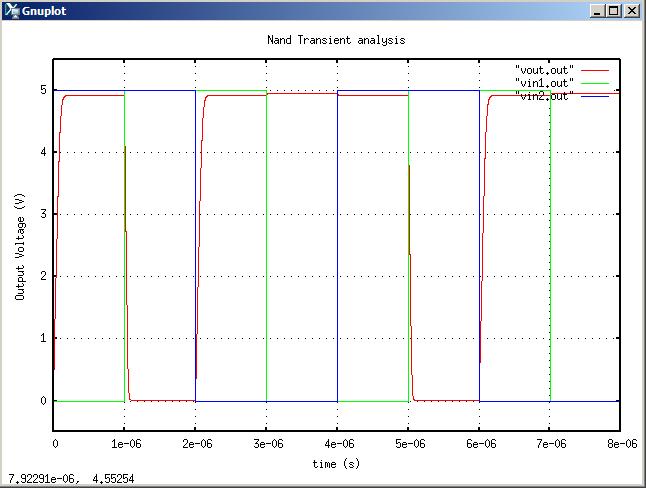
.out plot term 22 vt in "vin1.out"

.out plot term 33 vt in "vin2.out"

.end

*Validation:*

The output graph from the above netlist is shown below:



*Version:* 2009.04.30

*Credits:*

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