"Signal to High Prio Thread" benchmark measurements March 11, 2022

Table 1. Armv7a (platform Sabre). Pattern 10/100, MCS kernel

	Min	Max	Mean	Std Dev	Min	Max	Mean	Std Dev				
10/100	Late processing				Lat	e process	sing w/ de	elay	Early processing			
Run #1	924	1492	1095	158.32	902	956	927	11.90	899	959	928	15.05
Run #2	914	1492	1086	162.27	898	958	928	13.27	899	969	925	11.98
Run #3	916	1508	1071	162.75	902	964	928	12.39	903	977	928	12.31
Run #4	912	1486	1105	153.16	900	960	925	13.36	907	963	929	12.43
Run #5	914	1492	1087	159.10	914	980	942	14.14	902	970	929	14.86
Run #6	934	1504	1114	158.68	914	976	940	11.73	899	969	928	13.17
Run #7	918	1492	1084	159.04	900	966	926	14.22	900	967	928	12.67
Run #8	930	1504	1106	157.46	900	968	926	14.17	913	979	939	13.43
Run #9	914	1492	1082	161.01	899	971	929	14.01	901	969	928	13.61
Run #10	932	1506	1112	152.09	914	982	939	13.69	899	959	928	12.99
	,	'			S	tats for th	e column	s			'	
Min	912	1486	1071	152	898	956	925	12	899	959	925	12
Max	934	1508	1114	163	914	982	942	14	913	979	939	15
Mean	921	1497	1094		904	968	931		902	968	929	

Table 2. Armv7a (platform Sabre). Pattern 10/100, Traditional kernel

	Min	Max	Mean	Std Dev	Min	Max	Mean	Std Dev				
10/100	Late processing				Lat	e process	sing w/ de	elay	Early processing			
Run #1	709	1770	933	194.94	698	764	730	15.15	695	770	730	14.75
Run #2	714	1785	942	190.60	693	761	732	15.52	699	765	731	13.83
Run #3	710	1368	936	174.62	689	763	730	15.62	696	769	730	14.12
Run #4	709	1362	926	171.55	683	760	734	15.38	697	769	733	15.73
Run #5	707	1363	928	171.01	697	764	729	15.01	697	769	731	13.95
Run #6	718	1780	941	192.86	686	752	728	15.53	697	769	731	13.90
Run #7	712	1816	926	196.51	693	761	730	16.42	704	761	729	14.28
Run #8	712	1364	924	175.58	688	764	728	16.06	689	770	730	15.19
Run #9	716	1765	926	190.62	696	769	730	14.15	699	764	732	13.51
Run #10	710	1364	926	177.76	688	769	731	16.42	684	763	728	15.35
	,	'			S	tats for th	e column	s	,	'	,	
Min	707	1362	924	171	683	752	728	14	684	761	728	14
Max	718	1816	942	197	698	769	734	16	704	770	733	16
Mean	712	1574	931		691	763	730		696	767	731	

Table 3. Armv8a (platform Tx1a). Pattern 10/100, MCS kernel

	Min	Max	Mean	Std Dev	Min	Max	Mean	Std Dev				
10/100		Late pro	cessing		La	te process	sing w/ de	elay	Early processing			
Run #1	688	772	699	13.57	683	690	685	1.80	664	712	664	5.85
Run #2	688	832	699	17.44	685	692	687	1.53	659	710	664	5.66
Run #3	688	769	695	8.65	689	737	690	4.94	665	762	666	10.74
Run #4	688	811	698	16.31	685	689	685	0.59	665	752	666	11.78
Run #5	685	749	692	8.40	679	686	681	1.97	665	736	665	7.63
Run #6	688	755	696	11.18	679	714	708	3.44	665	713	665	5.09
Run #7	691	898	699	21.39	685	692	687	1.78	665	692	665	3.70
Run #8	688	808	696	17.73	689	696	691	1.85	665	713	665	5.85
Run #9	691	738	698	6.77	679	686	681	1.53	665	712	665	5.71
Run #10	680	720	686	5.15	689	696	691	1.76	665	712	665	5.71
	-			-	S	tats for th	e column	s			'	
Min	680	720	686	5	679	686	681	1	659	692	664	4
Max	691	898	699	21	689	737	708	5	665	762	666	12
Mean	688	785	696		684	698	689		664	721	665	

Table 4. Armv8a (platform Tx1a). Pattern 10/100, Traditional kernel

	Min	Max	Mean	Std Dev	Min	Max	Mean	Std Dev				
10/100	Late processing				Lat	e process	sing w/ de	elay	Early processing			
Run #1	589	702	606	19.82	619	628	622	2.48	604	661	604	6.67
Run #2	589	705	606	19.22	619	628	622	2.40	622	683	623	7.04
Run #3	589	709	605	18.11	619	628	622	2.41	612	674	623	9.36
Run #4	589	687	606	18.62	619	628	622	2.50	614	673	614	7.16
Run #5	589	705	606	19.38	619	628	622	2.38	620	721	621	10.61
Run #6	589	692	608	22.49	619	628	622	2.52	610	636	616	2.70
Run #7	589	728	607	24.48	619	628	622	2.44	620	737	621	12.25
Run #8	589	700	605	18.85	619	628	622	2.39	616	639	616	3.06
Run #9	589	718	606	23.65	619	628	622	2.40	614	682	615	9.03
Run #10	589	791	610	32.69	619	627	622	2.31	620	716	622	11.97
		'			S	tats for th	e column	s			-	
Min	589	687	605	18	619	627	622	2	604	636	604	3
Max	589	791	610	33	619	628	622	3	622	737	623	12
Mean	589	714	607		619	628	622		615	682	618	