xCORE-200 explorerKIT Hardware Manual

IN THIS DOCUMENT

xCORE-200 explorerKIT is an evaluation board for the configurable xCORE-200 multicore microcontroller products from XMOS. It's easy to use and provides lots of advanced features on a small, extremely low cost platform.

xCORE lets you software-configure the interfaces that you need for your system; so with xCORE-200 explorerKIT you can configure the board to match your exact requirements. The xCORE-200 multicore microcontroller has sixteen 32bit logical cores that deliver up to 2000MIPs completely deterministically, making xCORE-200 explorerKIT an ideal platform for functions ranging from robotics and motion control to networking and digital audio.

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1 Features

A block diagram of the xCORE-200 explorerKIT is shown below:

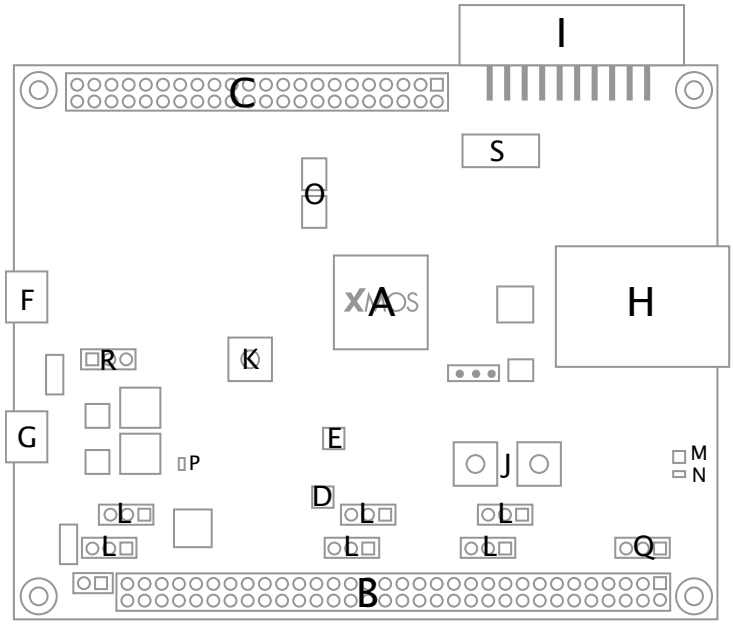

Figure 1: xCORE-200 explorerKIT block diagram

It includes the following features:

- A: xCORE-200 (XEF216-512-TQ128) Multicore Microcontroller device
- B: 32 GPIO connections from core 1, arranged on a 0.1" grid
- C: 21 GPIO connections from core 1, arranged on a 0.1" grid
- D: A BMG160 3-axis gyroscope sensor
- E: An FXOS8700CQ Digital Sensor - 3D Accelerometer (±2g/±4g/±8g) + 3D Magnetometer
- F: A micro USB connector for connection to a USB device
- G: A micro USB connector for connection to a power supply
- H: An RGMII connector for connection to a 10/100/1000Mbps ethernet network
- I: An xSYS connector for connection to an xTAG debug adapter
- J: Two general purpose push-button switches
- K: A reset switch

- L: Six servo connections
- M: A general purpose green lED
- N: A general purpose RGB LED
- O: A QSPI flash
- P: A green 3.3v power-good LED
- Q, R: Two power supply headers
- S: 24MHz Oscillator

2 xCORE Multicore Microcontroller Device

xCORE-200 explorerKIT is based on a two-tile xCORE-200 device (XEF216-512-TQ128). Each tile is user-programmable, providing eight logical cores with a total of up to 1000 MIPS compute. A total of 53 general-purpose digital I/O have been brought out to header pins, providing tremendous flexibility for connecting peripherals to the xCORE-200 explorerKIT board.

For information on xCORE-200 tiles and cores see the xCORE-200 Architecture Overview[1].

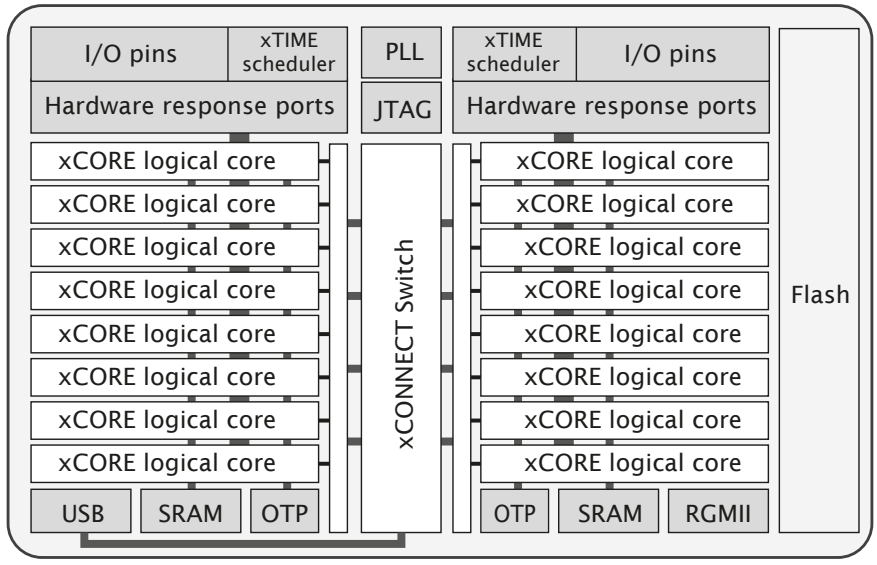

Figure 2: xCORE-200 XEF216-512-TQ128 device

[1] http://www.xmos.com/published/xcore-architecture

3 GPIO headers (J1 & J3)

J1 and J3 provide a rich set of IO that can be readily connected to off-board components.

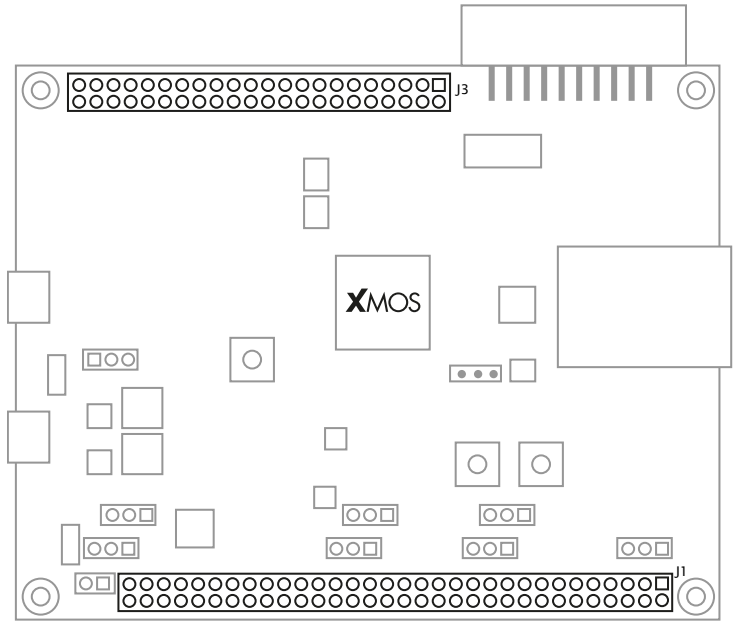

Figure 3: GPIO connectors

The xCORE ports are mapped to the GPIO connector pins as shown in Figure 4 and Figure 5:

Notes:

1 - X0D31 is connected to the red terminal of the general purpose RGB LED (N). This GPIO may be used for other purposes.

2 - X0D30 is connected to the green terminal of the general purpose RGB LED (N). This GPIO may be used for other purposes.

3 - X0D29 is connected to the blue terminal of the general purpose RGB LED (N). This GPIO may be used for other purposes.

4 - X0D28 is connected to the general purpose green LED (M). This GPIO may be used for other purposes.

5 - X0D27 is connected to BUTTON B (SW2). This GPIO may be used for other purposes, but care must be taken.

6 - X0D26 is connected to BUTTON A (SW1). This GPIO may be used for other purposes, but care must be taken.

Signal	GPIO J1	Signal	GPIO J1
X0D31[1]	1	GND	2
X0D30[2]	3	GND	4
X0D29[3]	5	GND	6
X0D28[4]	7	GND	8
X0D33	9	GND	10
X0D32	11	GND	12
X0D27[5]	13	GND	14
X0D26[6]	15	GND	16
X0D35	17	GND	18
X0D34	19	GND	20
X0D25	21	GND	22
X0D24	23	GND	24
X0D19	25	GND	26
X0D18	27	GND	28
X0D17	29	GND	30
X0D16	31	GND	32
X0D23	33	GND	34
X0D22	35	GND	36
X0D13[7]	37	GND	38
X0D12[8]	39	GND	40
X0D21	41	GND	42
X0D20	43	GND	44
X0D15	45	GND	46
X0D14	47	GND	48
X0D09	49	GND	50
X0D08	51	GND	52
X0D03	53	GND	54
X0D02	55	GND	56
X0D39	57	GND	58
X0D38	59	GND	60
X0D37	61	GND	62
X0D36	63	GND	64

Figure 4: GPIO J1 connector .. :class: horizontal-borders

7 - X0D13 is connected to clock (SDA) line of the I2C bus connected to the on-board sensors. A 0R link is provided (R52), so that this connection can be isolated if necessary.

8 - X0D12 is connected to clock (SCL) line of the I2C bus connected to the on-board sensors. A 0R link is provided (R49), so that this connection can be isolated if necessary.

Signal	GPIO J3	Signal	GPIO J3
GND	1	X1D35	2
GND	3	X1D38	4
GND	5	X1D39	6
GND	7	X1D16	8
GND	9	X1D17	10
GND	11	X1D18	12
GND	13	X1D19	14
GND	15	X1D14	16
GND	17	X1D15	18
GND	19	X1D20	20
GND	21	X1D21	22
GND	23	X1D04	24
GND	25	X1D05	26
GND	27	X1D06	28
GND	29	X1D07	30
GND	31	X1D02	32
GND	33	X1D03	34
GND	35	X1D08	36
GND	37	X1D09	38
GND	39	X1D00	40
GND	41	X1D01	42
GND	43	GND	44

Figure 5: GPIO J3 connector

4 Gyroscope and accelerometer

The xCORE-200 explorerKIT provides a BMG160 3-axis gyroscope sensor and an FXOS8700CQ Digital Sensor (3D Accelerometer (±2g/±4g/±8g) + 3D Magnetometer). These are connected via an I2C interface as described in Figure 7.

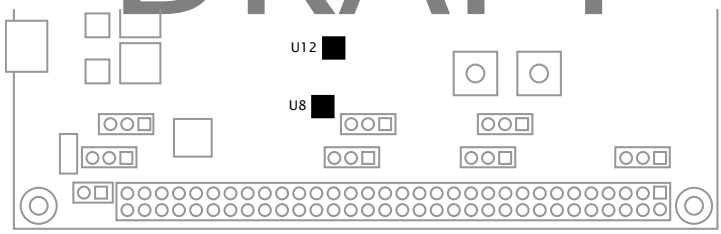

Figure 6: Gyroscope and Accelerometer

Pin	I2C signal
X0D12	SCL
X0D13	SDA

Figure 7: I2C sensor interface

5 USB connections

Two micro-USB (B-type) connections are provided:

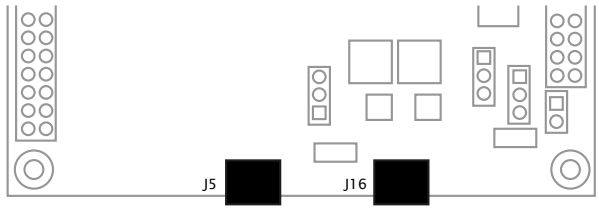

Figure 8: USB connectors

Note that J16 must be connected at all times, to provide power to the xCORE-200 explorerKIT. J5 should also be connected when developing USB applications.

6 RGMII connection

An RJ45 connector is available for the development of 10/100/1000 Mbps ethernet applications.

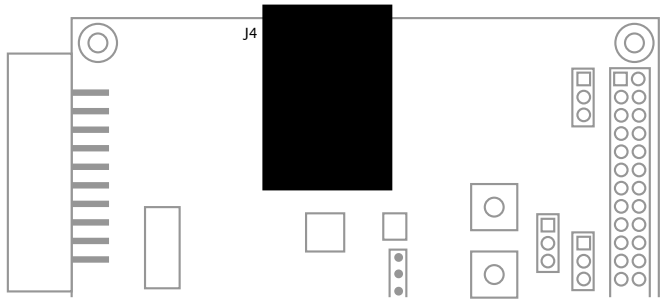

Figure 9: 10/100/1000 Ethernet connector

7 xSYS connector

The xSYS connector is provided to interface to an xTAG debug adapter. The xTAG debug adapter allows the xTIMEcomposer tools to interrogate the application running on the xCORE-200 device using the XMOS debugger and the xSCOPE library which provides non-intrusive program instrumentation.

8 General purpose push-button switches

Two general purpose push-button switches are provided as shown below. When depressed, the push-buttons create a connection from the IO to GND. Care must be taken to ensure that this does not cause undesirable behaviour on the xCORE-200 or other components connected through the GPIO headers:

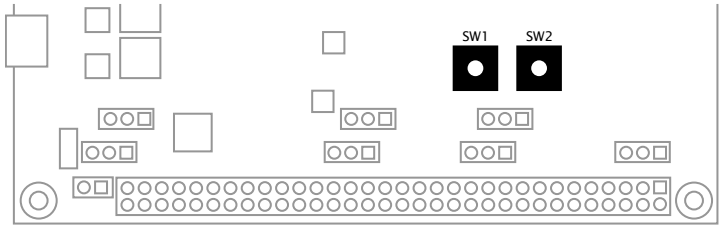

Figure 10: General purpose push-button switches

Each push-button switch is connected to a different IO on the xCORE-200 device as described in Figure 11:

Figure 11: General purpose push-button switches

Pin	BUTTON
X0D26	SW1
X0D27	SW2

9 Servo connectors

Up to six servos can be connected to the xCORE-200 explorerKIT using the header sockets provided. Note that it is up to the user to ensure that sufficient supply power is available to drive the servos.

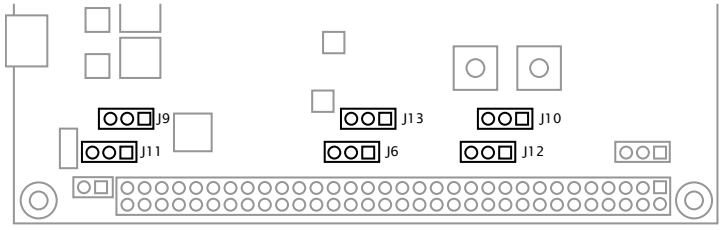

Figure 12: Servo connectors

Connector	Pin 1	Pin 2	Pin 3
J8	X0D22	+5V	GND
J9	X0D37	+5V	GND
J10	X0D35	+5V	GND
J11	X0D36	+5V	GND
J12	X0D34	+5V	GND
J13	X0D23	+5V	GND

Figure 13: GPIO servo connector

10 User LEDs

xCORE-200 explorerKIT provides two LEDs, a green LED and an RGD LED arranged as shown below:

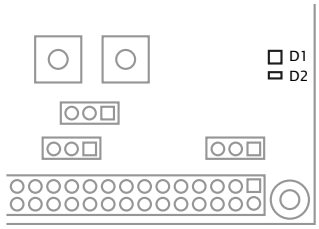

Figure 14: User LEDs

The green LED and each colour terminal of the RGB LED are connected to a different pin as described in Figure 15:

Pin	LED
X0D28	Green
X0D29	RGB (blue term)
X0D30	RGB (green term)
X0D31	RGB (red term)

Figure 15: User LEDs

11 QSPI Flash

xCORE-200 explorerKIT provides 1Mbytes of Quad Serial Peripheral Interface (QSPI) FLASH memory, which is interfaced by the GPIO connections shown in Figure 16:

The xTIMEcomposer tools include the xFLASH utility for programming compiled programs into the flash memory. xCORE-200 explorerKIT designs may also access the FLASH memory at run-time by interfacing with the above pins.

Pin	QSPI connection
X0D01	CE_n
X0D04	IO0
X0D05	IO1
X0D06	IO2
X0D07	IO3
X0D10	SPI_CLK

Figure 16: QSPI Flash

12 24MHz Crystal Oscillator

The xCORE-200 explorerKIT board is clocked at 24MHz by a crystal oscillator. Each tile is clocked at 500 MIPS, and all I/O ports are 100MHz.

13 Power connector

xCORE-200 explorerKIT requires a 5V power source input via the micro-USB cable.

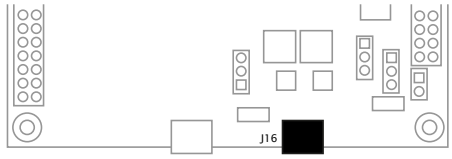

Figure 17: Power connection via micro-USB

The voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components. Additional or alternative power sources may use the power headers provided as shown in Figure 18:

Connector	Pin 1	Pin 2	Pin 3
J14	+5V	+3.3V	GND
J15	+5V	+3.3V	GND

Figure 18: Power connectors

See the *Operating requirements* section §14 for further information.

14 Operating requirements

A USB 2.0 high-speed compliant cable of less than 3m in length should be used when operating the xCORE-200 explorerKIT. XMOS cannot guarantee correct operation of the xCORE-200 explorerKIT should any other cable be used.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the xCORE-200 explorerKIT with appropriate ESD precautions in place.

15 Dimensions

The xCORE-200 explorerKIT dimensions are 105 x 80mm. The mounting holes are 2mm in diameter.

16 xCORE-200 explorerKIT Portmap

The table below provides a full description of the port-pin mappings described throughout this document.

Pin	link	1-bit	4-bit	8-bit	16-bit	32-bit	GPIO	SPI	BUTTON	LED	uplink	RGMII
X0D00		$1A^{0}$						MISO				
X0D01	D^{2} out	$1B^{0}$						CS				
X0D02			$4A^{0}$	$8A^{0}$	$16A^{0}$	$32A^{20}$	$J1^{55}$					
X0D03			$4A^{1}$	$8A^{1}$	$16A^{1}$	$32A^{21}$	$J1^{53}$					
X0D04			$4B^{0}$	$8A^{2}$	$16A^{2}$	$32A^{22}$		D0				
X0D05			$4B^{1}$	$8A^{3}$	$16A^{3}$	$32A^{23}$		D1				
X0D06			$4B^{2}$	$8A^{4}$	$16A^{4}$	$32A^{24}$		D2				
X0D07			$4B^{3}$	$8A^{5}$	$16A^{5}$	$32A^{25}$		D3				
X0D08			$4A^{2}$	$8A^{6}$	$16A^{6}$	$32A^{26}$	$J1^{51}$					
X0D09			$4A^{3}$	$8A^{7}$	$16A^{7}$	$32A^{27}$	$J1^{49}$					
X0D10	D^{3} out	$1C^{0}$						CLK				
X0D11		$1D^{0}$						MOSI				
X0D12		$1E^{0}$					$J1^{39}$					
X0D13		$1F^{0}$					$J1^{37}$					
X0D14			$4C^{0}$	$8B^{0}$	$16A^{8}$	$32A^{28}$	$J1^{47}$					
X0D15			$4C^{1}$	$8B^{1}$	$16A^{9}$	$32A^{29}$	$J1^{45}$					
X0D16	E^{4} in		$4D^{0}$	$8B^{2}$	$16A^{10}$		$J1^{31}$					
X0D17	E^{3} in		$4D^{1}$	$8B^{3}$	$16A^{11}$		$J1^{29}$					
X0D18	E^{2} in		$4D^{2}$	$8B^{4}$	$16A^{12}$		$J1^{27}$					
X0D19	E^{1} in		$4D^{3}$	$8B^{5}$	$16A^{13}$		$J1^{25}$					
X0D20			$4C^{2}$	$8B^{6}$	$16A^{14}$	$32A^{30}$	$J1^{43}$					
X0D21			$4C^{3}$	$8B^{7}$	$16A^{15}$	$32A^{31}$	$J1^{41}$					
X0D22		$1G^{0}$					$J1^{35}$					
X0D23		$1H^{0}$					$J1^{33}$					
X0D24	H^{0} in	$1I^{0}$					$J1^{23}$					
X0D25	H^{0} out	$1J^{0}$					$J1^{21}$					
X0D26	H^{3} out		$4E^{0}$	$8C^{0}$	$16B^{0}$		$J1^{15}$		A			
X0D27	H^{4} out		$4E^{1}$	$8C^{1}$	$16B^{1}$		$J1^{13}$		B			
X0D28			$4F^{0}$	$8C^{2}$	$16B^{2}$		$J1^{7}$			Green		
X0D29			$4F^{1}$	$8C^{3}$	$16B^{3}$		$J1^{5}$			RGB^{B}		
X0D30			$4F^{2}$	$8C^{4}$	$16B^{4}$		$J1^{3}$			RGB^{G}		
X0D31			$4F^{3}$	$8C^{5}$	$16B^{5}$		$J1^{1}$			RGB^{R}		
X0D32			$4E^{2}$	$8C^{6}$	$16B^{6}$		$J1^{11}$					
X0D33			$4E^{3}$	$8C^{7}$	$16B^{7}$		$J1^{9}$					
X0D34	H^{1} out	$1K^{0}$					$J1^{19}$					
X0D35	H^{2} out	$1L^{0}$					$J1^{17}$					
X0D36		$1M^{0}$		$8D^{0}$	$16B^{8}$		$J1^{63}$					
X0D37	A^{4} in	$1N^{0}$		$8D^{1}$	$16B^{9}$		$J1^{61}$					
X0D38	A^{3} in	$1O^{0}$		$8D^{2}$	$16B^{10}$		$J1^{59}$					
X0D39	A^{2} in	$1P^{0}$		$8D^{3}$	$16B^{11}$		$J1^{57}$					
X0D40	A^{1} in			$8D^{4}$	$16B^{12}$						DN1	
X0D41	A^{0} in			$8D^{5}$	$16B^{13}$						DN0	
X0D42	A^{0} out			$8D^{6}$	$16B^{14}$						UP0	
X0D43	A^{1} out			$8D^{7}$	$16B^{15}$						UP1	

Figure 19: xCORE-200 explorerKIT Portmap

Pin	link	1-bit	4-bit	8-bit	16-bit	32-bit	GPIO	SPI	BUTTON	LED	uplink	RGMII
X1D00	H^2 in	$1A^0$					$J3^{40}$					
X1D01	H^1 in	$1B^0$					$J3^{42}$					
X1D02	E^0 in		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	$J3^{32}$					
X1D03	E^0 out		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	$J3^{34}$					
X1D04	E^1 out		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	$J3^{24}$					
X1D05	E^2 out		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	$J3^{26}$					
X1D06	E^3 out		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	$J3^{28}$					
X1D07	E^4 out		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	$J3^{30}$					
X1D08	H^4 in		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	$J3^{36}$					
X1D09	H^3 in		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	$J3^{38}$					
X1D10		$1C^0$										MDIO
X1D11		$1D^0$										MDC
X1D14			$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	$J3^{16}$					
X1D15			$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	$J3^{18}$					
X1D16	D^1 in		$4D^0$	$8B^2$	$16A^{10}$		$J3^8$					
X1D17	D^0 in		$4D^1$	$8B^3$	$16A^{11}$		$J3^{10}$					
X1D18	D^0 out		$4D^2$	$8B^4$	$16A^{12}$		$J3^{12}$					
X1D19	D^1 out		$4D^3$	$8B^5$	$16A^{13}$		$J3^{14}$					
X1D20			$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	$J3^{20}$					
X1D21			$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	$J3^{22}$					
X1D26			$4E^0$	$8C^0$	$16B^0$							TX_CLK
X1D27			$4E^1$	$8C^1$	$16B^1$							TX_EN
X1D28			$4F^0$	$8C^2$	$16B^2$							RX_CLK
X1D29			$4F^1$	$8C^3$	$16B^3$							RX_DV
X1D30			$4F^2$	$8C^4$	$16B^4$							RX0
X1D31			$4F^3$	$8C^5$	$16B^5$							RX1
X1D32			$4E^2$	$8C^6$	$16B^6$							RX2
X1D33			$4E^3$	$8C^7$	$16B^7$							RX3
X1D35	A^3 out	$1L^0$					$J3^2$					
X1D36	A^4 out	$1M^0$		$8D^0$	$16B^8$							INT
X1D37	D^4 in	$1N^0$		$8D^1$	$16B^9$							PHY_RSTn
X1D38	D^3 in	$1O^0$		$8D^2$	$16B^{10}$		$J3^4$					
X1D39	D^2 in	$1P^0$		$8D^3$	$16B^{11}$		$J3^6$					
X1D40				$8D^4$	$16B^{12}$							TX3
X1D41				$8D^5$	$16B^{13}$							TX4
X1D42				$8D^6$	$16B^{14}$							TX5
X1D43				$8D^7$	$16B^{15}$							TX6

Figure 20: xCORE-200 explorerKIT Portmap

17 xCORE-200 explorerKIT schematics

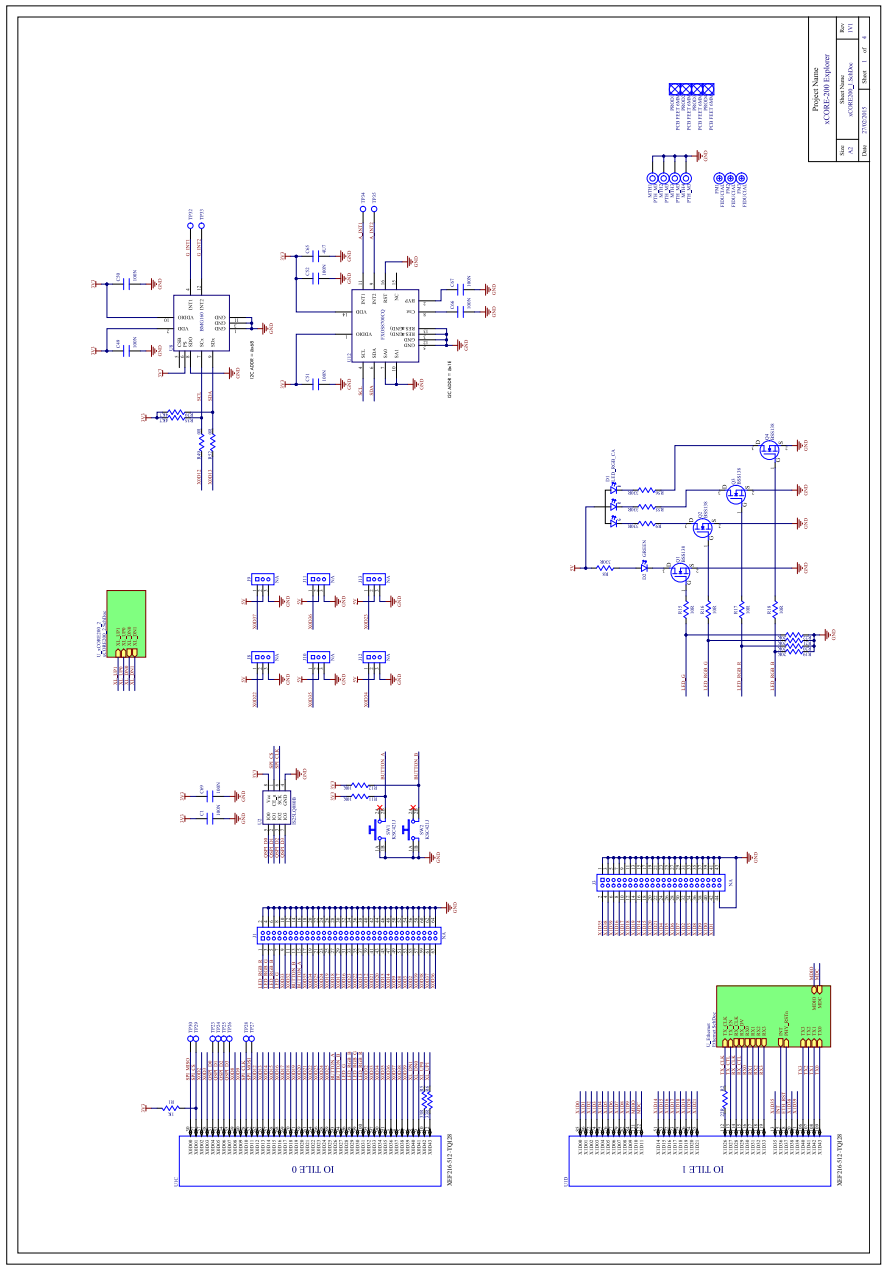

Figure 21: xCORE-200 explorerKIT schematic

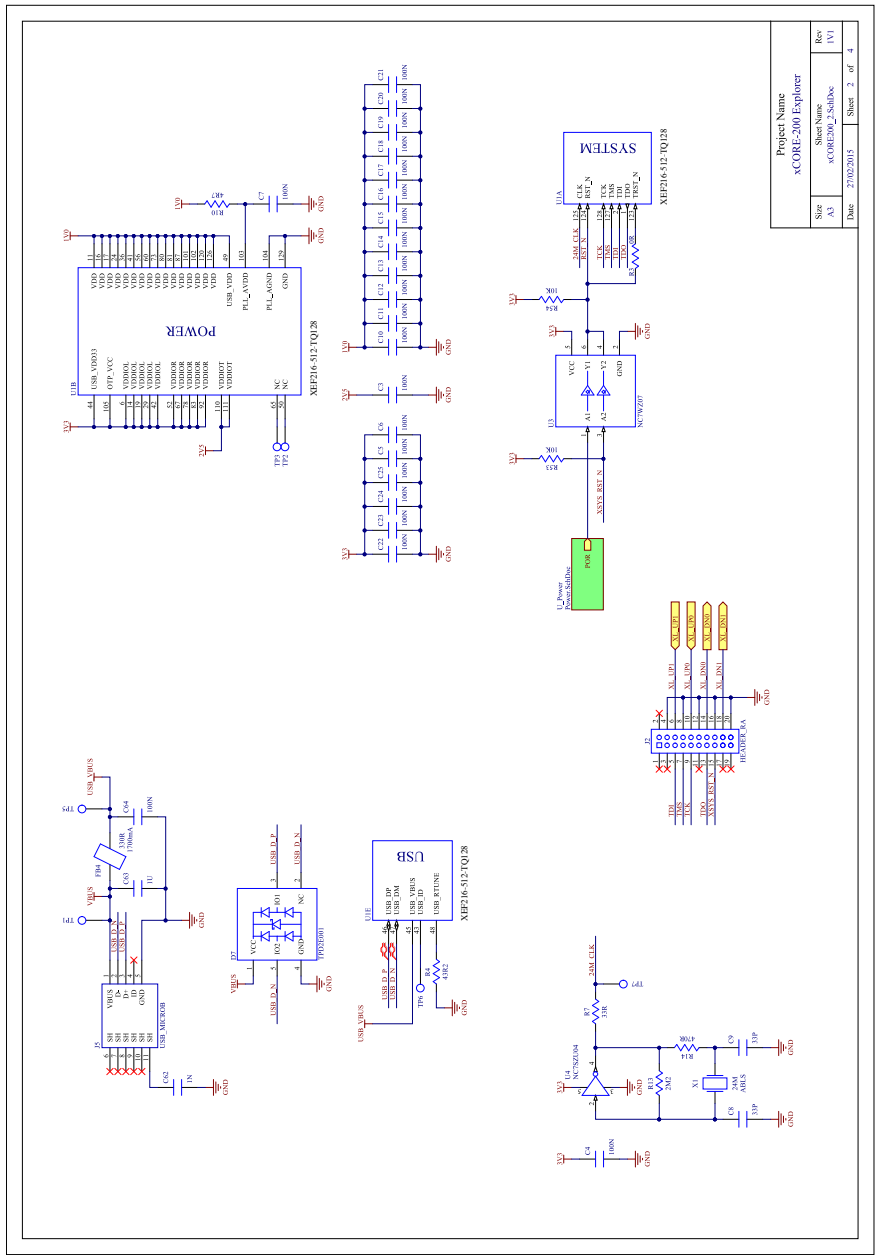

Figure 22: xCORE-200 explorerKIT USB schematic

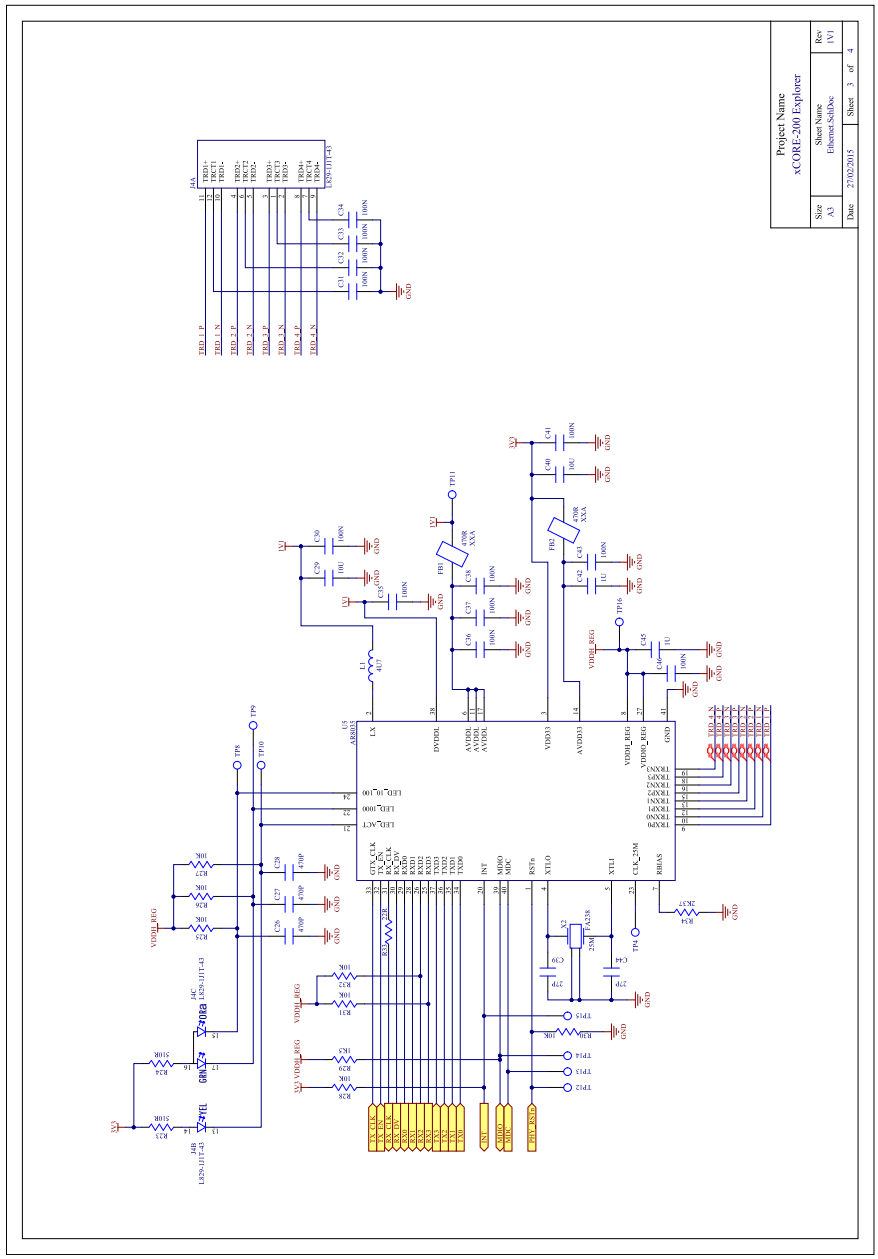

Figure 23: xCORE-200 explorerKIT Ethernet schematic

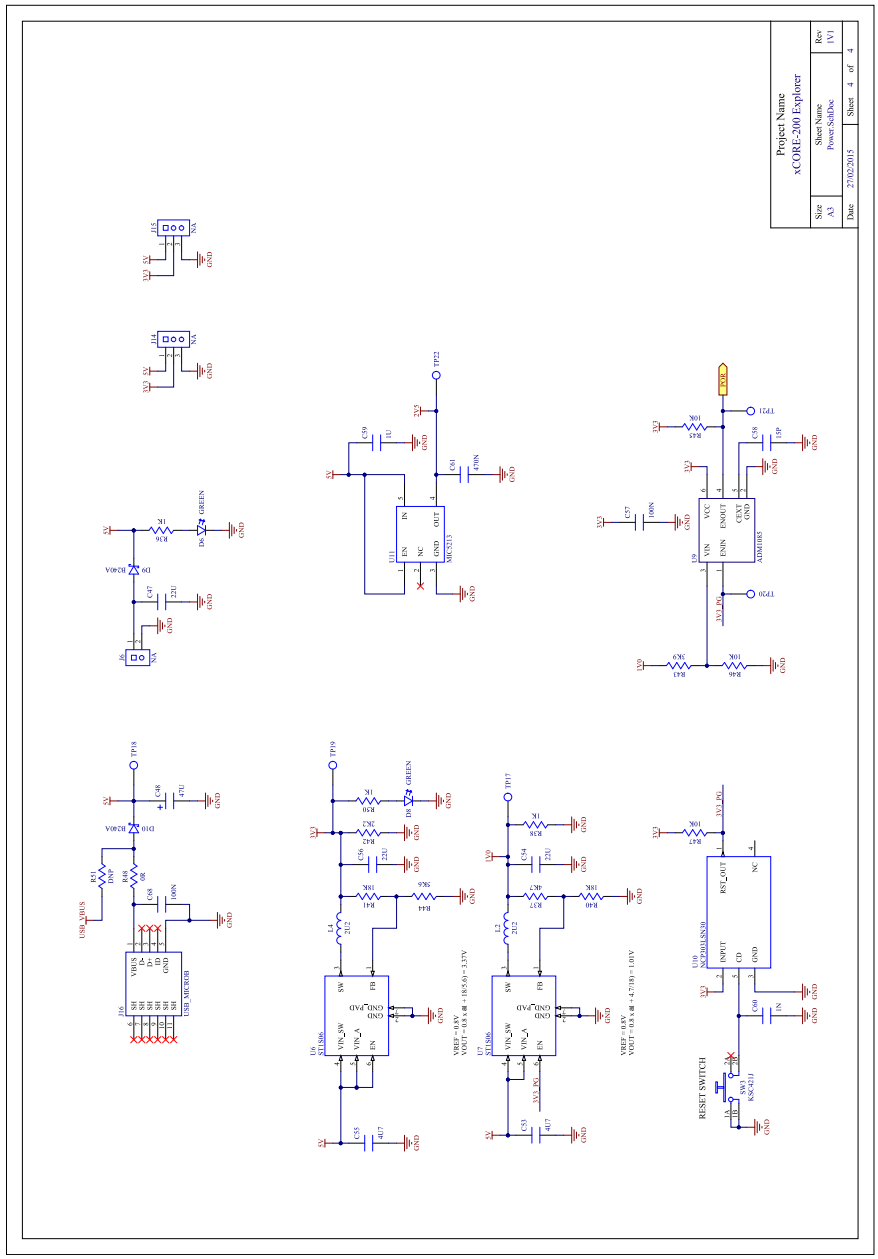

Figure 24: xCORE-200 explorerKIT power schematic

18 Regulatory compliance

The xCORE-200 explorerKIT has been tested to the applicable electromagnetic compatibility (EMC) test standards as listed in the table below.

Test	Standard	Notes
Radiated Emissions (30MHz – 1GHz)	FCC CFR 47 Part 15	Tested to Class A limits
Radiated Emissions (1GHz – 6GHz)	FCC CFR 47 Part 15	Tested to Class A limits
Immunity from Radiated Fields	EN55024:2010	Tested to Class A limits
Radiated Emissions (30MHz – 1GHz)	EN55022:2010	Tested to Class A limits
Radiated Emissions (1GHz – 6GHz)	EN55022:2010	Tested to Class A limits

18.1 European Region

This product complies with the Economic Area (EEA) EMC Directive 2004/108/EC and has been tested and found to comply in full with the requirements of:

- EN 55022:2010 – Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement. CISPR 22:2008 (Modified)
- EN 55024:2010 – Information technology equipment – Immunity characteristics – Limits and methods of measurement. CISPR 24:2010

It meets Class A Limits as described in EN 55022:2010. Class A equipment is equipment suitable for use in all establishments other than domestic.

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

18.2 North America Region

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

18.3 RoHS and REACH

The xCORE-200 explorerKIT complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The xCORE-200 explorerKIT is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.

Any unapproved devices connected to this product by the GPIO headers or connector may affect compliance to these standards, and end users should take appropriate precautions in this case.

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