### 36. DMA Controller (XDMAC)

### 36.1 Description

The DMA Controller (XDMAC) is a AHB-protocol central direct memory access controller. It performs peripheral data transfer and memory move operations over one or two bus ports through the unidirectional communication channel. Each channel is fully programmable and provides both peripheral or memory-to-memory transfers. The channel features are configurable at implementation.

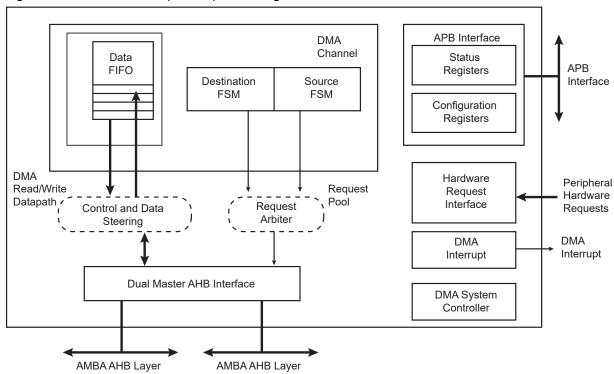
### 36.2 Embedded Characteristics

- · 2 AHB Master Interfaces
- 24 DMA Channels
- · 43 Hardware Requests
- 3.1 Kbytes Embedded FIFO
- Supports Peripheral-to-Memory, Memory-to-Peripheral, or Memory-to-Memory Transfer Operations
- Peripheral DMA Operation Runs on Bytes (8-bit), Half-Word (16-bit) and Word (32-bit)
- · Memory DMA Operation Runs on Bytes (8 bit), Half-Word (16-bit) and Word (32 -bit)
- · Supports Hardware and Software Initiated Transfers
- · Supports Linked List Operations
- · Supports Incrementing or Fixed Addressing Mode
- Supports Programmable Independent Data Striding for Source and Destination
- · Supports Programmable Independent Microblock Striding for Source and Destination
- · Configurable Priority Group and Arbitration Policy
- · Programmable AHB Burst Length
- · Configuration Interface Accessible through APB Interface
- · XDMAC Architecture Includes Multiport FIFO
- Supports Multiple View Channel Descriptor
- · Automatic Flush of Channel Trailing Bytes
- · Automatic Coarse-Grain and Fine-Grain Clock Gating
- · Hardware Acceleration of Memset Pattern

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#### 36.3 **Block Diagram**

Figure 36-1. DMA Controller (XDMAC) Block Diagram



#### 36.4 **DMA Controller Peripheral Connections**

Table 36-1. Peripheral Hardware Requests

Peripheral Name	Transfer Type	HW Interface Number (XDMAC_CC.PERID)
HSMCI	Transmit/Receive	0
SPI0	Transmit	1
SPI0	Receive	2
SPI1	Transmit	3
SPI1	Receive	4
QSPI	Transmit	5
QSPI	Receive	6
USART0	Transmit	7
USART0	Receive	8
USART1	Transmit	9
USART1	Receive	10
USART2	Transmit	11
USART2	Receive	12

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continued		
Peripheral Name	Transfer Type	HW Interface Number (XDMAC_CC.PERID)
PWM0	Transmit	13
TWIHS0	Transmit	14
TWIHS0	Receive	15
TWIHS1	Transmit	16
TWIHS1	Receive	17
TWIHS2	Transmit	18
TWIHS2	Receive	19
UART0	Transmit	20
UART0	Receive	21
UART1	Transmit	22
UART1	Receive	23
UART2	Transmit	24
UART2	Receive	25
UART3	Transmit	26
UART3	Receive	27
UART4	Transmit	28
UART4	Receive	29
DACC	Transmit	30
SSC	Transmit	32
SSC	Receive	33
PIOA	Receive	34
AFEC0	Receive	35
AFEC1	Receive	36
AES	Transmit	37
AES	Receive	38
PWM1	Transmit	39
TC0	Receive	40
TC3	Receive	41
TC6	Receive	42
TC9	Receive	43
I2SC0	Transmit Left	44
I2SC0	Receive Left	45
I2SC1	Transmit Left	46
I2SC1	Receive Left	47
I2SC0	Transmit Right	48

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continued										
Peripheral Name	Transfer Type	HW Interface Number (XDMAC_CC.PERID)								
I2SC0	Receive Right	49								
I2SC1	Transmit Right	50								
I2SC1	Receive Right	51								

### 36.5 Functional Description

### 36.5.1 Basic Definitions

**Source Peripheral**: Slave device, memory mapped on the interconnection network, from where the XDMAC reads data. The source peripheral teams up with a destination peripheral to form a channel. A data read operation is scheduled when the peripheral transfer request is asserted.

**Destination Peripheral**: Slave device, memory mapped on the interconnection network, to which the XDMAC writes. A write data operation is scheduled when the peripheral transfer request is asserted.

Channel: The data movement between source and destination creates a logical channel.

**Transfer Type**: The transfer is hardware-synchronized when it is paced by the peripheral hardware request, otherwise the transfer is self-triggered (memory to memory transfer).

### 36.5.2 Transfer Hierarchy Diagram

**XDMAC Master Transfer**: The Master Transfer is composed of a linked list of blocks. The channel address, control and configuration registers can be modified at the inter block boundary. The descriptor structure modifies the channel registers conditionally. Interrupts can be generated on a per block basis or when the end of linked list event occurs.

**XDMAC Block**: An XDMAC block is composed of a programmable number of microblocks. The channel configuration registers remain unchanged at the inter microblock boundary. The source and destination addresses are conditionally updated with a programmable signed number.

**XDMAC Microblock**: The microblock is composed of a programmable number of data. The channel configuration registers remain unchanged at the data boundary. The data address may be fixed (a FIFO location, a peripheral transmit or receive register), incrementing (a memory-mapped area) by a programmable signed number.

**XDMAC Burst and Incomplete Burst**: In order to improve the overall performance when accessing dynamic external memory, burst access is mandatory. Each data of the microblock is considered as a part of a memory burst. The programmable burst value indicates the largest memory burst allowed on a per channel basis. When the microblock length is not an integral multiple of the burst size, an incomplete burst is performed to read or write the last trailing bytes.

**XDMAC Chunk and Incomplete Chunk**: When a peripheral synchronized transfer is activated, the microblock splits into a number of data chunks. The chunk size is programmable. The larger the chunk is, the better the performance is. When the transfer size is not a multiple of the chunk size, the last chunk may be incomplete.

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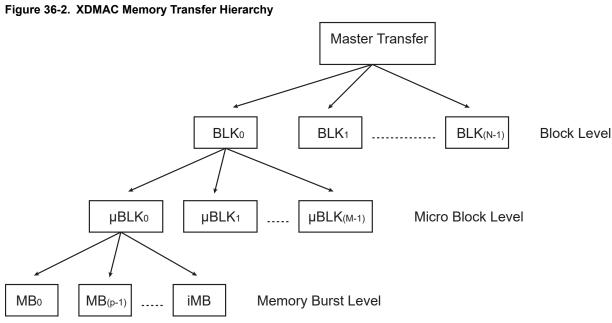
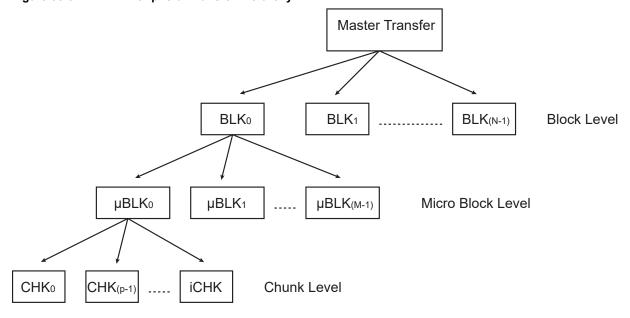


Figure 36-3. XDAMC Peripheral Transfer Hierarchy



#### 36.5.3 **Peripheral Synchronized Transfer**

A peripheral hardware request interface is used to control the pace of the chunk transfer. When a peripheral is ready to transmit or receive a chunk of data, it asserts its request line and the DMA Controller transfers a data to or from the memory to the peripheral.

### 36.5.3.1 Software Triggered Synchronized Transfer

The Peripheral hardware request can be software controlled using the SWREQ field of the XDMAC Global Channel Software Request Register (XDMAC\_GSWR). The peripheral synchronized transfer is paced using a processor write access in the XDMAC GSWR. Each bit of that register triggers a transfer request. The XDMAC Global Channel Software Request Status Register (XDMAC GSWS) indicates the status of the request; when set, the request is still pending.

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**DMA Controller (XDMAC)** 

### 36.5.4 XDMAC Transfer Software Operation

### 36.5.4.1 Single Block Transfer With Single Microblock

- 1. Read the XDMAC Global Channel Status Register (XDMAC GS) to select a free channel.
- 2. Clear the pending Interrupt Status bit(s) by reading the selected XDMAC Channel x Interrupt Status Register (XDMAC CISx).
- 3. Write the XDMAC Channel x Source Address Register (XDMAC CSAx) for channel x.
- 4. Write the XDMAC Channel x Destination Address Register (XDMAC\_CDAx) for channel x.
- Program field UBLEN in the XDMAC Channel x Microblock Control Register (XDMAC\_CUBCx) with the number of data.
- 6. Program the XDMAC Channel x Configuration Register (XDMAC\_CCx):
  - 6.1. Clear XDMAC\_CCx.TYPE for a memory-to-memory transfer, otherwise set this bit.
  - 6.2. Configure XDMAC CCx.MBSIZE to the memory burst size used.
  - 6.3. Configure XDMAC CCx.SAM and DAM to Memory Addressing mode.
  - 6.4. Configure XDMAC CCx.DSYNC to select the peripheral transfer direction.
  - 6.5. Configure XDMAC\_CCx.CSIZE to configure the channel chunk size (only relevant for peripheral synchronized transfer).
  - 6.6. Configure XDMAC\_CCx.DWIDTH to configure the transfer data width.
  - 6.7. Configure XDMAC\_CCx.SIF, XDMAC\_CCx.DIF to configure the master interface used to read data and write data, respectively.
  - 6.8. Configure XDMAC\_CCx.PERID to select the active hardware request line (only relevant for a peripheral synchronized transfer).
  - 6.9. Set XDMAC\_CCx.SWREQ to use a software request (only relevant for a peripheral synchronized transfer).
- Clear the following five registers:
  - XDMAC Channel x Next Descriptor Control Register (XDMAC CNDCx)
  - XDMAC Channel x Block Control Register (XDMAC CBCx)
  - XDMAC Channel x Data Stride Memory Set Pattern Register (XDMAC CDS MSPx)
  - XDMAC Channel x Source Microblock Stride Register (XDMAC CSUSx)
  - XDMAC Channel x Destination Microblock Stride Register (XDMAC\_CDUSx)
     This indicates that the linked list is disabled, there is only one block and striding is disabled.
- 8. Enable the Microblock interrupt by writing a '1' to bit BIE in the XDMAC Channel x Interrupt Enable Register (XDMAC\_CIEx). Enable the Channel x Interrupt Enable bit by writing a '1' to bit IEx in the XDMAC Global Interrupt Enable Register (XDMAC\_GIE).
- 9. Enable channel x by writing a '1' to bit ENx in the XDMAC Global Channel Enable Register (XDMAC\_GE). XDMAC\_GS.STx (XDMAC Channel x Status bit) is set by hardware.
- 10. Once completed, the DMA channel sets XDMAC\_CISx.BIS (End of Block Interrupt Status bit) and generates an interrupt. XDMAC\_GS.STx is cleared by hardware. The software can either wait for an interrupt or poll the channel status bit.

### 36.5.4.2 Single Block Transfer With Multiple Microblock

- 1. Read the XDMAC\_GS register to choose a free channel.
- 2. Clear the pending Interrupt Status bit by reading the chosen XDMAC\_CISx register.
- 3. Write the XDMAC CSAx register for channel x.
- 4. Write the XDMAC CDAx register for channel x.
- 5. Program XDMAC CUBCx.UBLEN with the number of data.
- 6. Program XDMAC\_CCx register (see "Single Block Transfer With Single Microblock").
- 7. Program XDMAC\_CBCx.BLEN with the number of microblocks of data.
- Clear the following registers:
  - XDMAC CNDCx
  - XDMAC CDS MSPx
  - XDMAC CSUSx XDMAC CDUSx

**DMA Controller (XDMAC)** 

This indicates that the linked list is disabled and striding is disabled.

- Enable the Block interrupt by writing a '1' to XDMAC\_CIEx.BIE, enable the Channel x Interrupt Enable bit by writing a '1' to XDMAC\_GIEx.IEx.
- 10. Enable channel x by writing a '1' to the XDMAC\_GE.ENx. XDMAC\_GS.STx is set by hardware.
- 11. Once completed, the DMA channel sets XDMAC\_CISx.BIS (End of Block Interrupt Status bit) and generates an interrupt. XDMAC\_GS.STx is cleared by hardware. The software can either wait for an interrupt or poll the channel status bit.

### 36.5.4.3 Master Transfer

- 1. Read the XDMAC\_GS register to choose a free channel.
- 2. Clear the pending Interrupt Status bit by reading the chosen XDMAC CISx register.
- Build a linked list of transfer descriptors in memory. The descriptor view is programmable on a per descriptor basis. The linked list items structure must be word aligned. MBR\_UBC.NDE must be configured to 0 in the last descriptor to terminate the list.
- 4. Configure field NDA in the XDMAC Channel x Next Descriptor Address Register (XDMAC\_CNDAx) with the first descriptor address and bit XDMAC\_CNDAx.NDAIF with the master interface identifier.
- 5. Configure the XDMAC\_CNDCx register:
  - 5.1. Set XDMAC CNDCx.NDE to enable the descriptor fetch.
  - 5.2. Set XDMAC\_CNDCx.NDSUP to update the source address at the descriptor fetch time, otherwise clear this bit.
  - 5.3. Set XDMAC\_CNDCx.NDDUP to update the destination address at the descriptor fetch time, otherwise clear this bit.
  - 5.4. Configure XDMAC CNDCx.NDVIEW to define the length of the first descriptor.
- 6. Enable the End of Linked List interrupt by writing a '1' to XDMAC CIEx.LIE.
- 7. Enable channel x by writing a '1' to XDMAC GE.ENx. XDMAC GS.STx is set by hardware.
- 8. Once completed, the DMA channel sets XDMAC\_CISx.BIS (End of Block Interrupt Status bit) and generates an interrupt. XDMAC\_GS.STx is cleared by hardware. The software can either wait for an interrupt or poll the channel status bit.

### 36.5.4.4 Disabling A Channel Before Transfer Completion

Under normal operation, the software enables a channel by writing a '1' to XDMAC\_GE.ENx, then the hardware disables a channel on transfer completion by clearing bit XDMAC\_GS.STx. To disable a channel, write a '1' to bit XDMAC GD.DIx and poll the XDMAC GS register.

### 36.6 Linked List Descriptor Operation

### 36.6.1 Linked List Descriptor View

### 36.6.1.1 Channel Next Descriptor View 0-3 Structures

### Table 36-2. Channel Next Descriptor View 0-3 Structures

Channel Next Descriptor	Offset	Structure member	Name
View 0 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Transfer Address Member	MBR_TA
View 1 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA

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continued			
Channel Next Descriptor	Offset	Structure member	Name
View 2 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
	DSCR_ADDR+0x10	Configuration Register	MBR_CFG
View 3 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
	DSCR_ADDR+0x10	Configuration Member	MBR_CFG
	DSCR_ADDR+0x14	Block Control Member	MBR_BC
	DSCR_ADDR+0x18	Data Stride Member	MBR_DS
	DSCR_ADDR+0x1C	Source Microblock Stride Member	MBR_SUS
	DSCR_ADDR+0x20	Destination Microblock Stride Member	MBR_DUS

## 36.6.2 Descriptor Structure Members Description

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### 36.6.2.1 Descriptor Structure Microblock Control Member

MBR\_UBC Name: Read-only Property:

Bit	31	30	29	28	27	26	25	24	
				NVIE	W[1:0]	NDEN	NSEN	NDE	
Access			•	R	R	R	R	R	
Reset									
Bit	23	22	21	20	19	18	17	16	
				UBLEN	N[23:16]				
Access	R	R	R	R	R	R	R	R	
Reset									
Bit	15	14	13	12	11	10	9	8	
				UBLEI	N[15:8]				
Access	R	R	R	R	R	R	R	R	
Reset									
Bit	7	6	5	4	3	2	1	0	
	UBLEN[7:0]								
Access	R	R	R	R	R	R	R	R	
Reset									

### Bits 28:27 - NVIEW[1:0] Next Descriptor View

		<u> </u>
Value	Name	Description
0	NDV0	Next Descriptor View 0
1	NDV1	Next Descriptor View 1
2	NDV2	Next Descriptor View 2
3	NDV3	Next Descriptor View 3

### Bit 26 - NDEN Next Descriptor Destination Update

Value	Description
0	Destination parameters remain unchanged.
1	Destination parameters are updated when the descriptor is retrieved.

### Bit 25 - NSEN Next Descriptor Source Update

Value	Description
0	Source parameters remain unchanged.
1	Source parameters are updated when the descriptor is retrieved.

### Bit 24 - NDE Next Descriptor Enable

٧	alue	Description
0		Descriptor fetch is disabled.
1		Descriptor fetch is enabled.

### Bits 23:0 – UBLEN[23:0] Microblock Length

This field indicates the number of data in the microblock. The microblock contains UBLEN data.

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**DMA Controller (XDMAC)** 

#### 36.7 **XDMAC Maintenance Software Operations**

#### 36.7.1 Disabling a Channel

A disable channel request occurs when a write operation is performed in the XDMAC GD register. If the channel is source peripheral synchronized (bit XDMAC\_CCx.TYPE is set and bit XDMAC\_CCx.DSYNC is cleared), then pending bytes (bytes located in the FIFO) are written to memory and bit XDMAC\_CISx.DIS is set. If the channel is not source peripheral synchronized, the current channel transaction (read or write) is terminated and XDMAC CISx.DIS is set. XDMAC GS.STx is cleared by hardware when the current transfer is completed. The channel is no longer active and can be reused.

#### 36.7.2 Suspending a Channel

A disable channel request occurs when a write operation is performed in the XDMAC\_GD register. If the channel is source peripheral synchronized (bit XDMAC\_CCx.TYPE is set and bit XDMAC\_CCx.DSYNC is cleared), then pending bytes (bytes located in the FIFO) are written to memory and bit XDMAC\_CISx.DIS is set. If the channel is not source peripheral synchronized, the current channel transaction (read or write) is terminated and XDMAC CISx.DIS is set. XDMAC GS.STx is cleared by hardware when the current transfer is completed. The channel is no longer active and can be reused.

#### 36.7.3 Flushing a Channel

A FIFO flush command is issued by writing to the XDMAC\_SWF register. The content of the FIFO is written to memory. XDMAC CISx.FIS (End of Flush Interrupt Status bit) is set when the last byte is successfully transferred to memory. The channel is not disabled. The flush operation is not blocking, meaning that read operation can be scheduled during the flush write operation. The flush operation is only relevant for peripheral to memory transfer where pending peripheral bytes are buffered into the channel FIFO.

#### 36.7.4 **Maintenance Operation Priority**

### 36.7.4.1 Disable Operation Priority

- When a disable request occurs on a suspended channel, the XDMAC GWS.WSx (Channel x Write Suspend bit) is cleared. If the transfer is source peripheral synchronized, the pending bytes are drained to memory. The bit XDMAC CISx.DIS is set.
- When a disable request follows a flush request, if the flush last transaction is not yet scheduled, the flush request is discarded and the disable procedure is applied. Bit XDMAC\_CISx.FIS is not set. Bit XDMAC CISx.DIS is set when the disable request is completed. If the flush request transaction is already scheduled, the XDMAC CISx.FIS is set. XDMAC CISx.DIS is also set when the disable request is completed.

### 36.7.4.2 Flush Operation Priority

- When a flush request occurs on a suspended channel, if there are pending bytes in the FIFO, they are written out to memory, XDMAC CISx.FIS is set. If the FIFO is empty, XDMAC CISx.FIS is also set.
- If the flush operation is performed after a disable request, the flush command is ignored. XDMAC CISx.FIS is not set.

### 36.7.4.3 Suspend Operation Priority

If the suspend operation is performed after a disable request, the write suspend operation is ignored.

#### 36.8 **XDMAC Software Requirements**

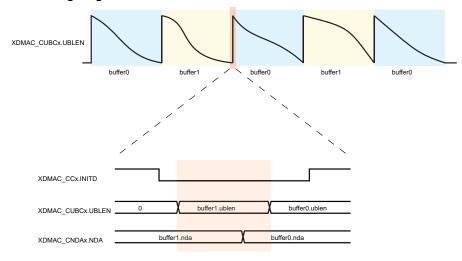
- Write operations to channel registers are not be performed in an active channel after the channel is enabled. If any channel parameters must be reprogrammed, this can only be done after disabling the XDMAC channel.
- XDMAC\_CSAx and XDMAC\_CDAx channel registers are to be programmed with a byte, half-word or word aligned address depending on the Channel x Data Width field (DWIDTH) of the XDMAC Channel x Configuration Register.

**Datasheet** DS60001527D-page 464 When XDMAC\_CC.INITD is set to 0, XDMAC\_CUBC.UBLEN and XDMAC\_CNDA.NDA field values are unreliable when the descriptor is being updated. The following procedure applies to get the buffer descriptor identifier and the residual bytes:

```
Read XDMAC_CNDAx.NDA(nda0)
Read XDMAC_CCx.INITD(initd0)
Read XDMAC_CCx.INITD(initd0)
Read XDMAC_CUBCx.UBLEN(ublen)
Read XDMAC_CUBCx.UBLEN(initd1)
Read XDMAC_CCx.INITD(initd1)
Read XDMA_CNDAx.NDA(nda1)
If (nda0 == nda1 && initd0 == 1 && initd1 == 1).
Then the ublen is correct, the buffer id is nda.
Else retry
```

See the figure below.

Figure 36-4. INITD Timing Diagram



## 36.9 Register Summary

Offset	Name	Bit Pos.								
		7:0		FIFO_SZ[2:0]				NB CH[4:0]		
	V	15:8				FIFO S	SZ[10:3]			
0x00	XDMAC_GTYPE	23:16								
		31:24								
		7:0					CGDISIF	CGDISFIFO	CGDISPIPE	CGDISREG
0x04	XDMAC_GCFG	15:8								BXKBEN
0.04	ADMAC_GOLG	23:16								
		31:24					PW0[3:0]   PW2[3:0]   PW2[3:0]			
		7:0		PW1						
0x08	XDMAC_GWAC	15:8		PW3	[3:0]	i		PW2	2[3:0]	i
		23:16								
		31:24	157	IEC	IE E	154	IFO	IFO	IE4	IFO
		7:0	IE7	IE6	IE5					IE0
0x0C	XDMAC_GIE	15:8	IE15 IE23	IE14	IE13 IE21					IE8
		23:16 31:24	IE23	IE22	IEZ I	IE20	1519	IE 10	IE17	IE16
		7:0	ID7	ID6	ID5	ID4	ID3	ID3	ID1	ID0
		15:8	ID15	ID14	ID13		-			ID8
0x10	XDMAC_GID	23:16	ID15	ID14 ID22	ID13					ID16
		31:24	IDZJ	IDZZ	IDZI	IDZU	פוטו	סוטו	וטו	טוטו
		7:0	IM7	IM6	IM5	IM4	IM3	IM2	IM1	IMO
	x14 XDMAC_GIM	15:8	IM15	IM14	IM13		-			IM8
0x14		23:16	IM23	IM22	IM21					IM16
		31:24	20			20				
		7:0	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
		15:8	IS15	IS14	IS13		-			IS8
0x18	XDMAC_GIS	23:16	IS23	IS22	IS21					IS16
		31:24								
	VD1440-05	7:0	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
0::10		15:8	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
0x1C	XDMAC_GE	23:16	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
		31:24								
		7:0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0x20	XDMAC_GD	15:8	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0,20	ADWAC_GD	23:16	DI23	DI22	DI21	DI20	DI19	DI18	DI17	DI16
		31:24								
		7:0	ST7	ST6	ST5		ST3			ST0
0x24	XDMAC_GS	15:8	ST15	ST14	ST13		ST11		ST9	ST8
OALI	ABINI 10_00	23:16	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16
		31:24								
		7:0	RS7	RS6	RS5					RS0
0x28	XDMAC_GRS	15:8	RS15	RS14	RS13				-	RS8
		23:16	RS23	RS22	RS21	RS20	RS19	RS18	RS17	RS16
		31:24								
		7:0	WS7	WS6	WS5					WS0
0x2C	XDMAC_GWS	15:8	WS15	WS14	WS13					WS8
	_	23:16	WS23	WS22	WS21	WS20	WS19	WS18	WS17	WS16
		31:24	DMCZ	DWCC	DMCE	DIMOA	DWC3	DWCO	DMC4	RWS0
		7:0	RWS7	RWS6	RWS5					
0x30	XDMAC_GRWS	15:8 23:16	RWS15 RWS23	RWS14 RWS22	RWS13 RWS21					RWS8 RWS16
		31:24	KVV323	RVVSZZ	RVV321	KVV320	LM918	LWOID	KW01/	KWSIO
		7:0	RWR7	RWR6	RWR5	RWR4	RWR3	RWR2	RWR1	RWR0
		15:8	RWR15	RWR14	RWR13	RWR12	RWR11	RWR10	RWR9	RWR8
0x34	XDMAC_GRWR	23:16	RWR13	RWR22	RWR13	RWR20	RWR19	RWR18	RWR17	RWR16
		31:24	1111120	1111122	1 ( ) ( )	11771120	1444110	1444410	13771317	11771110
		01.24								

Offset										
	Name	Bit Pos.								
	Name		OWEG	OWEGO	OWEGE	OWEGA	OWEGO	OWEGO	OWEGA	OWEGO
		7:0 15:8	SWREQ7 SWREQ15	SWREQ6 SWREQ14	SWREQ5 SWREQ13	SWREQ4 SWREQ12	SWREQ3 SWREQ11	SWREQ2 SWREQ10	SWREQ1 SWREQ9	SWREQ0 SWREQ8
0x38	XDMAC_GSWR	23:16	SWREQ13	SWREQ22	SWREQ13	SWREQ12	SWREQ19	SWREQ10	SWREQ17	SWREQ16
		31:24	SWINEQ23	SWINEQZZ	SWINEQZI	3WKEQ20	SWILEGIS	SWILCIO	SWILCIT	SWILLEGIO
		7:0	SWRS7	SWRS6	SWRS5	SWRS4	SWRS3	SWRS2	SWRS1	SWRS0
		15:8	SWRS15	SWRS14	SWRS13	SWRS12	SWRS11	SWRS10	SWRS9	SWRS8
0x3C	XDMAC_GSWS	23:16	SWRS23	SWRS22	SWRS21	SWRS20	SWRS19	SWRS18	SWRS17	SWRS16
		31:24	3W1(023	OWNOZZ	OWNOZI	3W1(020	OWNOIS	SWIGH	OWNOT	SWINGTO
		7:0	SWF7	SWF6	SWF5	SWF4	SWF3	SWF2	SWF1	SWF0
		15:8	SWF15	SWF14	SWF13	SWF12	SWF11	SWF10	SWF9	SWF8
0x40	XDMAC_GSWF	23:16	SWF23	SWF22	SWF21	SWF20	SWF19	SWF18	SWF17	SWF16
		31:24	3111 20	3111 EE	311121	OW1 20	3111 10	3111 10	34417	011110
0x44		01.24								
	Reserved									
0x4F	110001100									
0/(1)		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
		15:8					· <u>-</u>			
0x50	XDMAC_CIE0	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8								
0x54	XDMAC_CID0	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
0x58	XDMAC_CIM0	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
0x5C	XDMAC_CIS0	23:16								
		31:24								
		7:0				SA[	7:0]			
		15:8				SA[ <sup>2</sup>				
0x60	XDMAC_CSA0	23:16				SA[2				
		31:24				SA[3				
		7:0				DA[				
004	VDMAQ ODAQ	15:8				DA[	15:8]			
0x64	XDMAC_CDA0	23:16				DA[2	3:16]			
		31:24				DA[3	1:24]			
		7:0			NDA	[5:0]				NDAIF
0.460	VDMAC CNDAO	15:8				NDA	[13:6]			
0x68	XDMAC_CNDA0	23:16				NDA[	21:14]			
		31:24				NDA[	29:22]			
		7:0					:W[1:0]	NDDUP	NDSUP	NDE
0x6C	XDMAC_CNDC0	15:8								
UXUC	VDINIUC_CINDCO	23:16								
		31:24								
		7:0				UBLE	N[7:0]			
0x70	XDMAC CUBC0	15:8					N[15:8]			
UXIU	XDIVIAC_COBCO	23:16				UBLEN	I[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
0x74	XDMAC_CBC0	15:8						BLEN	[11:8]	
UX/4	VDINIMO_CDC0	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
	VDMAC CCC	15:8		DIF	SIF	DWID	ΓH[1:0]		CSIZE[2:0]	
0.70	XDMAC_CC0	00.40	WRIP	RDIP	INITD		DAM	[1:0]	SAM	I[1:0]
0x78	7/DIVI/10_000	23:16	VVIXII							

con	tinued									
Offset	Name	Bit Pos.								
		7:0				SDS_M	CD(7:01			
	XDMAC_CDS_MSP	15:8				SDS_MS				
0x7C	ADMAC_CDS_MSP	23:16				DDS_M				
	0									
		31:24				DDS_MS				
		7:0				SUBS				
0x80	XDMAC_CSUS0	15:8				SUBS				
		23:16				SUBS[	23.10]			
		31:24				DUDO	217-01			
		7:0				DUBS				
0x84	XDMAC_CDUS0	15:8				DUBS				
		23:16				DUBS[	23:16]			
0.00		31:24								
0x88	December									
 0v0E	Reserved									
0x8F		7.0		DOLE	WDIE	DDIE	FIE	DIE		DIE
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x90	XDMAC_CIE1	15:8								
		23:16								
		31:24		DOID	WDEID	DDEID	ריה	DID	LID	DID
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x94	XDMAC_CID1	15:8								
		23:16								
		31:24		500.4	\4/5=11.4	55511		511.4		
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x98	XDMAC_CIM1	15:8								
	_	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x9C	XDMAC_CIS1	15:8								
		23:16								
		31:24								
		7:0				SA[7				
0xA0	XDMAC_CSA1	15:8				SA[1				
		23:16				SA[2				
		31:24				SA[3				
		7:0				DA[				
0xA4	XDMAC_CDA1	15:8				DA[1				
		23:16				DA[2				
		31:24			NIDA	DA[3	1:24]			NDAIE
		7:0			NDA		12.61			NDAIF
0xA8	XDMAC_CNDA1	15:8				NDA!				
		23:16				NDA[2				
		31:24				NDA[2		NDDUP	NDSUP	NDE
		7:0 15:8				NDVIE	vv[1.∪]	אטטטאו	NDSUP	NDE
0xAC	XDMAC_CNDC1									
		23:16								
		31:24				LIDI E	NITZ-01			
		7:0				UBLEI				
0xB0	XDMAC_CUBC1	15:8				UBLEN				
		23:16				UBLEN	[23:16]			
		31:24				DI EL	1[7,0]			
		7:0				BLEN	ı[/:U]	חורי	1[11.0]	
0xB4	XDMAC_CBC1	15:8						BLEN	I[11:8]	
	_	23:16								
		31:24	MENTOET	OMES		D0)(1)0		Manage	75(4.0)	TVDE
		7:0	MEMSET	SWREQ	015	DSYNC	TI I[4.0]	MBSIZ	ZE[1:0]	TYPE
0xB8	XDMAC_CC1	15:8	MDID	DIF	SIF	DWIDT		M[4,0]	CSIZE[2:0]	[4.0]
		23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
	1	31:24					PERID[6:0]			

con	tinued									
		Dit Das								
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0xBC	XDMAC_CDS_MSP	15:8				SDS_M				
	1	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0xC0	XDMAC_CSUS1	15:8				SUBS				
	_	23:16				SUBS	[23:16]			
		31:24				5115	0.5			
		7:0					S[7:0]			
0xC4	XDMAC_CDUS1	15:8					S[15:8]			
		23:16				DORS	[23:16]			
0,,00		31:24								
0xC8	Reserved									
0xCF	Reserved									
UXCF		7:0		POIE	WALE	DDIE	CIC	DIE	115	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0xD0	XDMAC_CIE2	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8		מוטא	WOLID	KDEID	FID	טוט	LID	טוט
0xD4	XDMAC_CID2	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8		TOIN	WDLIN	KDLIW	T IIVI	Dilvi	LIIVI	Dilvi
0xD8	XDMAC_CIM2	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8		11010	WDLIO	RDEIO	110	DIO	LIO	ыо
0xDC	XDMAC_CIS2	23:16								
		31:24								
		7:0				SAI	7:0]			
		15:8					15:8]			
0xE0	XDMAC_CSA2	23:16				SA[2				
		31:24				SA[3				
		7:0					[7:0]			
		15:8					15:8]			
0xE4	XDMAC_CDA2	23:16					3:16]			
		31:24				DA[3				
		7:0			NDA	A[5:0]				NDAIF
	V-11-	15:8				NDA	[13:6]			1
0xE8	XDMAC_CNDA2	23:16					21:14]			
		31:24					29:22]			
		7:0					:W[1:0]	NDDUP	NDSUP	NDE
		15:8								
0xEC	XDMAC_CNDC2	23:16								
		31:24								
		7:0				UBLE	N[7:0]			
	\ \	15:8				UBLE				
0xF0	XDMAC_CUBC2	23:16					I[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
c = :	VD1410 5===	15:8					· ·	BLEN	[11:8]	
0xF4	XDMAC_CBC2	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
a -		15:8		DIF	SIF		TH[1:0]		CSIZE[2:0]	1
0xF8	XDMAC_CC2	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	I[1:0]
		31:24					PERID[6:0]			
							[0]			

cont	tinued									
Offset	Name	Bit Pos.								
Onset	Name					252.	100:00:00			
	VD1110 0D0 110D	7:0					ISP[7:0]			
0xFC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	2	23:16					MSP[7:0]			
		31:24					ISP[15:8]			
		7:0					S[7:0]			
0x0100	XDMAC_CSUS2	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24				DUD	017.01			
		7:0					S[7:0]			
0x0104	XDMAC_CDUS2	15:8					S[15:8]			
		23:16				DORS	[23:16]			
0::0400		31:24								
0x0108	Decembed									
 0x010F	Reserved									
UXUTUF		7:0		POIE	WALE	DDIE	EIE	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0110	XDMAC_CIE3	23:16								
		31:24 7:0		ROID	WBEID	RBEID	FID	DID	ΠD	BID
		7:0 15:8		KOID	WEID	KDEID	FID	DID	LID	BID
0x0114	XDMAC_CID3									
		23:16								
		31:24		DOIM	VA/DEIN4	DDEIM	FINA	DIM	1.154	DIM
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0118	XDMAC_CIM3	15:8								
		23:16								
		31:24		5010	14/2510	55510	=10	510		510
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x011C	XDMAC_CIS3	15:8								
	_	23:16								
		31:24				0.41				
		7:0					[7:0]			
0x0120	XDMAC_CSA3	15:8					15:8]			
		23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x0124	XDMAC_CDA3	15:8					15:8]			
		23:16					23:16]			
		31:24			ND		31:24]			NDAIE
		7:0			NDA	N[5:0]				NDAIF
0x0128	XDMAC_CNDA3	15:8					[13:6]			
	_	23:16					[21:14]			
		31:24					[29:22]	NDSUS	NDCUE	NDE
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x012C	XDMAC_CNDC3	15:8								
	_	23:16								
		31:24				115: 5	NICZ-01			
		7:0					EN[7:0]			
0x0130	XDMAC_CUBC3	15:8					N[15:8]			
	_	23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLE	N[7:0]	·	1544 03	
0x0134	XDMAC_CBC3	15:8						BLEN	[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x0138	XDMAC_CC3	15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
5 100	/12.11.10_000	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

nort!	inund									
conti										
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x013C	XDMAC_CDS_MSP	15:8					SP[15:8]			
0.0130	3	23:16					ISP[7:0]			
		31:24				DDS_M	SP[15:8]			
		7:0					S[7:0]			
0x0140	XDMAC_CSUS3	15:8				SUBS	[15:8]			
0.00140	ADMAC_COOOS	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0144	XDMAC_CDUS3	15:8					S[15:8]			
0,0144	XDIVINO_ODOGG	23:16				DUBS	[23:16]			
		31:24								
0x0148										
	Reserved									
0x014F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0150	XDMAC_CIE4	15:8								
		23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0154	XDMAC_CID4	15:8								
		23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0158	XDMAC_CIM4	15:8								
		23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x015C	XDMAC_CIS4	15:8								
0,0100	XBINI/(0_0101	23:16								
		31:24								
		7:0					7:0]			
0x0160	XDMAC_CSA4	15:8					15:8]			
	_	23:16					3:16]			
		31:24					1:24]			
		7:0					[7:0]			
0x0164	XDMAC_CDA4	15:8					15:8]			
		23:16					3:16]			
		31:24					1:24]			
		7:0			NDA					NDAIF
0x0168	XDMAC_CNDA4	15:8				NDA				
-	_	23:16					21:14]			
		31:24				NDA[				
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x016C	XDMAC_CNDC4	15:8								
	_	23:16								
		31:24					NIET 02			
		7:0					N[7:0]			
0x0170	XDMAC_CUBC4	15:8					N[15:8]			
-		23:16				UBLEN	I[23:16]			
		31:24								
		7:0				BLEN	V[7:0]			
0x0174	XDMAC_CBC4	15:8						BLEN	I[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
		15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
0x0178	XDMAC CC4 +									
0x0178	XDMAC_CC4	23:16 31:24	WRIP	RDIP	INITD		PERID[6:0]	M[1:0]	SAM	[1:0]

cont	tinued									
		Dia B								
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x017C	XDMAC_CDS_MSP	15:8				SDS_M				
0,0170	4	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0				SUBS				
0x0180	XDMAC_CSUS4	15:8				SUBS	[15:8]			
0.00100	ADMAC_COOG4	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0184	XDMAC_CDUS4	15:8				DUBS	S[15:8]			
000104	ADMAC_CD004	23:16				DUBS	[23:16]			
		31:24								
0x0188										
	Reserved									
0x018F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0190	XDMAC_CIE5	15:8								
070190	ADWAG_OILS	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0194	XDMAC CID5	15:8								
000134	ADMAC_CIDS	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0198	XDMAC_CIM5	15:8								
080196	ADIVIAC_CIIVIS	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0v0100	VDMAC CISE	15:8								
0x019C	XDMAC_CIS5	23:16								
		31:24								
		7:0				SA[	7:0]			
0x01A0	XDMAC_CSA5	15:8				SA[	15:8]			
UXUTAU	ADIVIAC_CSAS	23:16				SA[2	3:16]			
		31:24				SA[3	1:24]			
		7:0				DA[	[7:0]			
0,0144	VDMAC CDAE	15:8				DA[	15:8]			
0x01A4	XDMAC_CDA5	23:16				DA[2	3:16]			
		31:24				DA[3				
		7:0			NDA	N[5:0]				NDAIF
0.0440	VDMAC CNDAE	15:8				NDA				
0x01A8	XDMAC_CNDA5	23:16					21:14]			
		31:24					29:22]			
		7:0				NDVIE		NDDUP	NDSUP	NDE
0,04 * 0	VDMAQ ONDOS	15:8								
0x01AC	XDMAC_CNDC5	23:16								
		31:24								
		7:0				UBLE	N[7:0]			
0.045-	VD1110 0::==:	15:8				UBLE				
0x01B0	XDMAC_CUBC5	23:16					I[23:16]			
		31:24					-			
		7:0				BLEN	N[7:0]			
	\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \	15:8						BLEN	I[11:8]	
0x01B4	XDMAC_CBC5	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
		15:8		DIF	SIF		TH[1:0]	IVID OIZ	CSIZE[2:0]	<u>-</u>
0x01B8	XDMAC_CC5	23:16	WRIP	RDIP	INITD	31110		M[1:0]		1[1:0]
		31:24					PERID[6:0]	F1	2, 11	L 174
		1					[0.0]			

cont	tinued									
Offset	Name	Bit Pos.								
Onset	Name					252.				
	VD1440 0D0 140D	7:0					ISP[7:0]			
0x01BC	XDMAC_CDS_MSP 5	15:8					SP[15:8]			
	5	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0				SUB	S[7:0]			
0x01C0	XDMAC_CSUS5	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24				5.15	0.5			
		7:0					S[7:0]			
0x01C4	XDMAC_CDUS5	15:8					S[15:8]			
		23:16				DOBS	[23:16]			
00400		31:24								
0x01C8	Decembed									
 0x01CF	Reserved									
UXUTOF		7:0		POIE	WALE	DDIE	EIE	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x01D0	XDMAC_CIE6	23:16								
		31:24								
				DOID	WELD	DDEID	FID	DID	LID	DID
		7:0 15:8		ROID	WBEID	RBEID	FID	DID	LID	BID
0x01D4	XDMAC_CID6									
		23:16								
		31:24		DOIM	VA/DEIN4	DDEIM	E1N4	DIM	1.154	DIM
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x01D8	XDMAC_CIM6	15:8								
		23:16								
		31:24		5010	14/2510	55510	=10	510		510
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x01DC	XDMAC_CIS6	15:8								
	_	23:16								
		31:24				0.41	17.01			
		7:0					[7:0]			
0x01E0	XDMAC_CSA6	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x01E4	XDMAC_CDA6	15:8					15:8]			
		23:16					23:16]			
		31:24			ND		31:24]			NDAIE
		7:0			NDA	N[5:0]	[40.0]			NDAIF
0x01E8	XDMAC_CNDA6	15:8					[13:6]			
		23:16					21:14]			
		31:24					29:22]	NDDUD	NDCUD	NDC
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x01EC	XDMAC_CNDC6	15:8								
	_	23:16								
		31:24				115: 5	NITZ-01			
		7:0					N[7:0]			
0x01F0	XDMAC_CUBC6	15:8					N[15:8]			
	_	23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLE	N[7:0]	·	1544 03	
0x01F4	XDMAC_CBC6	15:8						BLEN	[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x01F8	XDMAC_CC6	15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
5	7.210_000	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

cont	inued									
		Dia B								
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x01FC	XDMAC_CDS_MSP	15:8				SDS_M				
0,1011	6	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0				SUB				
0x0200	XDMAC_CSUS6	15:8				SUBS				
0.0200	7.510_0000	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0204	XDMAC_CDUS6	15:8					S[15:8]			
		23:16				DUBS	[23:16]			
		31:24								
0x0208										
	Reserved									
0x020F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0210	XDMAC_CIE7	15:8								
-		23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0214	XDMAC_CID7	15:8								
		23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0218	XDMAC_CIM7	15:8								
		23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x021C	XDMAC_CIS7	15:8								
0.0210	XBW/(0_0)01	23:16								
		31:24								
		7:0					7:0]			
0x0220	XDMAC_CSA7	15:8					15:8]			
0,10220	7121111110_007111	23:16					3:16]			
		31:24				SA[3				
		7:0					[7:0]			
0x0224	XDMAC CDA7	15:8					15:8]			
5ULLT	7.2(0_00/(1	23:16					3:16]			
		31:24				DA[3	1:24]			
		7:0			NDA	<b>\</b> [5:0]				NDAIF
0x0228	XDMAC_CNDA7	15:8				NDA				
00220		23:16					21:14]			
		31:24					29:22]			
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x022C	XDMAC_CNDC7	15:8								
0.0220	ADMAG_CIVDO7	23:16								
		31:24								
		7:0					N[7:0]			
0x0230	XDMAC_CUBC7	15:8				UBLE				
0.0230	ADMAG_CODG/	23:16				UBLEN	I[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
0x0234	XDMAC_CBC7	15:8						BLEN	I[11:8]	
UXUZ34	VDIMING_CDC1	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
0x0238	XDMAC_CC7	15:8		DIF	SIF	DWID	TH[1:0]		CSIZE[2:0]	
UXU236	VDINIWC_CC/	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	<b>1</b> [1:0]
		31:24					PERID[6:0]			

cont	inued									
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x023C	XDMAC_CDS_MSP	15:8				SDS_M				
*****	7	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0				SUB				
0x0240	XDMAC_CSUS7	15:8				SUBS				
		23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0244	XDMAC_CDUS7	15:8					S[15:8]			
		23:16				DORS	[23:16]			
0.0040		31:24								
0x0248	Reserved									
 0x024F	Reserved									
0.0241		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
		15:8		NOIL	AADIC	NDIE	1 15	DIE	LIL	DIL
0x0250	XDMAC_CIE8	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8			.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			2.3		5.5
0x0254	XDMAC_CID8	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
0x0258	XDMAC_CIM8	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
0x025C	XDMAC_CIS8	23:16								
		31:24								
		7:0				SA[	7:0]			
0,0000	VDMAC CCAG	15:8				SA[	15:8]			
0x0260	XDMAC_CSA8	23:16				SA[2	3:16]			
		31:24				SA[3	1:24]			
		7:0				DA[	[7:0]			
0x0264	XDMAC CDA8	15:8				DA[	15:8]			
0.0204	ADMAC_CDA0	23:16				DA[2	3:16]			
		31:24				DA[3	1:24]			
		7:0			NDA	A[5:0]				NDAIF
0x0268	XDMAC_CNDA8	15:8				NDA				
0,0200	ABNIKO_ONDKO	23:16					21:14]			
		31:24					29:22]			
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x026C	XDMAC_CNDC8	15:8								
		23:16								
		31:24								
		7:0					N[7:0]			
0x0270	XDMAC_CUBC8	15:8				UBLE				
-		23:16				UBLEN	I[23:16]			
		31:24					II - 01			
		7:0				BLEN	N[7:0]		1544 07	
0x0274	XDMAC_CBC8	15:8						BLEN	[11:8]	
		23:16								
		31:24	NENO==	014/5=0		D0):::0			75(4.0)	T) / D =
		7:0	MEMSET	SWREQ	015	DSYNC	TLU14-01	MBSIZ	ZE[1:0]	TYPE
0x0278	XDMAC_CC8	15:8	MDID	DIF	SIF	DWID	TH[1:0]	M14 - 01	CSIZE[2:0]	174 - 01
	_	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

cont	tinued									
		Dia B								
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x027C	XDMAC_CDS_MSP	15:8				SDS_M				
0,102.0	8	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x0280	XDMAC_CSUS8	15:8				SUBS				
0.0200	713111110_0000	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0284	XDMAC_CDUS8	15:8					S[15:8]			
		23:16				DUBS	[23:16]			
		31:24								
0x0288										
	Reserved									
0x028F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0290	XDMAC_CIE9	15:8								
		23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0294	XDMAC_CID9	15:8								
0,1020	7151111110_0.50	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0298	XDMAC_CIM9	15:8								
0.0200	ADM/ to_OM/o	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x029C	XDMAC_CIS9	15:8								
0.0230	XBW/XO_0103	23:16								
		31:24								
		7:0					[7:0]			
0x02A0	XDMAC_CSA9	15:8					15:8]			
0.02710	ADIVINO_OUNG	23:16					3:16]			
		31:24				SA[3				
		7:0					[7:0]			
0x02A4	XDMAC_CDA9	15:8					15:8]			
UNULA	YPINI/O_ODA9	23:16					3:16]			
		31:24				DA[3	1:24]			
		7:0			NDA	<b>\</b> [5:0]				NDAIF
0x02A8	XDMAC_CNDA9	15:8				NDA				
UNUZMU	VDINIUO_CIADVA	23:16					21:14]			
		31:24					29:22]			
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x02AC	XDMAC_CNDC9	15:8								
UXUZAC	VDINIMO_CIADCA	23:16								
		31:24								
		7:0					N[7:0]			
0,0000	VDMAC CURCO	15:8				UBLE	N[15:8]			
0x02B0	XDMAC_CUBC9	23:16					I[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
0,000 4	VDMAC OBOC	15:8						BLEN	[11:8]	
0x02B4	XDMAC_CBC9	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
	V=14.5	15:8		DIF	SIF		TH[1:0]		CSIZE[2:0]	1
0x02B8	XDMAC_CC9	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	I[1:0]
		31:24					PERID[6:0]			
							[]			

cont	tinued									
Offset	Name	Bit Pos.								
Onset	Name					252.	10017 01			
		7:0					1SP[7:0]			
0x02BC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	9	23:16					MSP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x02C0	XDMAC_CSUS9	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24				DUD	017.01			
		7:0					S[7:0]			
0x02C4	XDMAC_CDUS9	15:8					S[15:8]			
		23:16				DORS	[23:16]			
00000		31:24								
0x02C8	Decembed									
 0x02CF	Reserved									
UXUZCF		7:0		POIE	WALE	DDIE	CIC	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x02D0	XDMAC_CIE10	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	EID	DID	LID	PID
		15:8		KOID	WEID	LOEID	FID	DID	LID	BID
0x02D4	XDMAC_CID10	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8		KOIW	MPCIIN	KDEIIVI	FIIVI	DIIVI	LIIVI	DIIVI
0x02D8	XDMAC_CIM10	23:16								
		31:24		DOIG	MDEIO	DDEIG	FIG	DIO	1.10	DIO
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x02DC	XDMAC_CIS10	15:8								
		23:16								
		31:24 7:0				0.41	17.01			
		15:8					[7:0]			
0x02E0	XDMAC_CSA10						15:8]			
		23:16					23:16]			
		31:24 7:0					31:24] [7:0]			
		15:8					15:8]			
0x02E4	XDMAC_CDA10	23:16					23:16]			
		31:24					31:24]			
		7:0			NIDA	\[5:0]	01.24]			NDAIF
		15:8			NUF		[13:6]			NDAIF
0x02E8	XDMAC_CNDA10	23:16					21:14]			
		31:24					29:22]			
		7:0					29:22] EW[1:0]	NDDUP	NDSUP	NDE
		15:8				INDVIE	_vv[1.0]	INDDUF	NDOUP	INDE
0x02EC	XDMAC_CNDC10	23:16								
		31:24								
		7:0				I IDI F	[N[7:0]			
		15:8					N[15:8]			
0x02F0	XDMAC_CUBC10	23:16					N[15:8] N[23:16]			
						UBLEN	N[Z3.10]			
		31:24 7:0				ם כי	N[7:0]			
						BLEI	N[7:0]	DIEN	1[44.0]	
0x02F4	XDMAC_CBC10	15:8						BLEN	[11:8]	
	_	23:16								
		31:24	MENAGET	OMDEO		DOVALO		1100	75[4.03	TVDE
		7:0	MEMSET	SWREQ	OIF.	DSYNC	TU(4.03	MBSIZ		TYPE
0x02F8	XDMAC_CC10	15:8	WDID	DIF	SIF	DWID	TH[1:0]	M[4.0]	CSIZE[2:0]	[4.0]
	_	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name									
		7:0					ISP[7:0]			
0x02FC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	10	23:16					1SP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x0300	XDMAC_CSUS10	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0304	XDMAC_CDUS10	15:8					S[15:8]			
	_	23:16				DUBS	[23:16]			
		31:24								
0x0308										
	Reserved									
0x030F				50.5		55.5		5.5		5.5
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0310	XDMAC_CIE11	15:8								
	_	23:16								
		31:24			==					
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0314	XDMAC_CID11	15:8								
	_	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0318	XDMAC_CIM11	15:8								
		23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x031C	XDMAC_CIS11	15:8								
		23:16								
		31:24								
		7:0					[7:0]			
0x0320	XDMAC_CSA11	15:8					15:8]			
		23:16					23:16]			
		31:24					1:24]			
		7:0					[7:0]			
0x0324	XDMAC_CDA11	15:8					15:8]			
		23:16					23:16]			
		31:24					31:24]			
		7:0			NDA					NDAIF
0x0328	XDMAC_CNDA11	15:8					[13:6]			
0.0020	//ZZ//// // // // // // // // // // // /	23:16					21:14]			
		31:24					29:22]			
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x032C	XDMAC_CNDC11	15:8								
		23:16								
		31:24								
		7:0					N[7:0]			
0x0330	XDMAC_CUBC11	15:8					N[15:8]			
5		23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLEI	N[7:0]			
0x0334	XDMAC_CBC11	15:8						BLEN	[11:8]	
0A033 <del>4</del>	YPINIUO_ODO II	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x0338	VDMAC CC11	15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
UXUSSO	XDMAC_CC11	23:16	WRIP	RDIP	INITD		DAI	M[1:0]	SAM	[1:0]
	1	31:24					PERID[6:0]			

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name					252.	100:00:00			
		7:0					MSP[7:0]			
0x033C	XDMAC_CDS_MSP	15:8					SP[15:8]			
	11	23:16					MSP[7:0]			
		31:24					ISP[15:8]			
		7:0					S[7:0]			
0x0340	XDMAC_CSUS11	15:8					S[15:8]			
		23:16				SUBS	[23:16]			
		31:24				DUD	017.01			
		7:0					S[7:0]			
0x0344	XDMAC_CDUS11	15:8					S[15:8]			
		23:16				DOBS	[23:16]			
00040		31:24								
0x0348	Decembed									
 0x034F	Reserved									
UXU34F		7:0		POIE	WALE	DDIE	EIE	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0350	XDMAC_CIE12	23:16								
		31:24								
				DOID	WELD	DDEID	FID	DID	LID	DID
		7:0 15:8		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0354	XDMAC_CID12									
		23:16								
		31:24		DOIM	VA/DEIN4	DDEIM	FINA	DIM	1.154	DIM
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0358	XDMAC_CIM12	15:8								
		23:16								
		31:24		5010	14/2510	55510	=	5.0		510
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x035C	XDMAC_CIS12	15:8								
	_	23:16								
		31:24				0.41				
		7:0					[7:0]			
0x0360	XDMAC_CSA12	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x0364	XDMAC_CDA12	15:8					15:8]			
		23:16					23:16]			
		31:24			ND		31:24]			NDAIE
		7:0			NDA	N[5:0]	[40.0]			NDAIF
0x0368	XDMAC_CNDA12	15:8					[13:6]			
		23:16					[21:14]			
		31:24					[29:22]	NDDUD	NDCUD	NDC
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x036C	XDMAC_CNDC12	15:8								
		23:16								
		31:24				115: 5	NICZ-01			
		7:0					EN[7:0]			
0x0370	XDMAC_CUBC12	15:8					N[15:8]			
	_	23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLE	N[7:0]	·	1544 03	
0x0374	XDMAC_CBC12	15:8						BLEN	[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x0378	XDMAC_CC12	15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
		23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

cont	tinued									
Offset	Name	Bit Pos.								
		7:0				SDS_M	SD[7:0]			
	VDMAC CDS MSD	15:8				SDS_MS				
0x037C	XDMAC_CDS_MSP 12	23:16				DDS_M				
	12									
		31:24				DDS_MS				
		7:0				SUBS				
0x0380	XDMAC_CSUS12	15:8				SUBS				
		23:16		I		SUBS[	[23:16]			
		31:24								
		7:0				DUBS				
0x0384	XDMAC_CDUS12	15:8				DUBS				
	_	23:16				DUBS	[23:16]			
		31:24								
0x0388										
	Reserved									
0x038F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0390	XDMAC_CIE13	15:8								
55000	1.515_512.16	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0394	XDMAC_CID13	15:8								
0,00004	ADMAC_CID 13	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
00000	VDMAO OIMAO	15:8								
0x0398	0398 XDMAC_CIM13	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
0x039C	XDMAC_CIS13	23:16								
		31:24								
		7:0				SA[	7:01			
		15:8				SA[1				
0x03A0	XDMAC_CSA13	23:16				SA[2				
		31:24				SA[3				
		7:0				DA[				
		15:8				DA[1				
0x03A4	XDMAC_CDA13	23:16				DA[2				
		31:24				DA[3				
		7:0			NDA					NDAIF
		15:8			140/	NDA[	13:61			110/111
0x03A8	XDMAC_CNDA13	23:16				NDA[2				
		31:24				NDA[2				
		7:0				NDVIE		NDDUP	NDSUP	NDE
		15:8				INDVIE	[]	INDDOF	14200F	NDE
0x03AC	XDMAC_CNDC13	23:16								
		31:24				LIDIT	NI[7:0]			
		7:0				UBLE				
0x03B0	XDMAC_CUBC13	15:8				UBLEN				
		23:16				UBLEN	[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
0x03B4	XDMAC_CBC13	15:8						BLEN	I[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
	XDMAC_CC13	15:8		DIF	SIF	DWIDT			CSIZE[2:0]	
UXU3E8			WDID	RDIP	INITD		DVI	M[1:0]	SAM	[1.0]
0x03B8	ADIVIAC_CC13	23:16 31:24	WRIP	KUIF	טווווו		PERID[6:0]	vi[ 1.0]	SAIV	[1.0]

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name									
		7:0					MSP[7:0]			
0x03BC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	13	23:16					//SP[7:0]			
		31:24					ISP[15:8]			
		7:0					S[7:0]			
0x03C0	XDMAC_CSUS13	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x03C4	XDMAC_CDUS13	15:8					S[15:8]			
	_	23:16				DUBS	[23:16]			
		31:24								
0x03C8										
	Reserved									
0x03CF				5015		55.5		5.5		5.5
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x03D0	XDMAC_CIE14	15:8								
	_	23:16								
		31:24			==:=					
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x03D4	XDMAC_CID14	15:8								
	_	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x03D8	XDMAC_CIM14	15:8								
	OSDO ADMAC_CIMITA	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x03DC	XDMAC_CIS14	15:8								
		23:16								
		31:24								
		7:0					[7:0]			
0x03E0	XDMAC_CSA14	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x03E4	XDMAC CDA14	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0			NDA	\[5:0]				NDAIF
0x03E8	XDMAC_CNDA14	15:8					[13:6]			
		23:16					21:14]			
		31:24					[29:22]			
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x03EC	XDMAC_CNDC14	15:8								
		23:16								
		31:24								
		7:0					N[7:0]			
0x03F0	XDMAC_CUBC14	15:8					N[15:8]			
		23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLEI	N[7:0]			
0x03F4	XDMAC_CBC14	15:8						BLEN	[11:8]	
3,001 7	7.00014	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x03F8	XDMAC_CC14	15:8		DIF	SIF	DWID	TH[1:0]		CSIZE[2:0]	
UNUUFO	ADIVIAO_0014	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

con1	tinued											
Offset	Name	Bit Pos.										
Oliset	Name					252.						
	V	7:0					ISP[7:0]					
0x03FC	XDMAC_CDS_MSP	15:8					SP[15:8]					
	14	23:16				DDS_MSP[7:0]						
		31:24					SP[15:8]					
		7:0					S[7:0]					
0x0400	XDMAC_CSUS14	15:8					S[15:8]					
		23:16				SUBS	[23:16]					
		31:24				DUD	017-01					
		7:0					S[7:0]					
0x0404	XDMAC_CDUS14	15:8					S[15:8]					
		23:16				DOBS	[23:16]					
0:-0400		31:24										
0x0408	Decembed											
 0x040F	Reserved											
UXU4UF		7:0		POIE	WAL	DDIE	EIE	DIE	LIE	DIE		
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE		
0x0410	XDMAC_CIE15	23:16										
		31:24 7:0		ROID	WBEID	RBEID	FID	DID	LID	BIL		
				KUID	WEID	KDEID	FID	DID	LID	BID		
0x0414	XDMAC_CID15	15:8										
		23:16										
		31:24		DOIM	VA/DEIN4	DDEIM	E1N4	DIM	1.154	DIM		
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM		
0x0418	0418 XDMAC_CIM15	15:8										
		23:16										
		31:24		5010	11/25/10	55510	=10	510		510		
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS		
0x041C	XDMAC_CIS15	15:8										
	_	23:16										
		31:24				0.41	17.01					
		7:0					[7:0]					
0x0420	XDMAC_CSA15	15:8					15:8]					
	_	23:16					23:16]					
		31:24					31:24]					
		7:0					[7:0]					
0x0424	XDMAC_CDA15	15:8					15:8]					
		23:16					23:16]					
		31:24			ND		31:24]			NDAIE		
		7:0			NDA	N[5:0]	r40.01			NDAIF		
0x0428	XDMAC_CNDA15	15:8					[13:6]					
	_	23:16					21:14]					
		31:24					29:22]	NDSUS	NDCUE	NDE		
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE		
0x042C	XDMAC_CNDC15	15:8										
		23:16										
		31:24				115: 5	NITZ-01					
		7:0					N[7:0]					
0x0430	XDMAC_CUBC15	15:8					N[15:8]					
	_	23:16				UBLEN	N[23:16]					
		31:24										
		7:0				BLE	N[7:0]	·	1544 01			
0x0434	XDMAC_CBC15	15:8						BLEN	I[11:8]			
		23:16										
		31:24										
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE		
0x0438	XDMAC_CC15	15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]			
		23:16	WRIP	RDIP	INITD			M[1:0]	SAM	I[1:0]		
		31:24					PERID[6:0]					

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name									
		7:0					MSP[7:0]			
0x043C	XDMAC_CDS_MSP	15:8					SP[15:8]			
	15	23:16					/ISP[7:0]			
		31:24					ISP[15:8]			
		7:0					S[7:0]			
0x0440	XDMAC_CSUS15	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0444	XDMAC_CDUS15	15:8					S[15:8]			
	_	23:16				DUBS	[23:16]			
		31:24								
0x0448	Danamad									
	Reserved									
0x044F		7.0		DOLE	WDIE	DDIE	FIE	DIE		DIE
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0450	XDMAC_CIE16	15:8								
		23:16								
		31:24		DOID	WDEID	DDEID	E.D	DiD	LID	חים
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0454	XDMAC_CID16	15:8								
	_	23:16								
		31:24		50114	)A/DEIA	DDEM	F15.4	504		5114
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0458	XDMAC_CIM16	15:8								
	ADIVINO_CINITO	23:16								
		31:24			==					
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x045C	XDMAC_CIS16	15:8								
	_	23:16								
		31:24								
		7:0					[7:0]			
0x0460	XDMAC_CSA16	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x0464	XDMAC_CDA16	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0			NDA	<b>\[5:0]</b>				NDAIF
0x0468	XDMAC_CNDA16	15:8					[13:6]			
		23:16					[21:14]			
		31:24					[29:22]			
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x046C	XDMAC_CNDC16	15:8								
		23:16								
		31:24								
		7:0					N[7:0]			
0x0470	XDMAC_CUBC16	15:8					N[15:8]			
2		23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLEI	N[7:0]			
0x0474	XDMAC_CBC16	15:8						BLEN	[11:8]	
570717	7.5.0.0010	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x0478	XDMAC_CC16	15:8		DIF	SIF	DWID	TH[1:0]		CSIZE[2:0]	
UAU410	VPINIMO_CC 10	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
	1	31:24					PERID[6:0]			

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name									
		7:0					1SP[7:0]			
0x047C	XDMAC_CDS_MSP	15:8					SP[15:8]			
	16	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x0480	XDMAC_CSUS16	15:8					S[15:8]			
	_	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0484	XDMAC_CDUS16	15:8					S[15:8]			
	_	23:16				DUBS	[23:16]			
		31:24								
0x0488										
	Reserved									
0x048F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0490	XDMAC_CIE17	15:8								
	1_21_1	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0494	XDMAC_CID17	15:8								
		23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0498	XDMAC_CIM17	15:8								
	J490 ADIVIAC_CIVITY	23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x049C	XDMAC_CIS17	15:8								
000100	7.511.710_01017	23:16								
		31:24								
		7:0					[7:0]			
0x04A0	XDMAC_CSA17	15:8					15:8]			
0.00 17 10	7.2	23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x04A4	XDMAC_CDA17	15:8					15:8]			
0.001711	XBINITO_OBYTT	23:16					23:16]			
		31:24					31:24]			
		7:0			NDA					NDAIF
0x04A8	XDMAC_CNDA17	15:8					[13:6]			
ひんしすれし	ADM/ IO_ONDAT/	23:16					21:14]			
		31:24					29:22]			
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x04AC	XDMAC_CNDC17	15:8								
UNU4AC	VDIMVO_CIADCIA	23:16								
		31:24								
		7:0					N[7:0]			
0x04B0	XDMAC_CUBC17	15:8					N[15:8]			
UXU4DU	ADMAC_COBC17	23:16				UBLEN	N[23:16]			
	<u> </u>	31:24								
		7:0				BLEI	N[7:0]			
0x04B4	VDMAC CBC47	15:8						BLEN	[11:8]	
UXU4B4	XDMAC_CBC17	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
00450	VD144 C CC4=	15:8		DIF	SIF		TH[1:0]		CSIZE[2:0]	
0x04B8	XDMAC_CC17	23:16	WRIP	RDIP	INITD			M[1:0]		[1:0]
		31:24					PERID[6:0]		-	

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name					252.				
		7:0					ISP[7:0]			
0x04BC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	17	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x04C0	XDMAC_CSUS17	15:8					S[15:8]			
		23:16				SUBS	[23:16]			
		31:24				DUD	017-01			
		7:0					S[7:0]			
0x04C4	XDMAC_CDUS17	15:8					S[15:8]			
		23:16				DORS	[23:16]			
00400		31:24								
0x04C8	Decembed									
 0x04CF	Reserved									
UXU4CF		7:0		POIE	WALE	DDIE	CIC	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x04D0	XDMAC_CIE18	23:16								
		31:24 7:0		ROID	WBEID	RBEID	EID	DID	ΠD	BID
		7:0 15:8		KOID	WEID	KDEID	FID	DID	LID	BID
0x04D4	XDMAC_CID18									
		23:16								
		31:24		DOIM	VA/DEIN4	DDEIM	FINA	DIM	1.154	DIM
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x04D8	04D8 XDMAC_CIM18	15:8								
		23:16								
		31:24		5010	14/2510	55510	=10	510		510
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x04DC	XDMAC_CIS18	15:8								
	_	23:16								
		31:24				0.41	7.01			
		7:0					[7:0]			
0x04E0	XDMAC_CSA18	15:8					15:8]			
	_	23:16					3:16]			
		31:24					1:24]			
		7:0					[7:0]			
0x04E4	XDMAC_CDA18	15:8					15:8]			
		23:16					23:16]			
		31:24			ND		31:24]			NDAIE
		7:0			NDA	N[5:0]	[40.0]			NDAIF
0x04E8	XDMAC_CNDA18	15:8					[13:6]			
		23:16					21:14]			
		31:24					29:22]	NDDUD	NDCUD	NDE
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x04EC	XDMAC_CNDC18	15:8								
		23:16								
		31:24				115: 5	NIT-01			
		7:0					N[7:0]			
0x04F0	XDMAC_CUBC18	15:8					N[15:8]			
	_	23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLE	V[7:0]	<b></b>	1544 03	
0x04F4	XDMAC_CBC18	15:8						BLEN	[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x04F8	XDMAC_CC18	15:8	14/5:-	DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
- · <del>-</del>		23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

cont	tinued									
Offset	Name	Bit Pos.								
Oliset	Name					202				
	VD1440 0D0 140D	7:0					ISP[7:0]			
0x04FC	XDMAC_CDS_MSP 18	15:8					SP[15:8]			
	18	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x0500	XDMAC_CSUS18	15:8				SUBS				
	_	23:16				SUBS	[23:16]			
		31:24				DUD	017-01			
		7:0					S[7:0]			
0x0504	XDMAC_CDUS18	15:8					S[15:8]			
		23:16				D0B2	[23:16]			
0,0500		31:24								
0x0508	Reserved									
 0x050F	Reserved									
UXUSUF		7:0		POIE	WALE	DDIE	CIC	DIE	LIE	BIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	DIE
0x0510	XDMAC_CIE19	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8		KOID	WEID	KDEID	LID	טוט	LID	DID
0x0514	XDMAC_CID19	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8		KOIW	MPCIIN	KDEIIVI	FIIVI	DIIVI	LIIVI	DIIVI
0x0518	XDMAC_CIM19	23:16								
		31:24		DOIC	WDEIC	DDEIC	FIC	DIC	1.10	DIC
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x051C	XDMAC_CIS19	15:8								
		23:16								
		31:24 7:0				0.41	7.01			
							7:0]			
0x0520	XDMAC_CSA19	15:8					15:8]			
		23:16					3:16]			
		31:24					1:24] [7:0]			
		7:0 15:8					[7:0] 15:8]			
0x0524	XDMAC_CDA19									
		23:16					3:16]			
		31:24 7:0			NID A		1:24]			NDAIF
		15:8			NUF	NDA	[13:6]			NUAIF
0x0528	XDMAC_CNDA19	23:16					21:14]			
		31:24					29:22]			
		7:0					29:22] :W[1:0]	NDDUP	NDSUP	NDE
		15:8				INDAIE	. v v [ 1.0]	INDDUF	NDOUP	INDE
0x052C	XDMAC_CNDC19	23:16								
		31:24								
		7:0				I IDI F	N[7:0]			
		15:8					N[7:0] N[15:8]			
0x0530	XDMAC_CUBC19	23:16					N[15:6] N[23:16]			
		31:24				UBLEN	([23.10]			
		7:0				DI E	N[7:0]			
		15:8				DLEI	<b>ν</b> [	DI EN	[11:8]	
0x0534	XDMAC_CBC19	23:16						DLEN	[11.0]	
		31:24	MEMOET	SWIDEO		DSYNC		MDOL	7⊏[1·0]	TVDE
		7:0	MEMSET	SWREQ DIF	SIF		TH[1:0]	MBSIZ	ZE[1:0] CSIZE[2:0]	TYPE
0x0538	XDMAC_CC19	15:8	WRIP	RDIP		טויאט		M[1·0]		I[1·∩]
		23:16 31:24	WKIP	אטוץ	INITD		PERID[6:0]	M[1:0]	SAM	[ ι .υ]
		J1.24					רבעוט[ס:0]			

con	tinued									
		Dit D								
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x053C	XDMAC_CDS_MSP	15:8				SDS_M				
	19	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0				SUB				
0x0540	XDMAC_CSUS19	15:8				SUBS				
onco io	7.2.110_00010	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0544	XDMAC_CDUS19	15:8					S[15:8]			
		23:16				DUBS	[23:16]			ı
		31:24								
0x0548										
	Reserved									
0x054F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0550	XDMAC_CIE20	15:8								
	1	23:16								
		31:24								_
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0554	XDMAC_CID20	15:8								
		23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0558	XDMAC_CIM20	15:8								
		23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x055C	XDMAC_CIS20	15:8								
0,0000	7.5111/10_01020	23:16								
		31:24								
		7:0					7:0]			
0x0560	XDMAC_CSA20	15:8					15:8]			
CACCCC	712111110_001120	23:16					3:16]			
		31:24				SA[3				
		7:0					[7:0]			
0x0564	XDMAC_CDA20	15:8					15:8]			
OXOGO!	7.510_057.20	23:16					3:16]			
		31:24				DA[3	1:24]			
		7:0			NDA	<b>\</b> [5:0]				NDAIF
0x0568	XDMAC_CNDA20	15:8				NDA				
55555	1.2 1.5_01427.120	23:16					21:14]			
		31:24				NDA[				ı
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x056C	XDMAC_CNDC20	15:8								
0,0000	7.5.00 10_0145020	23:16								
		31:24								
		7:0					N[7:0]			
0x0570	XDMAC CUBC20	15:8				UBLE				
0,0370	ADIVIAO_COBC20	23:16				UBLEN	I[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
0x0574	XDMAC_CBC20	15:8						BLEN	I[11:8]	
0.00074	ADIVIAC_CBC20	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
0x0578	XDMAC_CC20	15:8		DIF	SIF	DWID	TH[1:0]		CSIZE[2:0]	
0,007.0	ADIVIAC_CC20	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	1[1:0]
		31:24					PERID[6:0]			
				-						

con1	tinued									
		Dit D								
Offset	Name	Bit Pos.								
		7:0					ISP[7:0]			
0x057C	XDMAC_CDS_MSP	15:8				SDS_M				
	20	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0				SUB				
0x0580	XDMAC_CSUS20	15:8				SUBS				
onocco	7.510_00020	23:16				SUBS	[23:16]			
		31:24								
		7:0					S[7:0]			
0x0584	XDMAC_CDUS20	15:8					S[15:8]			
		23:16				DUBS	[23:16]			
		31:24								
0x0588										
	Reserved									
0x058F										
		7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0590	XDMAC_CIE21	15:8								
		23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
0x0594	XDMAC_CID21	15:8								
		23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x0598	XDMAC_CIM21	15:8								
		23:16								
		31:24								
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x059C	XDMAC_CIS21	15:8								
OXOCCO	XBW/10_01021	23:16								
		31:24								
		7:0					7:0]			
0x05A0	XDMAC_CSA21	15:8					15:8]			
0,000,10	7.5.110_007.12.1	23:16					3:16]			
		31:24				SA[3				
		7:0					[7:0]			
0x05A4	XDMAC CDA21	15:8					15:8]			
500/14	7.210_05/121	23:16					3:16]			
		31:24				DA[3	1:24]			
		7:0			NDA	A[5:0]				NDAIF
0x05A8	XDMAC_CNDA21	15:8				NDA				
0.00A0	ADMINO_ONDAZI	23:16					21:14]			
		31:24				NDA[				
		7:0				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
0x05AC	XDMAC_CNDC21	15:8								
UNUSAU	ADIVIAO_CINDO21	23:16								
		31:24								
		7:0					N[7:0]			
0x05B0	XDMAC_CUBC21	15:8				UBLE				
UAUODU	ADIVIAC_COBC21	23:16				UBLEN	I[23:16]			
		31:24								
		7:0				BLEN	N[7:0]			
0x05B4	VDMAC CBCC4	15:8						BLEN	[11:8]	
いえいつば4	XDMAC_CBC21	23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
OVOEDO	VDMAC COS4	15:8		DIF	SIF	DWID	TH[1:0]		CSIZE[2:0]	
0x05B8	XDMAC_CC21	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	I[1:0]
		31:24					PERID[6:0]			
	-									

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name					252.				
		7:0					ISP[7:0]			
0x05BC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	21	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x05C0	XDMAC_CSUS21	15:8					S[15:8]			
		23:16				SUBS	[23:16]			
		31:24				DUD	017.01			
		7:0					S[7:0]			
0x05C4	XDMAC_CDUS21	15:8					S[15:8]			
		23:16				DOBS	[23:16]			
00500		31:24								
0x05C8	Decembed									
 0x05CF	Reserved									
UXUSCF		7:0		POIE	WALE	DDIE	EIE	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x05D0	XDMAC_CIE22	23:16								
		31:24 7:0		ROID	WBEID	RBEID	EID	DID	ΠD	חום
		7:0 15:8		KOID	WEID	KDEID	FID	DID	LID	BID
0x05D4	XDMAC_CID22									
		23:16								
		31:24		DOIM	VA/DEIN4	DDEIM	E1N4	DIM	1.154	DIM
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
0x05D8	D5D8 XDMAC_CIM22	15:8								
		23:16								
		31:24		5010	14/2510	55510	=10	5.0		510
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x05DC	XDMAC_CIS22	15:8								
	_	23:16								
		31:24				0.41	17.01			
		7:0					[7:0]			
0x05E0	XDMAC_CSA22	15:8					15:8]			
	_	23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0]			
0x05E4	XDMAC_CDA22	15:8					15:8]			
		23:16					23:16]			
		31:24			ND		31:24]			NDAIE
		7:0			NDA	N[5:0]	r40.01			NDAIF
0x05E8	XDMAC_CNDA22	15:8					[13:6]			
	_	23:16					21:14]			
		31:24					29:22]	NDDUP	NDCUD	NDC
		7:0				NDVIE	EW[1:0]	NDDUP	NDSUP	NDE
0x05EC	XDMAC_CNDC22	15:8								
		23:16								
		31:24				115: 5	NITZ-01			
		7:0					N[7:0]			
0x05F0	XDMAC_CUBC22	15:8					N[15:8]			
	_	23:16				UBLEN	N[23:16]			
		31:24								
		7:0				BLE	N[7:0]	·	1544 03	
0x05F4	XDMAC_CBC22	15:8						BLEN	[11:8]	
		23:16								
		31:24								
		7:0	MEMSET	SWREQ		DSYNC		MBSIZ		TYPE
0x05F8	XDMAC_CC22	15:8		DIF	SIF	DWID.	TH[1:0]		CSIZE[2:0]	
		23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

con1	tinued									
Offset	Name	Bit Pos.								
Oliset	Name					252.				
		7:0					ISP[7:0]			
0x05FC	XDMAC_CDS_MSP	15:8					SP[15:8]			
	22	23:16					ISP[7:0]			
		31:24					SP[15:8]			
		7:0					S[7:0]			
0x0600	XDMAC_CSUS22	15:8					S[15:8]			
		23:16				SUBS	[23:16]			
		31:24				DUD	017-01			
		7:0					S[7:0]			
0x0604	XDMAC_CDUS22	15:8					S[15:8]			
		23:16				D082	[23:16]			
00000		31:24								
0x0608	Reserved									
 0x060F	Reserved									
UXUUUF		7:0		POIE	WALE	DDIE	EIE	DIE	LIE	DIE
		7:0 15:8		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
0x0610	XDMAC_CIE23	23:16								
		31:24								
		7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8		KOID	WEID	NDEID	רוט	טוט	LID	טוט
0x0614	XDMAC_CID23	23:16								
		31:24								
		7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8		KOIW	MPCIIN	KDEIIVI	FIIVI	DIIVI	LIIVI	DIIVI
0x0618	0618 XDMAC_CIM23	23:16								
		31:24		DOIG	MDEIO	DDEIG	FIG	DIO	1.10	DIO
		7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
0x061C	XDMAC_CIS23	15:8								
		23:16								
		31:24 7:0				0.41	17.01			
		15:8					[7:0]			
0x0620	XDMAC_CSA23						15:8]			
		23:16					23:16]			
		31:24					31:24]			
		7:0					[7:0] 15:0]			
0x0624	XDMAC_CDA23	15:8 23:16					15:8] 23:16]			
		31:24			ND	DA[3 [5:0]	31:24]			NDAIE
		7:0 15:8			NDF		[13:6]			NDAIF
0x0628	XDMAC_CNDA23	23:16					21:14]			
		31:24					29:22]	NDDUP	NDSUP	NDE
		7:0 15:8				NDVIE	EW[1:0]	NDDOP	NDSUP	NDE
0x062C	XDMAC_CNDC23									
		23:16								
		31:24				LIDIE	NITZ-01			
		7:0					N[7:0]			
0x0630	XDMAC_CUBC23	15:8					N[15:8]			
		23:16				ORLEN	N[23:16]			
		31:24				DI T	NITZ-01			
		7:0				BLEI	N[7:0]	DI E	1[44.0]	
0x0634	XDMAC_CBC23	15:8						BLÉN	I[11:8]	
	_	23:16								
		31:24	ME: :0==	01:75=		D0\#:=			7514.63	T. (2)
		7:0	MEMSET	SWREQ	0:=	DSYNC	T. 154 03	MBSIZ	ZE[1:0]	TYPE
0x0638	XDMAC_CC23	15:8	MOLO	DIF	SIF	DWID	TH[1:0]	M14 - 01	CSIZE[2:0]	1[4.0]
	_	23:16	WRIP	RDIP	INITD			M[1:0]	SAM	[1:0]
		31:24					PERID[6:0]			

**DMA Controller (XDMAC)** 

cont	tinued									
Offset	Name	Bit Pos.								
		7:0			SDS_M	ISP[7:0]			_	
0x063C	XDMAC_CDS_MSP	15:8			SDS_M	SP[15:8]			_	
UXU63C	23	23:16			DDS_N	ISP[7:0]				
		31:24	DDS_MSP[15:8]							
		7:0	SUBS[7:0]							
0x0640	VDMAC COLICOS	15:8	SUBS[15:8]							
UXU04U	XDMAC_CSUS23	23:16			SUBS	[23:16]				
		31:24								
		7:0			DUB	S[7:0]				
0x0644	VDMAC CDUIS22	15:8			DUBS	6[15:8]				
UXU044	XDMAC_CDUS23	23:16			DUBS	[23:16]				
		31:24								

**DMA Controller (XDMAC)** 

### 36.9.1 XDMAC Global Type Register

Name: XDMAC\_GTYPE

 Offset:
 0x00

 Reset:
 0x0000000

 Property:
 Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					NB_REQ[6:0]			
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				FIFO_S	SZ[10:3]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
		FIFO_SZ[2:0]				NB_CH[4:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 22:16 - NB\_REQ[6:0] Number of Peripheral Requests Minus One

Bits 15:5 - FIFO\_SZ[10:0] Number of Bytes

Bits 4:0 - NB\_CH[4:0] Number of Channels Minus One

**DMA Controller (XDMAC)** 

### 36.9.2 XDMAC Global Configuration Register

Name: XDMAC\_GCFG

 Offset:
 0x04

 Reset:
 0x0000000

 Property:
 Read/Write

Bit	31	30	29	28	27	26	25	24
Access		•				•		
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
								BXKBEN
Access								R/W
Reset								0
Bit	7	6	5	4	3	2	1	0
					CGDISIF	CGDISFIFO	CGDISPIPE	CGDISREG
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

#### Bit 8 - BXKBEN Boundary X Kilobyte Enable

Value	Description
0	The 1 Kbyte boundary is used.
1	The controller does not meet the AHB specification.

#### Bit 3 - CGDISIF Bus Interface Clock Gating Disable

Value	Description
0	The automatic clock gating is enabled for the system bus interface.
1	The automatic clock gating is disabled for the system bus interface.

### Bit 2 - CGDISFIFO FIFO Clock Gating Disable

Value	Description
0	The automatic clock gating is enabled for the main FIFO.
1	The automatic clock gating is disabled for the main FIFO.

### Bit 1 - CGDISPIPE Pipeline Clock Gating Disable

V	alue	Description
0		The automatic clock gating is enabled for the main pipeline.
1		The automatic clock gating is disabled for the main pipeline.

#### Bit 0 - CGDISREG Configuration Registers Clock Gating Disable

Value	Description
0	The automatic clock gating is enabled for the configuration registers.
1	The automatic clock gating is disabled for the configuration registers.

**DMA Controller (XDMAC)** 

### 36.9.3 XDMAC Global Weighted Arbiter Configuration Register

Name: XDMAC\_GWAC

 Offset:
 0x08

 Reset:
 0x0000000

 Property:
 Read/Write

Bit	31	30	29	28	27	26	25	24	
Access									
Reset									
Bit	23	22	21	20	19	18	17	16	
Access									
Reset									
Bit	15	14	13	12	11	10	9	8	
		PW3	3[3:0]		PW2[3:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
	· ·	· ·	· ·	· ·	· ·	· ·	· ·	· ·	
Bit	7	6	5	4	3	2	1	0	
5	•		[3:0]				)[3:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

#### Bits 15:12 - PW3[3:0] Pool Weight 3

This field indicates the weight of pool 3 in the arbitration scheme of the DMA scheduler.

#### Bits 11:8 - PW2[3:0] Pool Weight 2

This field indicates the weight of pool 2 in the arbitration scheme of the DMA scheduler.

### Bits 7:4 - PW1[3:0] Pool Weight 1

This field indicates the weight of pool 1 in the arbitration scheme of the DMA scheduler.

#### Bits 3:0 - PW0[3:0] Pool Weight 0

This field indicates the weight of pool 0 in the arbitration scheme of the DMA scheduler.

**DMA Controller (XDMAC)** 

### 36.9.4 XDMAC Global Interrupt Enable Register

Name: XDMAC\_GIE

Offset: 0x0C Reset: -

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access		•	•					
Reset								
Bit	23	22	21	20	19	18	17	16
	IE23	IE22	IE21	IE20	IE19	IE18	IE17	IE16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – IE XDMAC Channel x Interrupt Enable

Value	Description
0	This bit has no effect. The Channel x Interrupt Mask bit (XDMAC_GIM.IMx) is not modified.
1	The corresponding mask bit is set. The XDMAC Channel x Interrupt Status register (XDMAC_GIS) can generate an interrupt.

**DMA Controller (XDMAC)** 

## 36.9.5 XDMAC Global Interrupt Disable Register

Name: XDMAC\_GID

Offset: 0x10 Reset: -

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	-

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – ID XDMAC Channel x Interrupt

Value	Description
0	This bit has no effect. The Channel x Interrupt Mask bit (XDMAC_GIM.IMx) is not modified.
1	The corresponding mask bit is reset. The Channel x Interrupt Status register interrupt (XDMAC_GIS) is masked.

**DMA Controller (XDMAC)** 

### 36.9.6 XDMAC Global Interrupt Mask Register

Name: XDMAC\_GIM

Offset: 0x14

Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	IM23	IM22	IM21	IM20	IM19	IM18	IM17	IM16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	IM15	IM14	IM13	IM12	IM11	IM10	IM9	IM8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	IM7	IM6	IM5	IM4	IM3	IM2	IM1	IM0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - IM XDMAC Channel x Interrupt Mask

١	/alue	Description
(	)	This bit indicates that the channel x interrupt source is masked. The interrupt line is not raised.
1		This bit indicates that the channel x interrupt source is unmasked.

**DMA Controller (XDMAC)** 

### 36.9.7 XDMAC Global Interrupt Status Register

Name: XDMAC\_GIS

 Offset:
 0x18

 Reset:
 0x00000000

 Property:
 Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	IS23	IS22	IS21	IS20	IS19	IS18	IS17	IS16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	IS15	IS14	IS13	IS12	IS11	IS10	IS9	IS8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – IS XDMAC Channel x Interrupt Status

Value	Description
0	This bit indicates that either the interrupt source is masked at the channel level or no interrupt is
	pending for channel x.
1	This bit indicates that an interrupt is pending for the channel x.

**DMA Controller (XDMAC)** 

## 36.9.8 XDMAC Global Channel Enable Register

Name: XDMAC\_GE

Offset: 0x1C Reset: -

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								-
Reset								
Bit	23	22	21	20	19	18	17	16
	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - EN XDMAC Channel x Enable

Value	Description
0	This bit has no effect.
1	Enables channel n. This operation is permitted if the Channel x Status bit (XDMAC_GS.STx) was read
	as '0'.

**DMA Controller (XDMAC)** 

## 36.9.9 XDMAC Global Channel Disable Register

Name: XDMAC\_GD

Offset: 0x20 Reset: -

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	DI23	DI22	DI21	DI20	DI19	DI18	DI17	DI16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - DI XDMAC Channel x Disable

Value	Description
0	This bit has no effect.
1	Disables channel x.

### 36.9.10 XDMAC Global Channel Status Register

Name: XDMAC\_GS

Offset: 0x24

**Reset:** 0x00000000 **Property:** Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - ST XDMAC Channel x Status

Value	Description
0	This bit indicates that the channel x is disabled.
1	This bit indicates that the channel x is enabled. If a channel disable request is issued, this bit remains
	asserted until pending transaction is completed.

**DMA Controller (XDMAC)** 

### 36.9.11 XDMAC Global Channel Read Suspend Register

Name: XDMAC\_GRS

 Offset:
 0x28

 Reset:
 0x0000000

 Property:
 Read/Write

Bit	31	30	29	28	27	26	25	24
Access		•	•					
Reset								
Bit	23	22	21	20	19	18	17	16
	RS23	RS22	RS21	RS20	RS19	RS18	RS17	RS16
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	RS15	RS14	RS13	RS12	RS11	RS10	RS9	RS8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	RS7	RS6	RS5	RS4	RS3	RS2	RS1	RS0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - RSx XDMAC Channel x Read Suspend

Value	Description
0	The read channel is not suspended.
1	The source requests for channel n are no longer serviced by the system scheduler.

**DMA Controller (XDMAC)** 

### 36.9.12 XDMAC Global Channel Write Suspend Register

Name: XDMAC\_GWS

 Offset:
 0x2C

 Reset:
 0x0000000

 Property:
 Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	WS23	WS22	WS21	WS20	WS19	WS18	WS17	WS16
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WS15	WS14	WS13	WS12	WS11	WS10	WS9	WS8
Access	R/W							
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	WS7	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Access	R/W							
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – WSx XDMAC Channel x Write Suspend

Value	Description
0	The write channel is not suspended.
1	Destination requests are no longer routed to the scheduler.

**DMA Controller (XDMAC)** 

## 36.9.13 XDMAC Global Channel Read Write Suspend Register

Name: XDMAC\_GRWS

Offset: 0x30 Reset: –

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access		•	•					-
Reset								
Bit	23	22	21	20	19	18	17	16
	RWS23	RWS22	RWS21	RWS20	RWS19	RWS18	RWS17	RWS16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	RWS15	RWS14	RWS13	RWS12	RWS11	RWS10	RWS9	RWS8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	RWS7	RWS6	RWS5	RWS4	RWS3	RWS2	RWS1	RWS0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - RWSx XDMAC Channel x Read Write Suspend

Value	Description
0	No effect.
1	Read and write requests are suspended.

**DMA Controller (XDMAC)** 

### 36.9.14 XDMAC Global Channel Read Write Resume Register

Name: XDMAC\_GRWR

Offset: 0x34 Reset:

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	RWR23	RWR22	RWR21	RWR20	RWR19	RWR18	RWR17	RWR16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	RWR15	RWR14	RWR13	RWR12	RWR11	RWR10	RWR9	RWR8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	RWR7	RWR6	RWR5	RWR4	RWR3	RWR2	RWR1	RWR0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - RWRx XDMAC Channel x Read Write Resume

Value	Description
0	No effect.
1	Read and write requests are serviced.

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**DMA Controller (XDMAC)** 

### 36.9.15 XDMAC Global Channel Software Request Register

Name: XDMAC\_GSWR

Offset: 0x38 Reset:

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	SWREQ23	SWREQ22	SWREQ21	SWREQ20	SWREQ19	SWREQ18	SWREQ17	SWREQ16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	15	14	13	12	11	10	9	8
	SWREQ15	SWREQ14	SWREQ13	SWREQ12	SWREQ11	SWREQ10	SWREQ9	SWREQ8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	SWREQ7	SWREQ6	SWREQ5	SWREQ4	SWREQ3	SWREQ2	SWREQ1	SWREQ0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - SWREQ XDMAC Channel x Software Request

Value	Description
0	No effect.
1	Requests a DMA transfer for channel x.

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**DMA Controller (XDMAC)** 

## 36.9.16 XDMAC Global Channel Software Request Status Register

Name:  ${\tt XDMAC\_GSWS}$ 

Offset: 0x3C 0x0000000 Reset: Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	SWRS23	SWRS22	SWRS21	SWRS20	SWRS19	SWRS18	SWRS17	SWRS16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	SWRS15	SWRS14	SWRS13	SWRS12	SWRS11	SWRS10	SWRS9	SWRS8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SWRS7	SWRS6	SWRS5	SWRS4	SWRS3	SWRS2	SWRS1	SWRS0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 - SWRS XDMAC Channel x Software Request Status

Value	Description
0	Channel x source request is serviced.
1	Channel x source request is pending.

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**DMA Controller (XDMAC)** 

### 36.9.17 XDMAC Global Channel Software Flush Request Register

Name: XDMAC\_GSWF

Offset: 0x40 Reset: –

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	SWF23	SWF22	SWF21	SWF20	SWF19	SWF18	SWF17	SWF16
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	-
Bit	15	14	13	12	11	10	9	8
	SWF15	SWF14	SWF13	SWF12	SWF11	SWF10	SWF9	SWF8
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	_
Bit	7	6	5	4	3	2	1	0
	SWF7	SWF6	SWF5	SWF4	SWF3	SWF2	SWF1	SWF0
Access	W	W	W	W	W	W	W	W
Reset	_	_	_	_	_	_	_	-

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – SWFx XDMAC Channel x Software Flush Request

Value	Description
0	No effect.
1	Requests a DMA transfer flush for channel x. This bit is only relevant when the transfer is source peripheral synchronized.

## 36.9.18 XDMAC Channel x Interrupt Enable Register [x=0..23]

Name: XDMAC\_CIE

**Offset:** 0x50 + n\*0x40 [n=0..23]

Reset: -

Reset

Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	. 22	21	20	19	18	17	16
Access						-		
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
Access		W	W	W	W	W	W	W

#### Bit 6 - ROIE Request Overflow Error Interrupt Enable Bit

Value	Description
0	No effect.
1	Enables request overflow error interrupt.

### Bit 5 - WBIE Write Bus Error Interrupt Enable Bit

	2.00 1.2.2 1.1.00 2.00 2.1.01 1.1.00 2.00 2				
1	Value	Description			
	0	No effect.			
	1	Enables write bus error interrupt.			

## Bit 4 - RBIE Read Bus Error Interrupt Enable Bit

Valu	Description
0	No effect.
1	Enables read bus error interrupt.

## Bit 3 - FIE End of Flush Interrupt Enable Bit

Value	Description
0	No effect.
1	Enables end of flush interrupt.

#### Bit 2 - DIE End of Disable Interrupt Enable Bit

Value	Description
0	No effect.
1	Enables end of disable interrupt.

#### Bit 1 - LIE End of Linked List Interrupt Enable Bit

Value	Description
0	No effect.
1	Enables end of linked list interrupt.

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Bit 0 - BIE	End of Block	Interrupt	Enable	Bit

Value	Description
0	No effect.
1	Enables end of block interrupt.

### 36.9.19 XDMAC Channel x Interrupt Disable Register [x = 0..23]

Name: XDMAC\_CID

**Offset:** 0x54 + n\*0x40 [n=0..23]

Reset: -

**Property:** Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access		•						
Reset								
Bit	7	6	5	4	3	2	1	0
		ROID	WBEID	RBEID	FID	DID	LID	BID
Access		W	W	W	W	W	W	W
Reset		_	_	_	_	_	_	_

### Bit 6 - ROID Request Overflow Error Interrupt Disable Bit

Value	Description
0	No effect.
1	Disables request overflow error interrupt.

### Bit 5 - WBEID Write Bus Error Interrupt Disable Bit

	2.00 1.22.2 1.11.0 2.00 2.11.0 1.10.11.0 2.10 2.1	
Va	alue	Description
0		No effect.
1		Disables bus error interrupt.

## Bit 4 - RBEID Read Bus Error Interrupt Disable Bit

Value	Description
0	No effect.
1	Disables bus error interrupt.

#### Bit 3 - FID End of Flush Interrupt Disable Bit

Value	Description
0	No effect.
1	Disables end of flush interrupt.

#### Bit 2 - DID End of Disable Interrupt Disable Bit

Value	Description
0	No effect.
1	Disables end of disable interrupt.

#### Bit 1 - LID End of Linked List Interrupt Disable Bit

	/alue	Description	
(	)	No effect.	
-	_	Disables end of linked list interrupt.	

**DMA Controller (XDMAC)** 

Bit 0 - BID End of Block Interrupt Disab	ole Bit
--	---------

Value	Description
0	No effect.
1	Disables end of block interrupt.

### 36.9.20 XDMAC Channel x Interrupt Mask Register [x = 0..23]

Name: XDMAC\_CIM

**Offset:** 0x58 + n\*0x40 [n=0..23]

**Reset:** 0x00000000 **Property:** Read-only

Bit	31	30	29	28	27	26	25	24
Access		•				•	•	
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
110001								
D:4	15	4.4	10	10	44	10	9	0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

#### Bit 6 - ROIM Request Overflow Error Interrupt Mask Bit

	The state of the s
Value	Description
0	Request overflow interrupt is masked.
1	Request overflow interrupt is activated.

### Bit 5 - WBEIM Write Bus Error Interrupt Mask Bit

	- 11 - 11 - 11 - 11 - 11 - 11 - 11 - 1	
Value	Value Description	
0	Bus error interrupt is masked.	
1	Bus error interrupt is activated.	

## Bit 4 - RBEIM Read Bus Error Interrupt Mask Bit

Value	Description	
0	Bus error interrupt is masked.	
1 Bus error interrupt is activated.		

## Bit 3 - FIM End of Flush Interrupt Mask Bit

Value	Description
0	End of flush interrupt is masked.
1	End of flush interrupt is activated.

#### Bit 2 - DIM End of Disable Interrupt Mask Bit

Value	Description
0	End of disable interrupt is masked.
1	End of disable interrupt is activated.

#### Bit 1 - LIM End of Linked List Interrupt Mask Bit

1	alue	Description
C		End of linked list interrupt is masked.
1		End of linked list interrupt is activated.

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Bit 0 - BIN	Bit 0 – BIM End of Block Interrupt Mask Bit		
Value	Description		
0	Block interrupt is masked.		
1	Block interrupt is activated		

### 36.9.21 XDMAC Channel x Interrupt Status Register [x = 0..23]

Name: XDMAC\_CIS

**Offset:** 0x5C + n\*0x40 [n=0..23]

**Reset:** 0x00000000 **Property:** Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
Access		R	R	R	R	R	R	R
Reset			0		0			0

#### Bit 6 - ROIS Request Overflow Error Interrupt Status Bit

Value	Description
0	Overflow condition has not occurred.
1	Overflow condition has occurred at least once. (This information is only relevant for peripheral synchronized transfers.)

### Bit 5 - WBEIS Write Bus Error Interrupt Status Bit

	TIPE TITLE TO THE BUS END INCOME CHARGE BY			
Valu	ue Description			
0	Write bus error condition has not occurred.			
1	At least one bus error has been detected in a write access since the last read of the Status register.			

### Bit 4 - RBEIS Read Bus Error Interrupt Status Bit

DIC 7 112	The Troud Buo Error Interrupt Otatao Bit			
Value	Value Description			
0	Read bus error condition has not occurred.			
1	At least one bus error has been detected in a read access since the last read of the Status register.			

### Bit 3 - FIS End of Flush Interrupt Status Bit

	- 10		
Value	Description		
0	End of flush condition has not occurred.		
1	End of flush condition has occurred since the last read of the Status register.		

### Bit 2 - DIS End of Disable Interrupt Status Bit

	2.14 0. 2.104.210 1.1101.410.211		
Value	Description		
0	End of disable condition has not occurred.		
1	End of disable condition has occurred since the last read of the Status register.		

#### Bit 1 - LIS End of Linked List Interrupt Status Bit

Value	Description
0	End of linked list condition has not occurred.

**DMA Controller (XDMAC)** 

Value	Description
1	End of linked list condition has occurred since the last read of the Status register.

### Bit 0 - BIS End of Block Interrupt Status Bit

Value	Description
0	End of block interrupt has not occurred.
1	End of block interrupt has occurred since the last read of the Status register.

**DMA Controller (XDMAC)** 

### 36.9.22 XDMAC Channel x Source Address Register [x = 0..23]

Name:

XDMAC\_CSA 0x60 + n\*0x40 [n=0..23] Offset:

0x00000000 Reset: Read/Write Property:

Bit	31	30	29	28	27	26	25	24
				SA[3	1:24]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
				SA[2	3:16]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				SA[′	15:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				SA[	7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 - SA[31:0] Channel x Source Address

Program this register with the source address of the DMA transfer.

A configuration error is generated when this address is not aligned with the transfer data size.

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## 36.9.23 XDMAC Channel x Destination Address Register [x = 0..23]

Name:

XDMAC\_CDA 0x64 + n\*0x40 [n=0..23] Offset:

0x00000000 Reset: Read/Write Property:

Bit	31	30	29	28	27	26	25	24
				DA[3	1:24]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
				DA[2	3:16]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				DA[′	15:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				DA[	7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 - DA[31:0] Channel x Destination Address

Program this register with the destination address of the DMA transfer.

A configuration error is generated when this address is not aligned with the transfer data size.

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### 36.9.24 XDMAC Channel x Next Descriptor Address Register [x = 0..23]

Name:

XDMAC\_CNDA 0x68 + n\*0x40 [n=0..23] Offset:

0x00000000 Reset: Read/Write Property:

31	30	29	28	27	26	25	24
			NDA[2	29:22]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16
			NDA[2	21:14]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
			NDA	[13:6]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
		NDA	[5:0]				NDAIF
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0	0	0	0	0	0		0
	R/W 0 23 R/W 0 15 R/W 0 7 R/W	R/W         R/W           0         0           23         22           R/W         0           0         0           15         14           R/W         0           0         0           7         6           R/W         R/W	R/W         R/W         R/W           0         0         0           23         22         21           R/W         R/W         R/W           0         0         0           15         14         13           R/W         R/W         R/W           0         0         0           7         6         5           NDA         R/W         R/W	R/W   R/W   R/W   R/W   0   0   0   0   0   0   0   0   0	R/W   R/W   R/W   R/W   R/W   R/W   0   0   0   0   0   0   0   0   0	R/W   R/W   R/W   R/W   R/W   R/W   0   0   0   0   0   0   0   0   0	R/W

### Bits 31:2 - NDA[29:0] Channel x Next Descriptor Address

The 30-bit width of the NDA field represents the next descriptor address range 31:2. The descriptor is word-aligned and the two least significant register bits 1:0 are ignored.

### Bit 0 - NDAIF Channel x Next Descriptor Interface

Value	Description
0	The channel descriptor is retrieved through system interface 0.
1	The channel descriptor is retrieved through system interface 1.

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**DMA Controller (XDMAC)** 

### 36.9.25 XDMAC Channel x Next Descriptor Control Register [x = 0..23]

Name: XDMAC\_CNDC

**Offset:** 0x6C + n\*0x40 [n=0..23]

**Reset:** 0x00000000 **Property:** Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
				NDVIE	W[1:0]	NDDUP	NDSUP	NDE
Access			•	R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

#### Bits 4:3 - NDVIEW[1:0] Channel x Next Descriptor View

Value	Name	Description
0	NDV0	Next Descriptor View 0
1	NDV1	Next Descriptor View 1
2	NDV2	Next Descriptor View 2
3	NDV3	Next Descriptor View 3

#### Bit 2 - NDDUP Channel x Next Descriptor Destination Update

0 (DST\_PARAMS\_UNCHANGED): Destination parameters remain unchanged.

### Bit 1 - NDSUP Channel x Next Descriptor Source Update

0 (SRC PARAMS UNCHANGED): Source parameters remain unchanged.

1 (SRC PARAMS UPDATED): Source parameters are updated when the descriptor is retrieved.

#### Bit 0 - NDE Channel x Next Descriptor Enable

0 (DSCR\_FETCH\_DIS): Descriptor fetch is disabled.

1 (DSCR\_FETCH\_EN): Descriptor fetch is enabled.

<sup>1 (</sup>DST\_PARAMS\_UPDATED): Destination parameters are updated when the descriptor is retrieved.

**DMA Controller (XDMAC)** 

## 36.9.26 XDMAC Channel x Microblock Control Register [x = 0..23]

Name:

XDMAC\_CUBC 0x70 + n\*0x40 [n=0..23] Offset:

0x00000000 Reset: Read/Write Property:

Bit	31	30	29	28	27	26	25	24
Access		•				•		_
Reset								
Bit	23	22	21	20	19	18	17	16
				UBLEN	I[23:16]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				UBLE	N[15:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				UBLE	N[7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 - UBLEN[23:0] Channel x Microblock Length

This field indicates the number of data in the microblock. The microblock contains UBLEN data.

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**DMA Controller (XDMAC)** 

## 36.9.27 XDMAC Channel x Block Control Register [x = 0..23]

Name:

XDMAC\_CBC 0x74 + n\*0x40 [n=0..23] Offset:

0x0000000 Reset: Read/Write Property:

Bit	31	30	29	28	27	26	25	24
Access		•	•			•	•	
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	-					BLEN		
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Neset					O	O	O	U
D:4	7	0	_	4	0	0	4	0
Bit		6	5	4	3	2	1	0
				BLEN				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 11:0 - BLEN[11:0] Channel x Block Length The length of the block is (BLEN+1) microblocks.

#### 36.9.28 XDMAC Channel x Configuration Register [x = 0..23]

Name: XDMAC\_CC

**Offset:** 0x78 + n\*0x40 [n=0..23]

**Reset:** 0x00000000 **Property:** Read/Write

Bit	31	30	29	28	27	26	25	24
			•		PERID[6:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WRIP	RDIP	INITD		DAM	I[1:0]	SAM	[1:0]
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8
		DIF	SIF	DWID <sup>-</sup>	TH[1:0]		CSIZE[2:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MEMSET	SWREQ		DSYNC		MBSIZ	ZE[1:0]	TYPE
Access	R/W	R/W		R/W		R/W	R/W	R/W
Reset	0	0		0		0	0	0

#### Bits 30:24 - PERID[6:0] Channel x Peripheral Hardware Request Line Identifier

This field contains the peripheral hardware request line identifier. PERID refers to identifiers defined in "DMA Controller Peripheral Connections".

### Bit 23 - WRIP Write in Progress (this bit is read-only)

0 (DONE): No active write transaction on the bus.

1 (IN\_PROGRESS): A write transaction is in progress.

### Bit 22 - RDIP Read in Progress (this bit is read-only)

0 (DONE): No active read transaction on the bus.

1 (IN\_PROGRESS): A read transaction is in progress.

#### Bit 21 - INITD Channel Initialization Done (this bit is read-only)

0 (IN\_PROGRESS): Channel initialization is in progress.

1 (TERMINATED): Channel initialization is completed.

Note: When set to 0, XDMAC\_CUBC.UBLEN and XDMAC\_CNDA.NDA field values are unreliable each time a descriptor is being updated. See 36.8 XDMAC Software Requirements.

Bits 19:18 - DAM[1:0] Channel x Destination Addressing Mode

	Dramit in a maintena	2 communication in the second mode
Value	Name	Description
0	FIXED_AM	The address remains unchanged.
1	INCREMENTED_AM	The addressing mode is incremented (the increment size is set to the data size).
2	UBS_AM	The microblock stride is added at the microblock boundary.
3	UBS_DS_AM	The microblock stride is added at the microblock boundary; the data stride is added at the data boundary.

Bits 17:16 - SAM[1:0] Channel x Source Addressing Mode

Value	Name	Description
0	FIXED_AM	The address remains unchanged.

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Value	Name	Description
1	INCREMENTED_AM	The addressing mode is incremented (the increment size is set to the data size).
2	UBS_AM	The microblock stride is added at the microblock boundary.
3	UBS_DS_AM	The microblock stride is added at the microblock boundary, the data stride is added at the data boundary.

#### Bit 14 - DIF Channel x Destination Interface Identifier

0 (AHB IF0): The data is written through system bus interface 0.

1 (AHB IF1): The data is written though system bus interface 1.

#### Bit 13 - SIF Channel x Source Interface Identifier

0 (AHB\_IF0): The data is read through system bus interface 0.

1 (AHB\_IF1): The data is read through system bus interface 1.

#### Bits 12:11 - DWIDTH[1:0] Channel x Data Width

	/alue	Name	Description
(	)	BYTE	The data size is set to 8 bits
-	1	HALFWORD	The data size is set to 16 bits
2	2	WORD	The data size is set to 32 bits

#### Bits 10:8 - CSIZE[2:0] Channel x Chunk Size

Value	Name	Description
0	CHK_1	1 data transferred
1	CHK_2	2 data transferred
2	CHK_4	4 data transferred
3	CHK_8	8 data transferred
4	CHK 16	16 data transferred

#### Bit 7 - MEMSET Channel x Fill Block of Memory

0 (NORMAL\_MODE): Memset is not activated.

1 (HW\_MODE): Sets the block of memory pointed by DA field to the specified value. This operation is performed on 8-, 16- or 32-bit basis.

#### Bit 6 - SWREQ Channel x Software Request Trigger

0 (HWR CONNECTED): Hardware request line is connected to the peripheral request line.

1 (SWR CONNECTED): Software request is connected to the peripheral request line.

#### Bit 4 - DSYNC Channel x Synchronization

0 (PER2MEM): Peripheral-to-memory transfer.

1 (MEM2PER): Memory-to-peripheral transfer.

#### Bits 2:1 - MBSIZE[1:0] Channel x Memory Burst Size

Value	Name	Description
0	SINGLE	The memory burst size is set to one.
1	FOUR	The memory burst size is set to four.
2	EIGHT	The memory burst size is set to eight.
3	SIXTEEN	The memory burst size is set to sixteen.

#### Bit 0 - TYPE Channel x Transfer Type

0 (MEM\_TRAN): Self-triggered mode (memory-to-memory transfer).

1 (PER\_TRAN): Synchronized mode (peripheral-to-memory or memory-to-peripheral transfer).

### 36.9.29 XDMAC Channel x Data Stride Memory Set Pattern Register [x = 0..23]

Name: XDMAC\_CDS\_MSP Offset: 0x7C + n\*0x40 [n=0..23]

**Reset:** 0x00000000 **Property:** Read/Write

Bit	31	30	29	28	27	26	25	24	
	DDS_MSP[15:8]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	23	22	21	20	19	18	17	16	
				DDS_M	ISP[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	
SDS_MSP[					SP[15:8]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	7	6	5	4	3	2	1	0	
				SDS_N	SDS_MSP[7:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

**Bits 31:16 – DDS\_MSP[15:0]** Channel x Destination Data Stride or Memory Set Pattern When XDMAC\_CCx.MEMSET = 0, this field indicates the destination data stride. When XDMAC\_CCx.MEMSET = 1, this field indicates the memory set pattern.

**Bits 15:0 – SDS\_MSP[15:0]** Channel x Source Data stride or Memory Set Pattern When XDMAC\_CCx.MEMSET = 0, this field indicates the source data stride. When XDMAC\_CCx.MEMSET = 1, this field indicates the memory set pattern.

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## 36.9.30 XDMAC Channel x Source Microblock Stride Register [x = 0..23]

Name:

XDMAC\_CSUS 0x80 + n\*0x40 [n=0..23] Offset:

0x0000000 Reset: Read/Write Property:

Bit	31	30	29	28	27	26	25	24	
Access									
Reset									
Bit	23	22	21	20	19	18	17	16	
		SUBS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	
	SUBS[15:8]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	7	6	5	4	3	2	1	0	
	SUBS[7:0]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

Bits 23:0 - SUBS[23:0] Channel x Source Microblock Stride Two's complement microblock stride for channel x.

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## 36.9.31 XDMAC Channel x Destination Microblock Stride Register [x = 0..23]

Name:

XDMAC\_CDUS 0x84 + n\*0x40 [n=0..23] Offset:

0x00000000 Reset: Read/Write Property:

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
				DUBS	[23:16]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	DUBS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
DUBS[7:0]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – DUBS[23:0] Channel x Destination Microblock Stride Two's complement microblock stride for channel x.

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