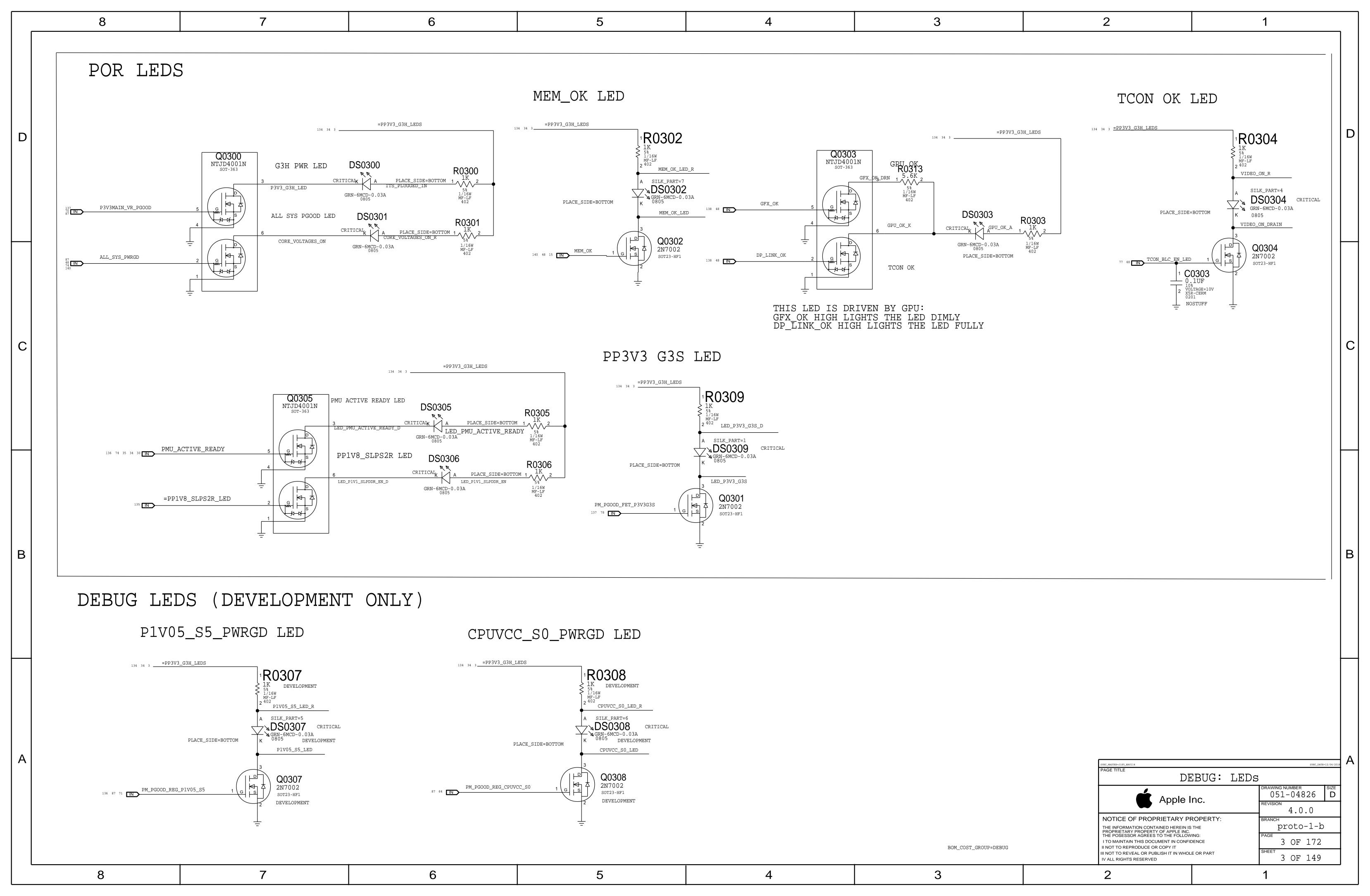
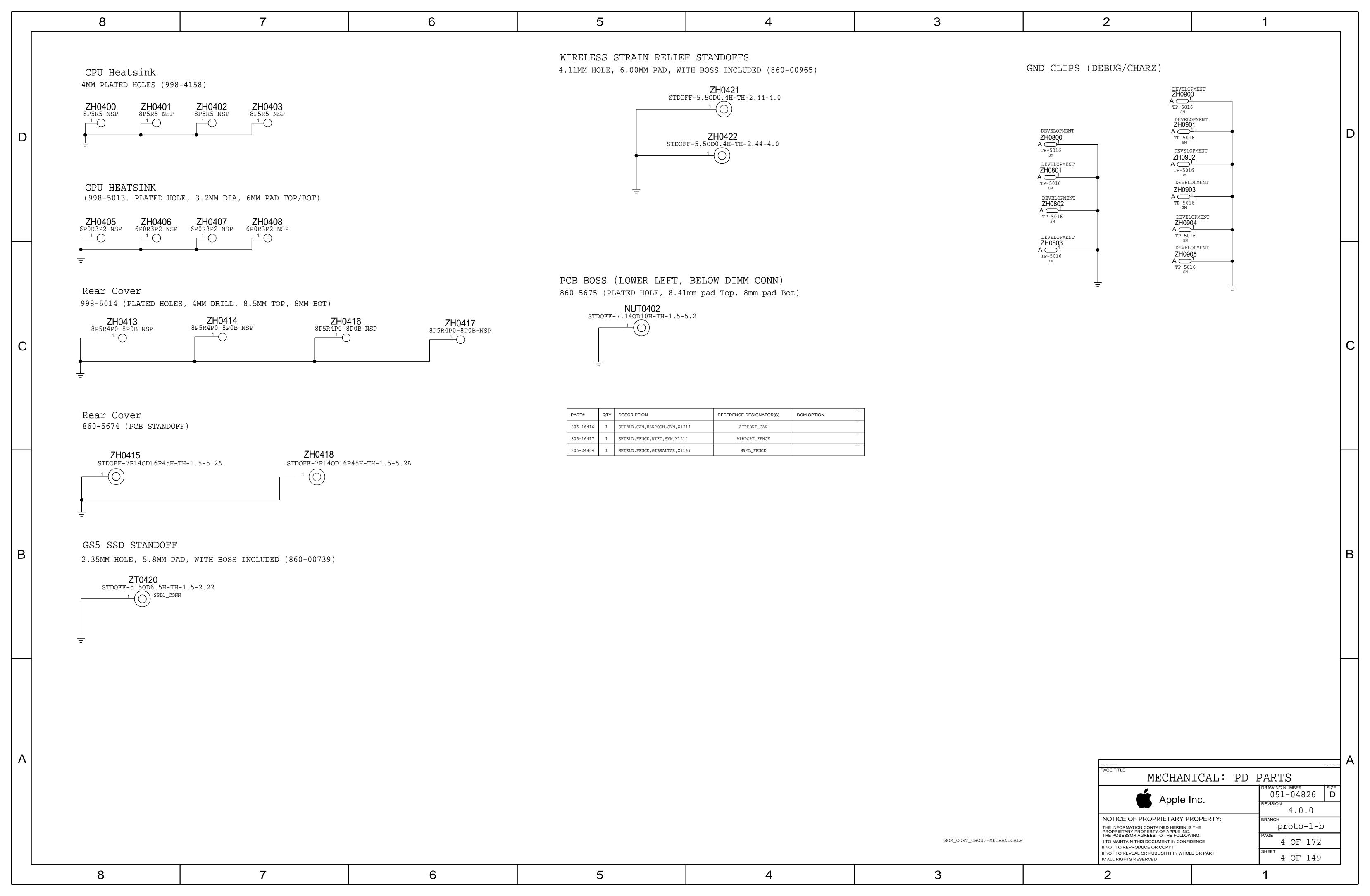
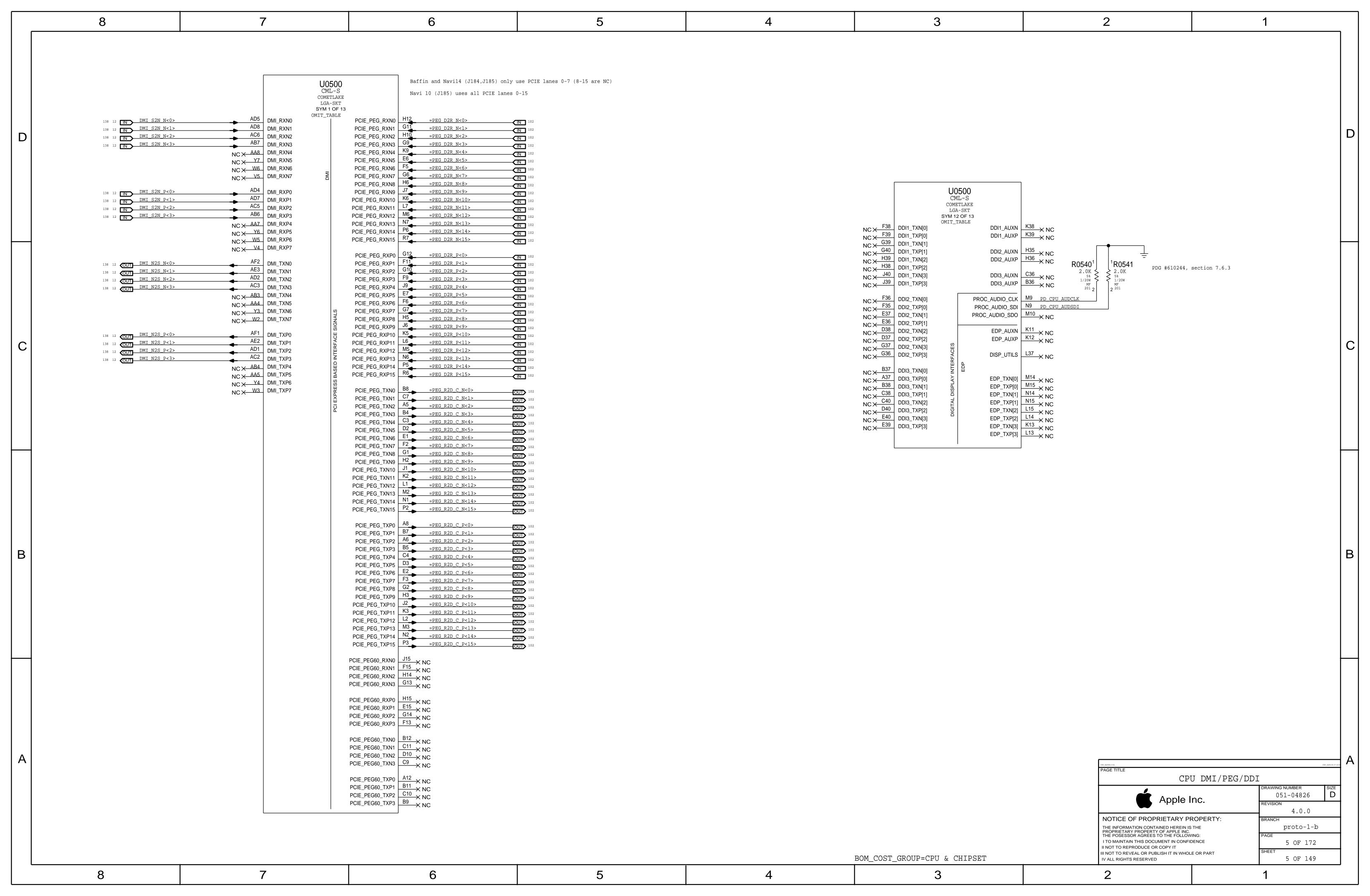
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PAGE CSA CONTE	NTS MLB_NAVI10	SYNC	DATE	PAGE CS		S CONNECTOR		SYNC DIRK	DATE		CONTENTS			SYNC	DATE	
<u> </u>	nfiguration	KRITHIKA	05/24/2019		CAMERA/AL			J184	12/12/2019 06/07/2019	-	GDDR6 X16 GPU CH F0, F1 GDDR6 X16 GPU CH G0, G1			RAYMOND RAYMOND	08/28/2019 08/28/2019	.
D 3 3 DEBUG		J185_NAVI14	12/04/2018	63 69	PLATFORM	POWER: CONNECTORS		JERRY	12/12/2019		GDDR6 X16 GPU CH H0, H1			RAYMOND	08/28/2019	
-	ICAL: PD PARTS I/PEG/DDI	KRITHIKA J184	09/24/2019 06/07/2019			ore & VCCGT Ctrl ORE PHASES 1-3		SUNIL SUNIL	08/27/2019		VR VDDCR_GFX, VDDCR_SOC (VR VDDCR_GFX PHASES 1-3	CTRL		SUNIL SUNIL	11/15/2019 10/02/2019	.
<u> </u>	ock/Misc/JTAG/CFG	MURPHY	10/28/2019			DRE PHASES 4-6		SUNIL	08/27/2019		VR VDDCR_GFX PHASES 1-3 VR VDDCR_GFX PHASES 4-6			SUNIL	10/02/2019	
	R4 Interface	Ј184	06/07/2019			PSET: CPU VDDQ VR		SUNIL	11/15/2019		VR VDDCR_GFX PHASES 7-9			SUNIL	10/02/2019	_
8 8 CPU Po 9 9 CPU G		MURPHY J184	10/31/2019 06/07/2019			PSET: VCCGT & VCCSA PSET: CPU VCCIO VR		SUNIL SUNIL	08/27/2019	-	VR GFX VDDIO, VDDCI CTRL GRAPHICS: GPU VDDCI VR			SUNIL SUNIL	08/27/2019 08/27/2019	
<u> </u>	COUPLING 1	MURPHY	09/26/2019			POWER: 3.3V G3H/5V G3S	VR	SUNIL	08/27/2019		GRAPHICS: GPU 0V75 VR			SUNIL	08/27/2019	
	COUPLING-2 I/eSPI/SPI/RTC/Sideband/PM	MURPHY RAYMOND	05/06/2019 11/01/2019	71 77		IPSET: PCH 1V05		SUNIL	11/15/2019		GRAPHICS: GPU 1V8 VR			SUNIL	10/16/2019	. 🔲
-	B/JTAG/HDA	MATTHEW	09/10/2019	$\frac{72}{73}$ 79	PMIC BUCK PMIC LDOs			MATTHEW MATTHEW	10/24/2019 10/11/2019		VR GFX VDDIO PHASES 1-2 GPU POWER RAIL DISCHARGE			SUNIL MATTHEW	08/27/2019 08/09/2019	.
-	Ie and Clocks	MATTHEW	09/04/2019	74 80) PMIC GPIC	Os Controls		MATTHEW	09/16/2019	134 155	POWER ALIASES - 1			KENNYC	04/29/2019	_
$\frac{15}{16} \frac{15}{16} \frac{PCH G}{PCH P}$	IO/Misc/NCTF wer	MATTHEW MATTHEW	09/04/2019 10/24/2019			LCD Backlight Driver (1 Backlight Driver 2	LP8565)	JERRYHU RAYMOND	06/13/2019 03/11/2019		POWER ALIASES - 2 FCT/ICT TPS -1			KRITHIKA J184	04/29/2019	.
	coupling	MATTHEW	10/24/2019		B DISPLAY:			RAYMOND	08/28/2019		CHARZ AUTOMATION TPS			MATTHEW	08/09/2019	.
18 18 CPU X		MATTHEW	10/11/2019		POWER FET			MATTHEW	10/11/2019		SIGNAL ALIASES			KRITHIKA	04/24/2019	-
	CHIPSET: Chipset Support t-Specific Chipset Support	MATTHEW MATTHEW	08/09/2019		POWER FET SSD0: S4E			MATTHEW KRITHIKA	08/09/2019		ALTERNATE TABLE FCT/ICT TPS -2			KRITHIKA KRITHIKA	10/11/2019 08/07/2019	-
	ALIASES AND BITSWAPS	RAYMOND	08/27/2019		7 SSD0: S4E			KRITHIKA	06/07/2019		TESTPOINTS TABLE 1			RRITITIA	00/07/2019	
	REF/VTT EN	RAYMOND	09/10/2019		8 SSD0: S4E			KRITHIKA	06/07/2019	-	TESTPOINTS TABLE 2					-
	SO-DIMM CONNECTOR A DIMM 0 SO-DIMM CONNECTOR A DIMM 1	RAYMOND RAYMOND	08/27/2019 08/27/2019		9 SSD0: S4E	E/S5E<3> PMIC & NAND VCC VR		KRITHIKA KRITHIKA	06/07/2019		TESTPOINTS TABLE 3 TESTPOINTS TABLE 4					-
25 25 DRAM:	O-DIMM CONNECTOR B DIMM 0	RAYMOND	08/27/2019		1 SSDO SUPI			KRITHIKA	06/07/2019		TESTPOINTS TABLE 5					-
	GO-DIMM CONNECTOR B DIMM 1 High Speed 1	RAYMOND J184	08/27/2019 06/07/2019		2 SSD 1 CON			KRITHIKA	06/07/2019		TESTPOINTS TABLE 6				00/05/0010	_
	High Speed 2	J184	06/07/2019			OWER SEQUENCING R SEQUENCING SO		MATTHEW MATTHEW	10/24/2019 08/09/2019		BOM Configuration CONFIGURATION BOMS P0			KRITHIKA KRITHIKA	09/26/2019	-
	Support Page	JACOB	11/14/2019			RNET CONTROLLER 1		MURPHY	07/01/2019		2 BOM CONFIGURATION					
	PORT CONTROLLER XA PORT CONTROLLER XB	JACOB JACOB	10/11/2019		8 10G ETHER9 10G ENET	RNET CONTROLLER 2		MURPHY MURPHY	09/11/2019 08/05/2019							-
32 33 USB-C		J185_NAVI14	12/04/2018		00 10G ENET			MURPHY	05/22/2019							-
33 36 SECUR		RAYMOND	08/05/2019		01 VR 10G EI			MURPHY	09/24/2019							-
$\frac{34}{35}$ 38 SOC D	PIO/SEP/USB/DDR/Test		06/07/2019 06/07/2019		02 VR 10G EI 03 SD CONTRO			SUNIL MURPHY	08/27/2019							-
36 40 SoC A		KRITHIKA	08/20/2019		04 SD CONNE			MURPHY	07/05/2019							-
	SP/I2C/UART/SPI/I2S	J184	06/07/2019	-		XTERNAL USB PORTS A & B		RAYMOND	08/27/2019							_
		J184 J184	06/07/2019		07 USB-A: E 10 WIFI/BT I	XTERNAL USB PORTS C & D)	RAYMOND KRITHIKA	08/27/2019 08/20/2019							- B
40 44 SoC F		J184	06/07/2019		11 WIFI/BT I			KRITHIKA	08/20/2019							-
$\frac{41}{42} \frac{45}{46} \text{SoC } = \frac{1}{4}$		J184 J184	06/07/2019		12 WIFI/BT			KRITHIKA	08/20/2019							_
	nared Support	J184	06/07/2019		20 GPU PCIE 21 GPU GPIO			RAYMOND RAYMOND	08/20/2019 09/10/2019							-
	ROJECT SUPPORT	KRITHIKA	08/20/2019	104 12	22 GPU DISP	LAYPORT		RAYMOND	09/10/2019							_
$\frac{45}{46}$ $\frac{49}{50}$ $\frac{50}{120}$ $\frac{5}{3}$	HARED SUPPORT IMAC 1 OC 1	MATTHEW JERRY	07/31/2019		23 GPU GND 24 GPU CLK	GEN TTAC		RAYMOND RAYMOND	08/20/2019							_
47 51 I2C S		RAYMOND	08/19/2019		25 GPU MEMO			RAYMOND	08/20/2019							
	roject Support	JERRY	12/12/2019	-	26 GPU CORE			RAYMOND	08/20/2019							
	HARED SUPPORT IMAC 2 RS: I and V Sense	J184 JERRY	06/07/2019 12/12/2019			PWR DECOUPLING CH A0, A1, B0, B1		RAYMOND RAYMOND	08/20/2019							
	RS: I and V Sense(Continued)	JERRY	12/12/2019			CH CO, C1, DO, D1		RAYMOND	08/20/2019							
	RS THERMAL 1	JERRY	12/12/2019	-		CH E0, E1, F0, F1		RAYMOND	08/20/2019							
53 57 SENSO 54 58 FAN:		JERRY JERRY	12/12/2019 12/12/2019		31 GPU MEM 32 GPU ROM	CH G0, G1, H0, H1		RAYMOND RAYMOND	08/20/2019 06/13/2019							
55 60 1G EN	ET PHY (Caesar IV)	MURPHY	08/07/2019	-	34 GPU ISO			RAYMOND	06/17/2019				SC	CHEM,MLB_NAVI	10	
' '	ET SUPPORT Jack CODEC	MURPHY DIRK	06/19/2019			6 GPU CH A0,A1		RAYMOND	06/24/2019			SYNC_MAST DRAWING	ER=KRITHIKA		SYNC_DATE=04/	24/2019 A
<u> </u>	Speaker Amps	DIRK	12/12/2019			.6 GPU CH B0,B1 .6 GPU CH C0, C1		RAYMOND RAYMOND	06/24/2019 06/24/2019					CHEM, MLB, NAVI10, X16	DRAWING NUMBER	SIZE
59 65 Right	Speaker Amp	DIRK	12/12/2019			.6 GPU CH DO, D1		RAYMOND	06/24/2019				Ap	ple Inc.	051-04826	D
60 66 Audio	Jack Connector	DIRK	12/12/2019	120 13	.39 GDDR6 X1	.6 GPU CH EO, E1		RAYMOND	08/28/2019			NOTIC	E OF PROPRIETA		REVISION 4.0.0	
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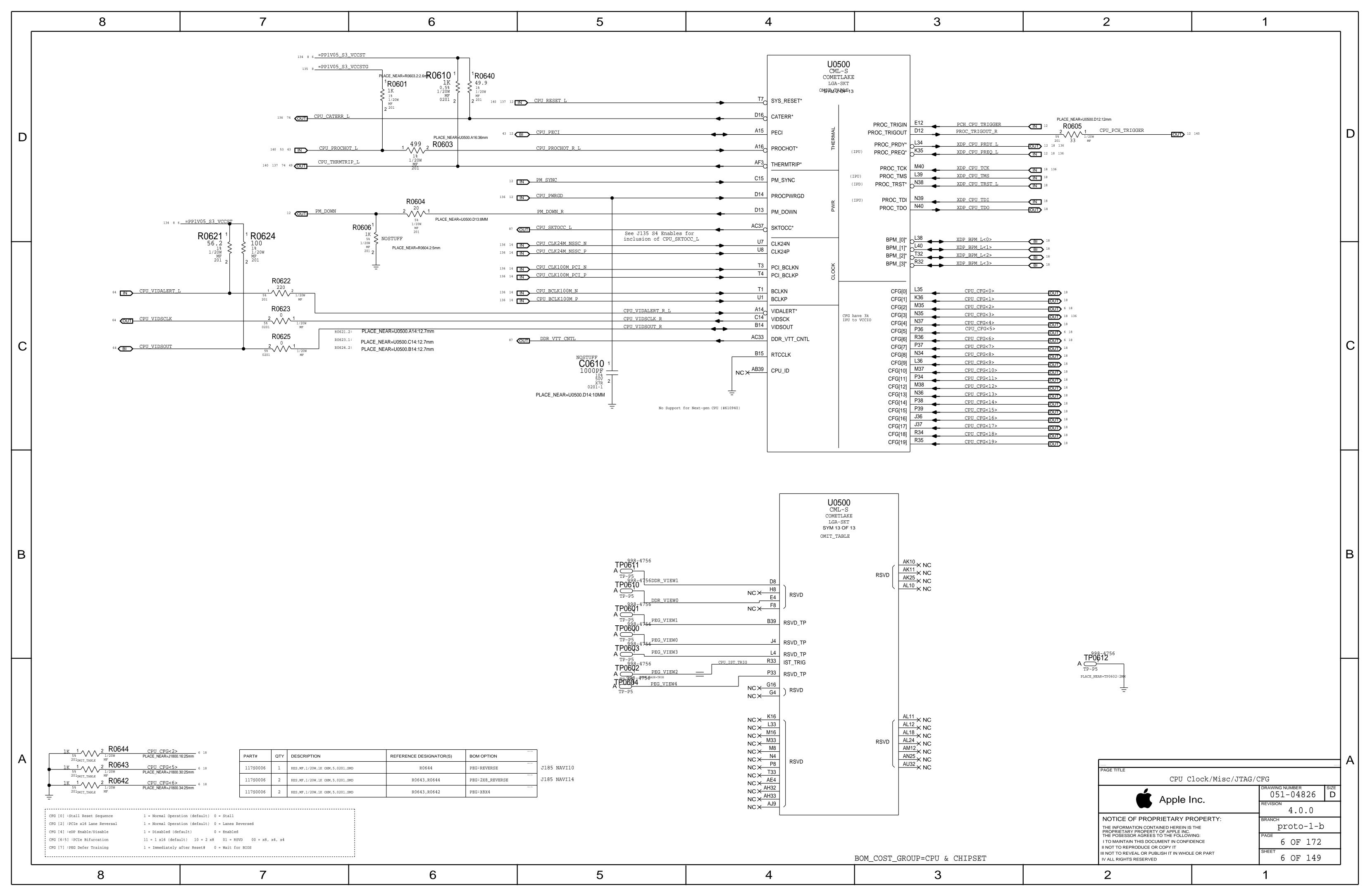
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	X1647	SCHEMATIC / PCB #	‡'S			BOM Groups					
	PART#	QTY DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	BOM GROUP		BOM OPTIONS	That promotes and		
	051-04826	1 SCHEM, MLB, NAVI10, X1647	SCH1	CRITICAL	X1647	X1647_COMMON	COMMON, ALTERNATE, X1647_P	ROGPARTS,1V8_AUDIO_DLY:N,PEG:REVERSE,LDO_CLIFDEN,NO_LDO_CLIFDEN,RF:TUN	NE		
	820-01823	1 PCBF,MLB,NAVI10,X1647	PCB1	CRITICAL	X1647	X1647_COMMON2	X1647,C10:N	O,PWR_SEQUENCE:SMC,SE:PROD,XDP:YES,WIFI:MURATA,BOARDREV_P1	THAN ASSESSMENT PROF.		
	685-00316	1 PCBA,COMMON,PARTS,MLB,NAVI10,X1647	CMNPTS	CRITICAL	MLB_CMNPTS	X1647_PROGPARTS	TBTROM:	PROG,WIFI_ROM:PROG,BT_ROM:PROG,SD_ROM:PROG	184,500007,70		
	685-00343	1 ITLC,SSD PARTS,NAVI10,4L S4E,X1647	SSD_S4E_4L		4L_S4E	X1647_DEVEL	DEVELOPMENT, SSD_DBG, XDP_CONN, U	JPC_DBG_HDR, DEBUG, DEBUG_LEDS, DBG_LED, SOC_DBG: YES, BOOTCFG0	THAN SERVICES P. PILL		
	685-00345	1 ITLC,SSD PARTS,NAVI10,4L S5E,X1647	SSD_S5E_4L		4L_S5E	X1647_SPECIFIC		BOARDID5, BOARDID1, BOARDID0 NAVI10 BOAR	RDID: 100011		D
		1 ENET PARTS,NAVI10,10G ENET,X1647	10G_ENET		10G_ENET	Main BOM Varian	n+ a				
	685-00363	1 ENETPARTS,NAVI10,1G ENET,X1647	1G_ENET		1G_ENET			DOM ODTIONS	1844,5000002-5460		
						985-01183	BOM NAME PCBA, MLB, NAVI10, DEV, X1647	BOM OPTIONS X1647_DEVEL	Takit, Millerdor, Phil		
	.					685-00316	PCBA, COMMON PARTS, MLB, NAVI10, X1647	X1647_COMMON, X1647_COMMON2, X1647	7 SPECIFIC		
	GPU PR	ROGRAMMABLE				685-00342	PCBA,MLB,NAVI10,2L_S4E,X1647	SSD0_2L,SSD0_S4E	**************************************		
	PART#	QTY DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	685-00343	PCBA,MLB,NAVI10,4L_S4E,X1647	SSD0_4L,SSD0_S4E,SSD0_S4E_4L	Teach processor, Pro-		
	341S01566	1 ROM, VBIOS, NAVI10-XTMA, GPU(V002) P1, X1647	UD200	CRITICAL	GPU_XTMA_ROM:PROG	685-00344	PCBA,MLB,NAVI10,2L_S5E,X1647	SSD0_2L,SSD0_S5E,SSD0_S5E_2L	146,50000-718		
		ROM, VBIOS, NAVIIO-XGA, GPU(V002) P1, X1647	UD200	CRITICAL	TAMA, A, FRM	685-00345	PCBA,MLB,NAV10,4L_S5E,X1647	SSD0_4L,SSD0_S5E,SSD0_S5E_4L	**************************************		
	335S00232	1 ic,spi serial flash,8mbits,3.0v,uson	UD200	CRITICAL	GPU_ROM:BLANK	685-00362	PCBA,MLB,NAV10,10G ENET,X1647	ENET:10G,10G_ENET_ROM:PROG	tan, panara-yte		
	GPU					685-00363	PCBA,MLB,NAV10,1G ENET,X1647	ENET:1G,1G_ENET_ROM:PROG	166,2400000,719		
		QTY DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	GPU BOM Groups					
	337S00771	1 GPU, AMD, NAVI10, XTMA, A2, ES, BGA1928	UC000	CRITICAL	GPU_SKU:XTMA	BOM GROUP		BOM OPTIONS	Total animotory state		
	337S00772	1 GPU, AMD, NAVIIO, XGA, A2, ES, BGA1928	UC000	CRITICAL	GPU_SKU:XGA	NV10_XTA_16GB_SAMSUNG	G	PU_SKU:XTMA,FB:16GB_SAMSUNG,GPU_XTMA_ROM:PROG	1642,2000037,704		
						NV10_XTA_16GB_MICRON		PU_SKU:XTMA,FB:16GB_MICRON,GPU_XTMA_ROM:PROG	164.060003-799		
						NV10_XTA_16GB_HYNIX	GE	PU_SKU:XTMA,FB:16GB_HYNIX,GPU_XTMA_ROM:PROG	1664, ASSESSED, FIN		
						NV10_XGA_8GB_SAMSUNG		GPU_SKU:XGA,FB:8GB_SAMSUNG,GPU_XGA_ROM:PROG	TOM, ADDRESS P. PM. TOMS ADDRESS P. PM.		C
						NV10_XGA_8GB_MICRON		GPU_SKU:XGA,FB:8GB_MICRON,GPU_XGA_ROM:PROG	Total analogy (Ne		
						NV10_XGA_8GB_HYNIX		GPU_SKU:XGA,FB:8GB_HYNIX,GPU_XGA_ROM:PROG			
	VRAM										
		QTY DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION						
	333S00223	8 IC,GDDR6,8GBIT,14GBPS,1.35V,19NM,H,BG180	UD500,UD600,UD700,UD800,UD900,UE100,UE200	CRITICAL	FB:8GB_HYNIX						
	333S00209	8 IC,GDDR6,8GBIT,14GBPS,1.35V,18NM,M,BG180	UD500, UD600, UD700, UD800, UD900, UE000, UE100, UE200	CRITICAL	FB:8GB_MICRON						
	333S00210	8 IC,GDDR6,8GBIT,14GBPS,1.35V,18NM,S,BG180	UD500, UD600, UD700, UD800, UD900, UE2000, UE100, UE200	CRITICAL	FB:8GB_SAMSUNG						
	333S00211 333S00212	8 IC,GDDR6,16GBIT,14GBPS,1.35V,19NM,H,B180	UD500, UD600, UD700, UD800, UD900, UE000, UE100, UE200	CRITICAL	FB:16GB_HYNIX FB:16GB_MICRON						
		8 IC,GDDR6,16GBIT,14GBPS,1.35V,18NM,S,B180	UDS00,UDS00,UD700,UD800,UD900,UD000,UD100,UD200 UD500,UD500,UD700,UD900,UD900,UD900,UD100,UD200		FB:16GB_SAMSUNG	_					
		<u> </u>	I		I						
	CPU SK	ζU									
	PART#	QTY DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION						
_	337S00828		CPU	CRITICAL	CPU:GOOD						
В	337S00832	1 CPU,CML-S,QUD6,QS,P-0,2.9,8C,65W,LG1200	CPU	CRITICAL	CPU:BEST						B
	337S00831	1 CPU,CML-S,QUCX,QS,P-0,3.8,8C,125W,L1200	CPU	CRITICAL	CPU:ULT						
	337S00830	1 CPU,CML-S,QUBQ,QS,P-0,3.7,10C,125W,L1200	СРИ	CRITICAL	CPU:CTO						

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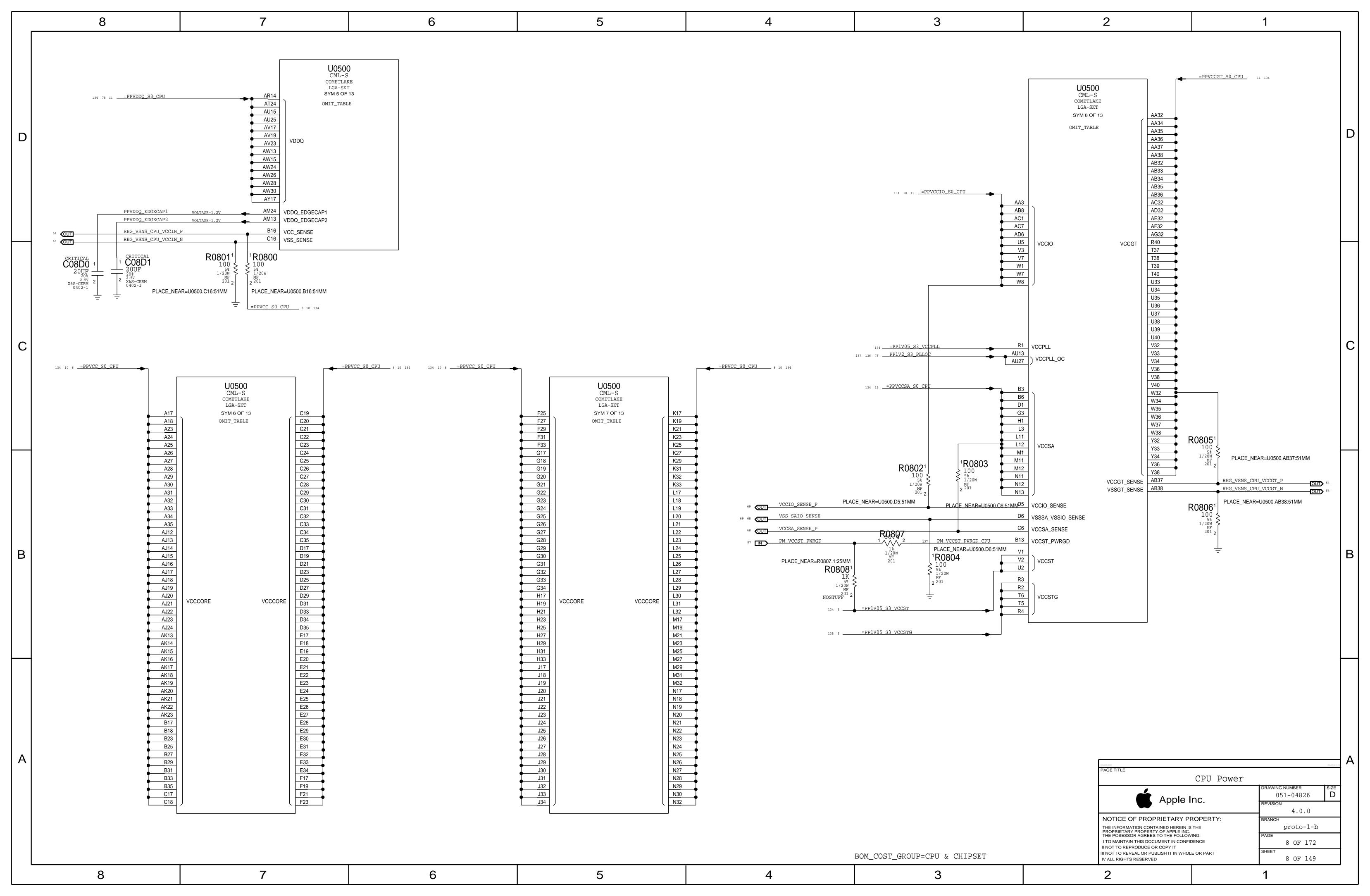


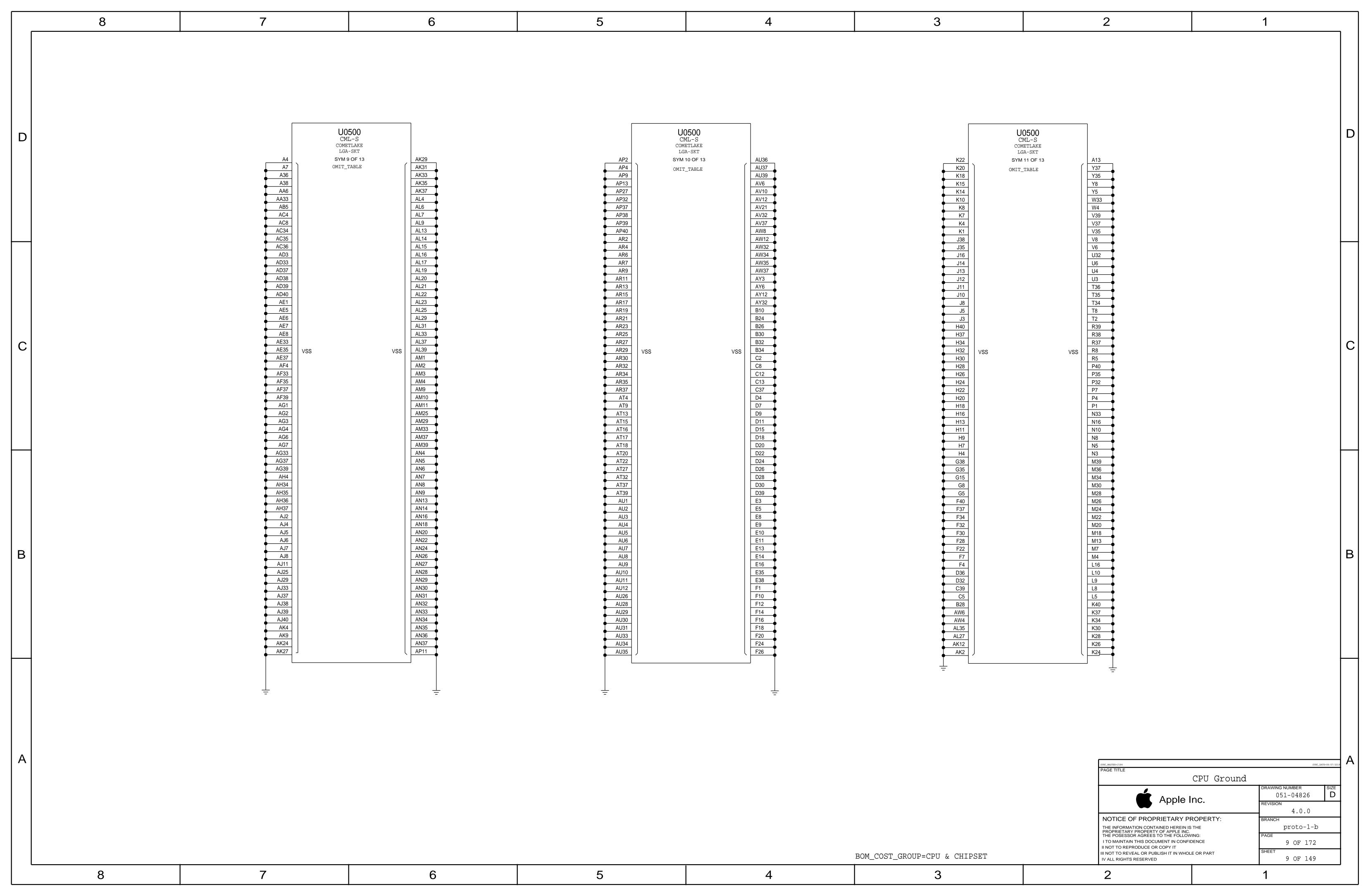




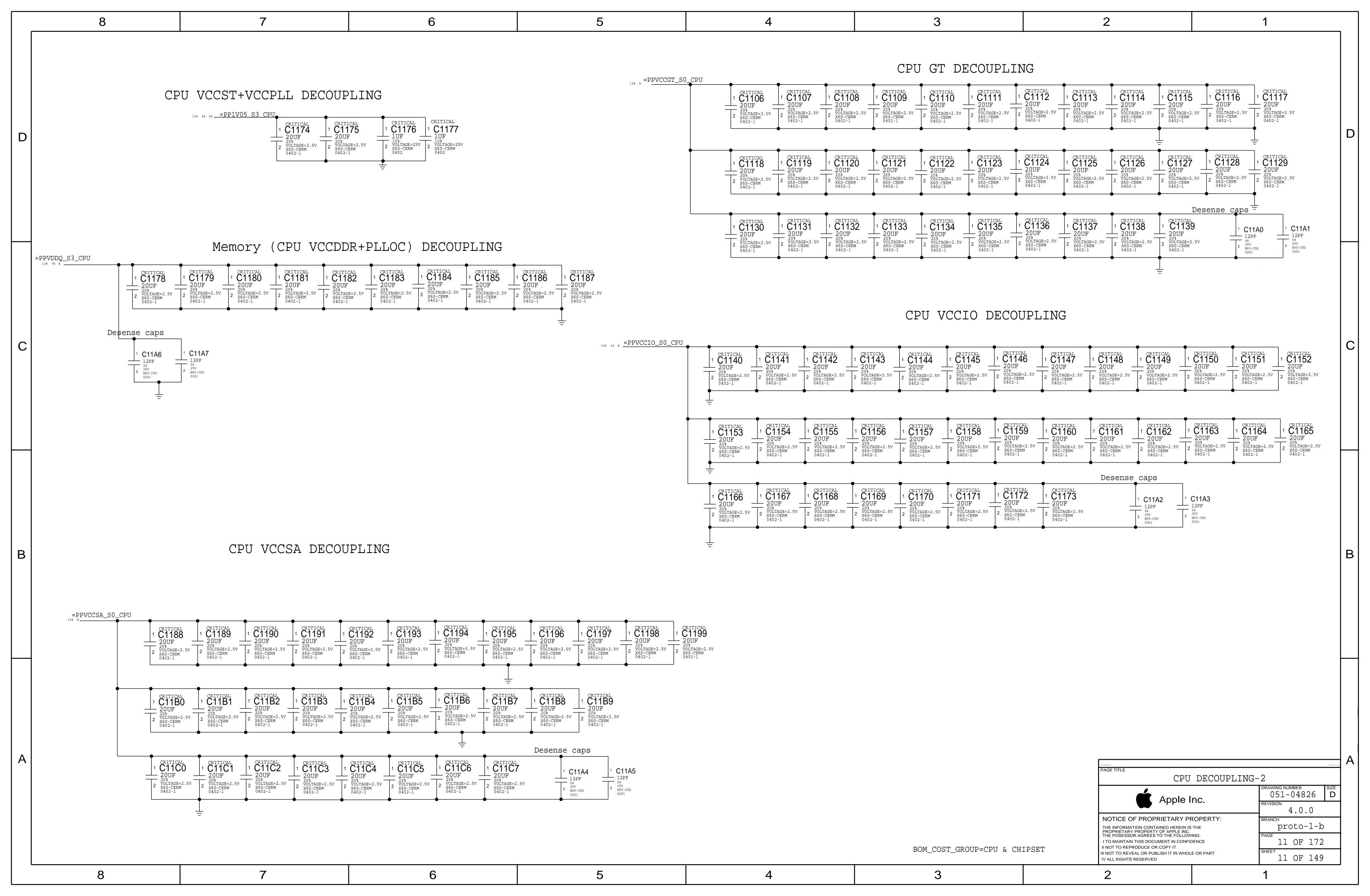


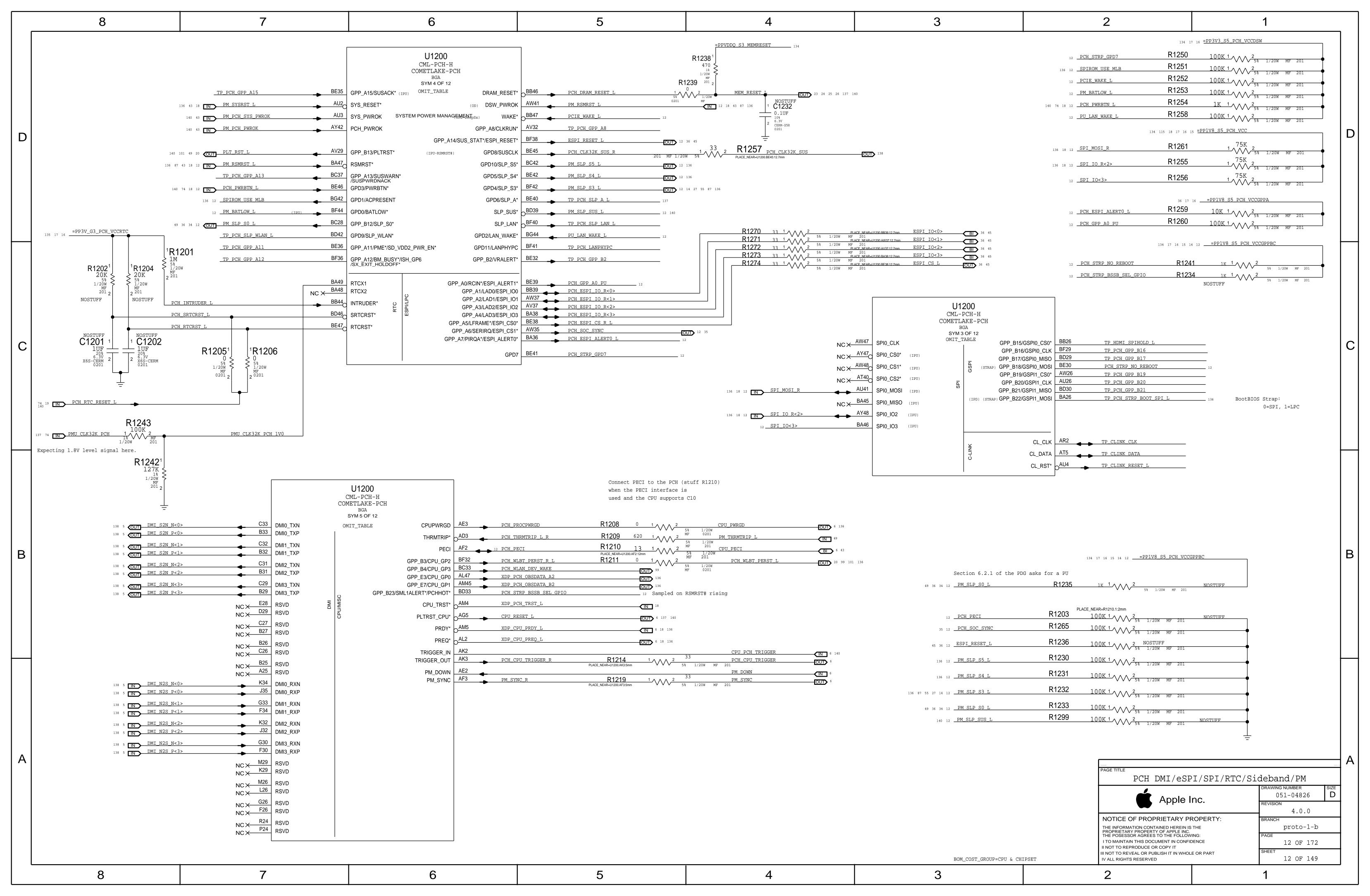


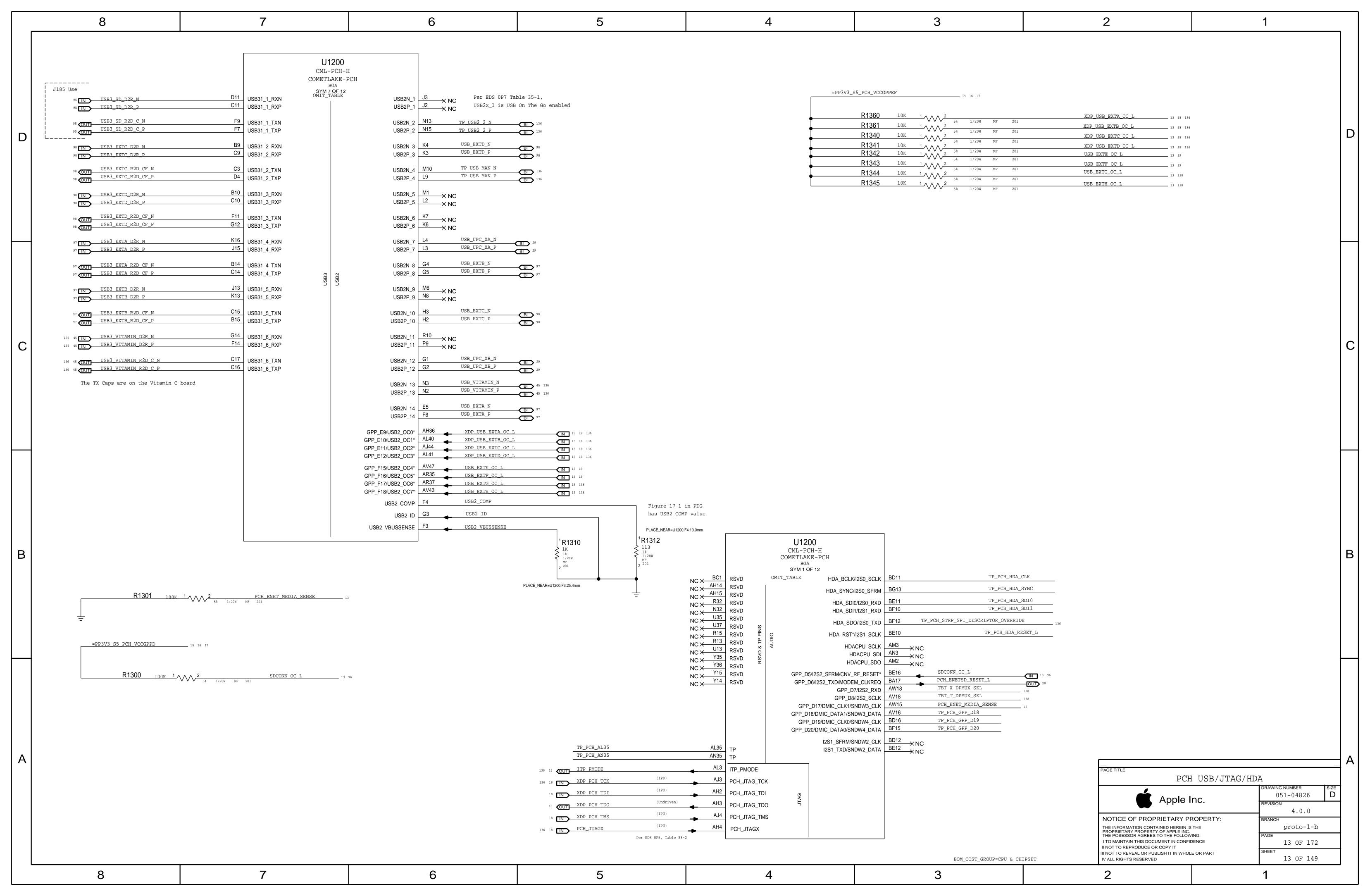


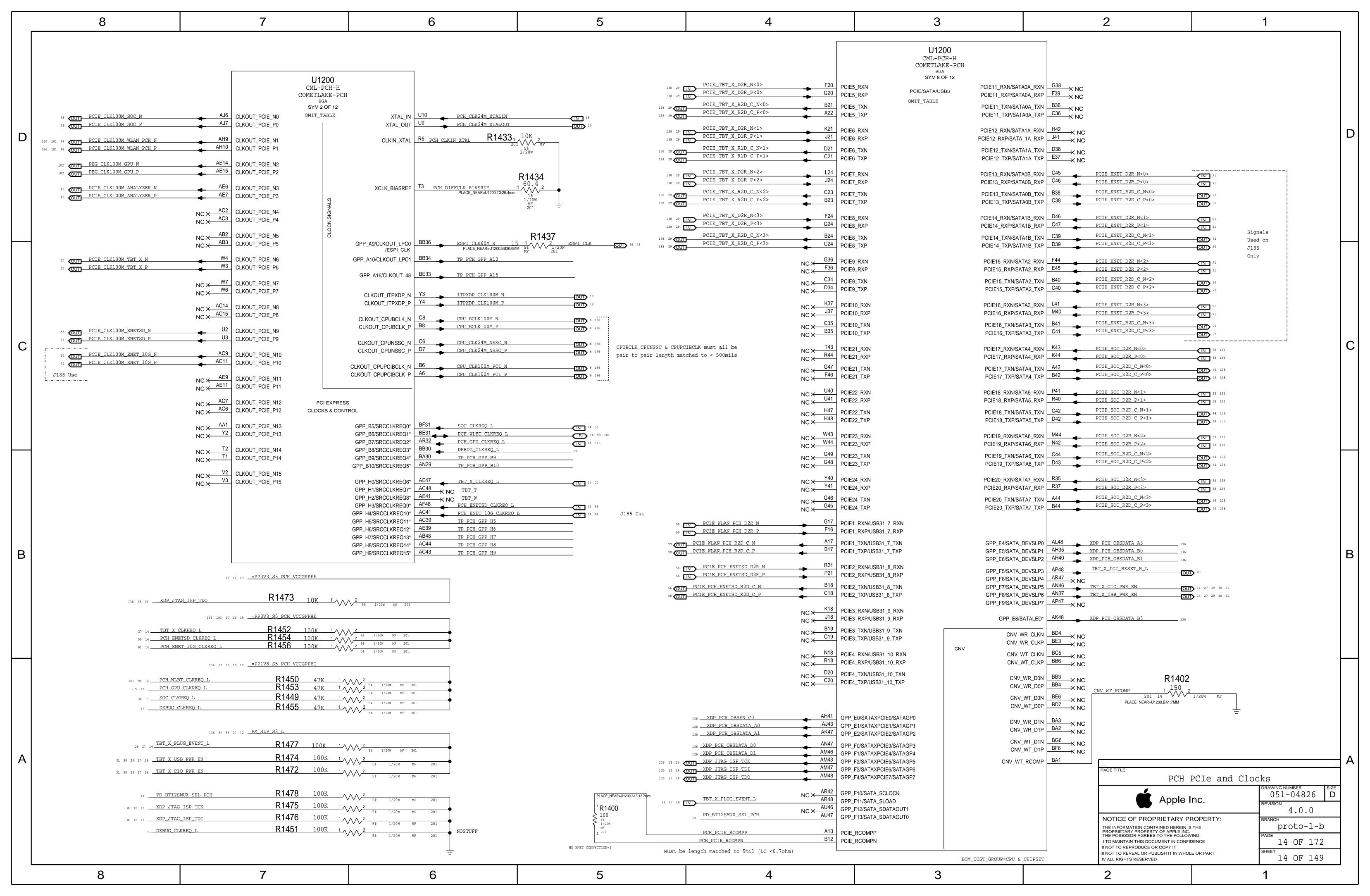


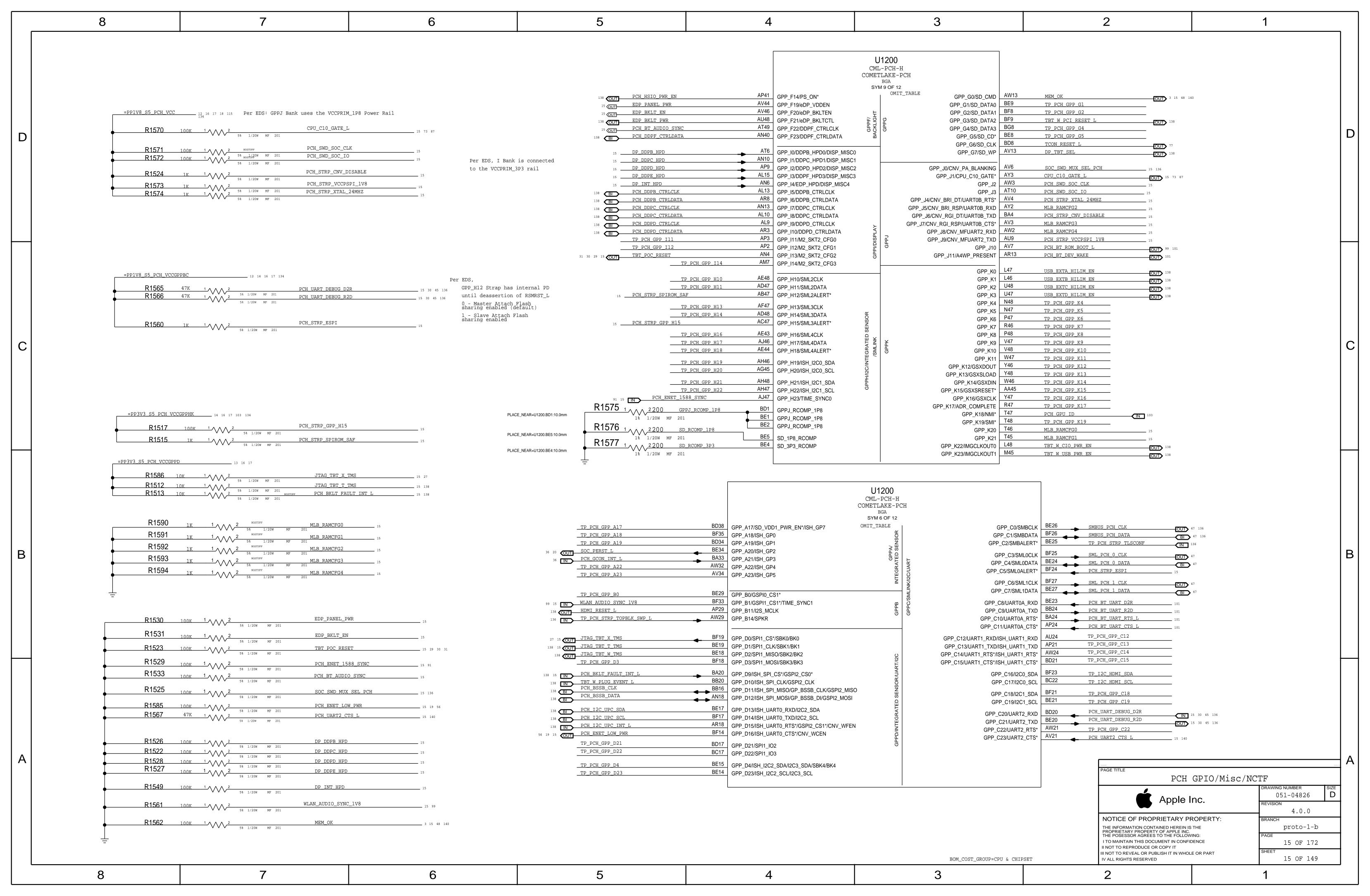


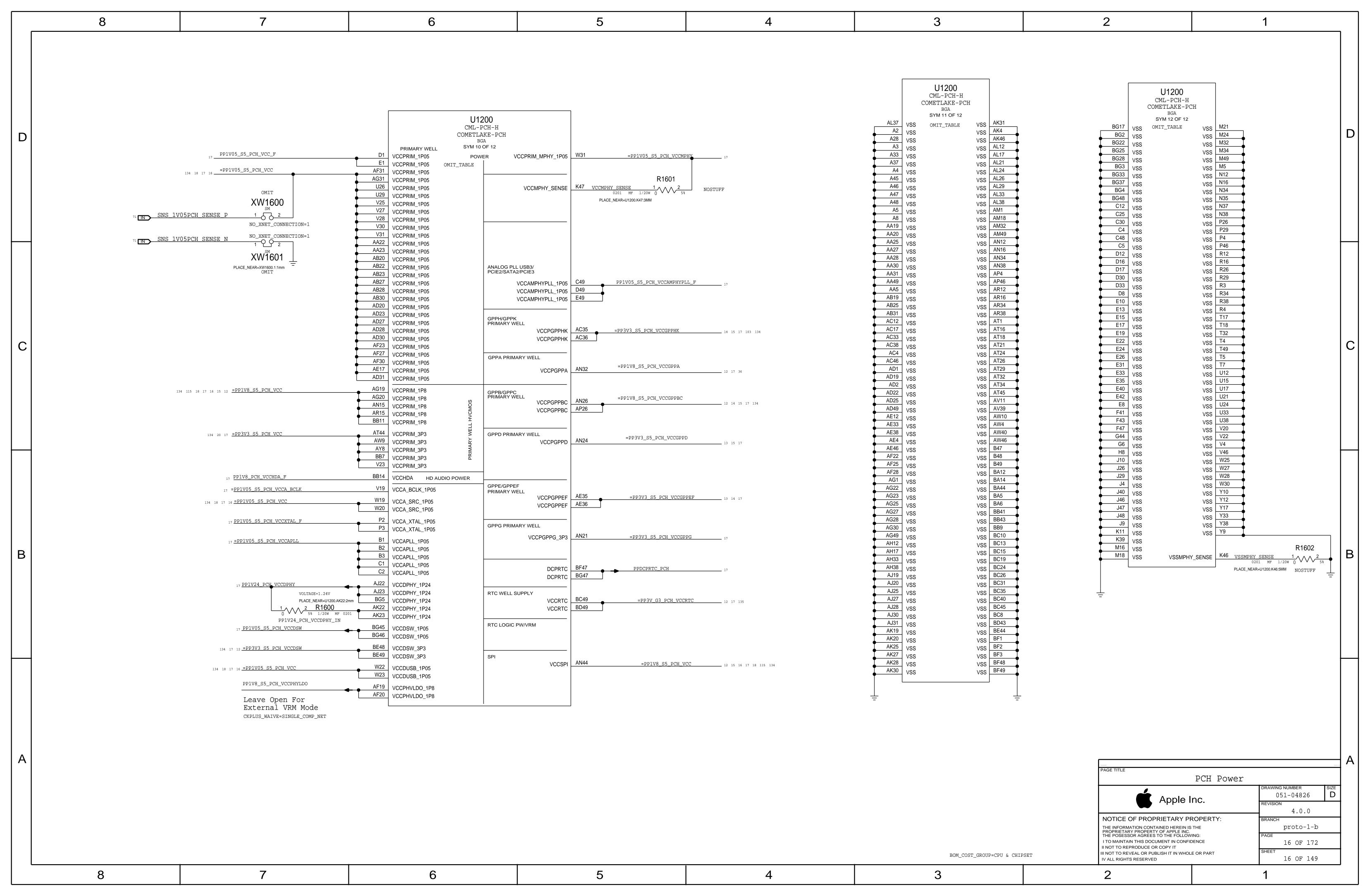


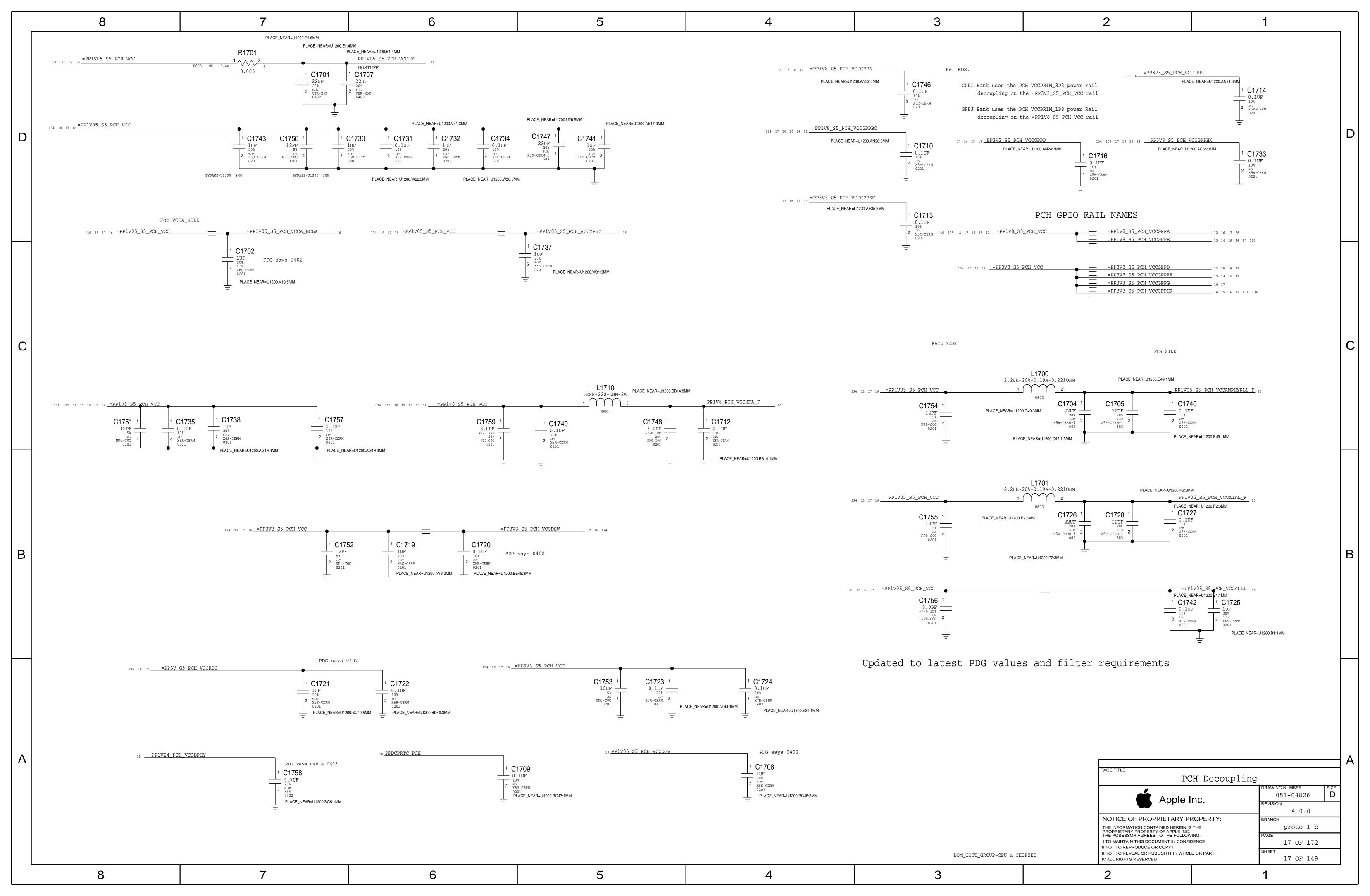


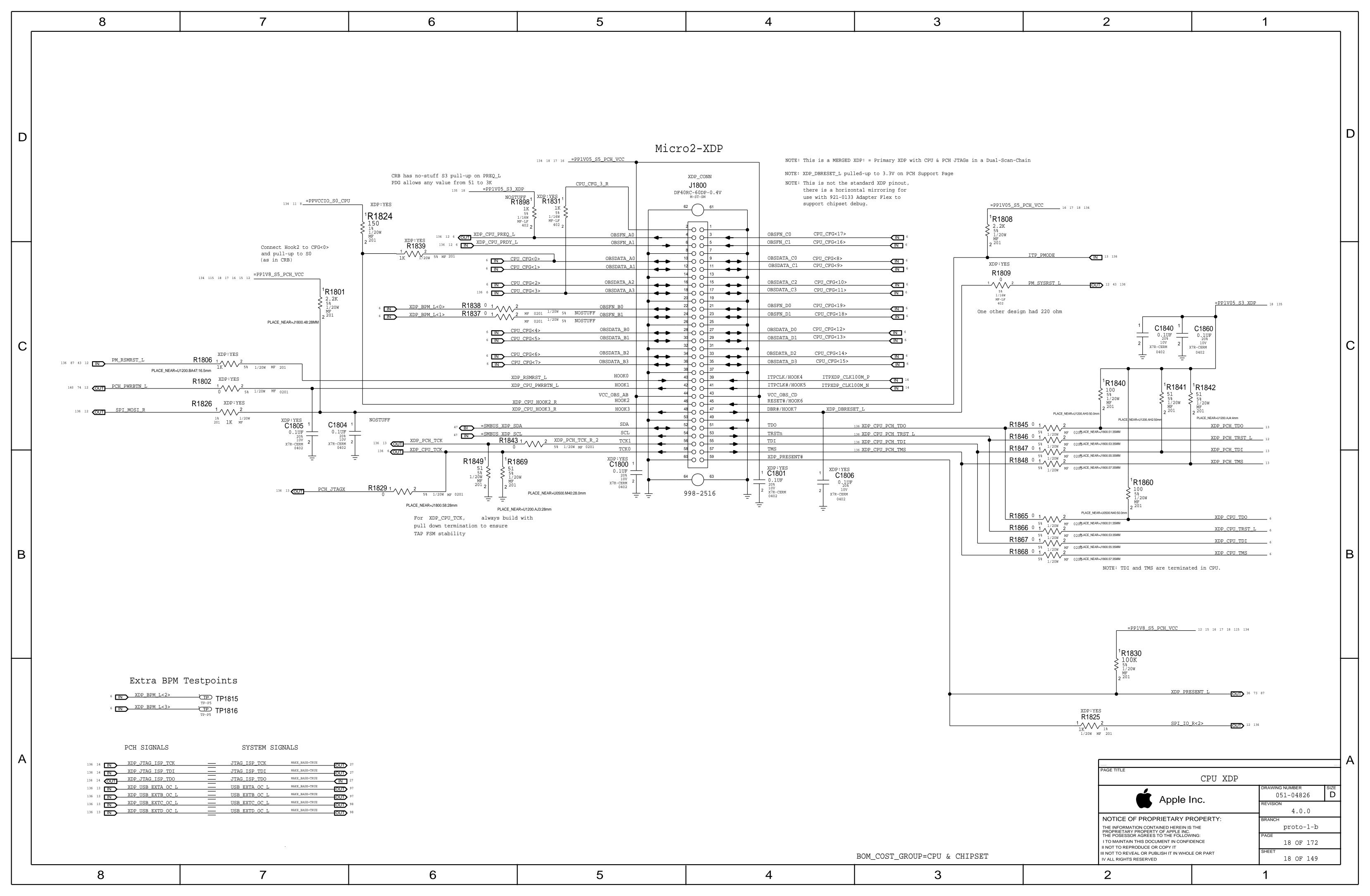


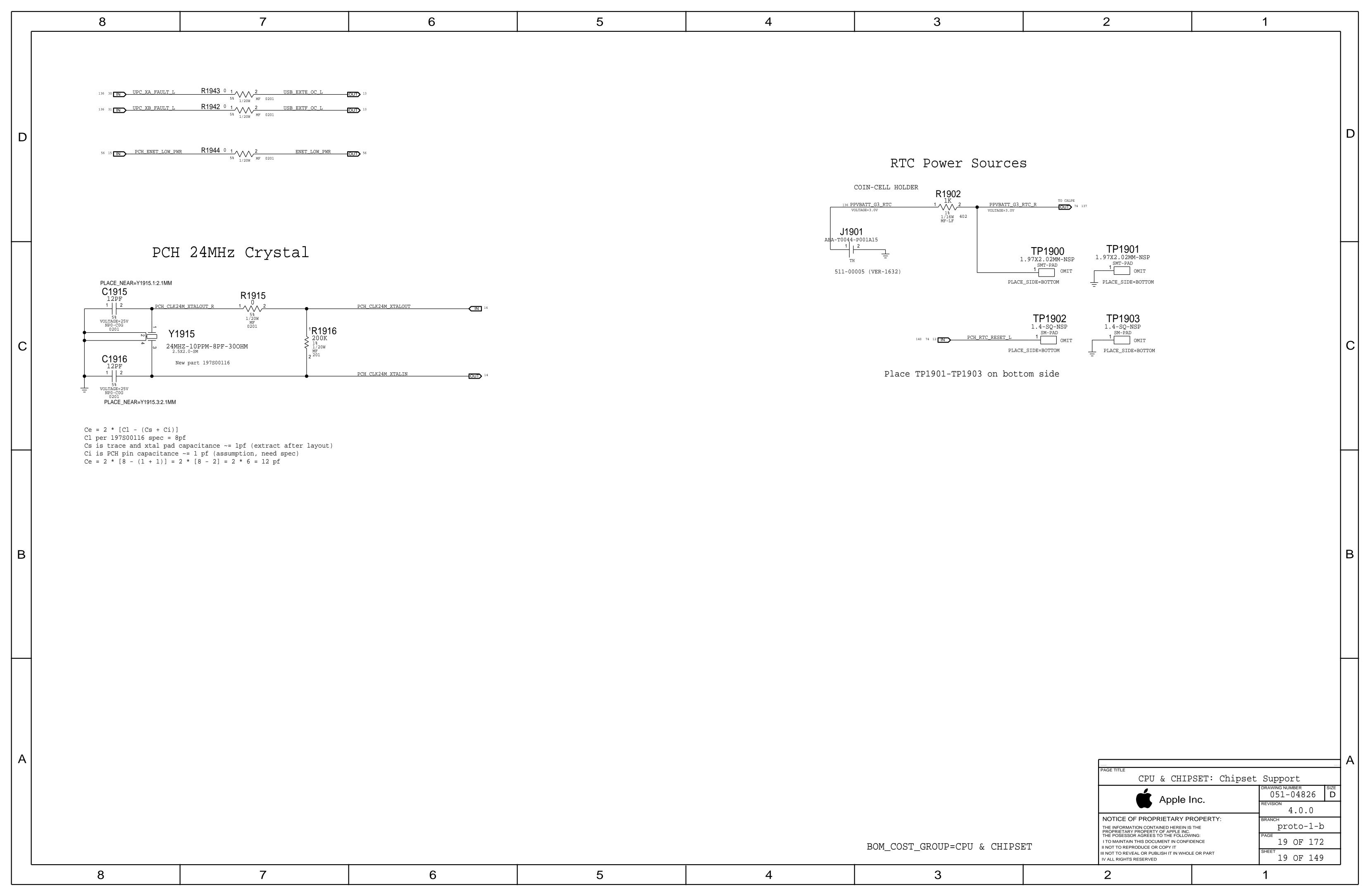


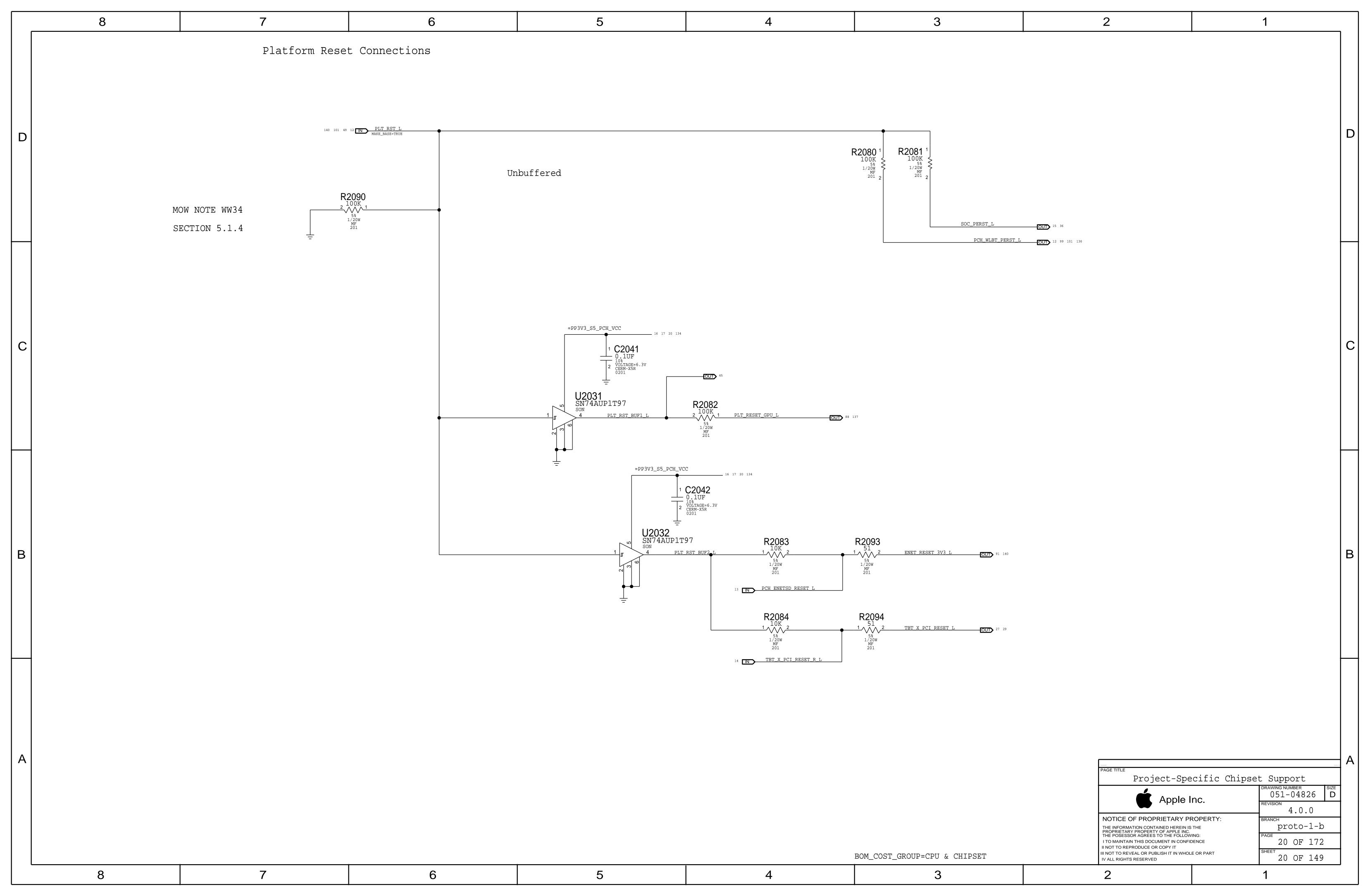




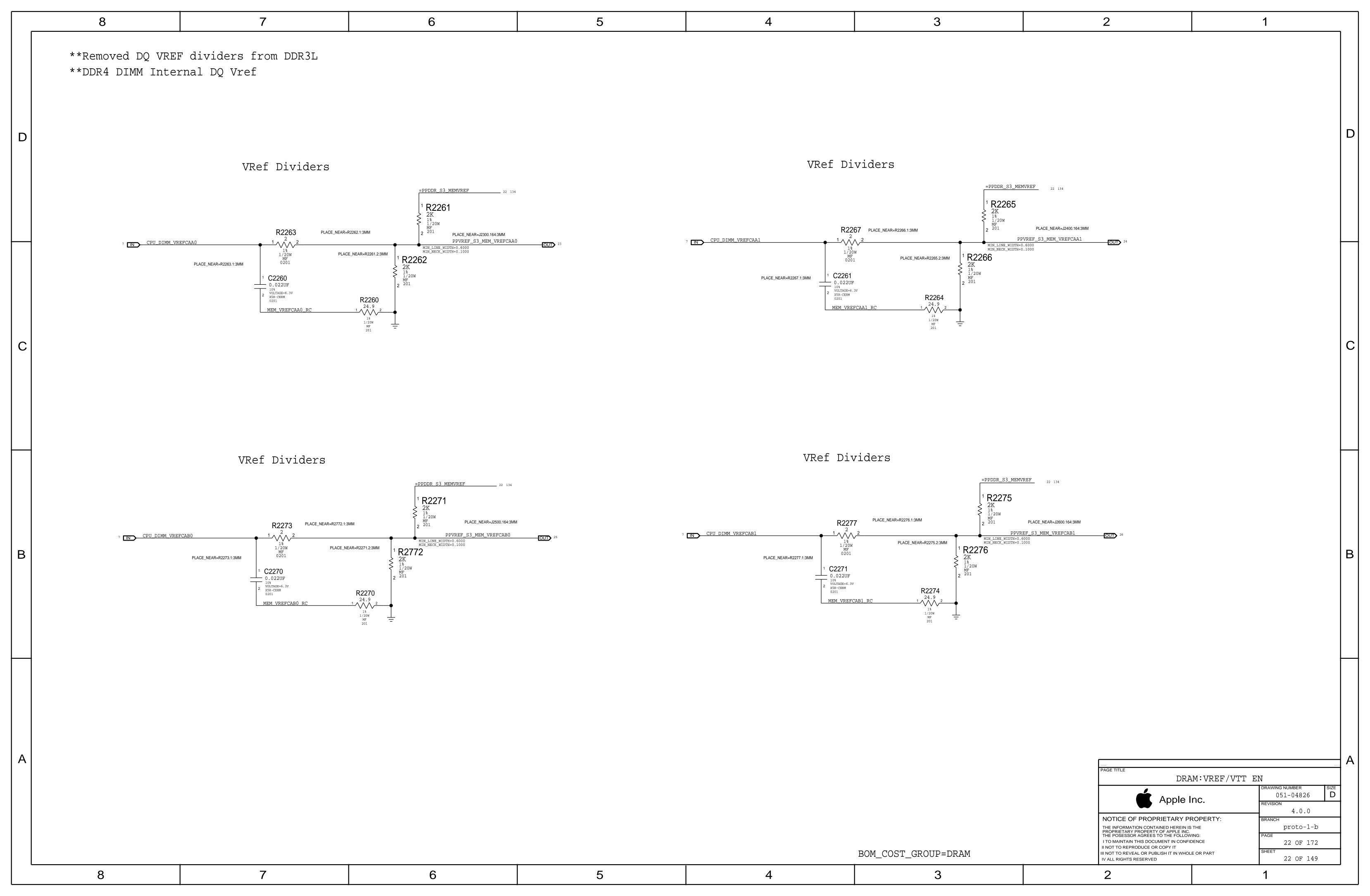


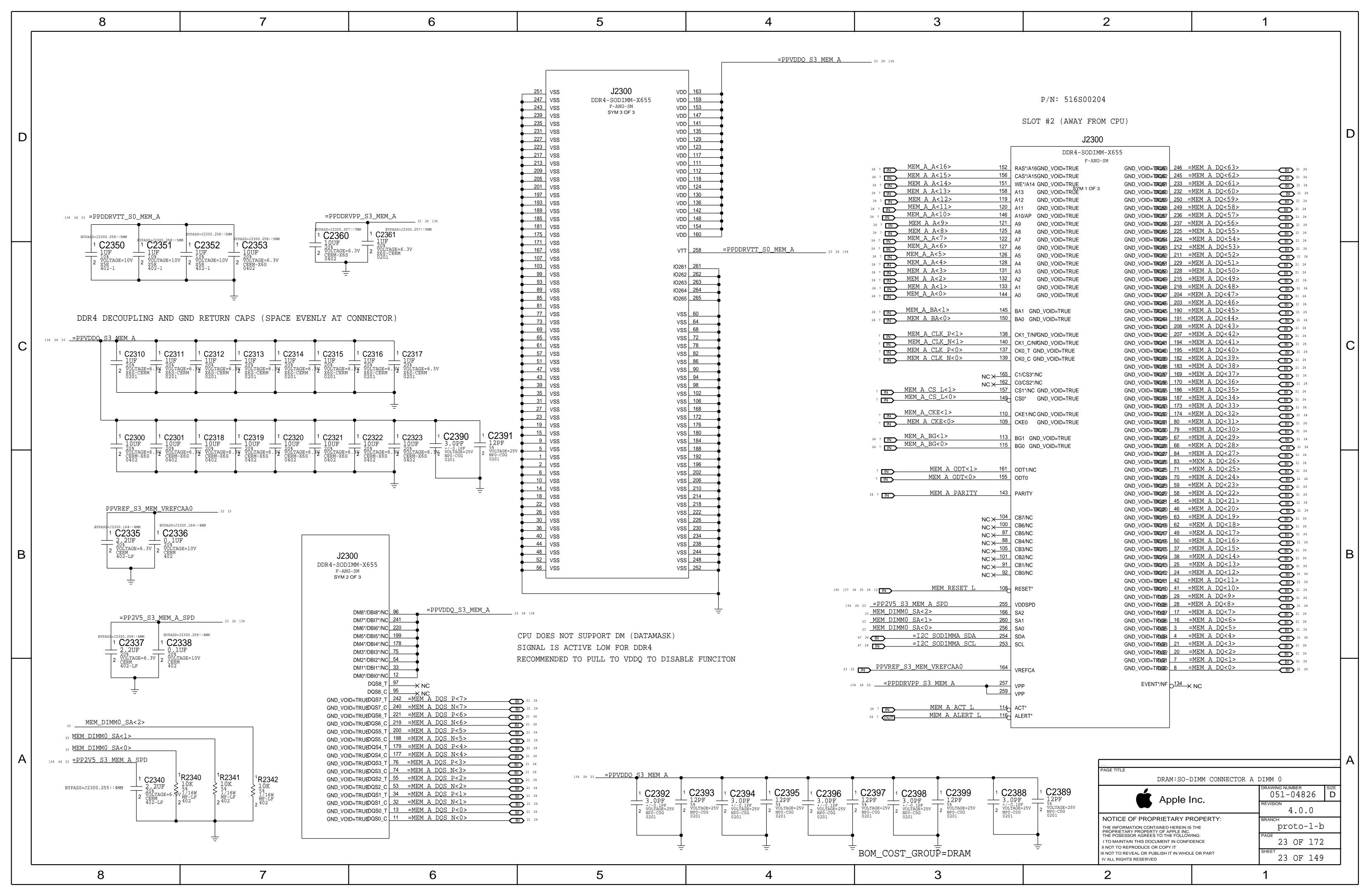


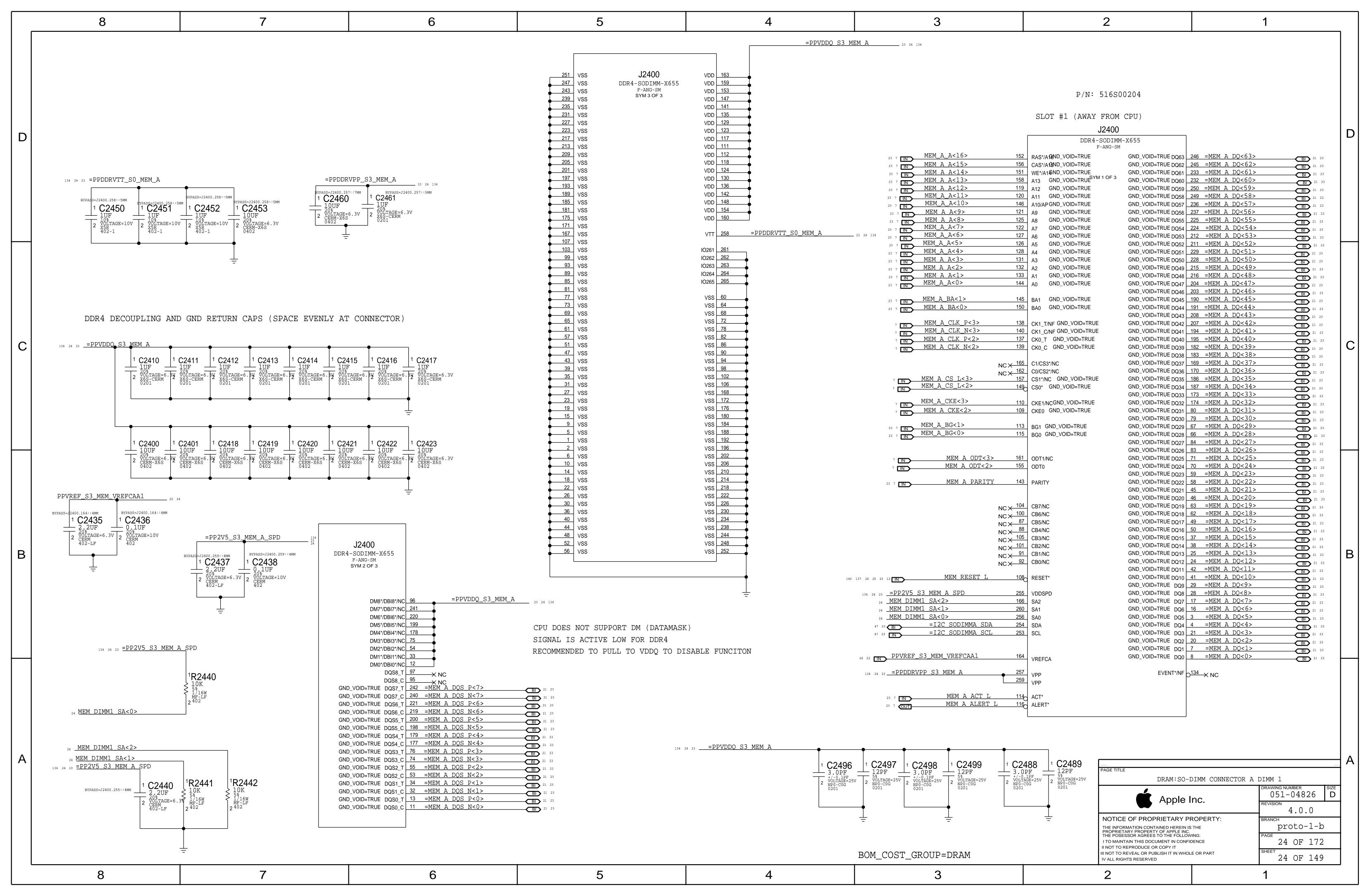


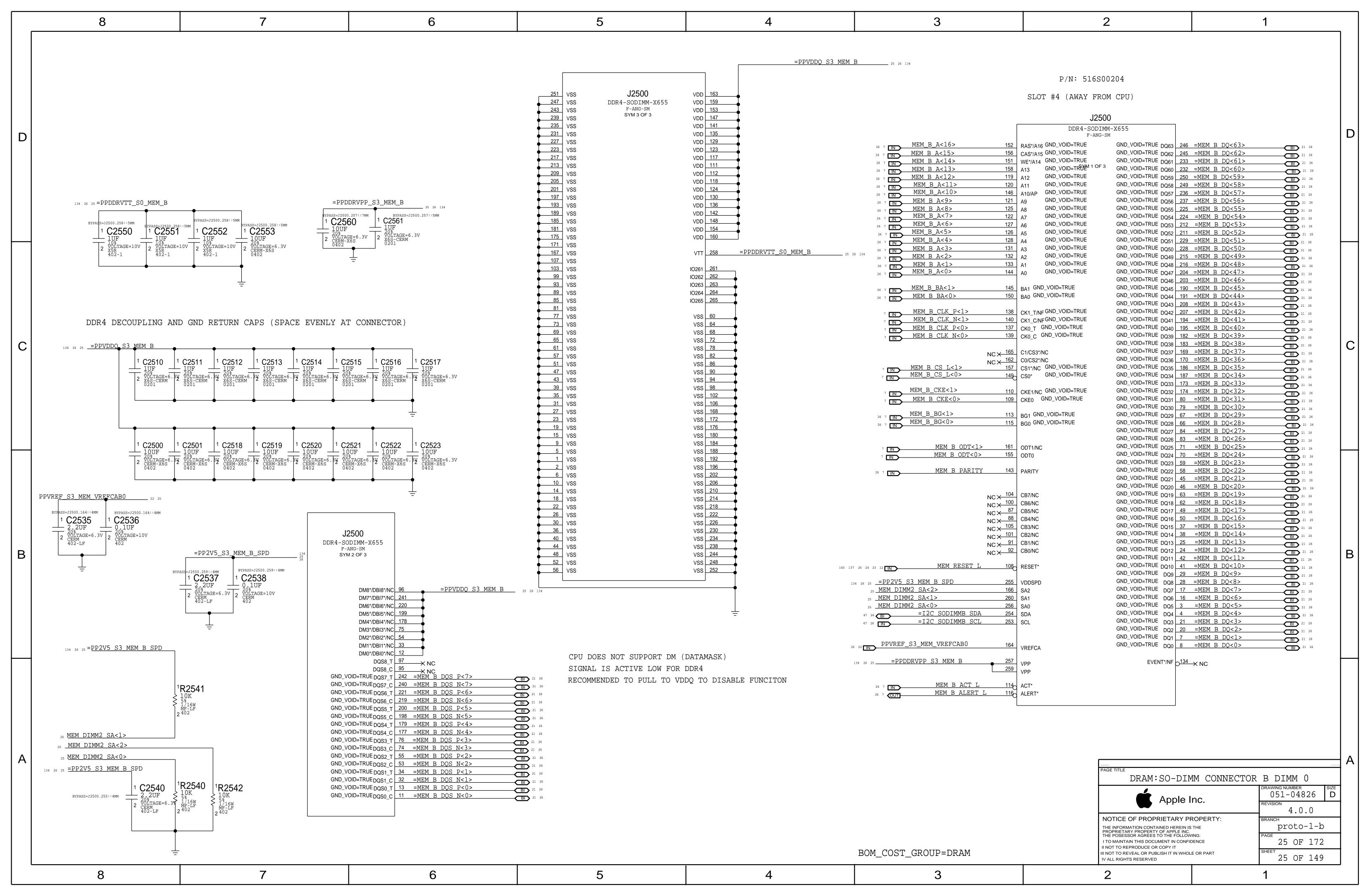


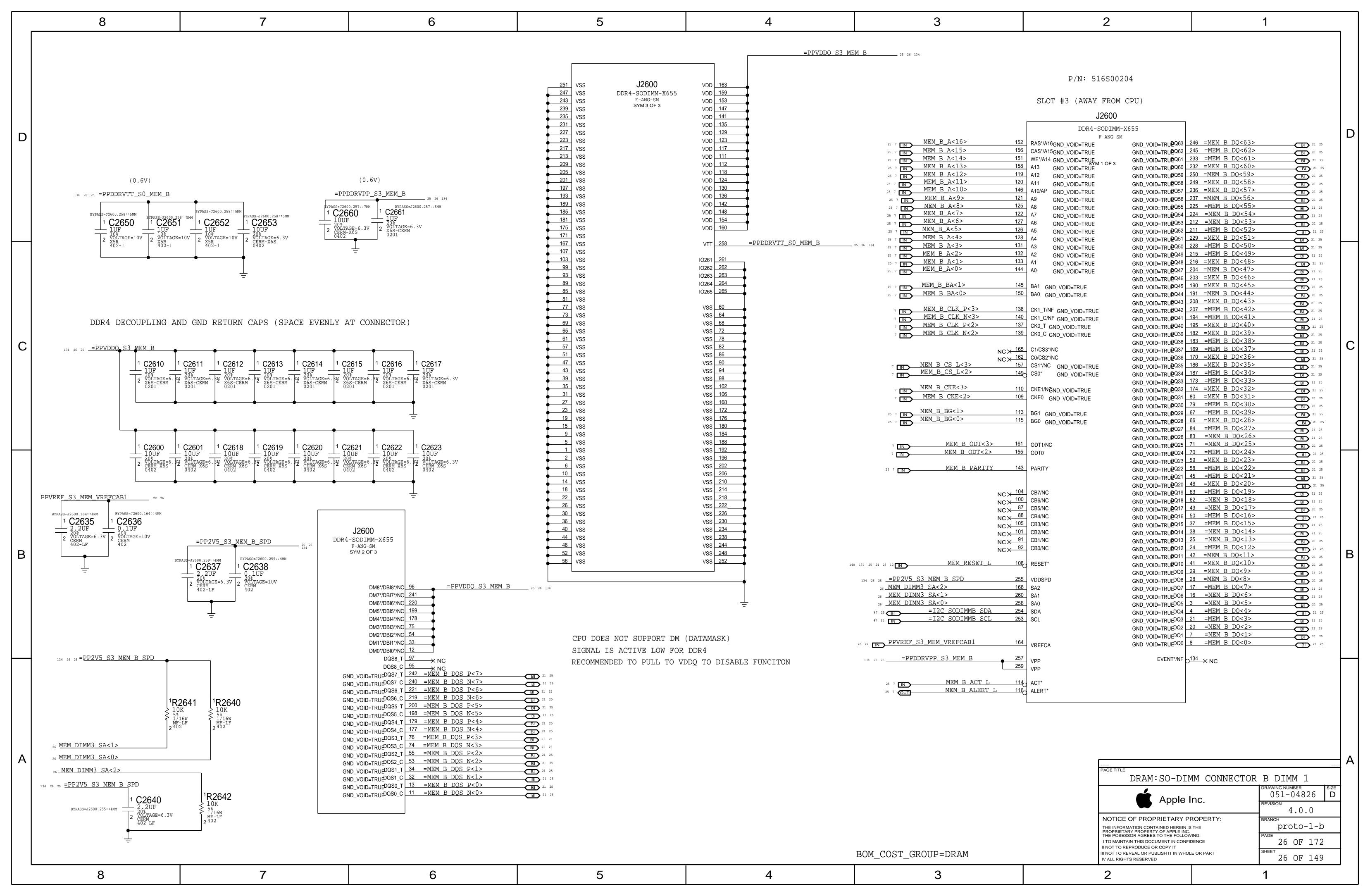
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		!	THERE ARE DQ PIN	SWAPS WITHIN A BYTE		•	•	•	
	7 MEM A DQS_N<0> MEM A DQS_P<0>	MAKE_BASE=TRUE	= MEM A DOS N<0> 23 24 = MEM A DOS P<0> 23 24	7 MEM B DQS N<0> ————————————————————————————————————	=MEM_B_DQS_N<0> 25 26 =MEM_B_DQS_P<0> 25 26				
	MEM A DO<7>	MAKE_BASE=TRUE ——	- =MEM A DO<6> 23 24	MAKE_BASE=TRUE —— 7 MEM B DQ<7> ——	=MEM_B_DQS_F<0> 25 26				
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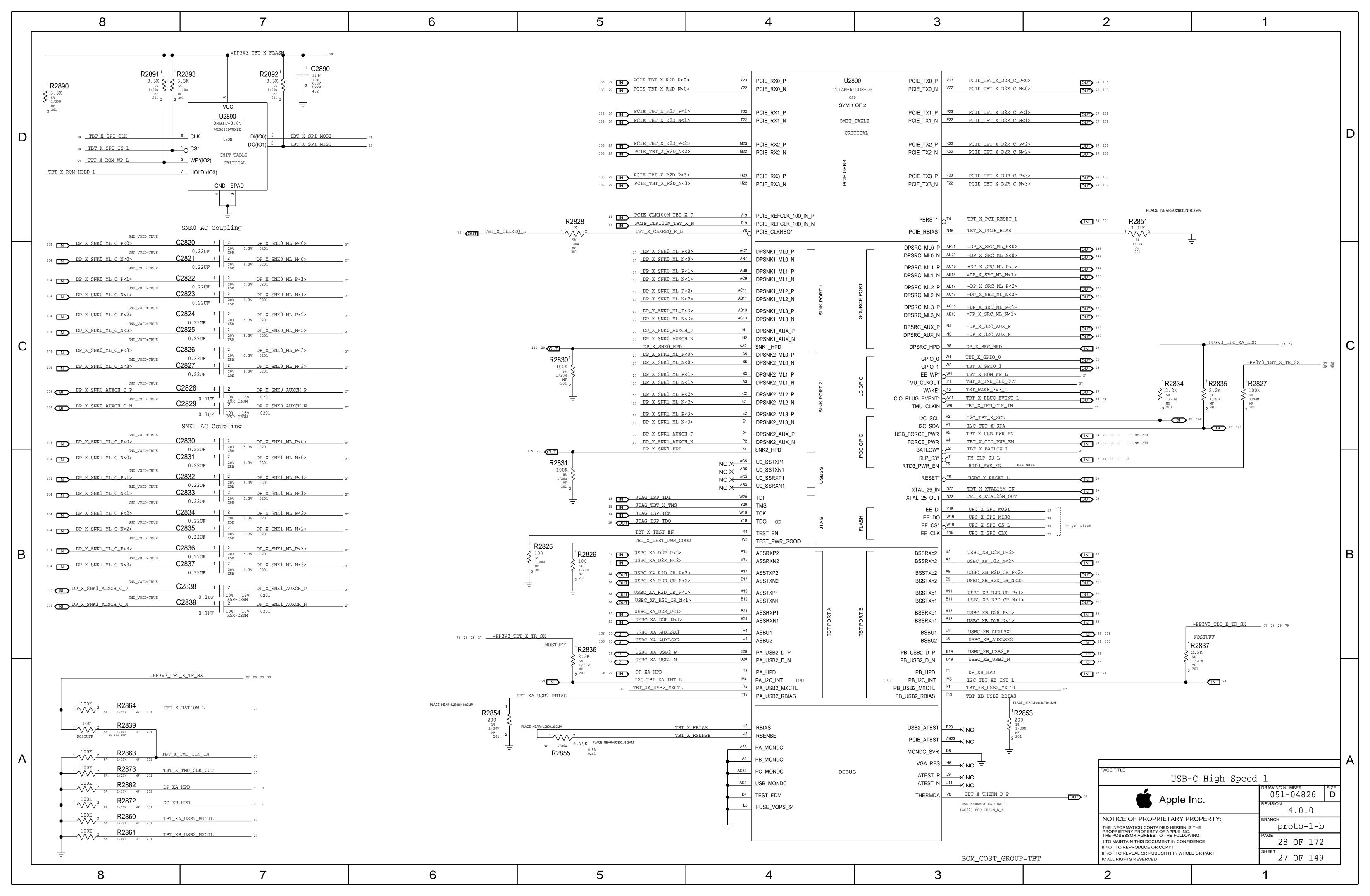


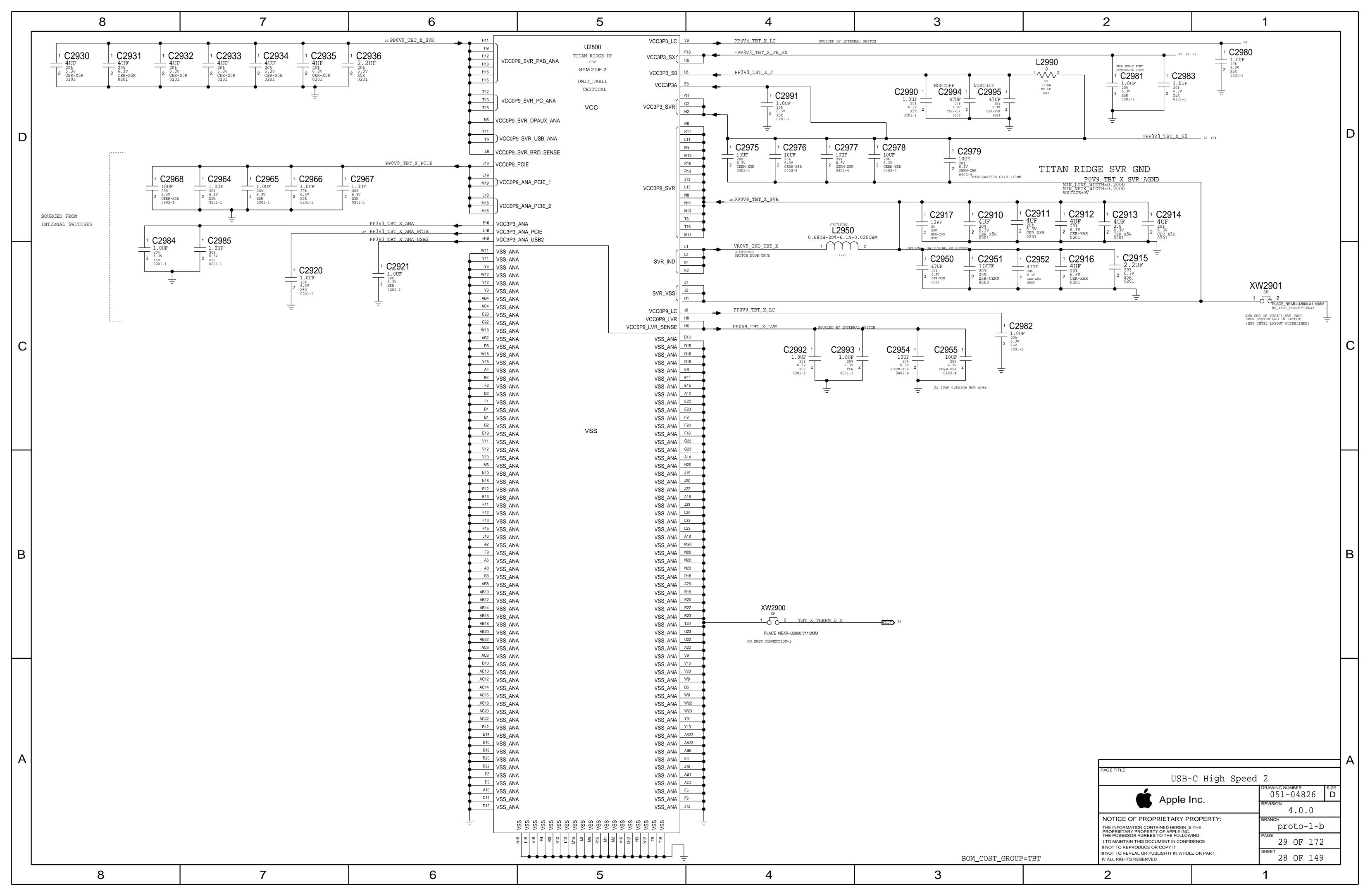


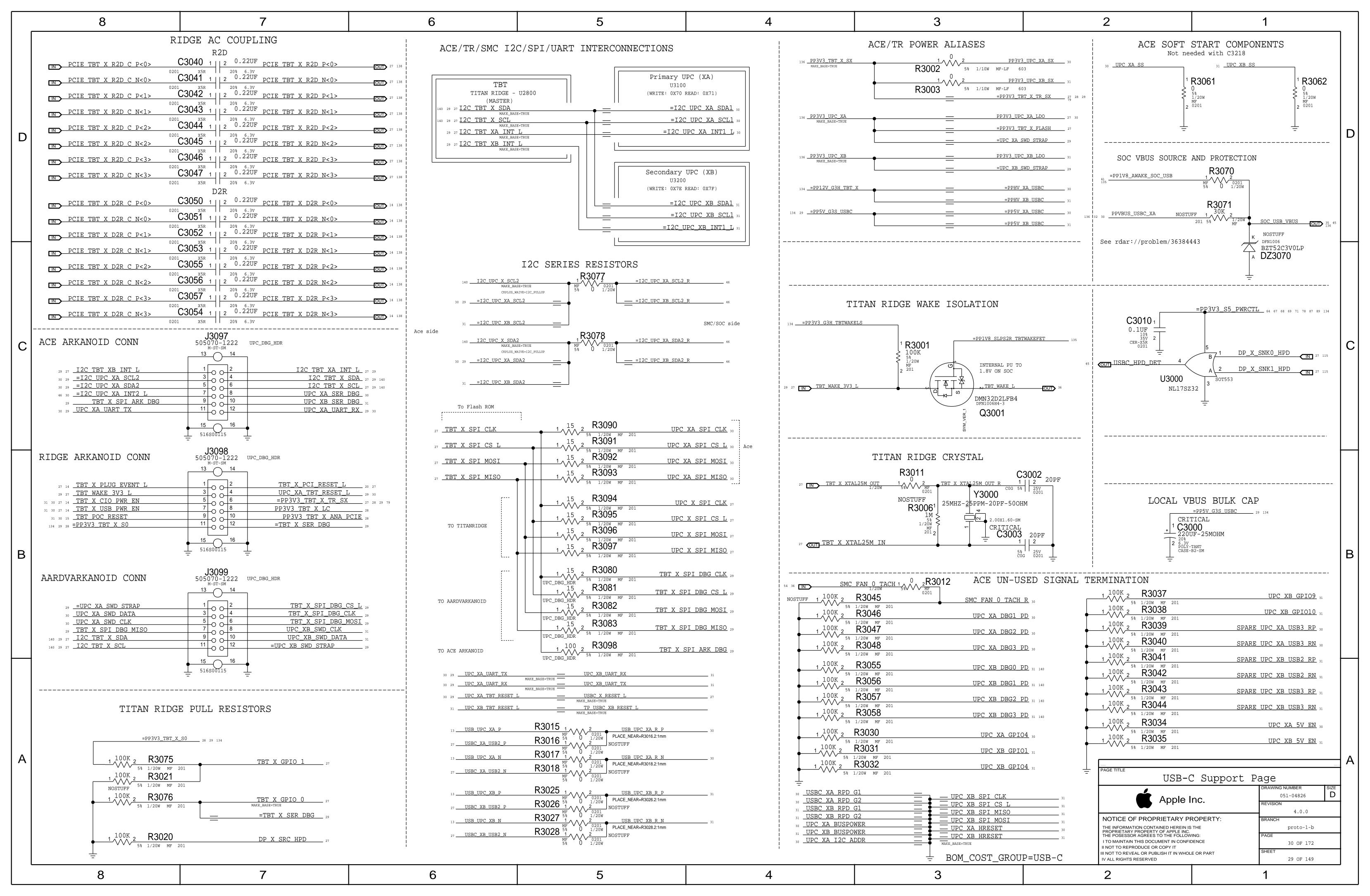


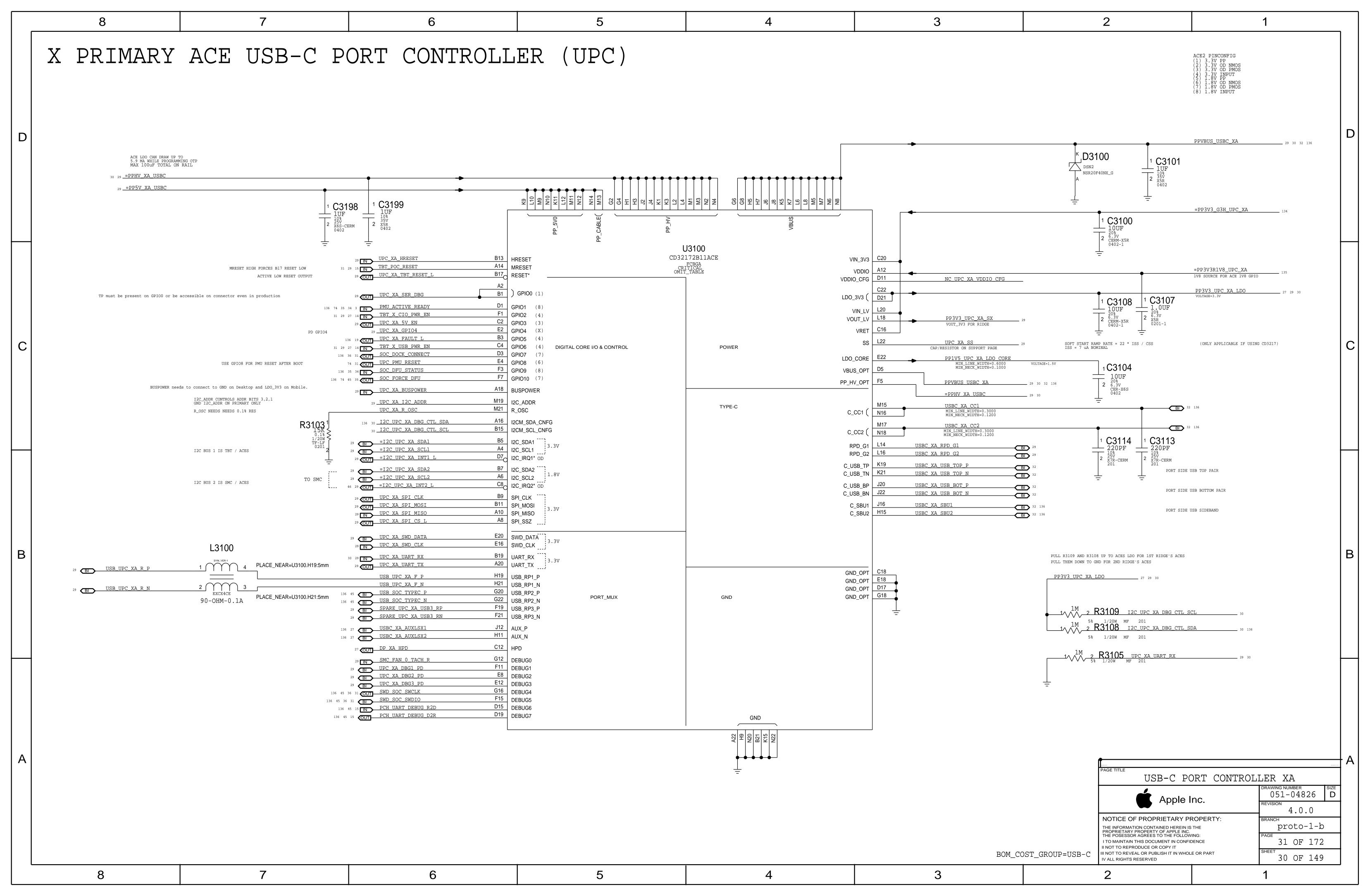


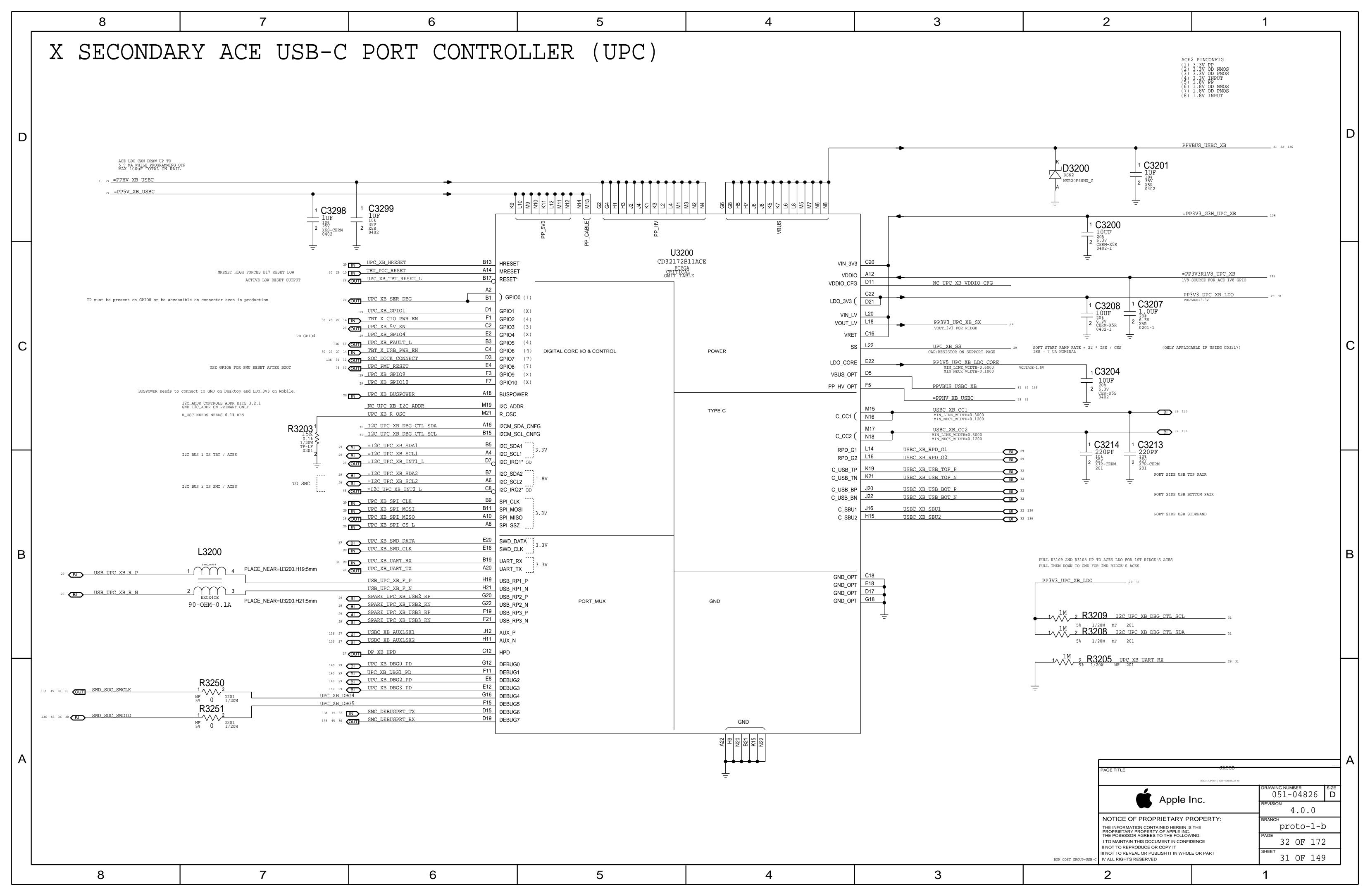


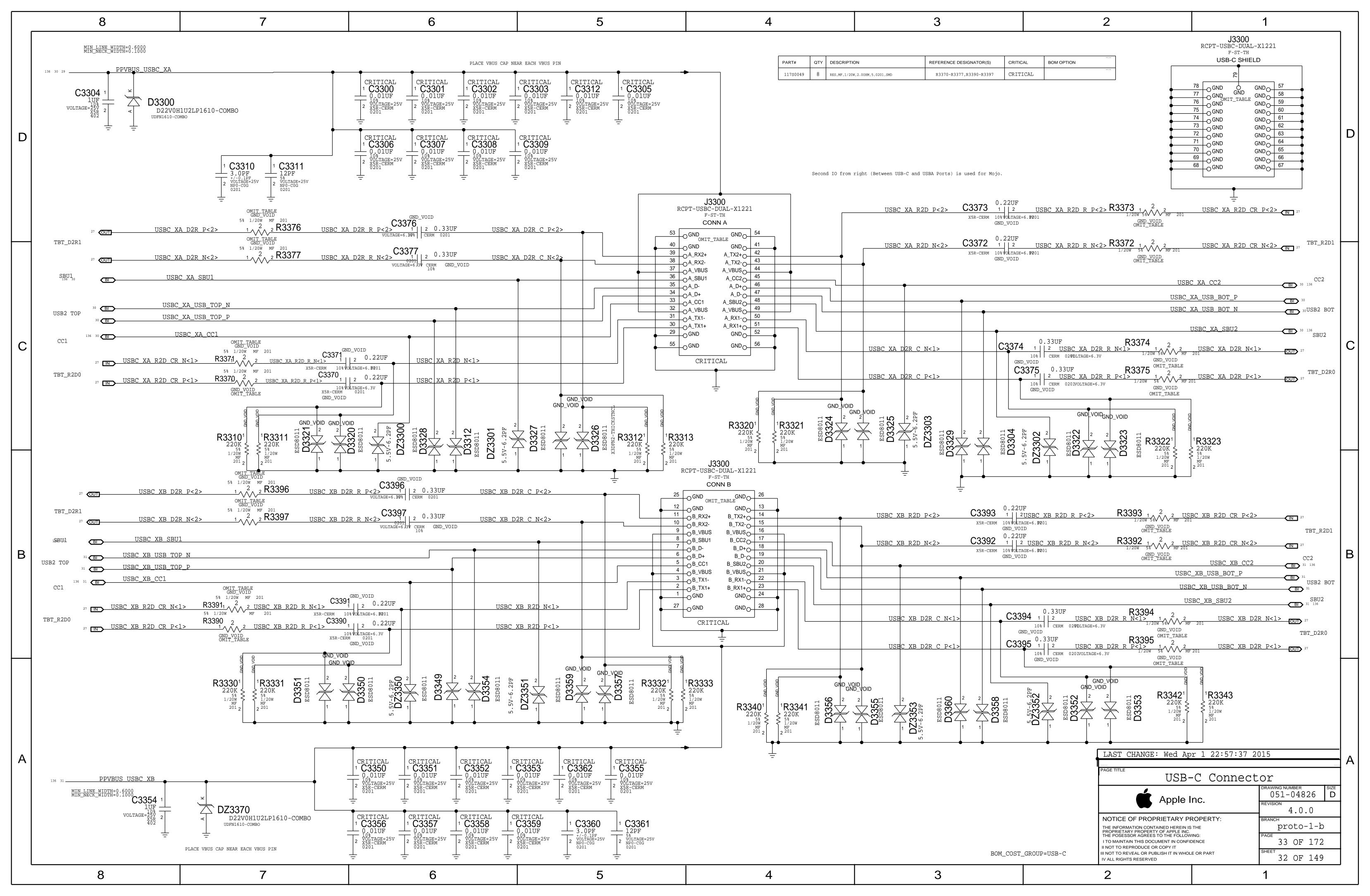


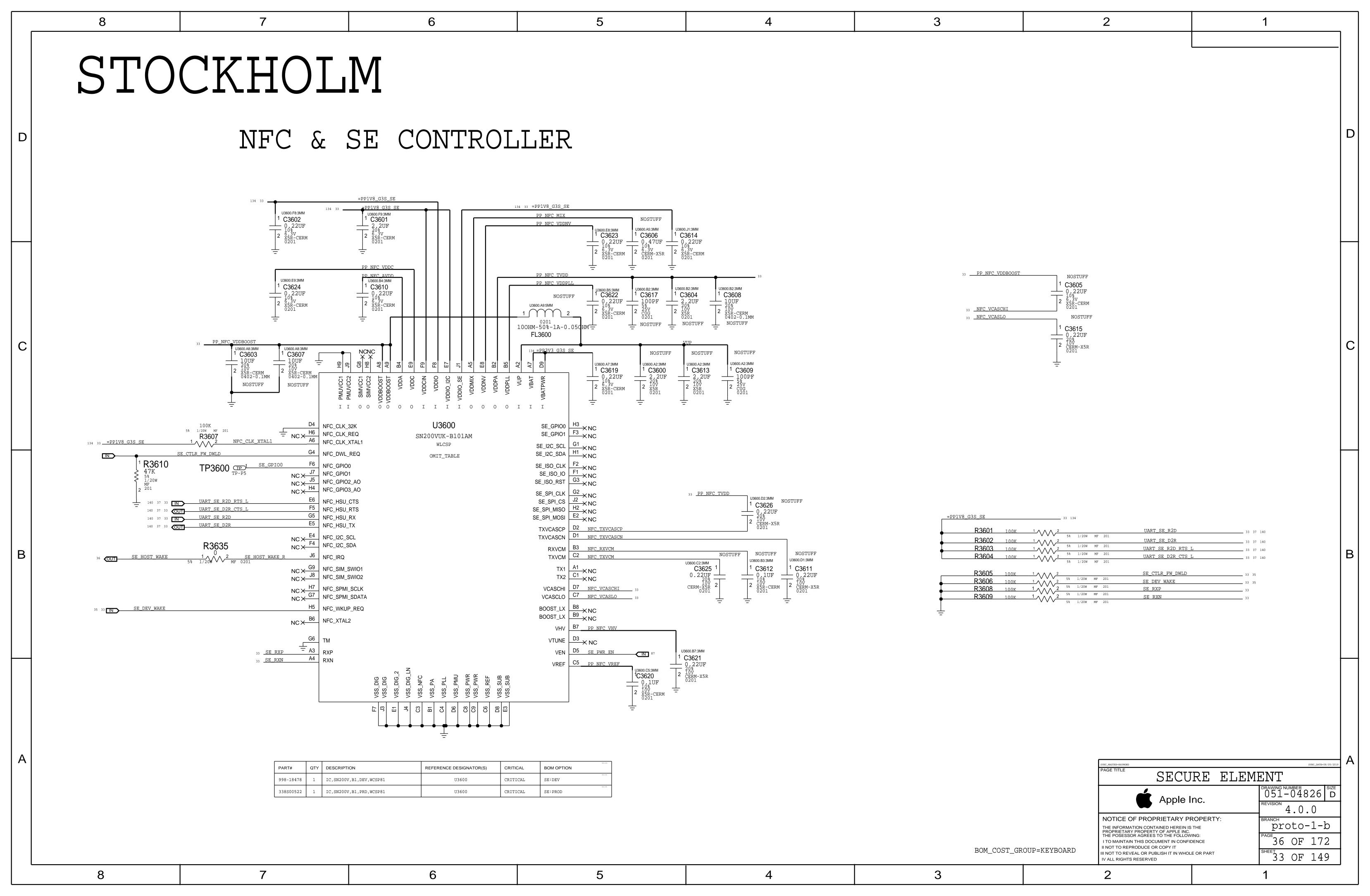


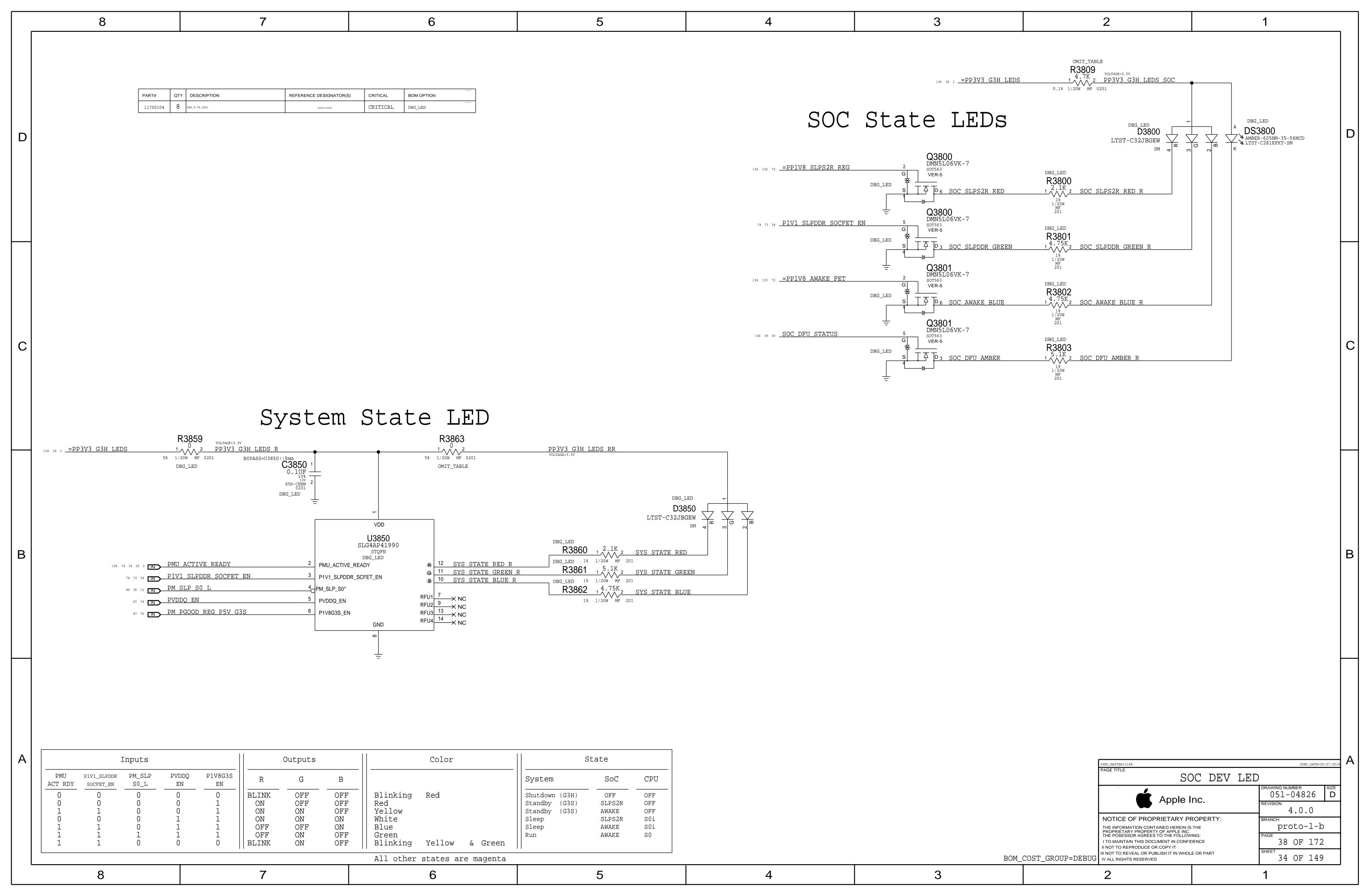


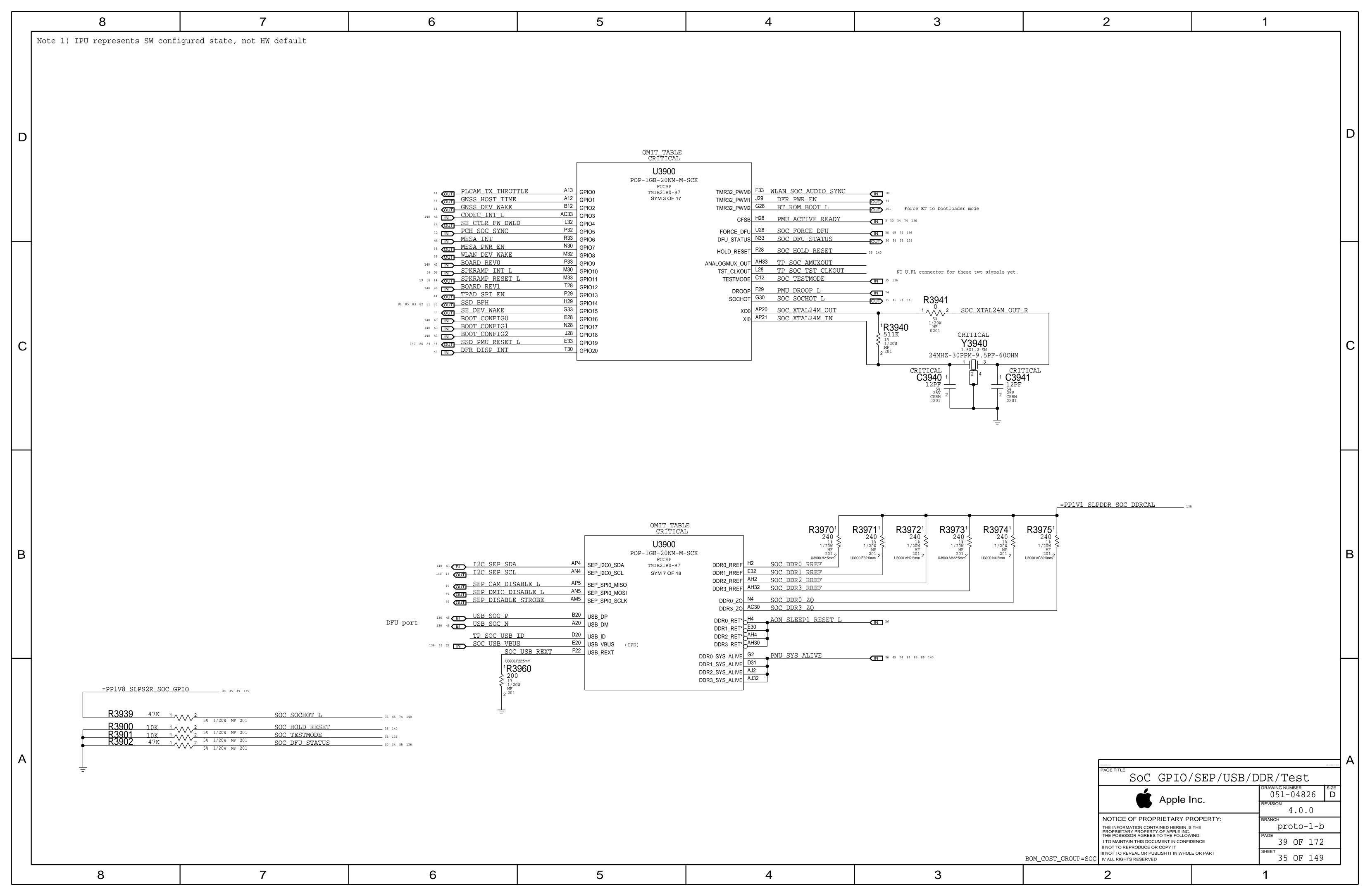


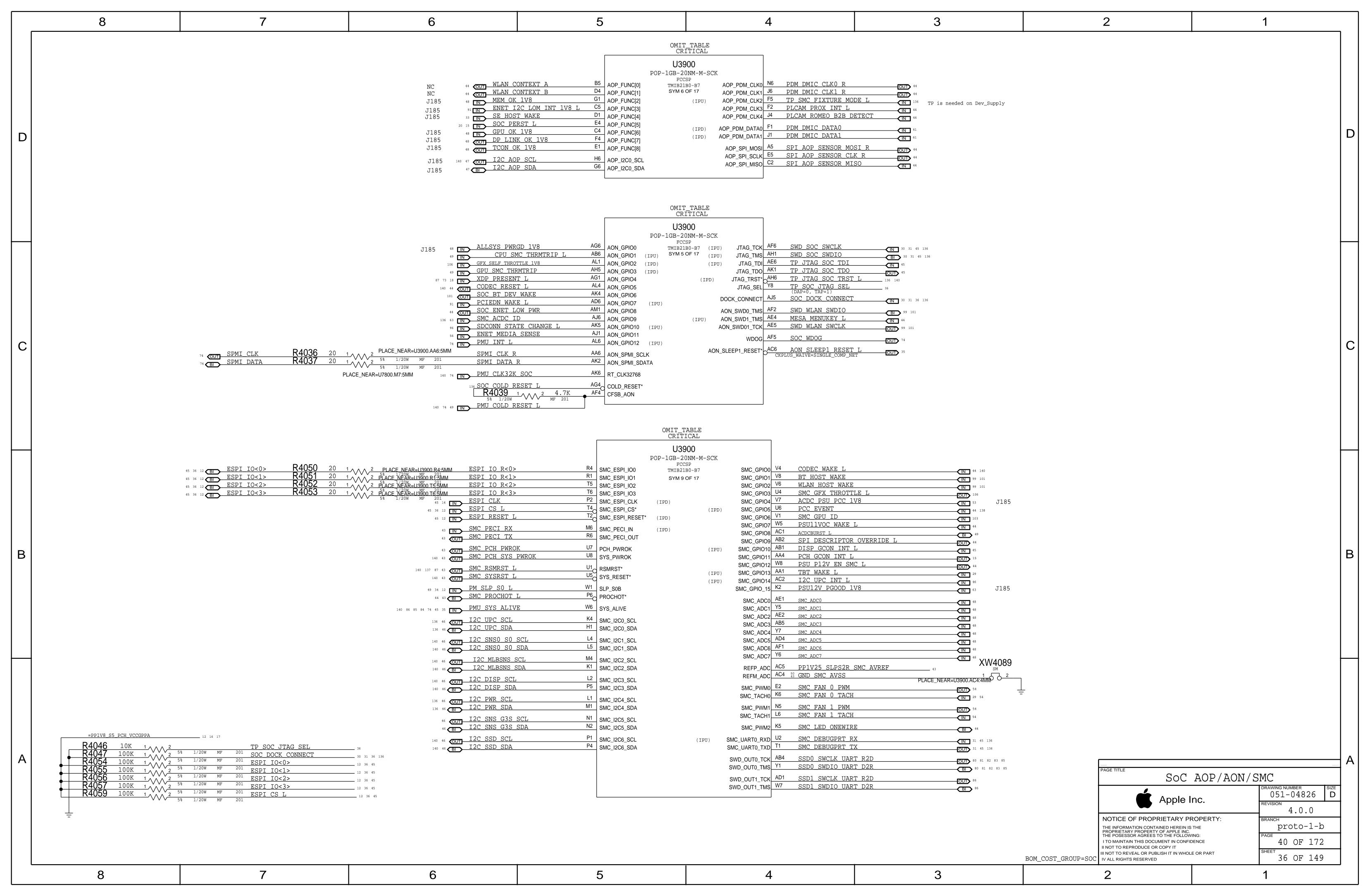




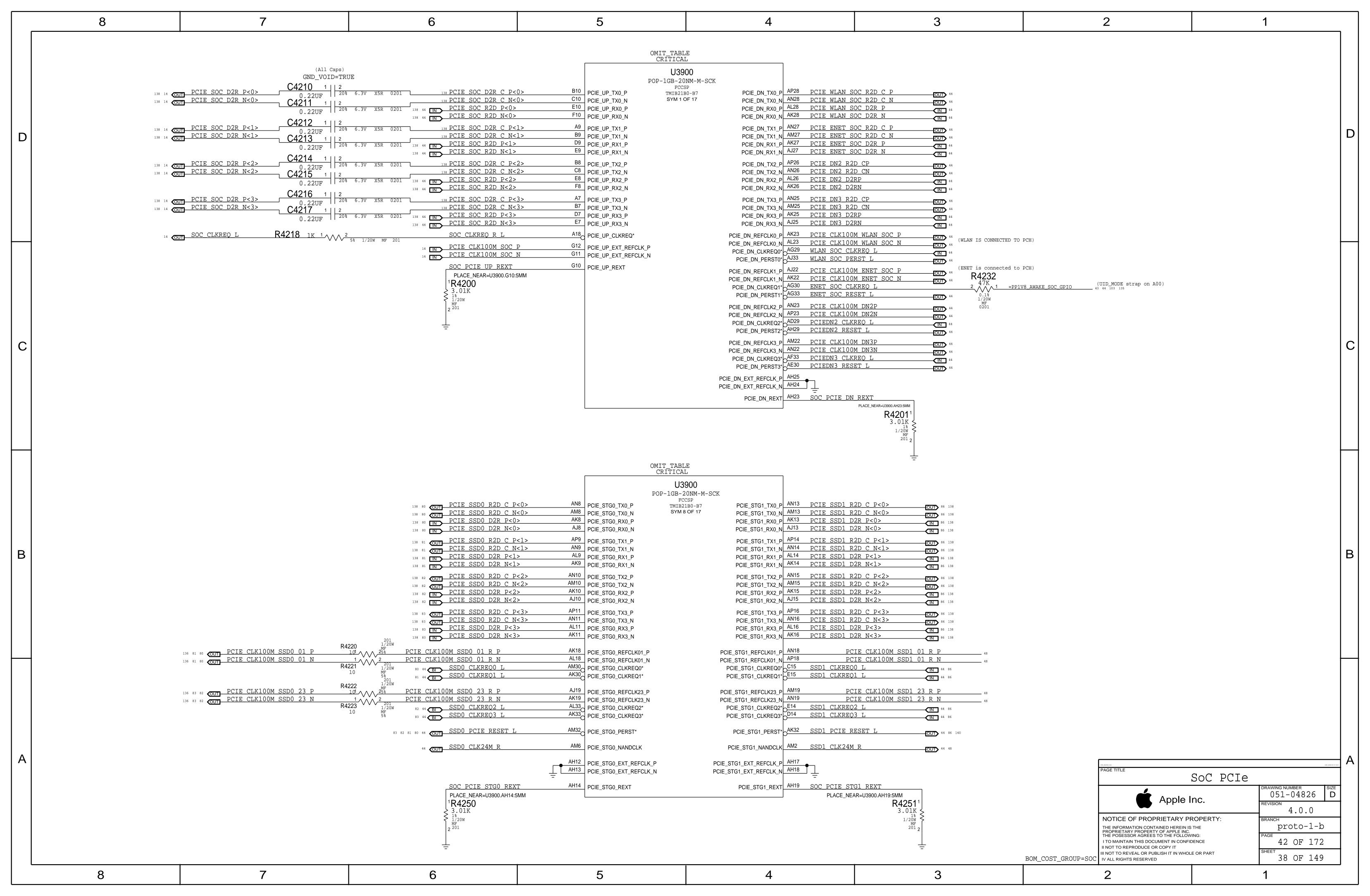


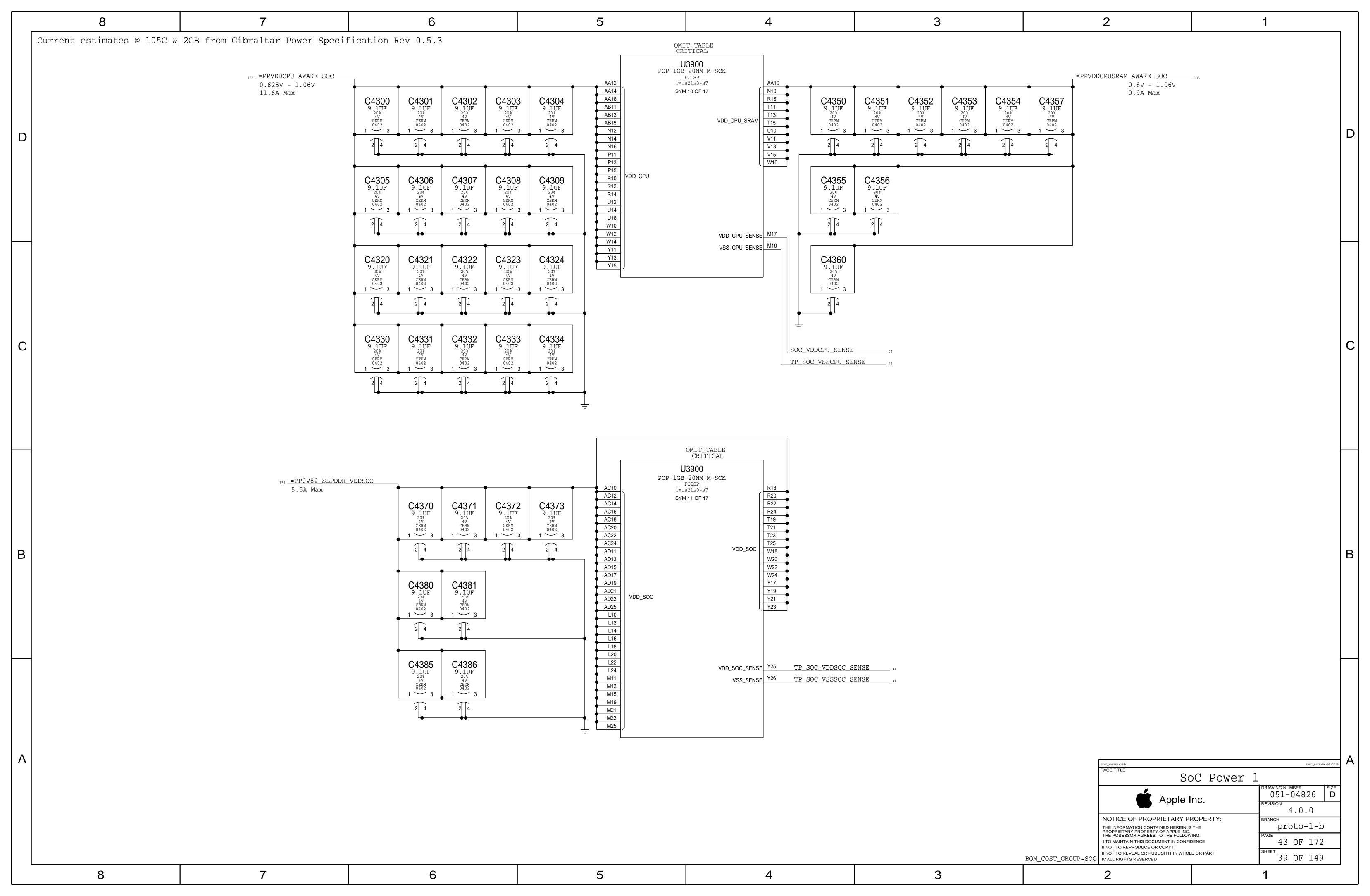


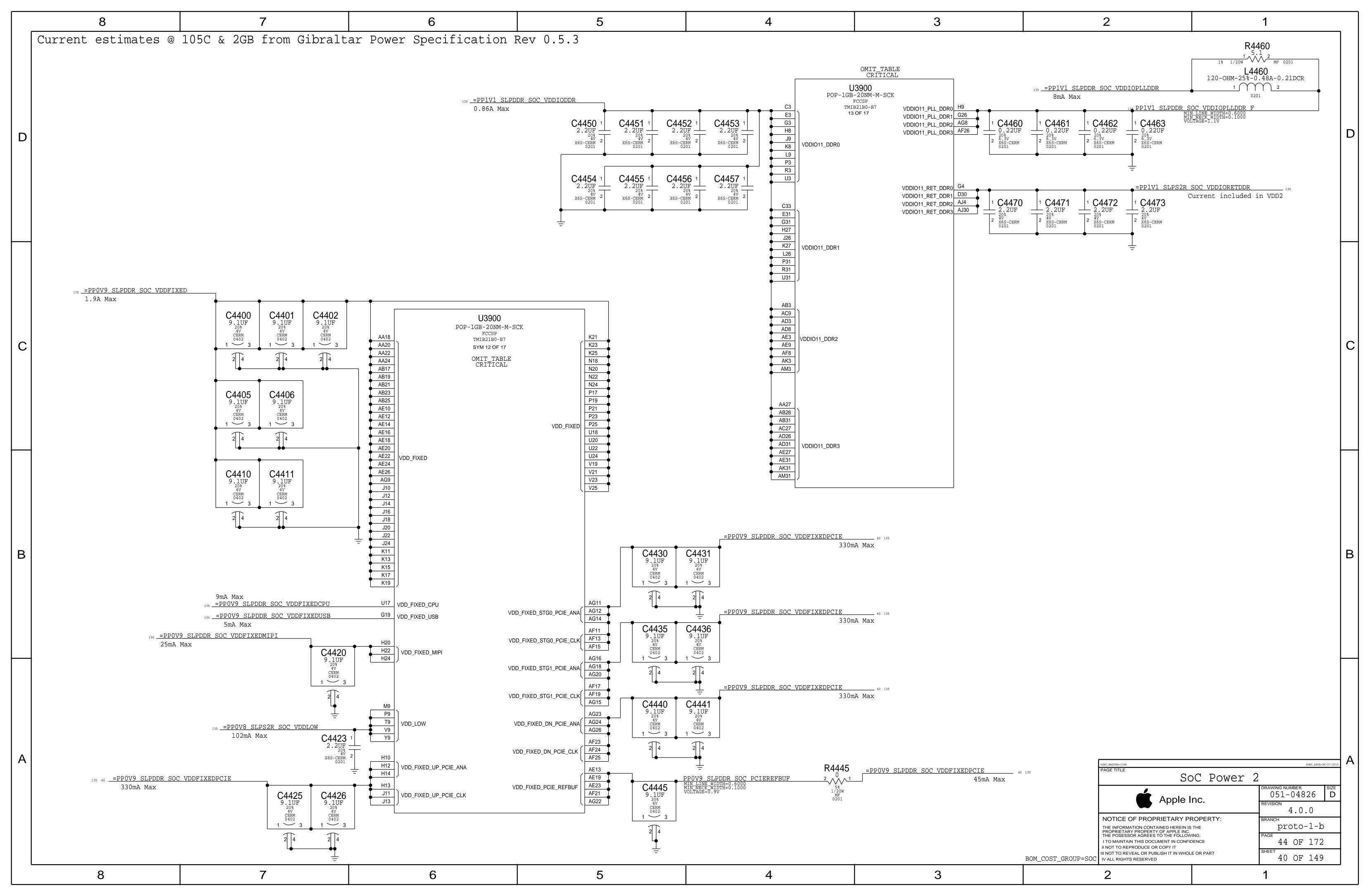


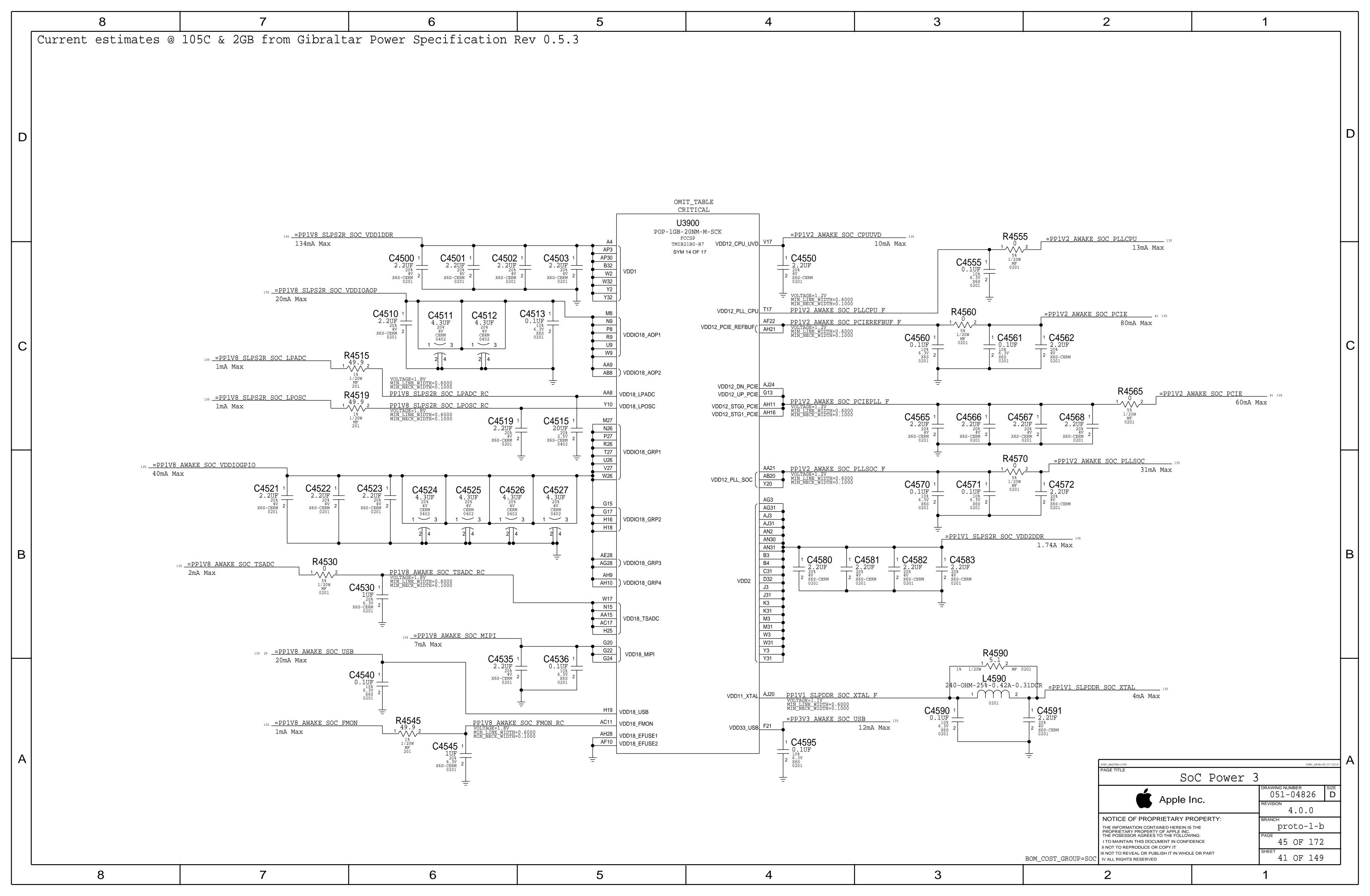


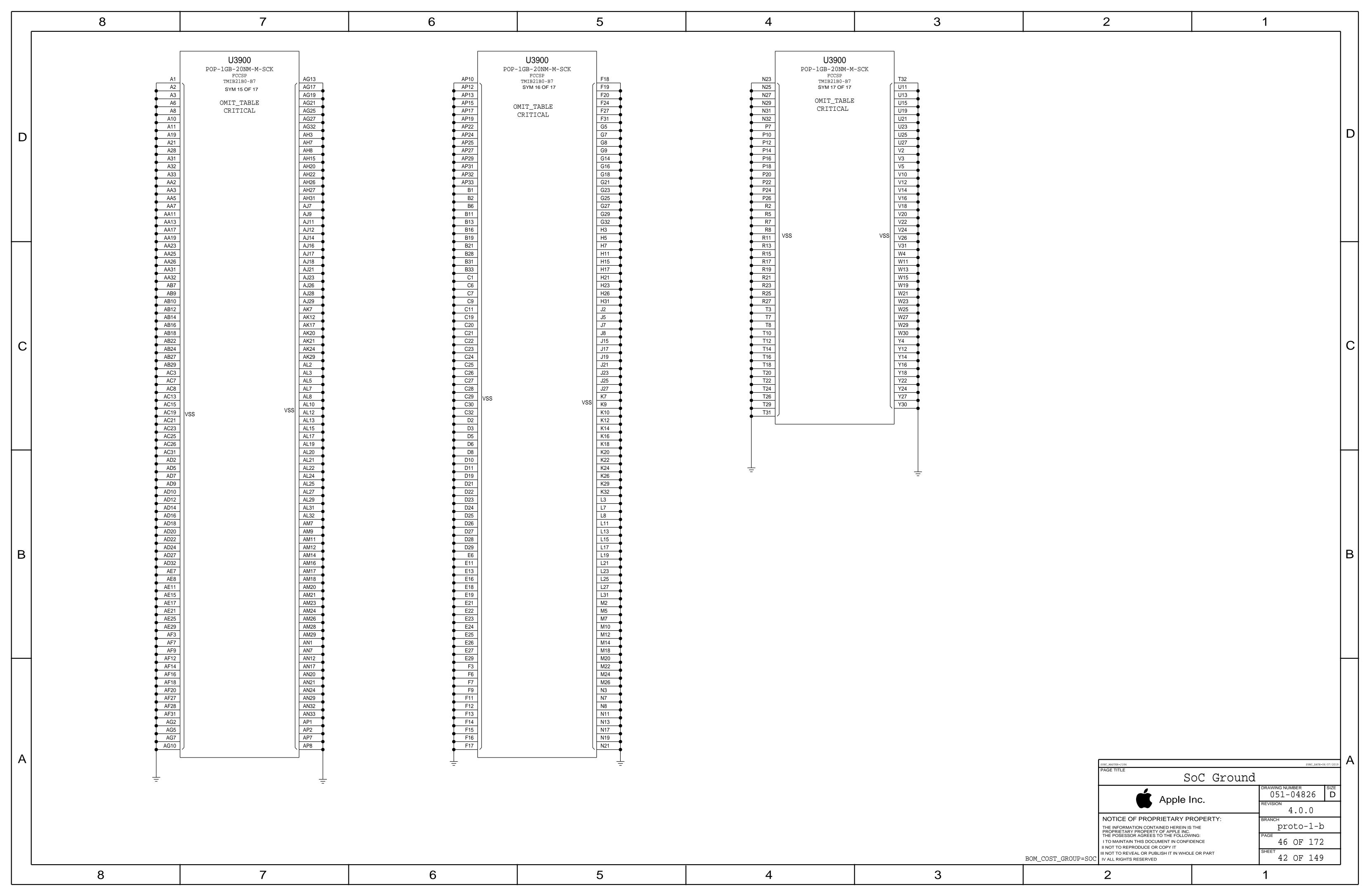


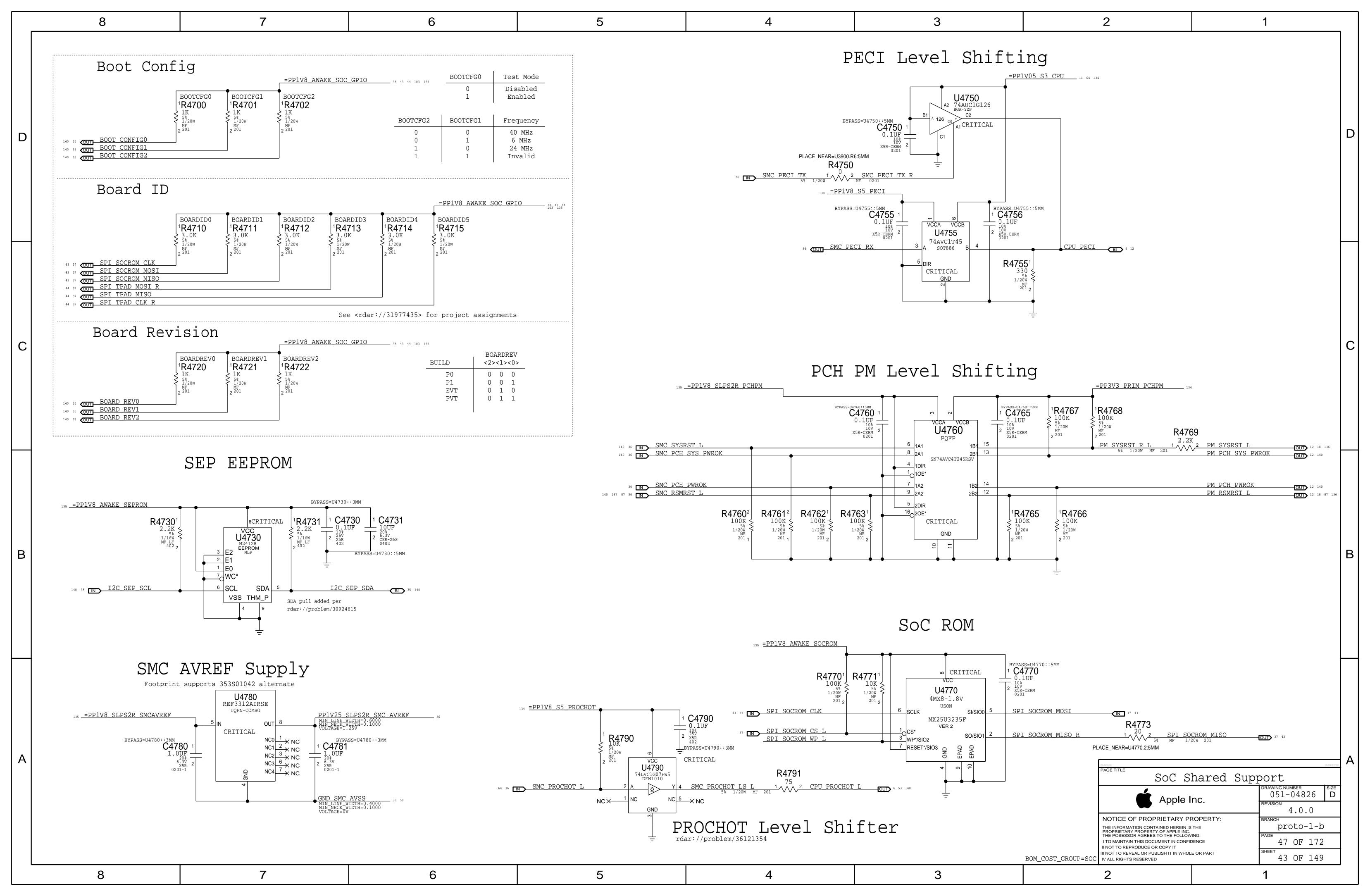




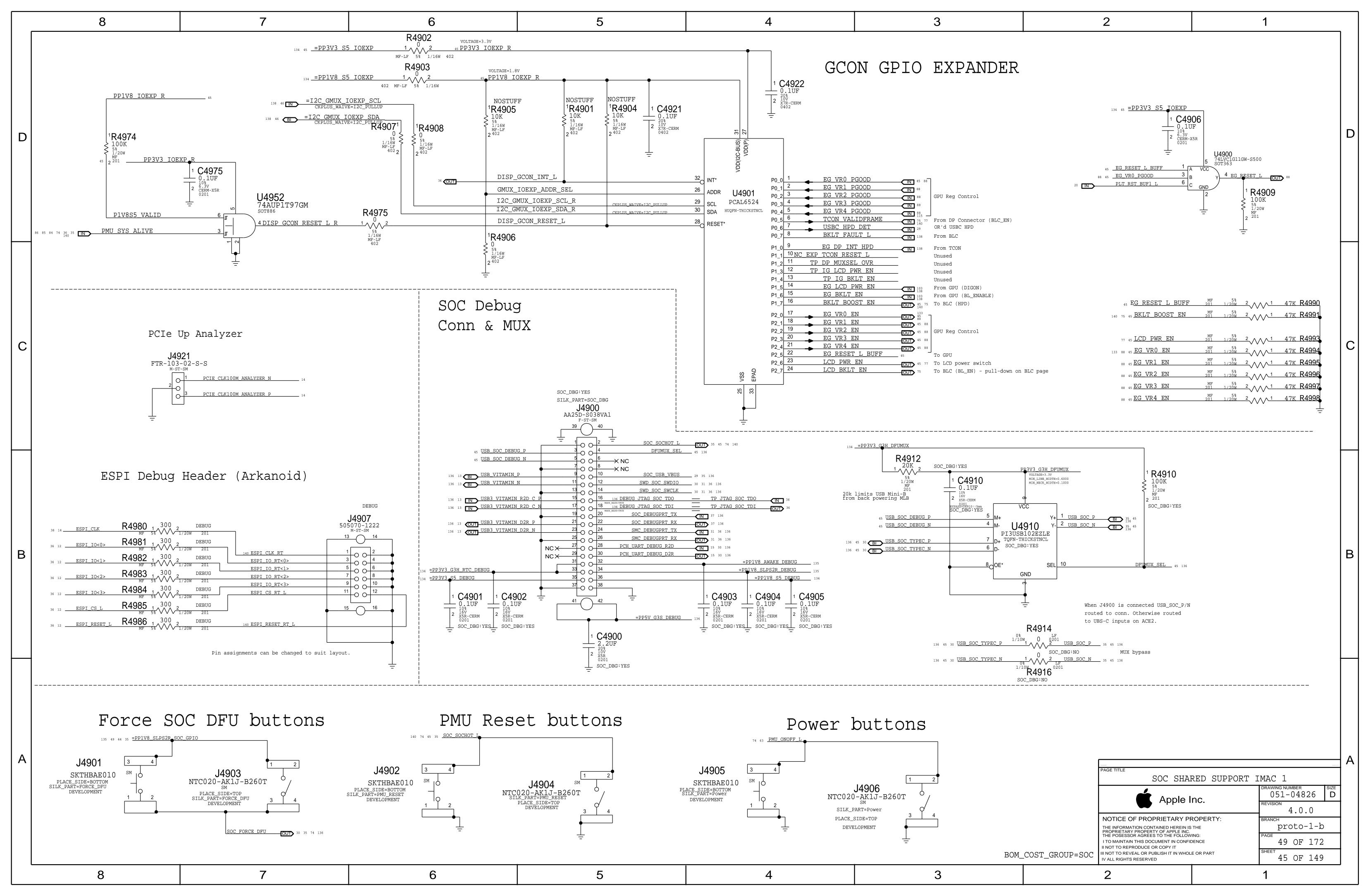


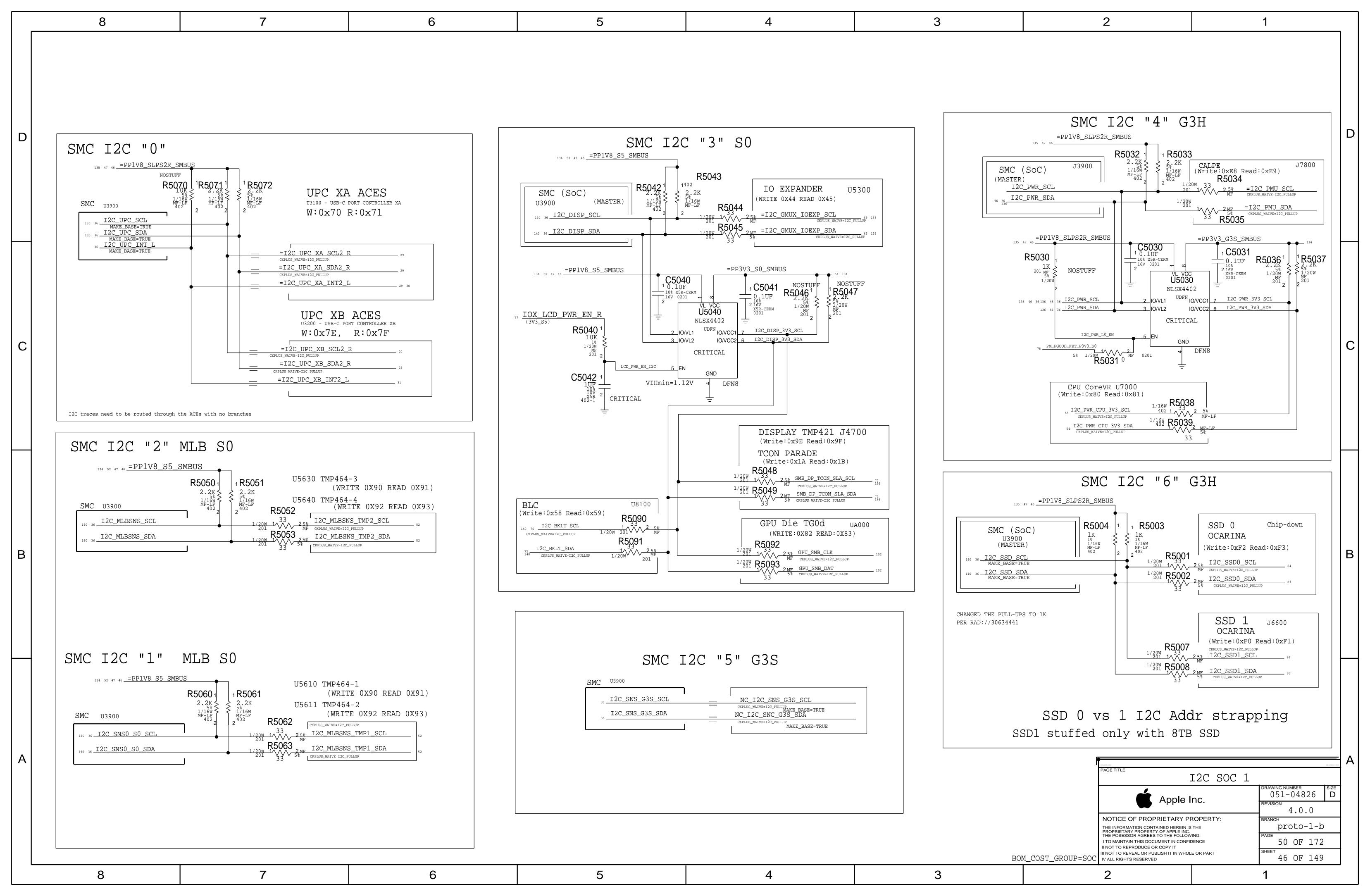


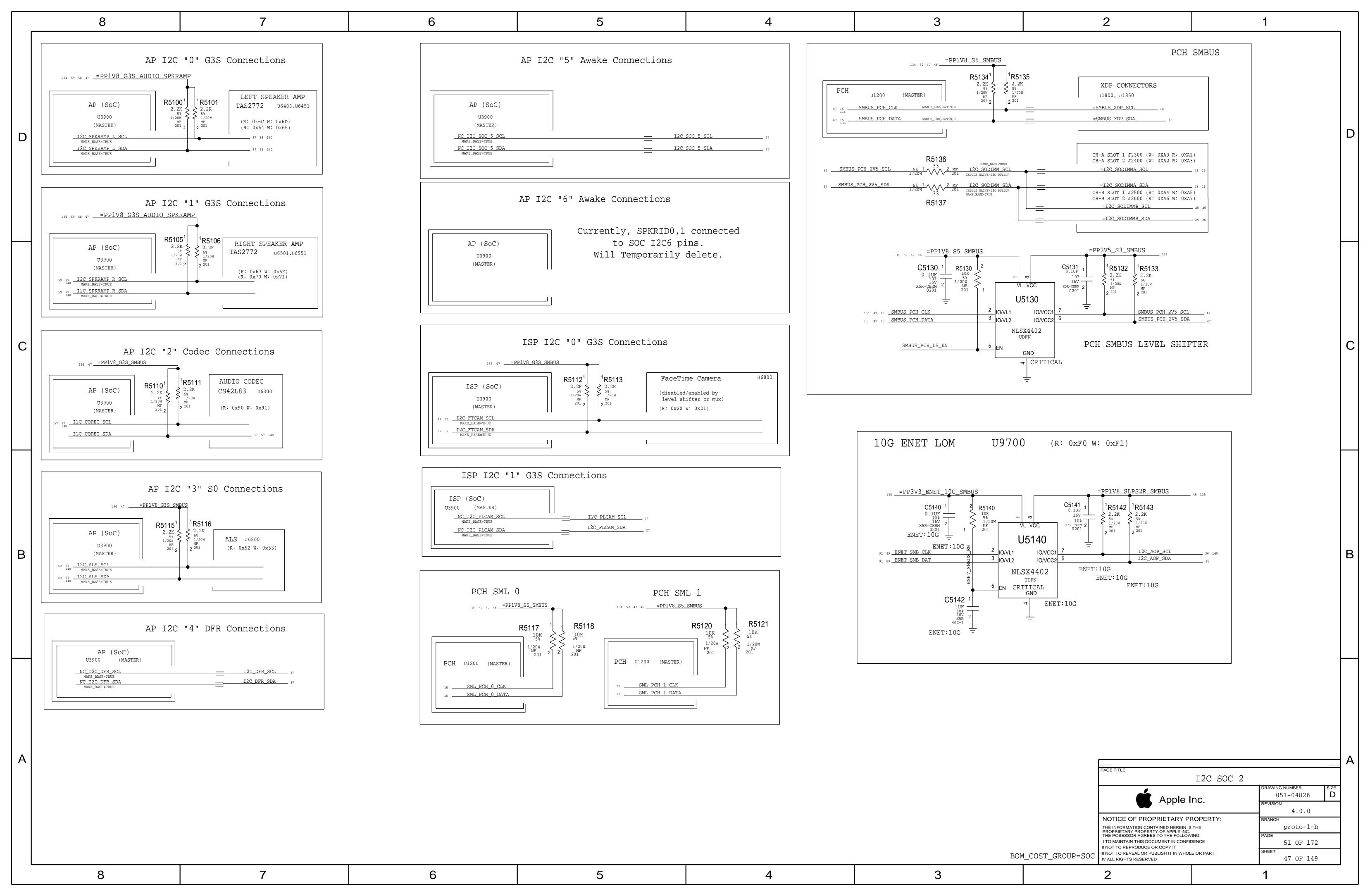


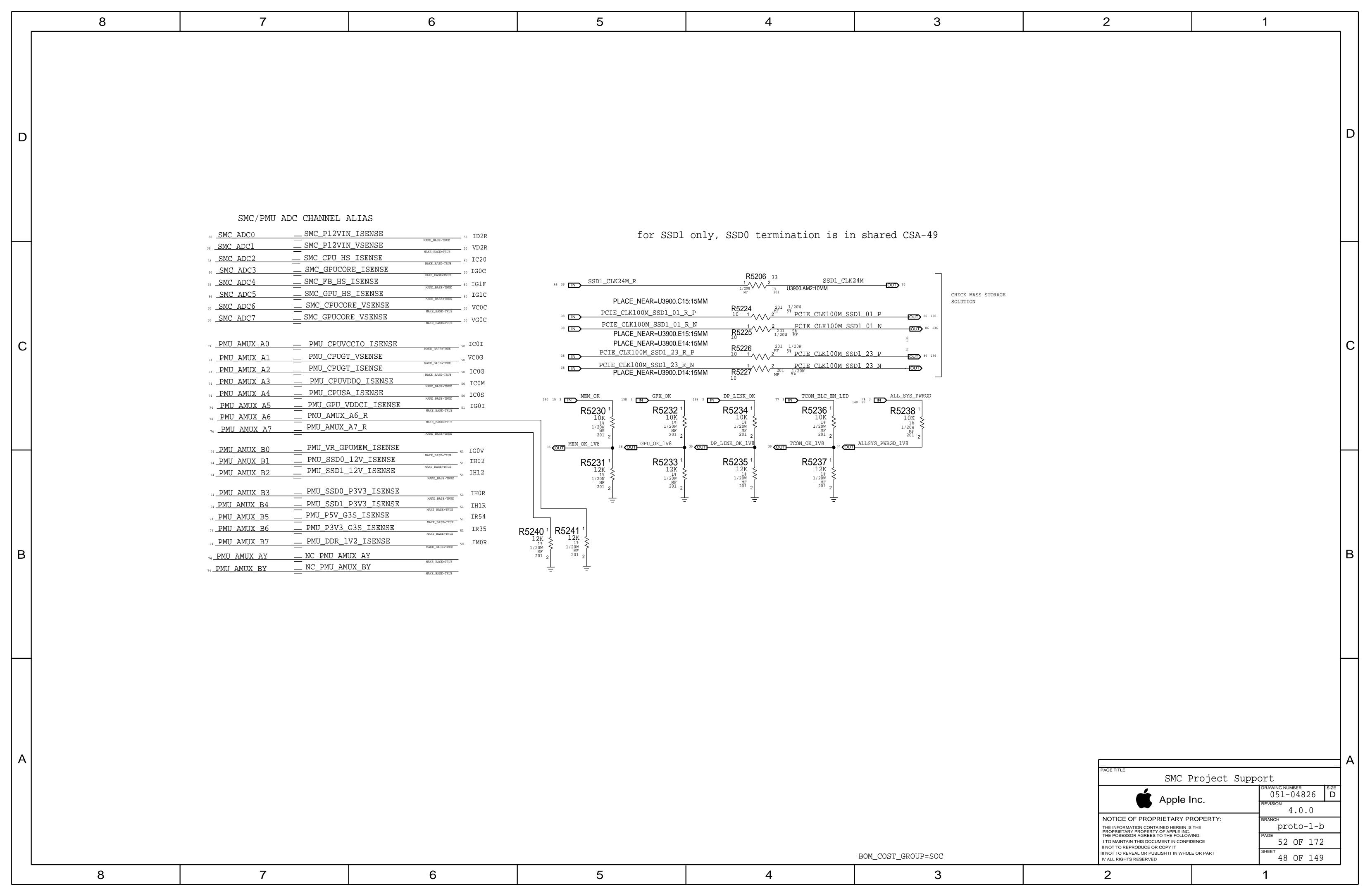


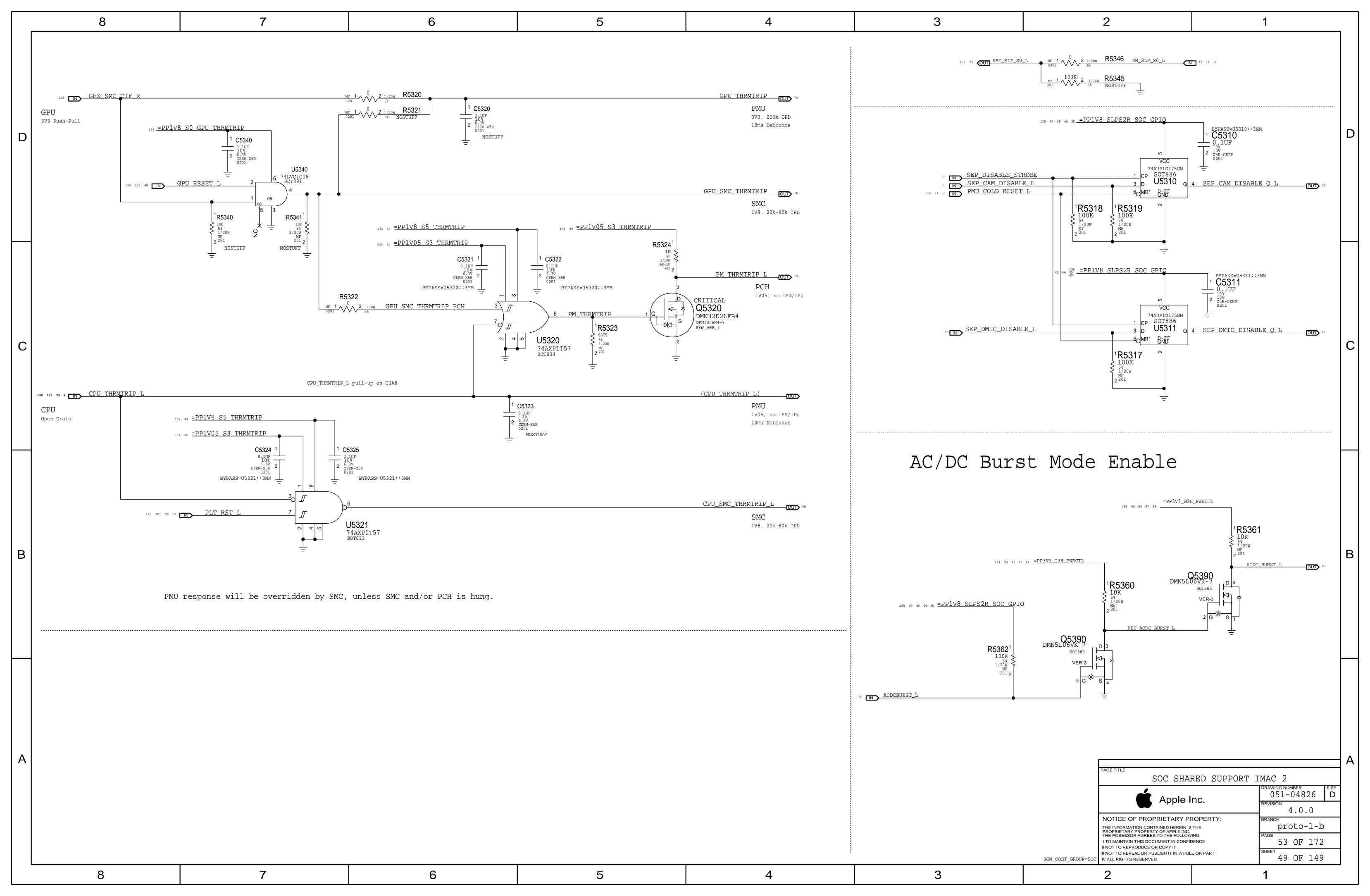


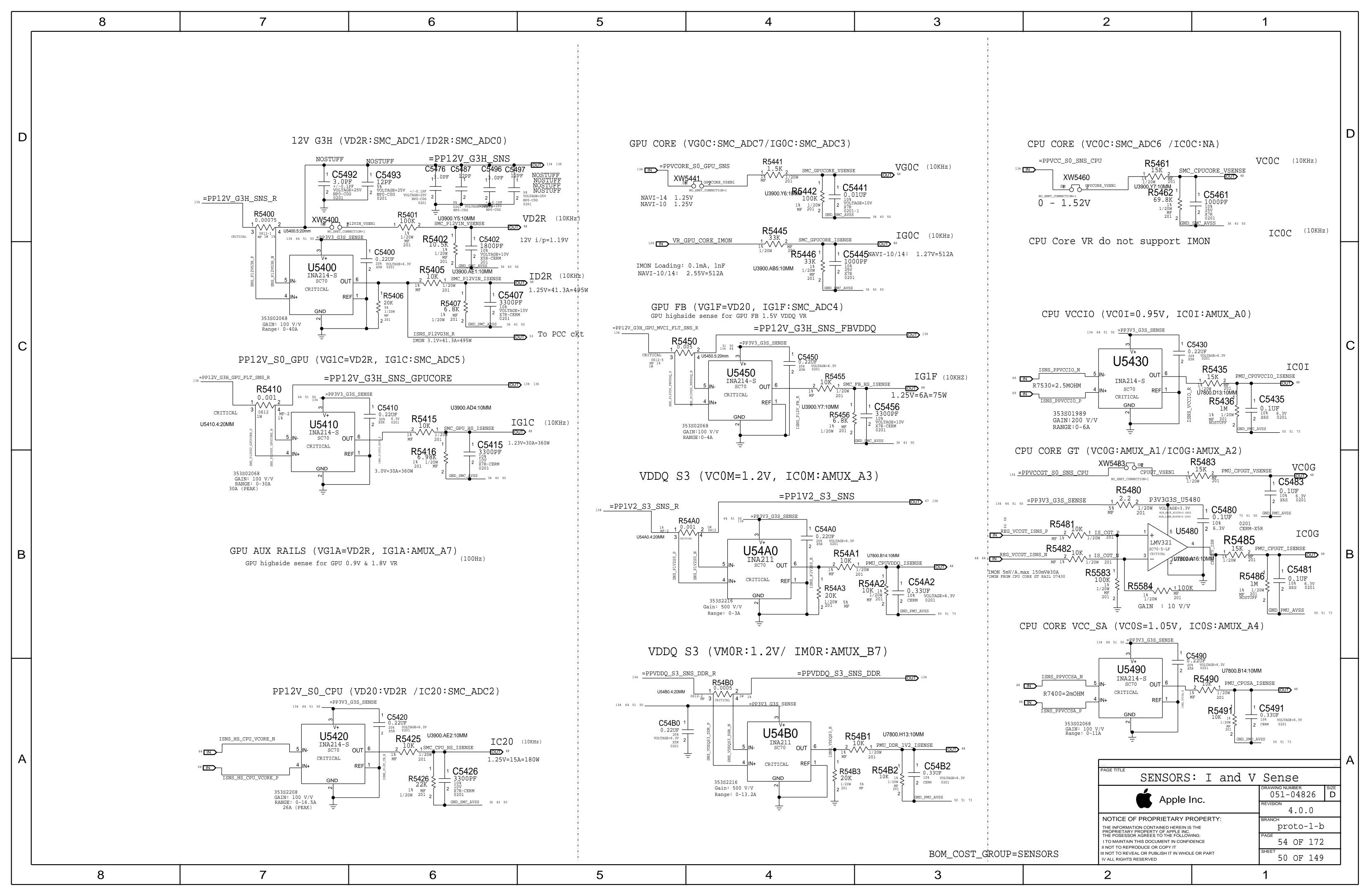


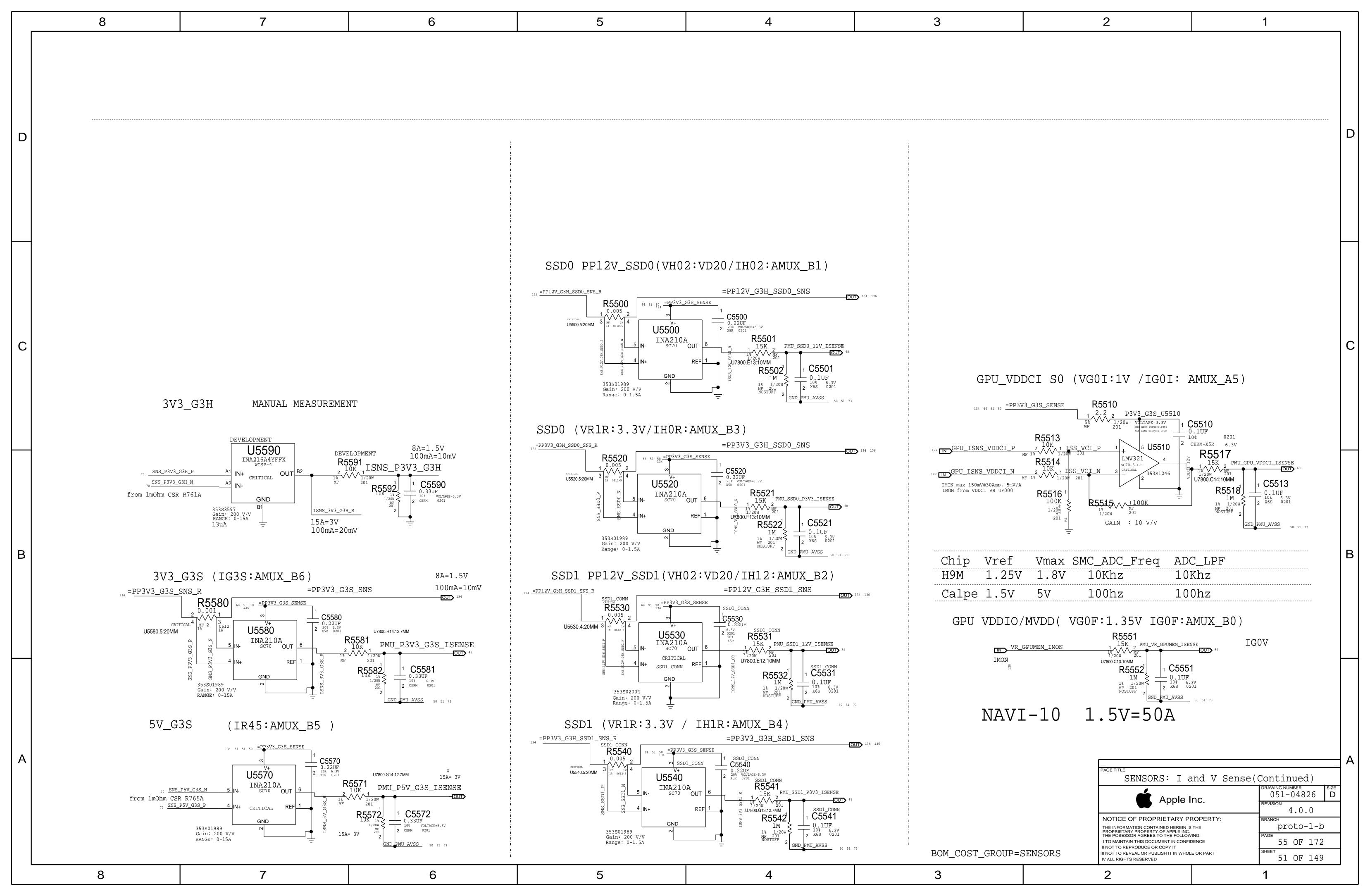


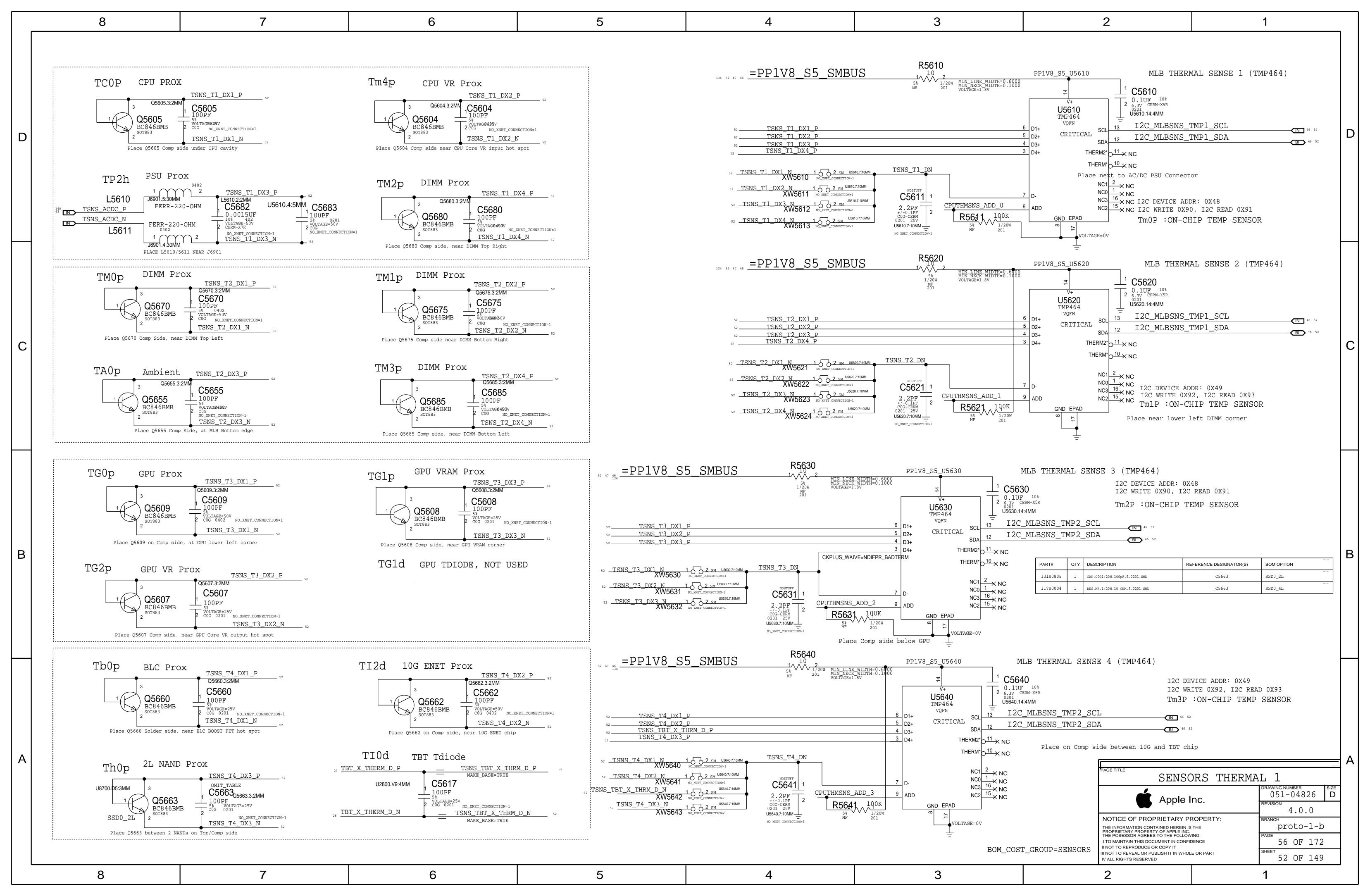


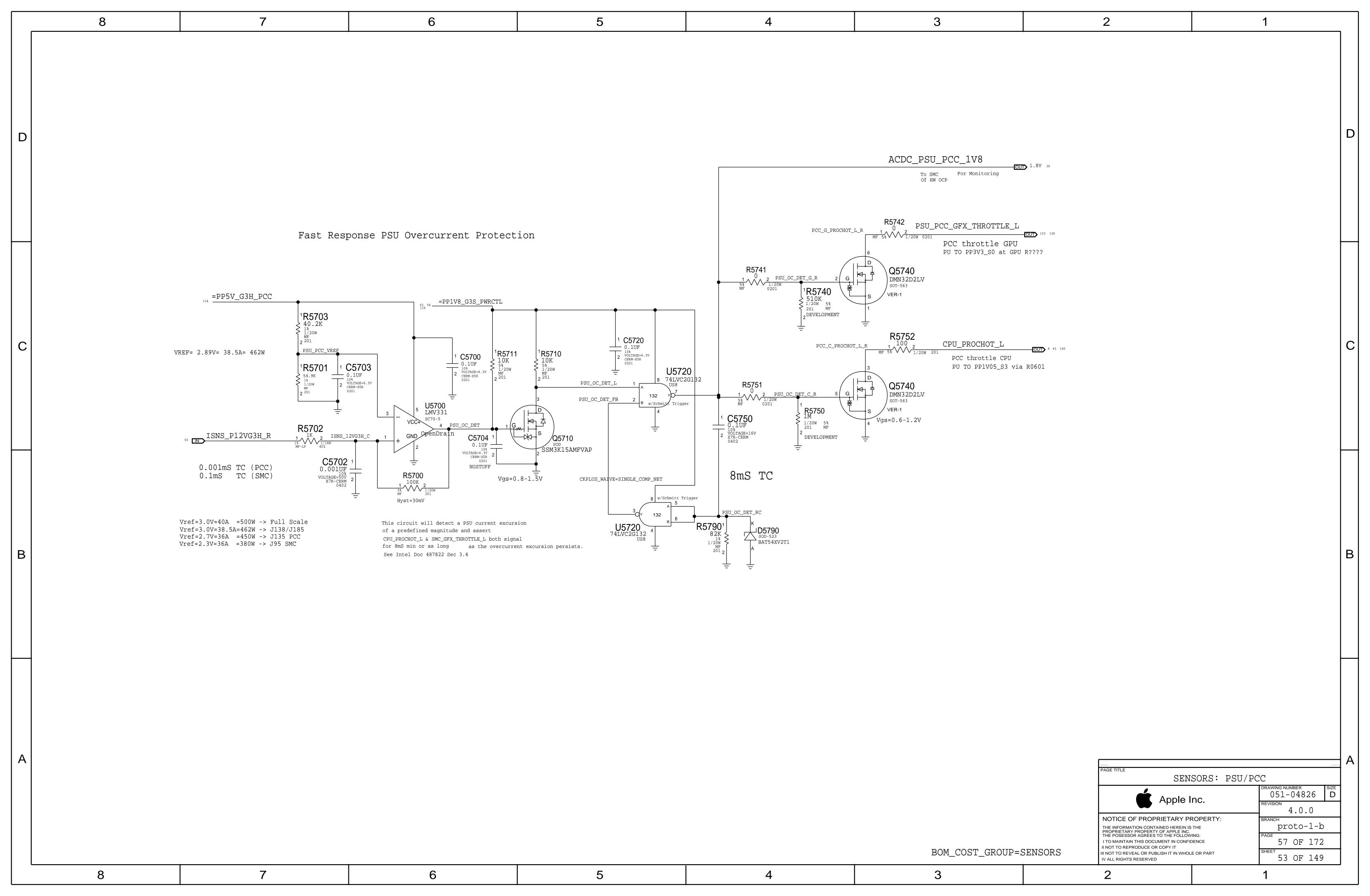


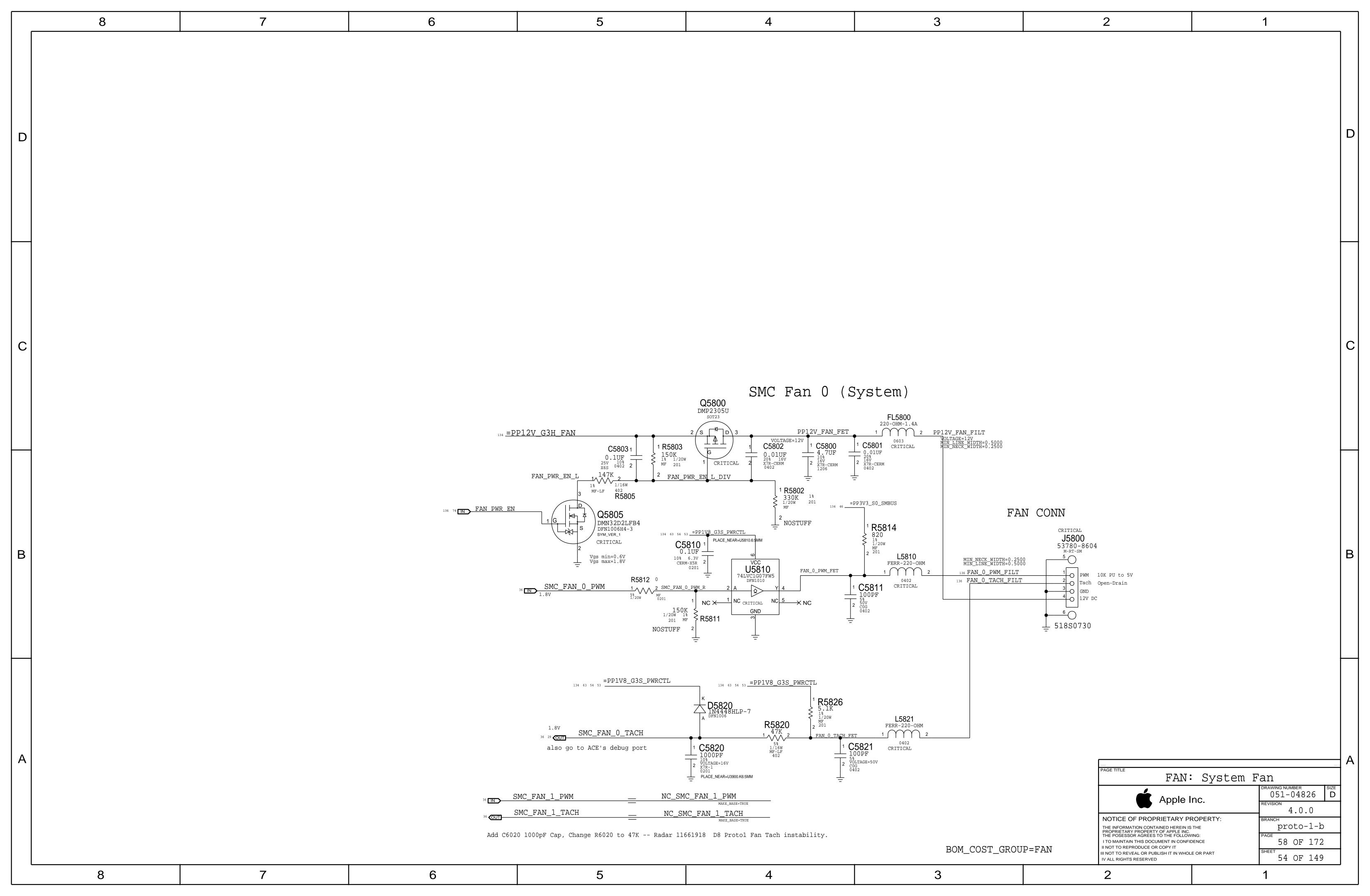


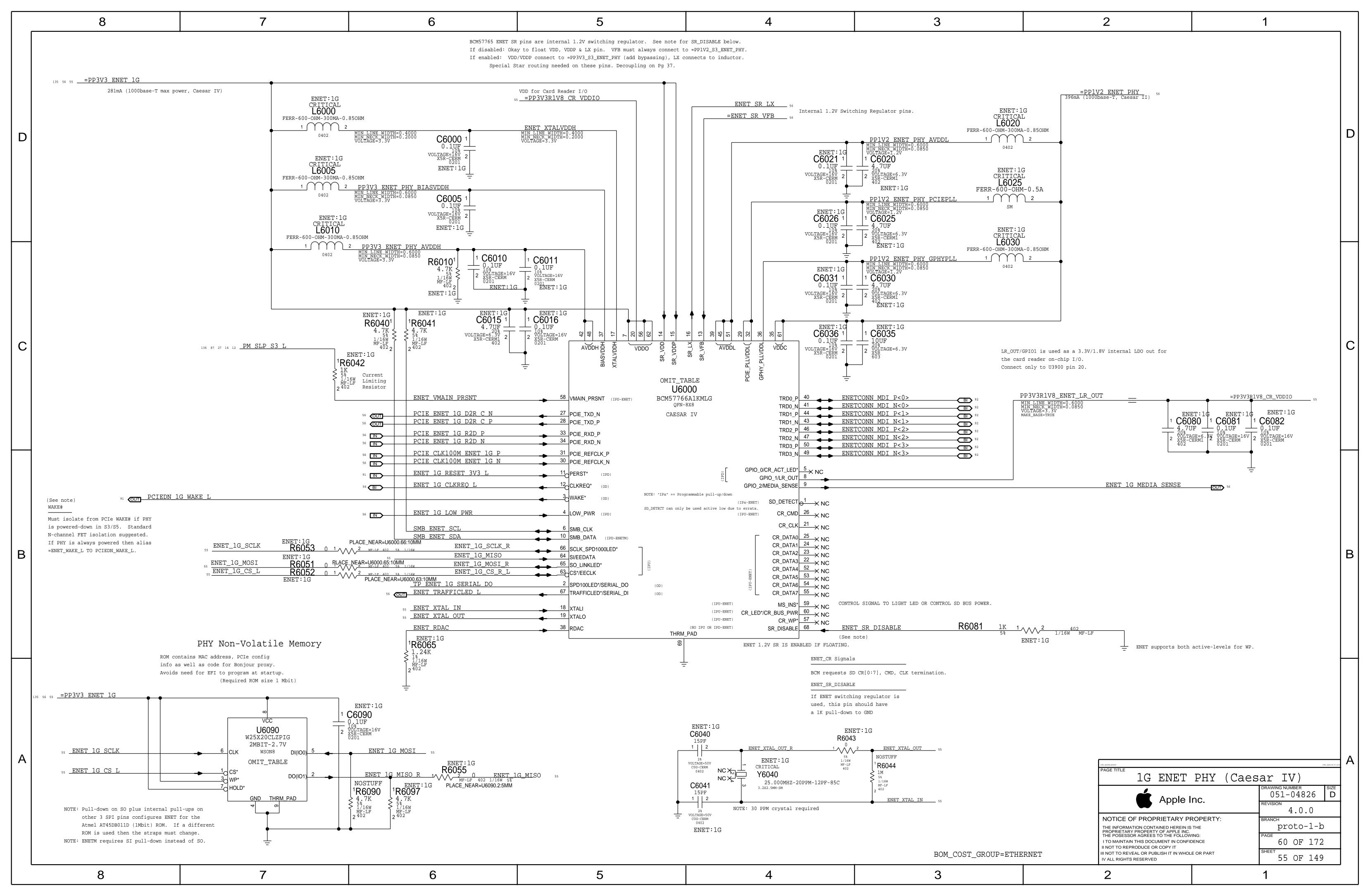


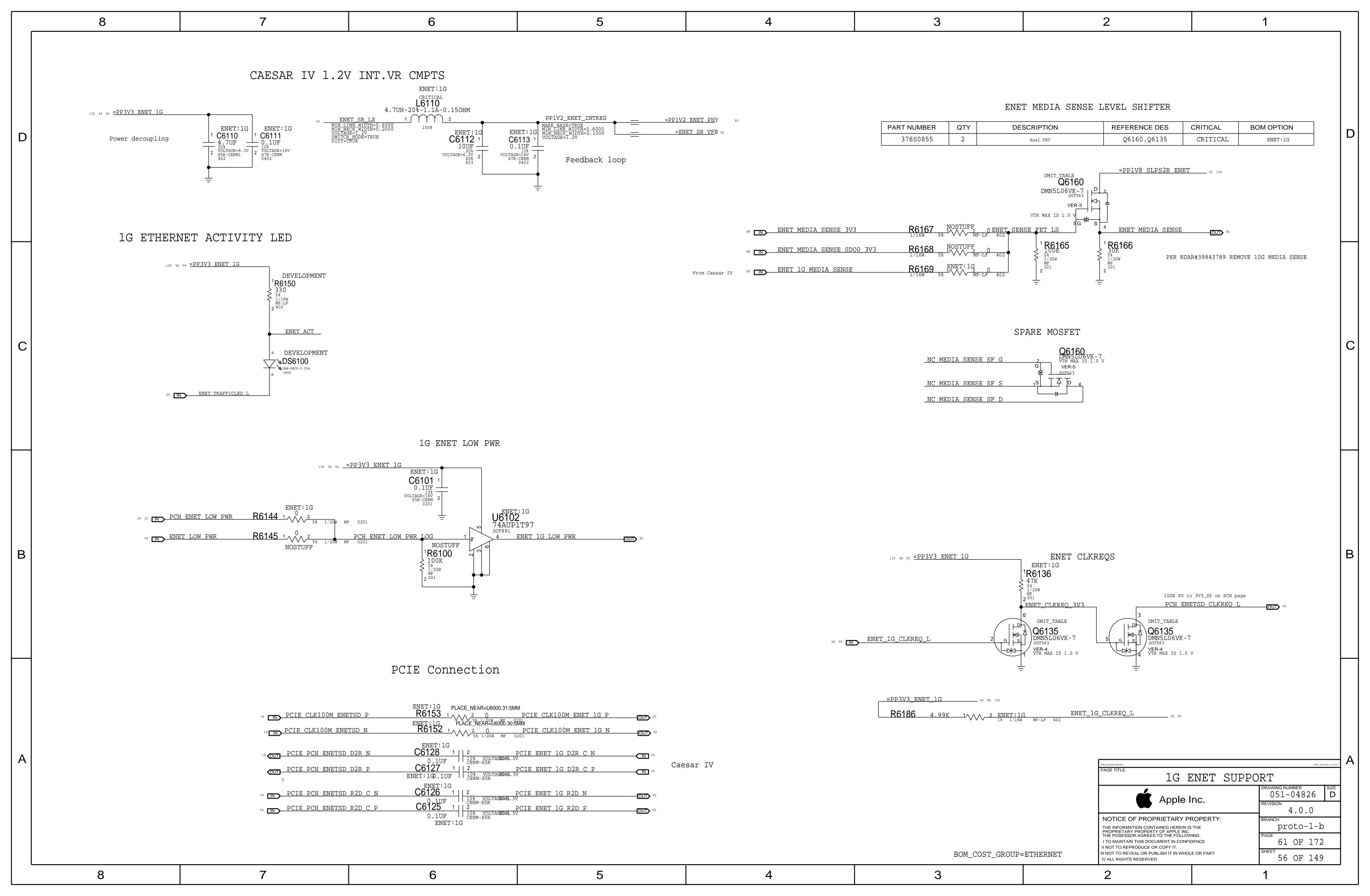


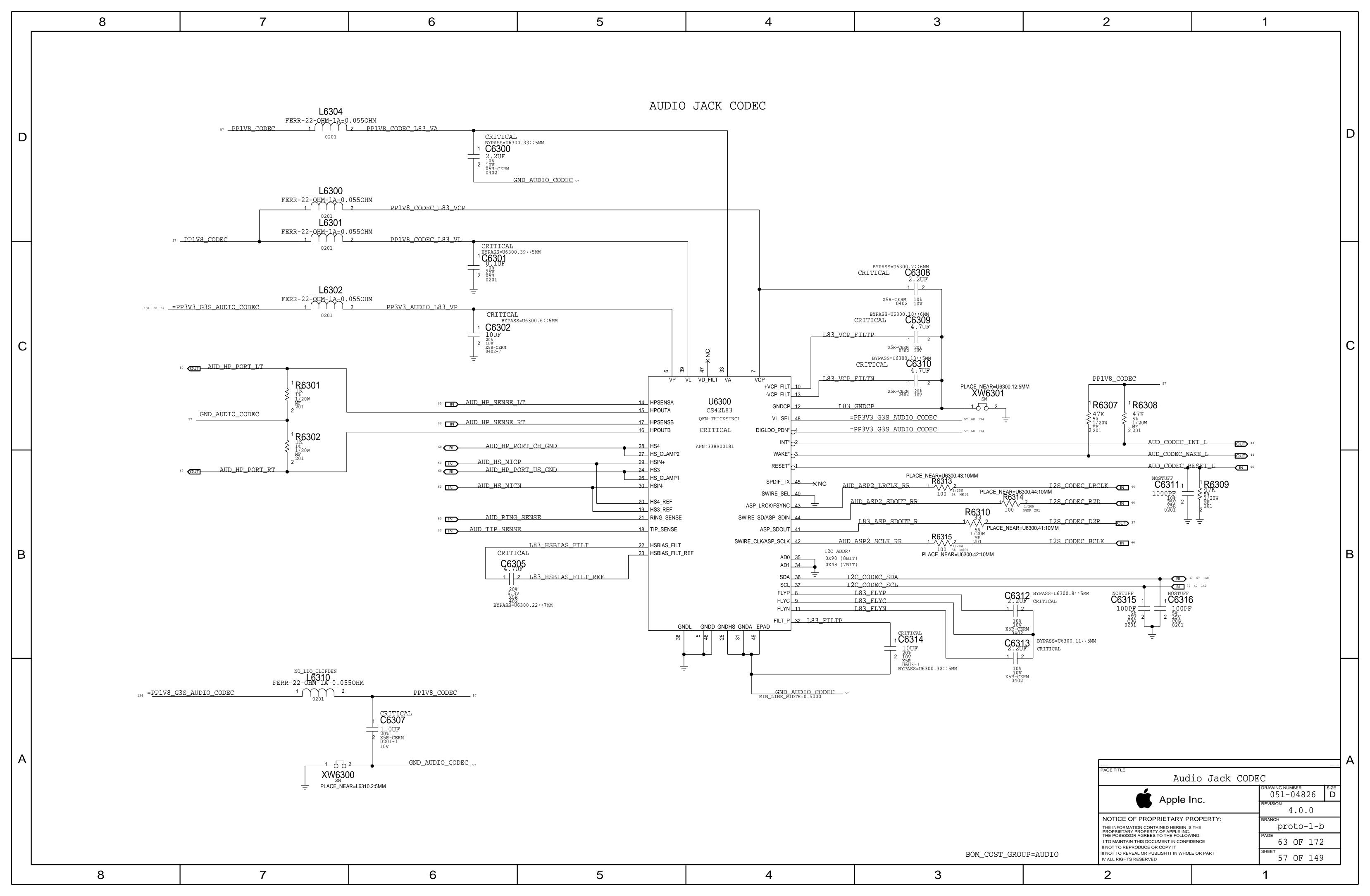


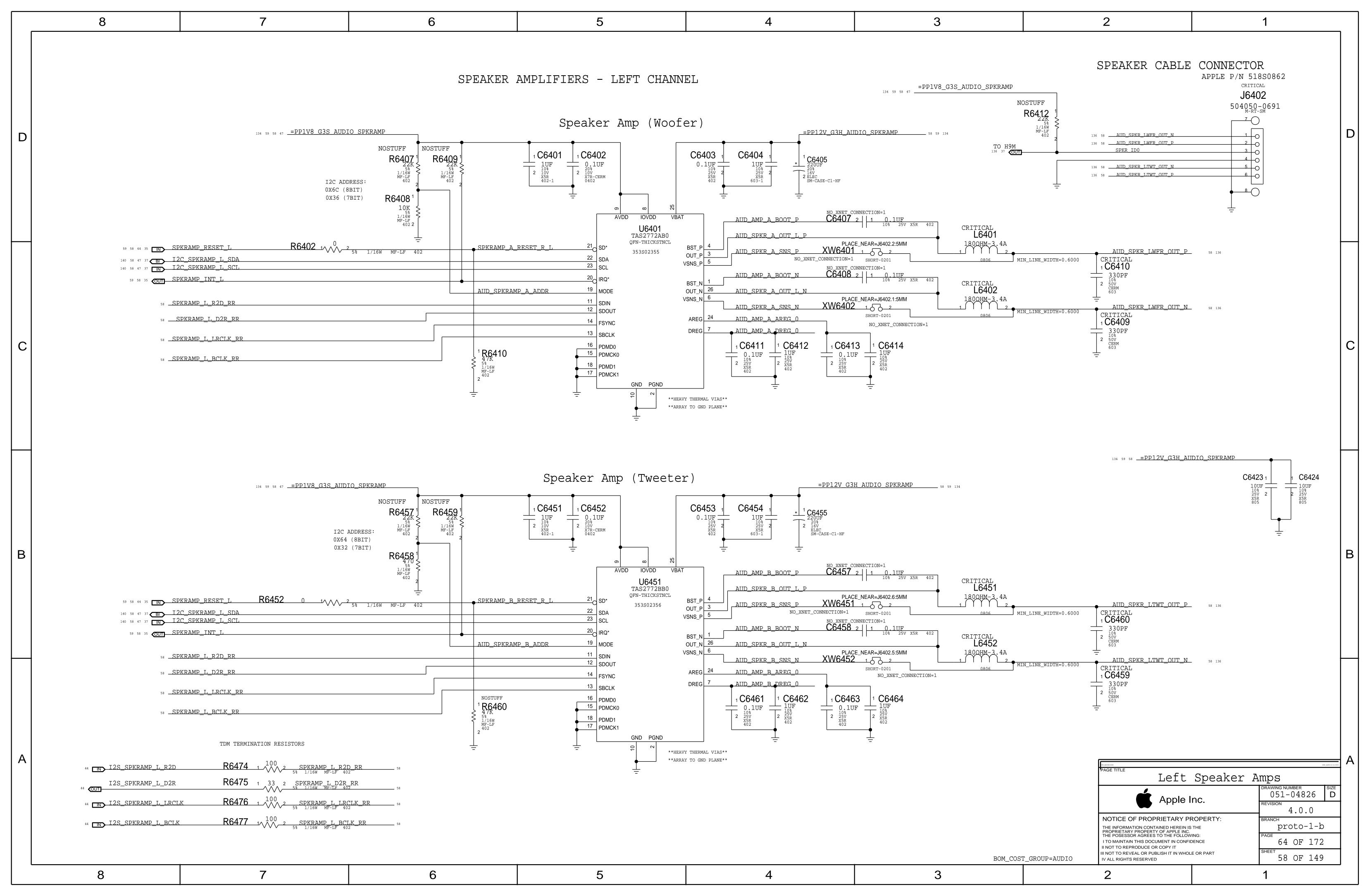


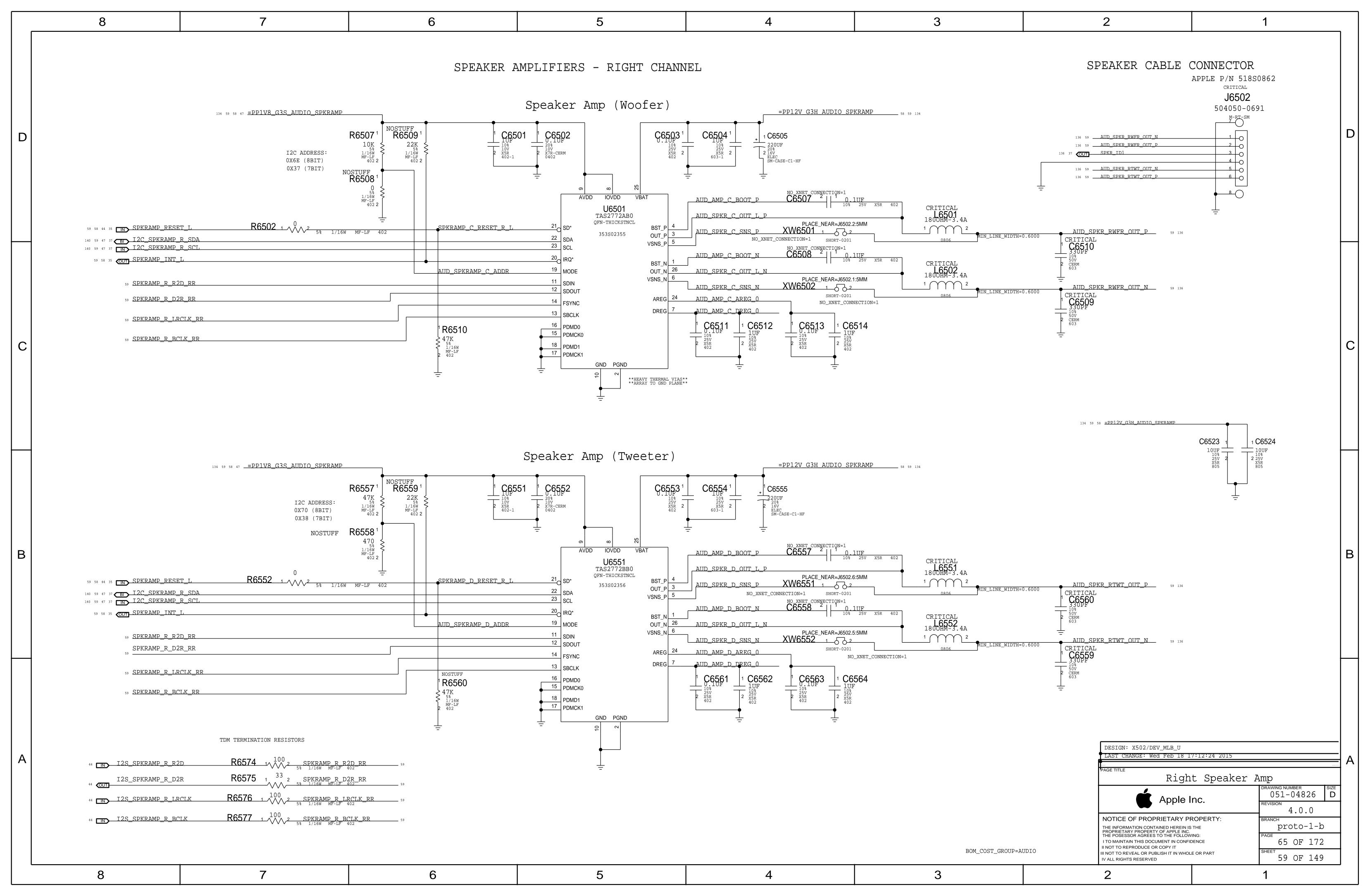


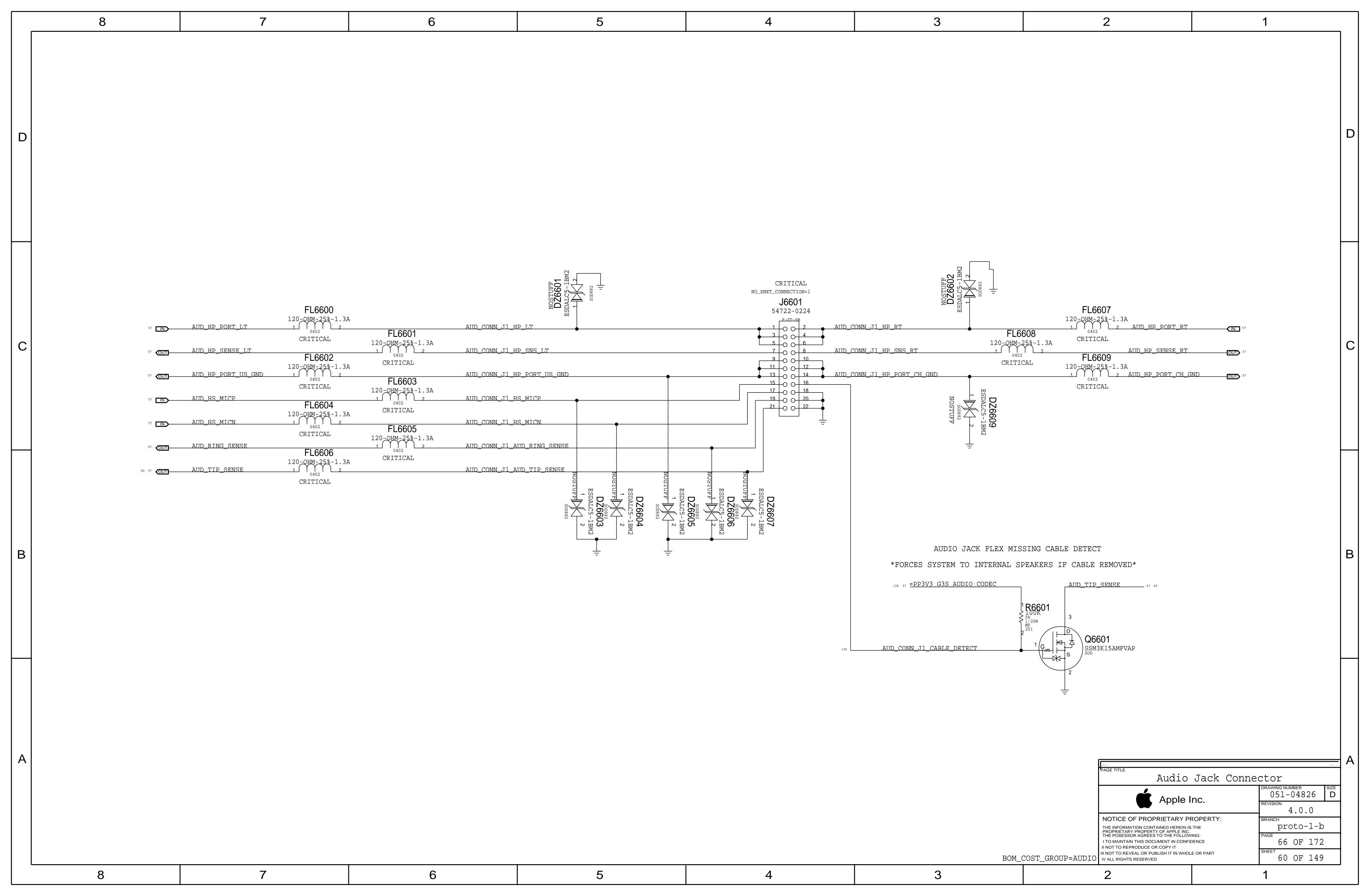


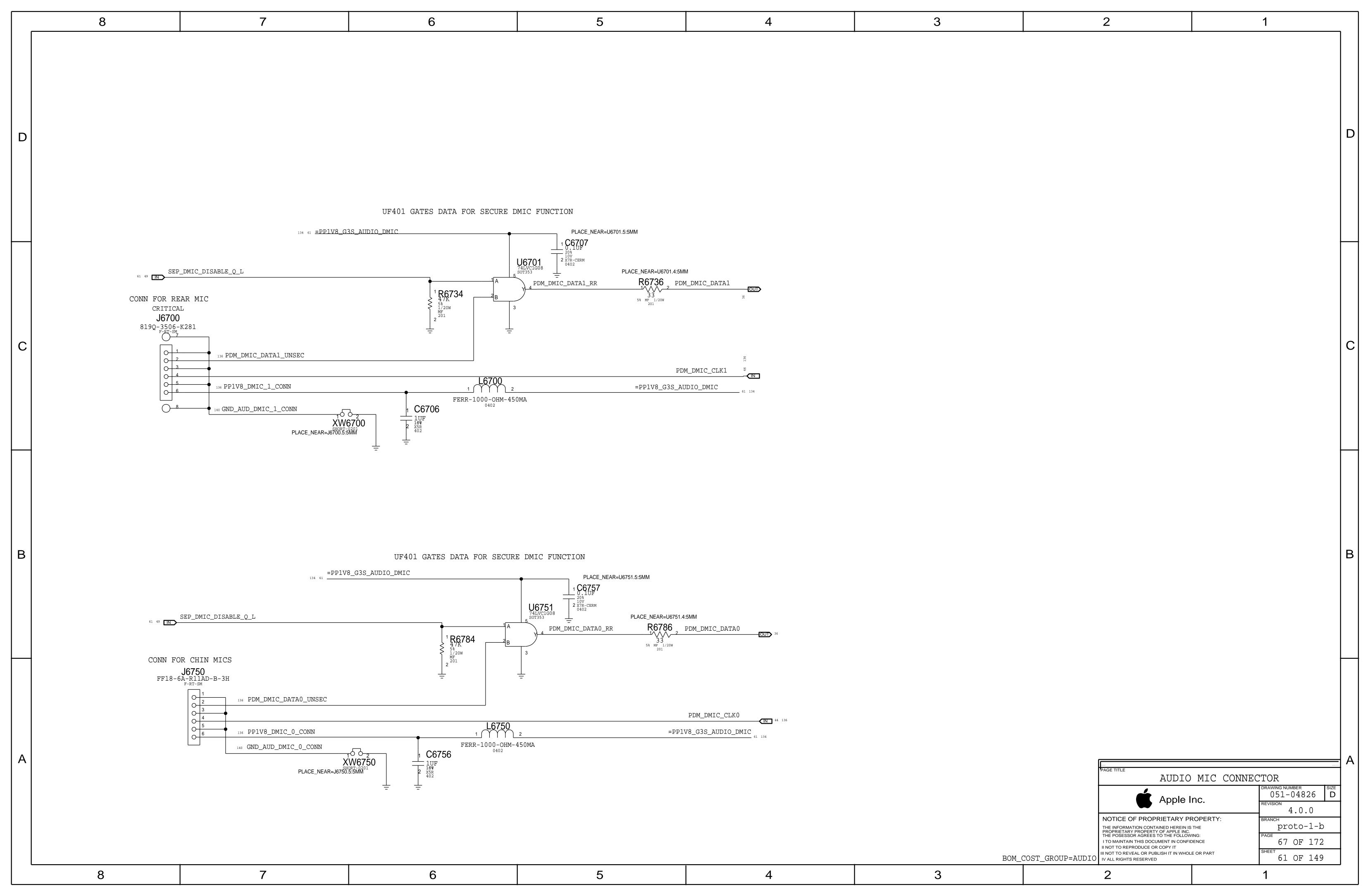


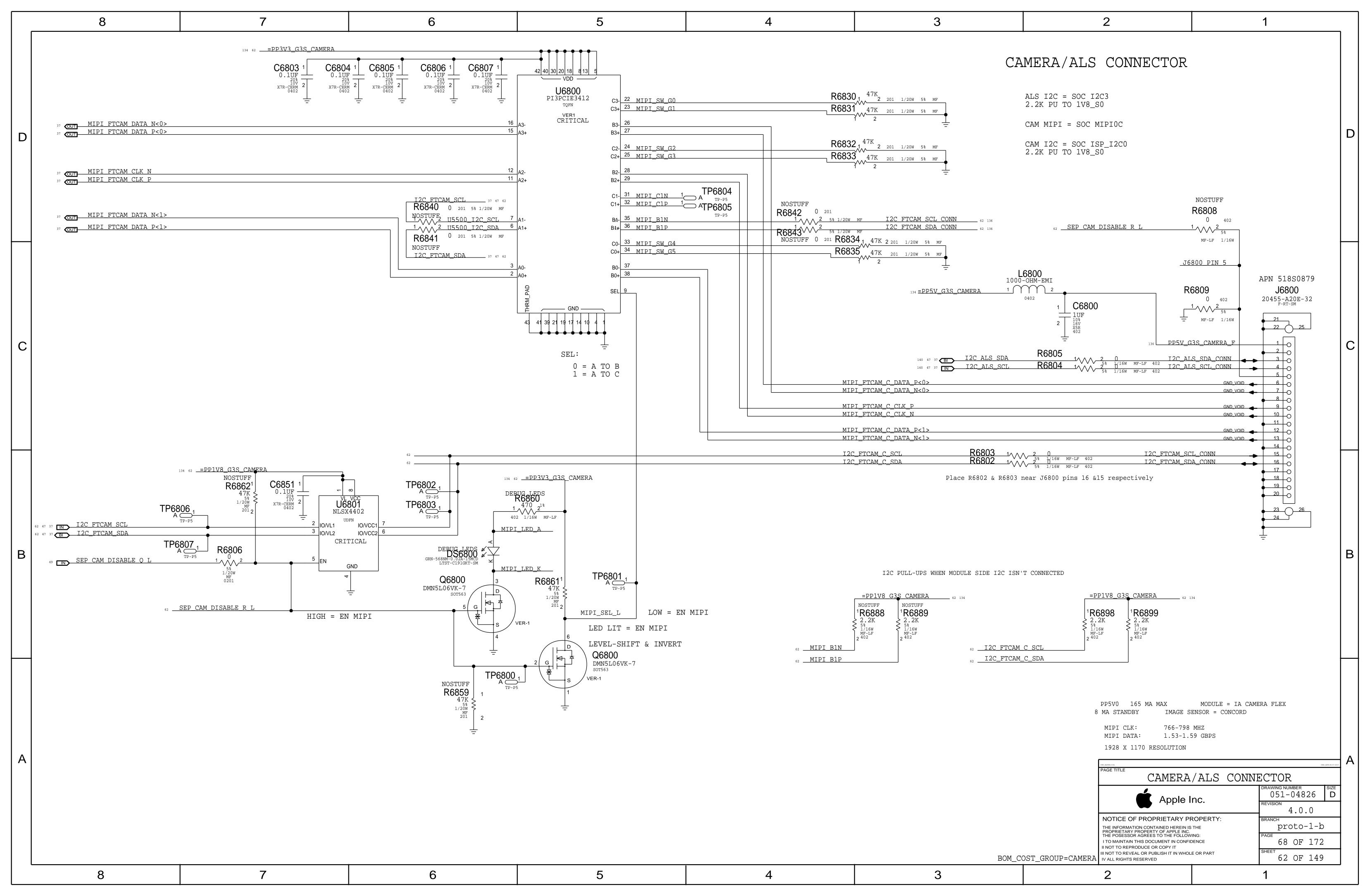


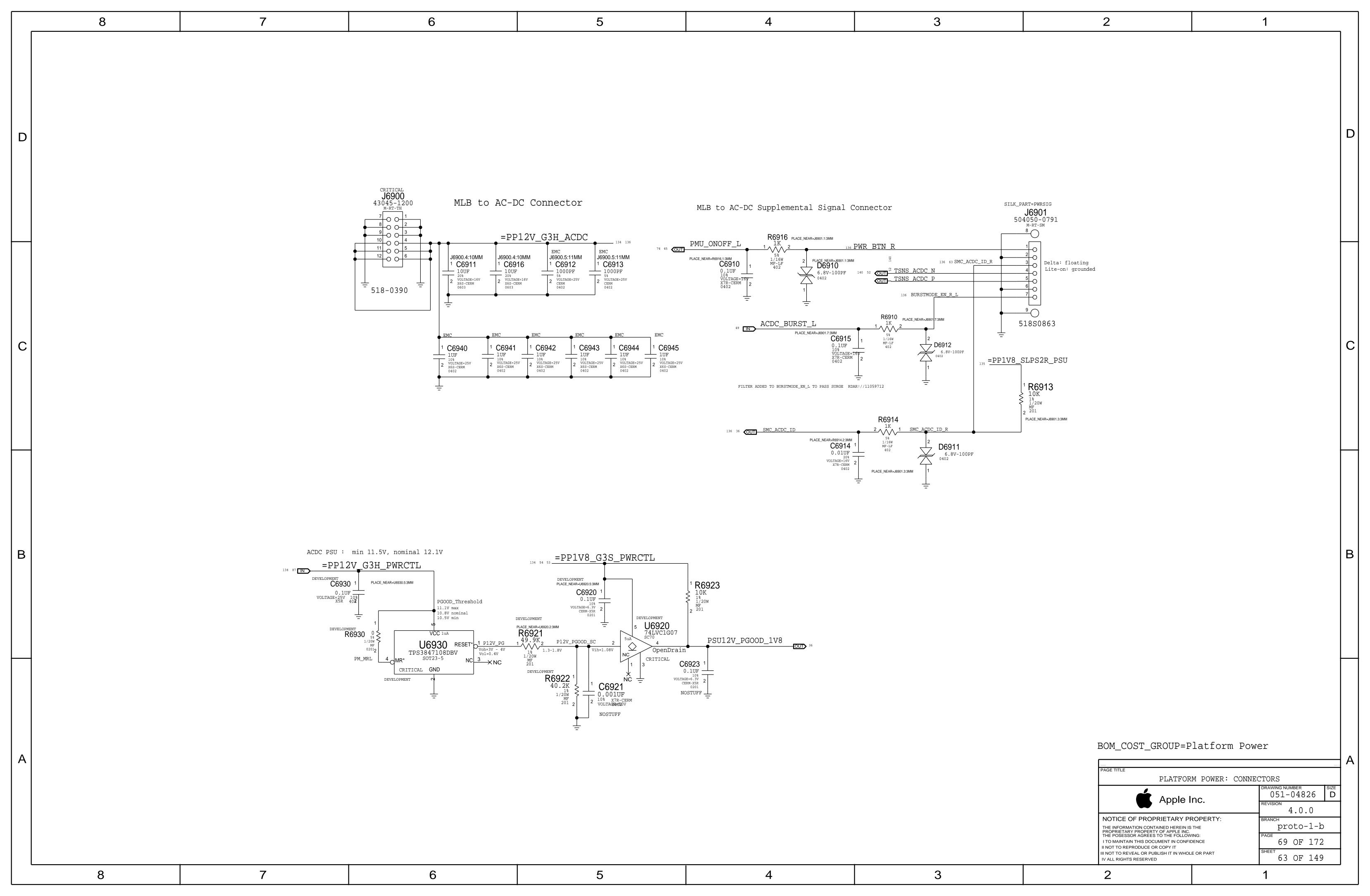


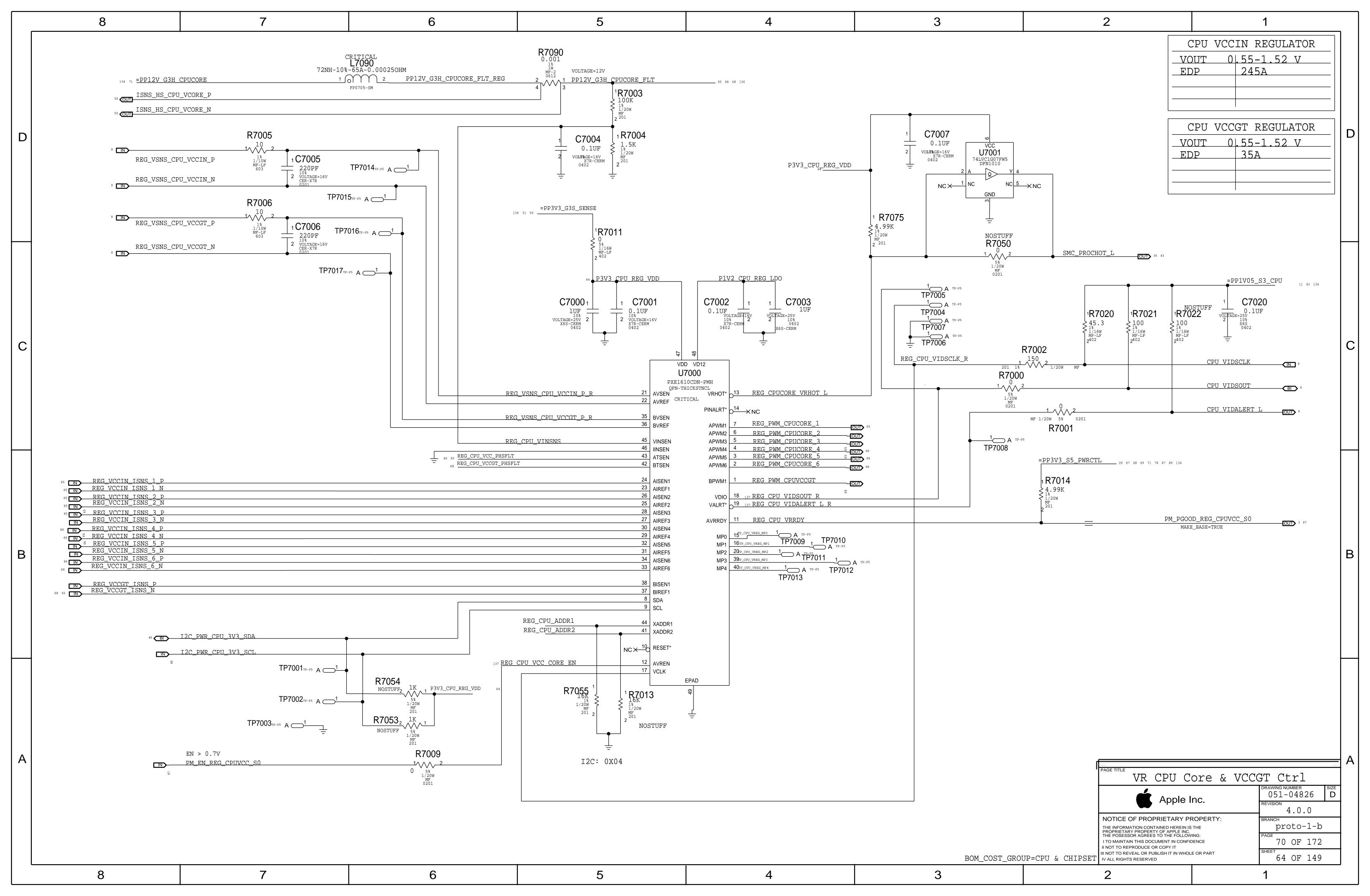


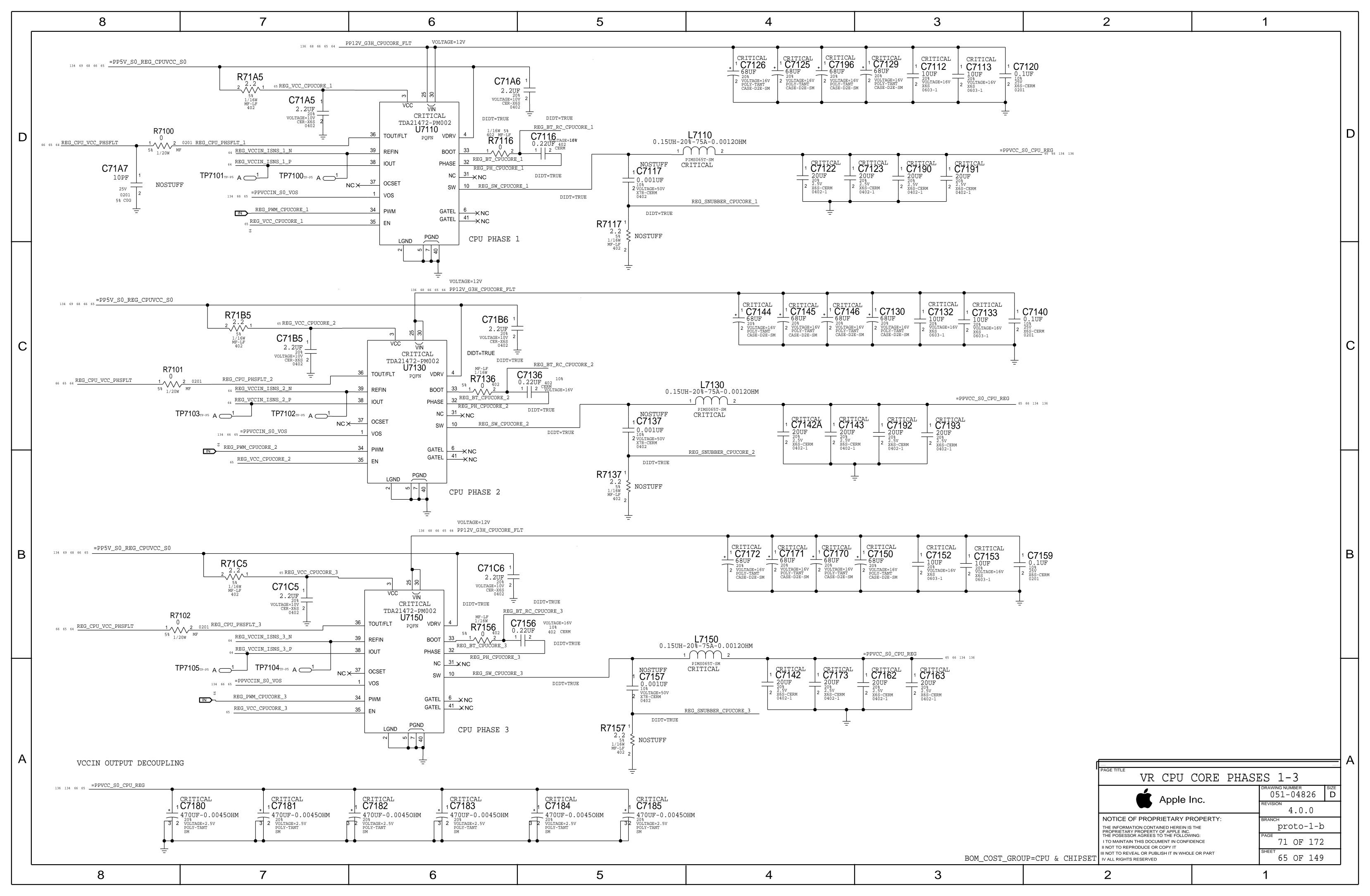


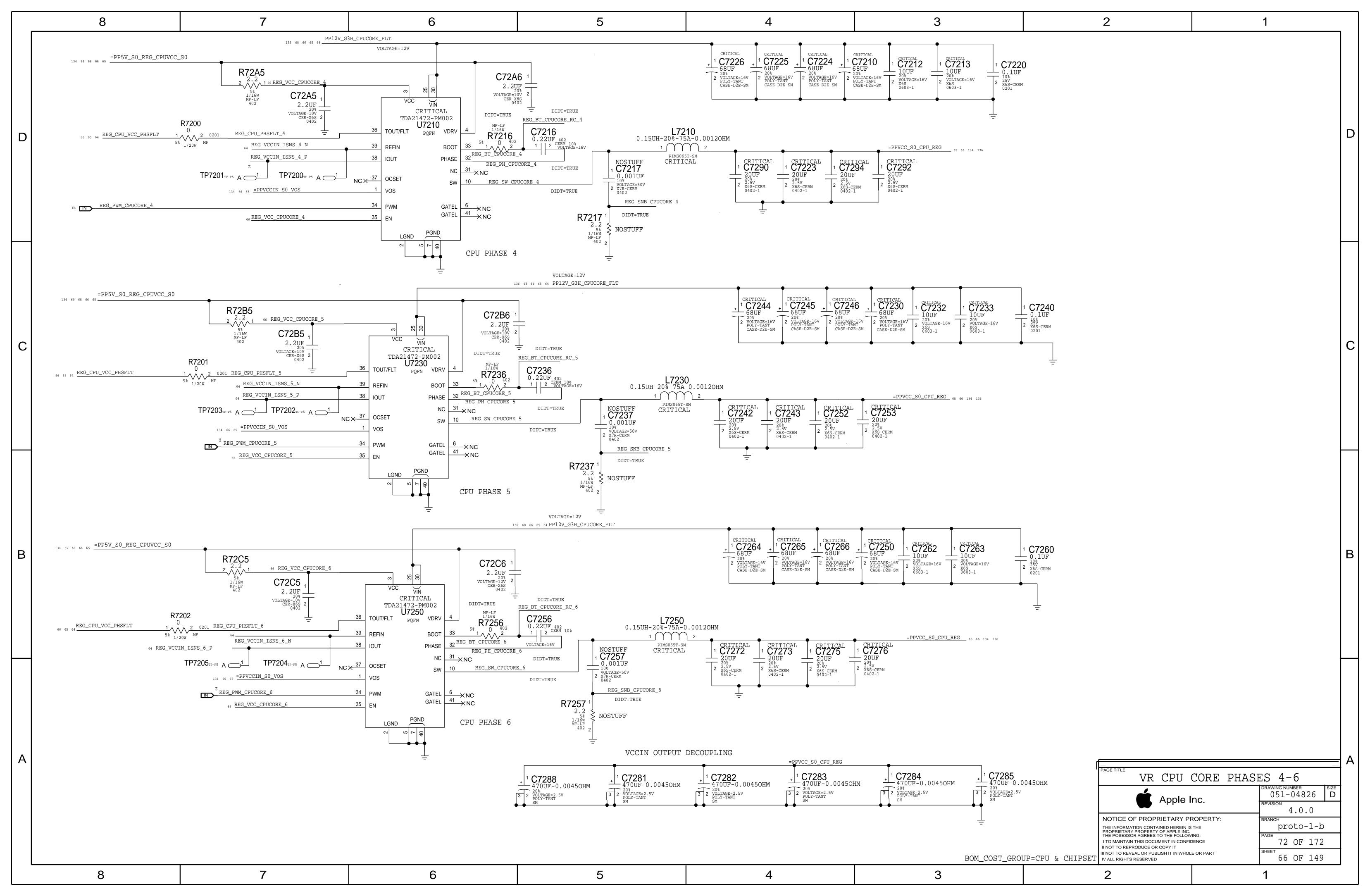


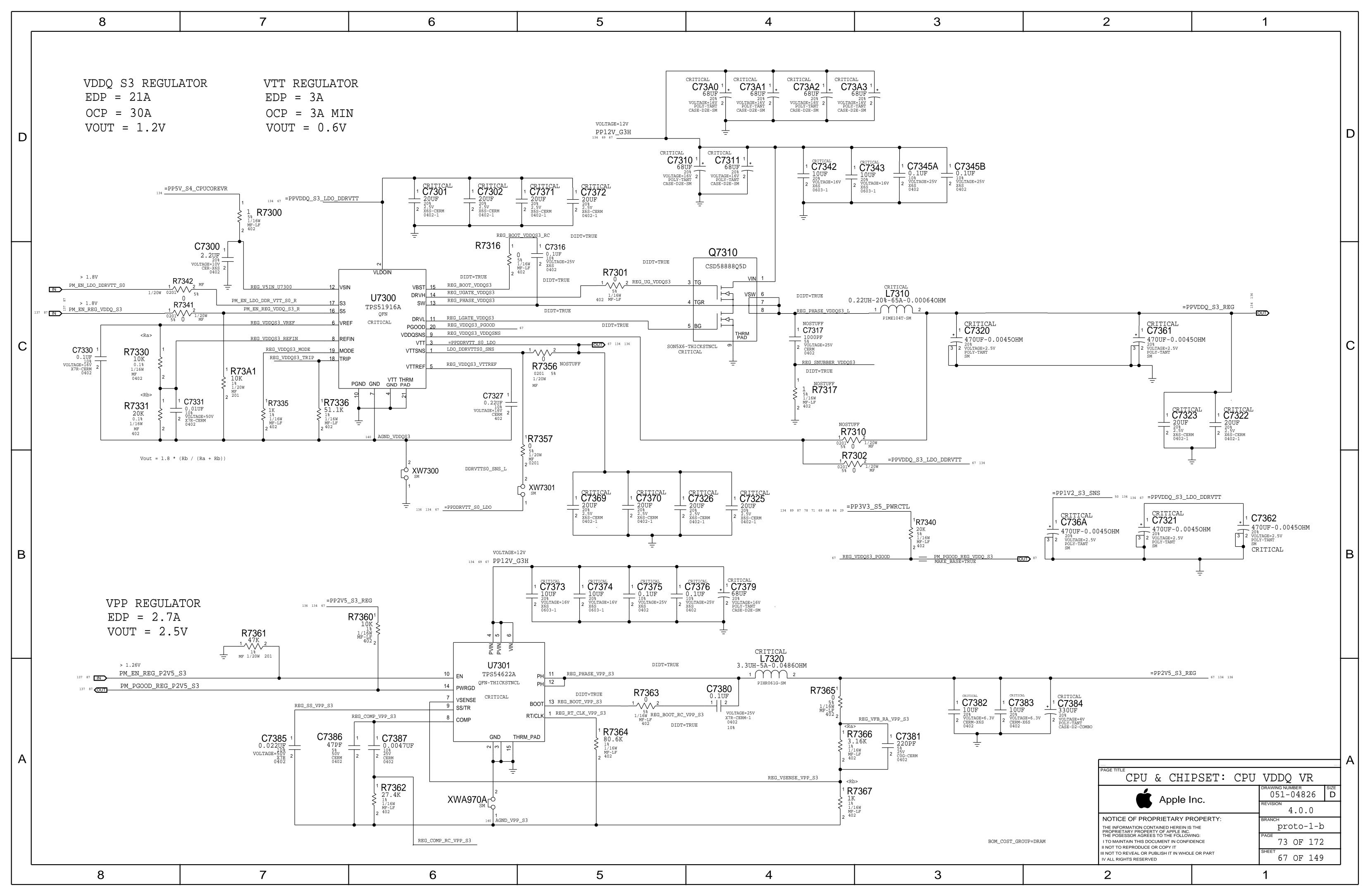


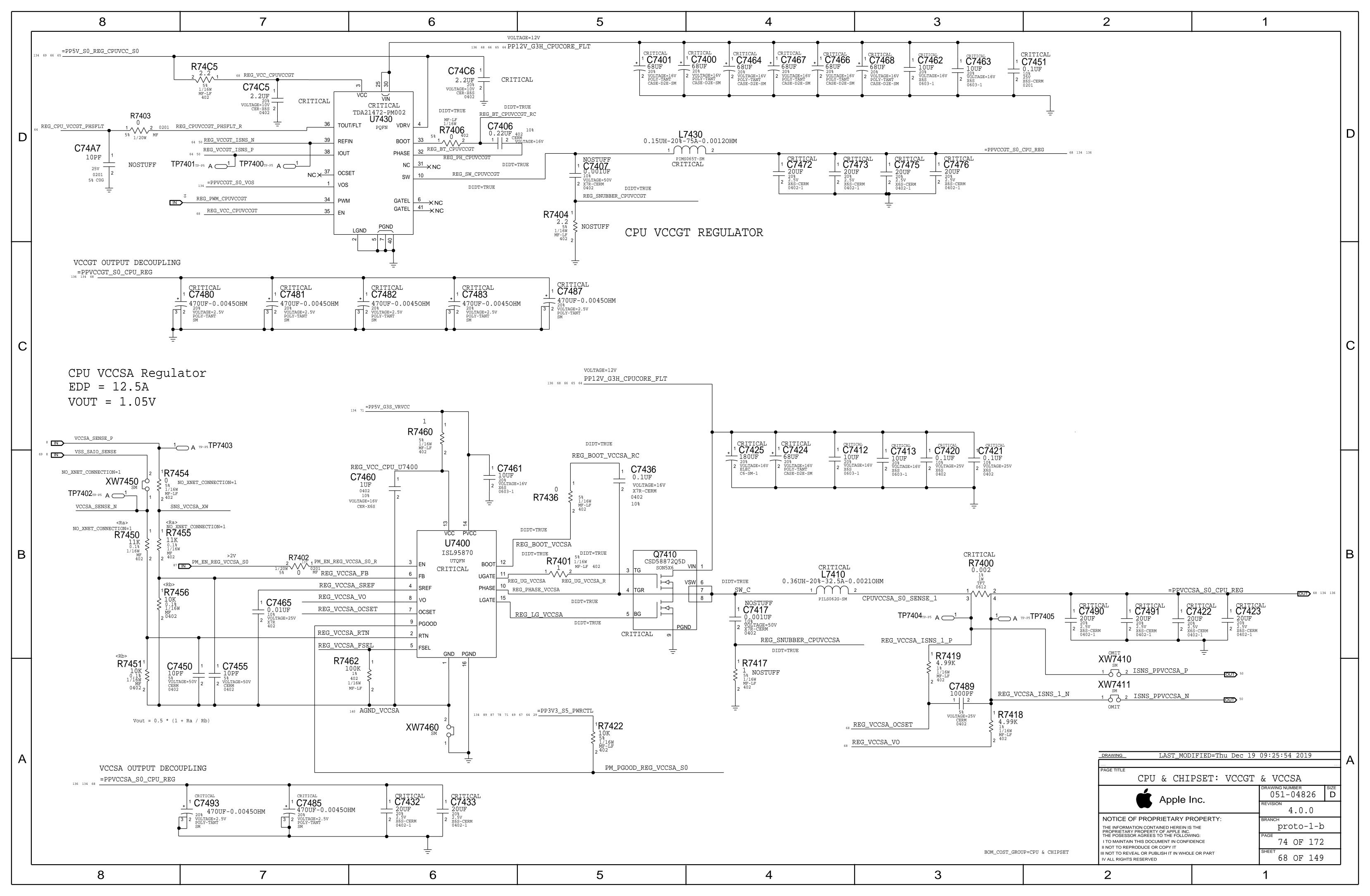


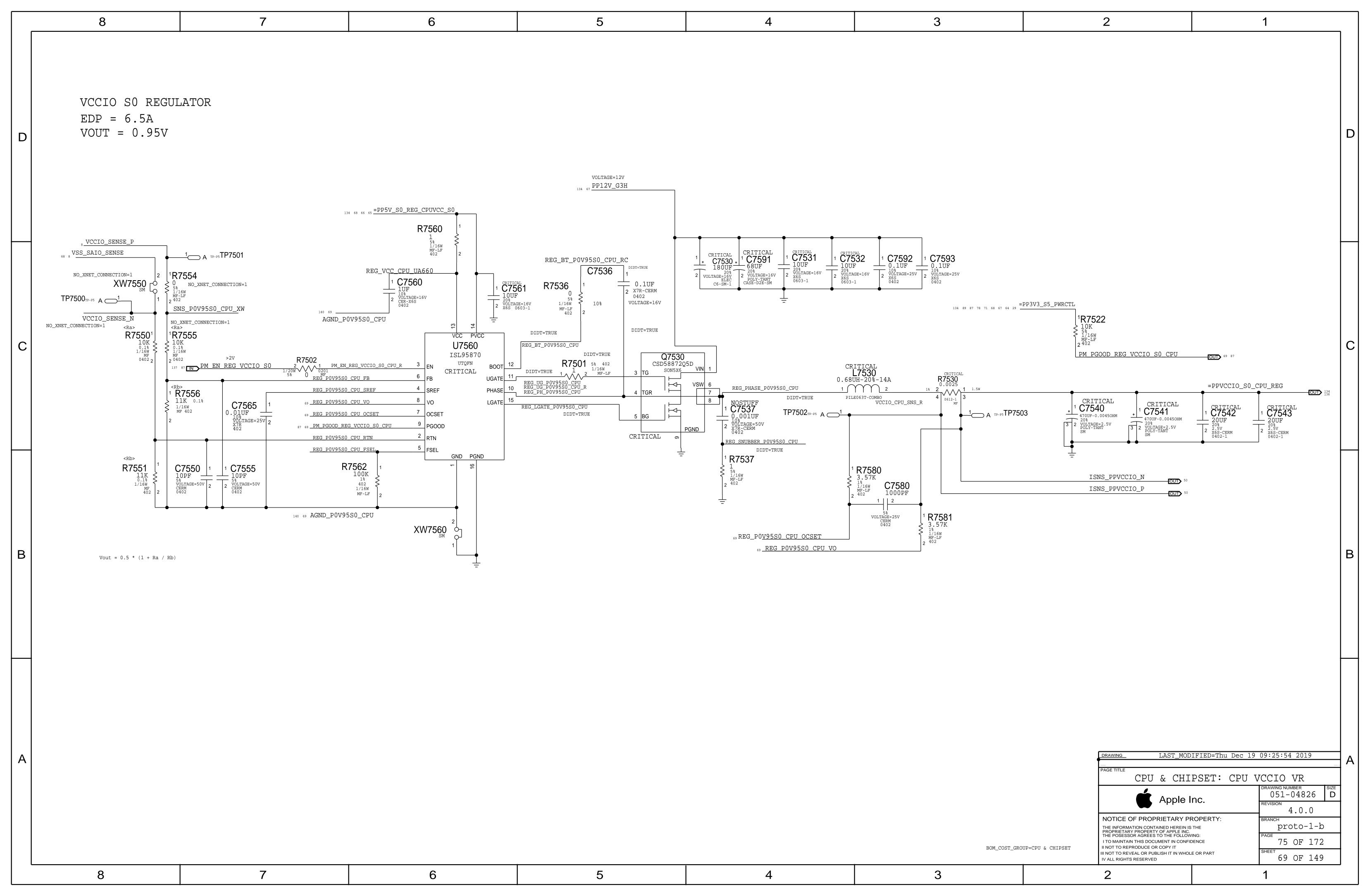


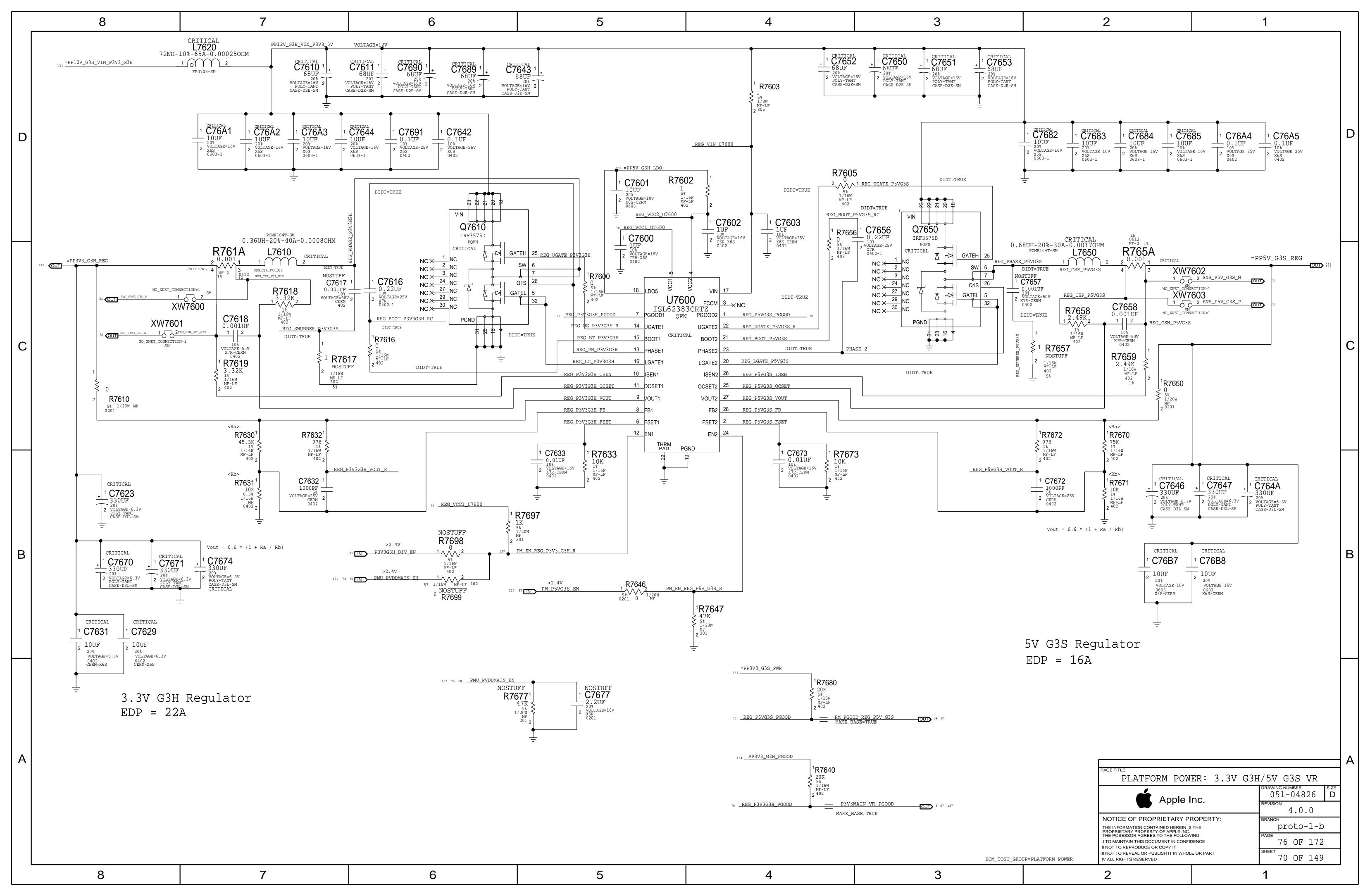


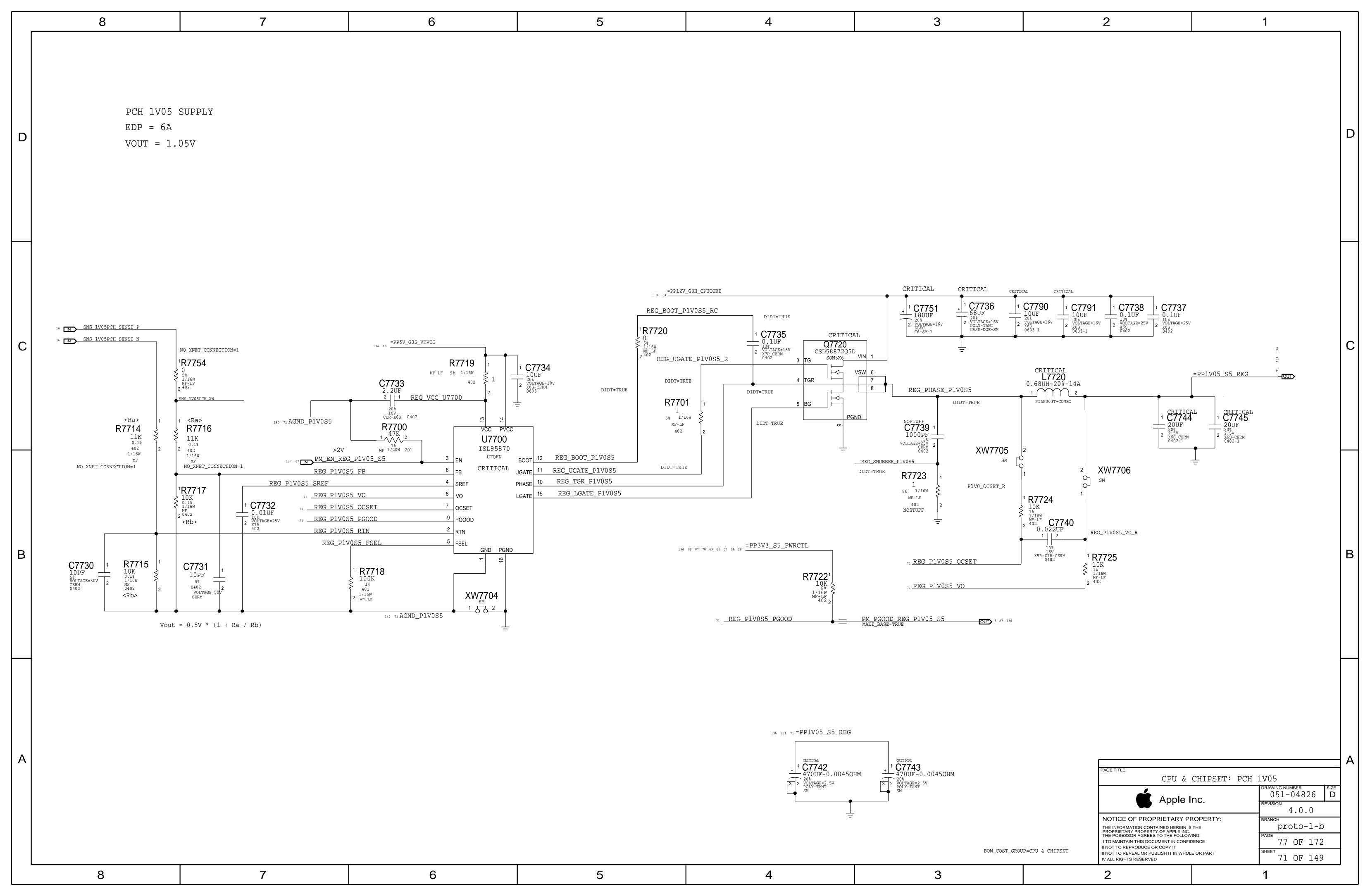


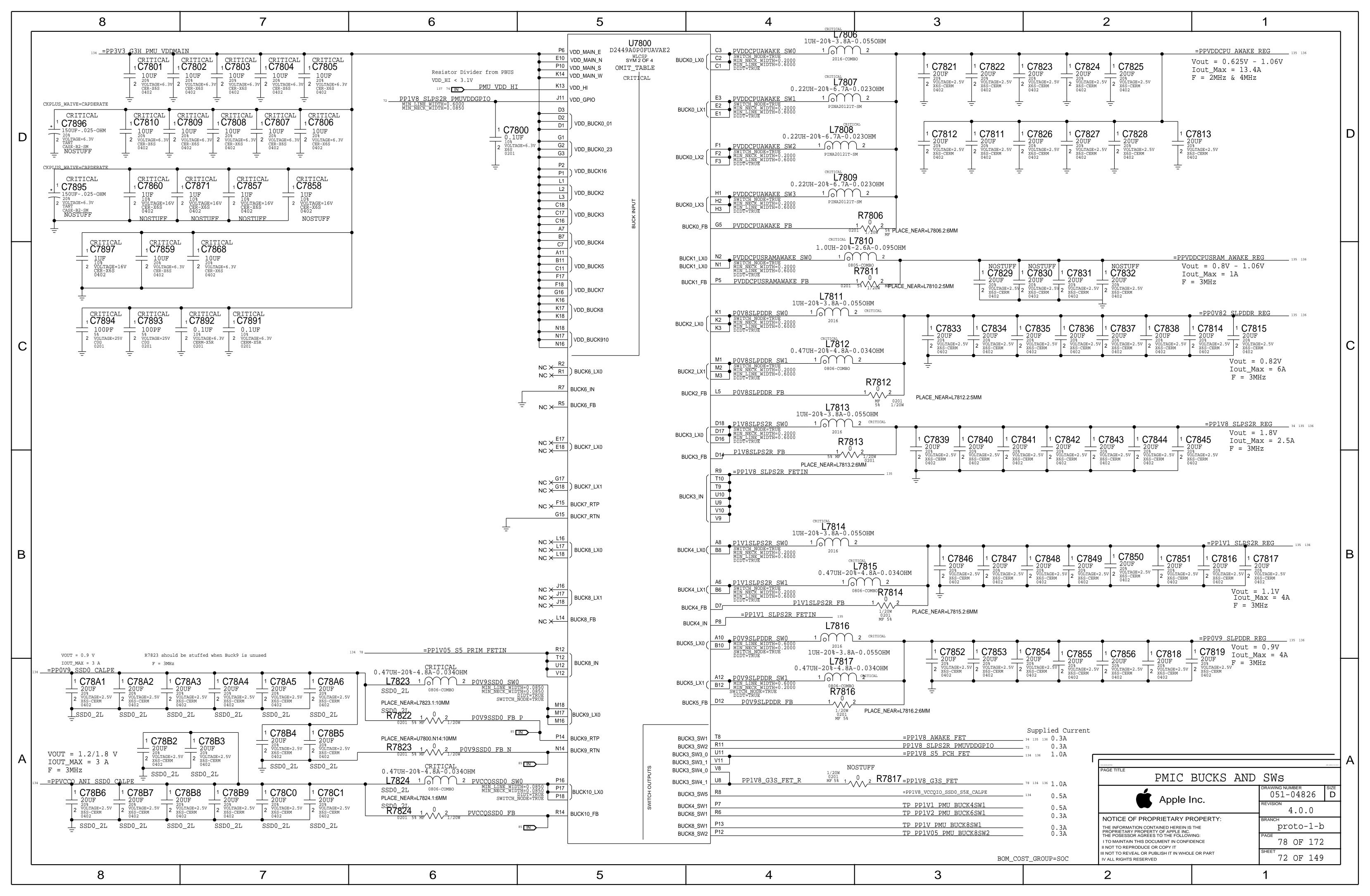


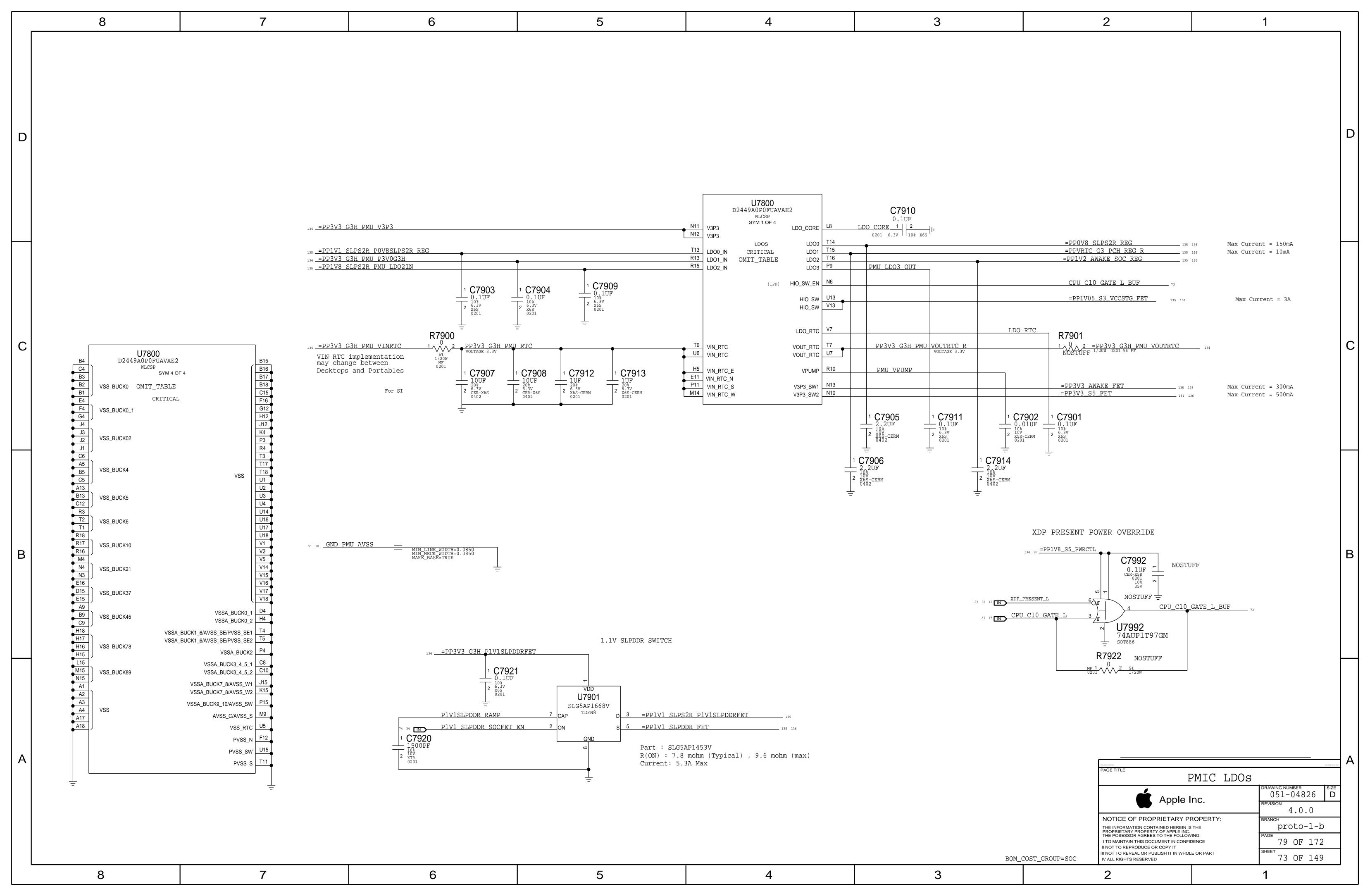


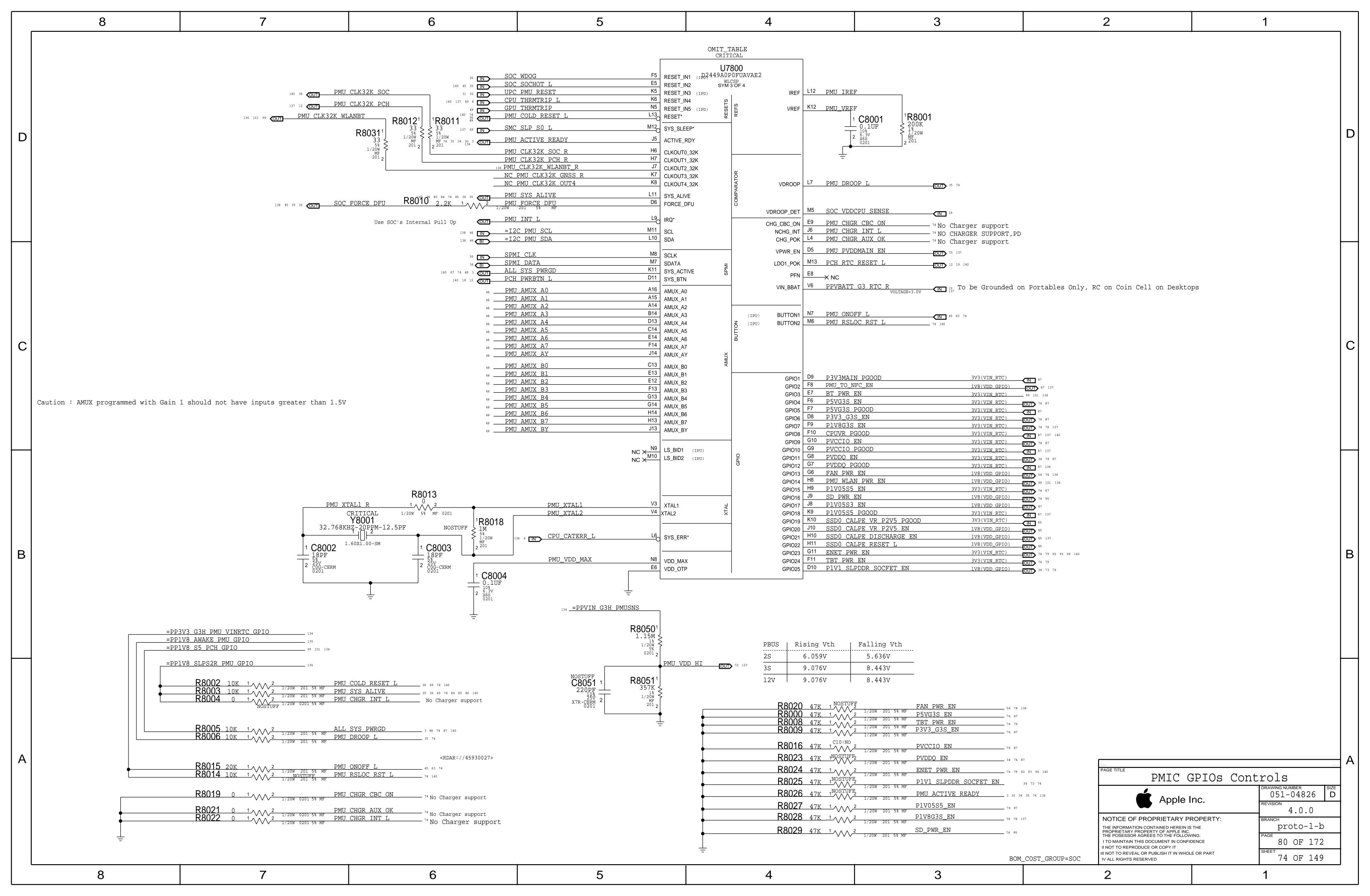


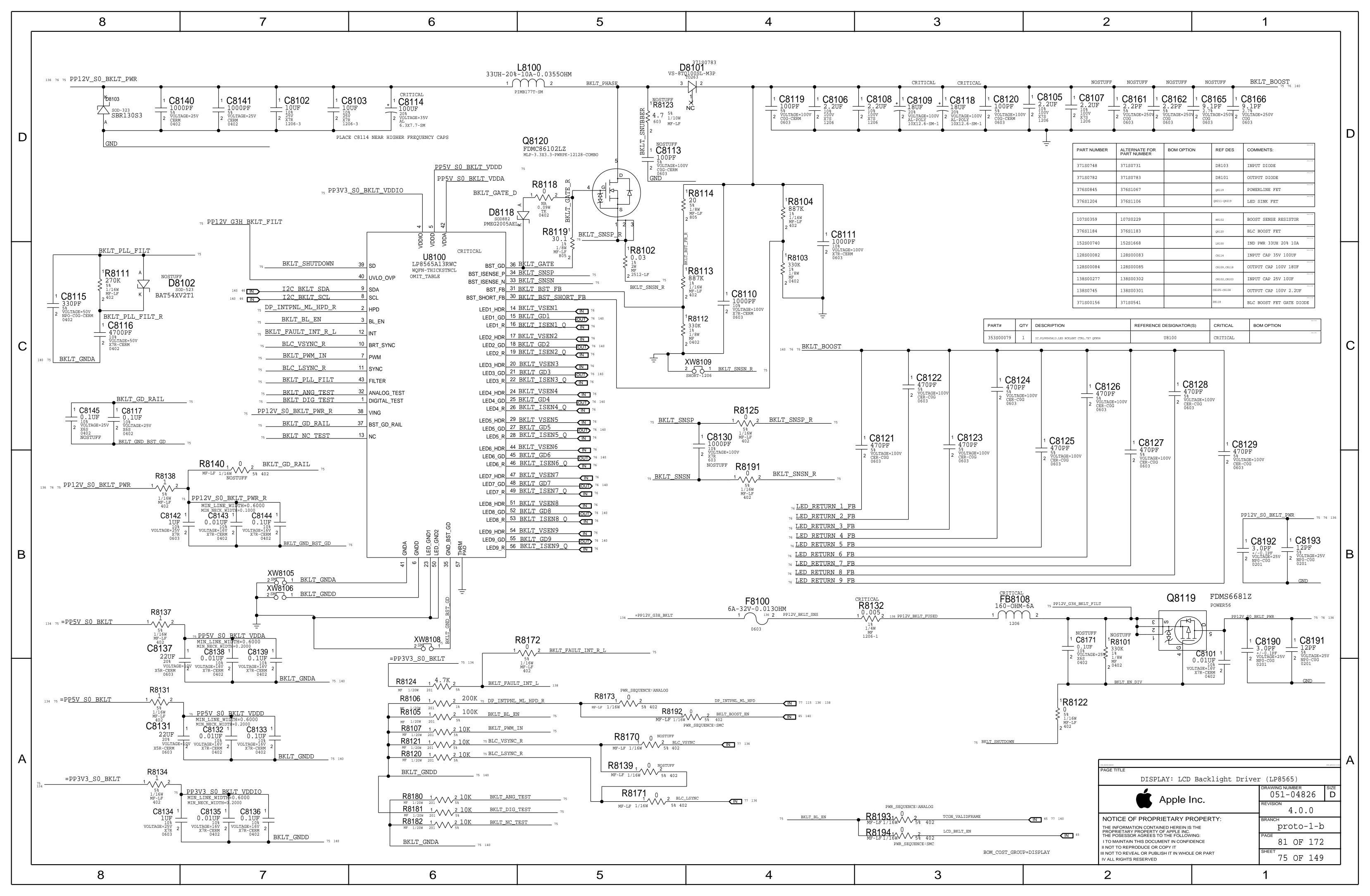


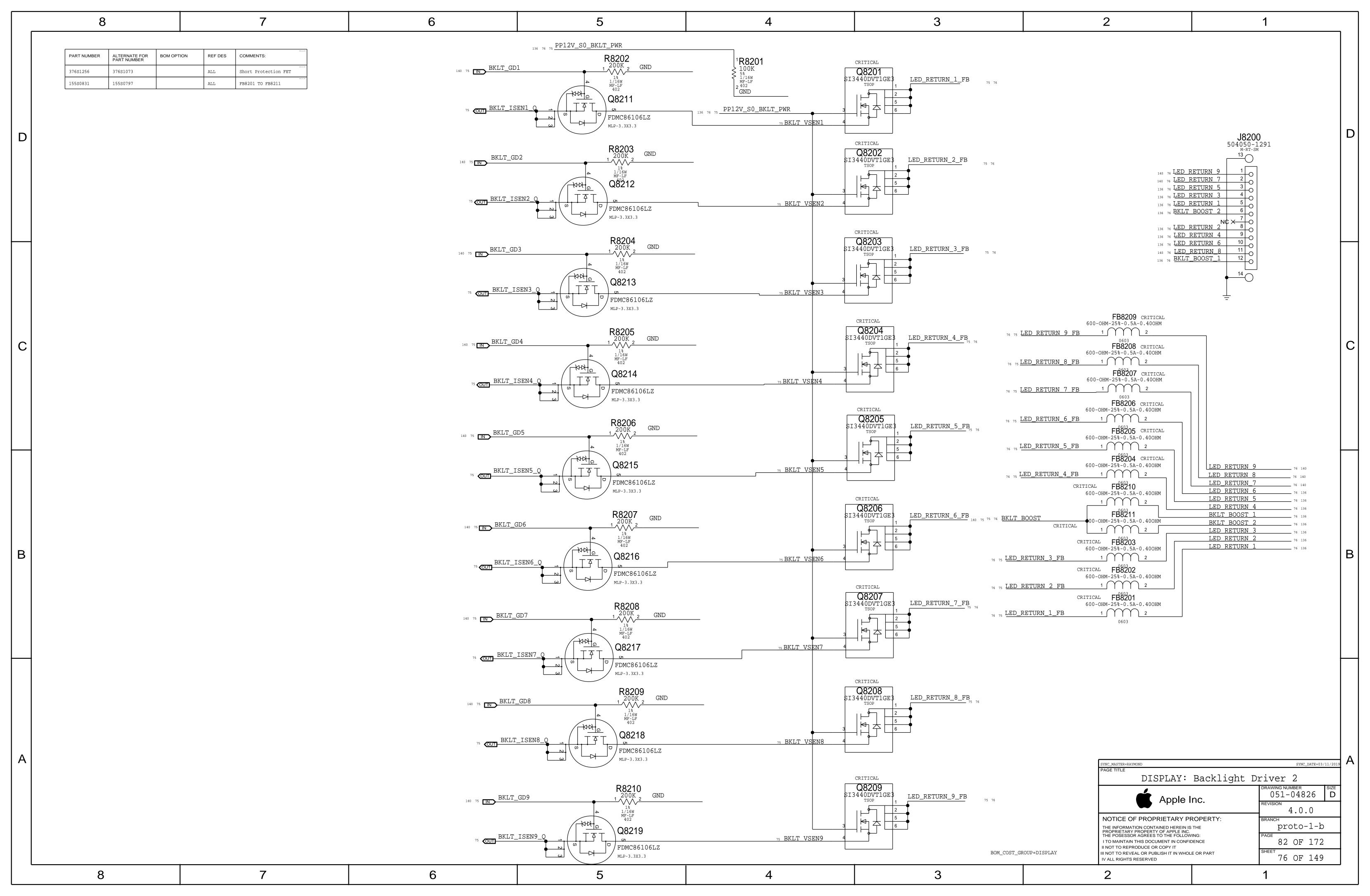


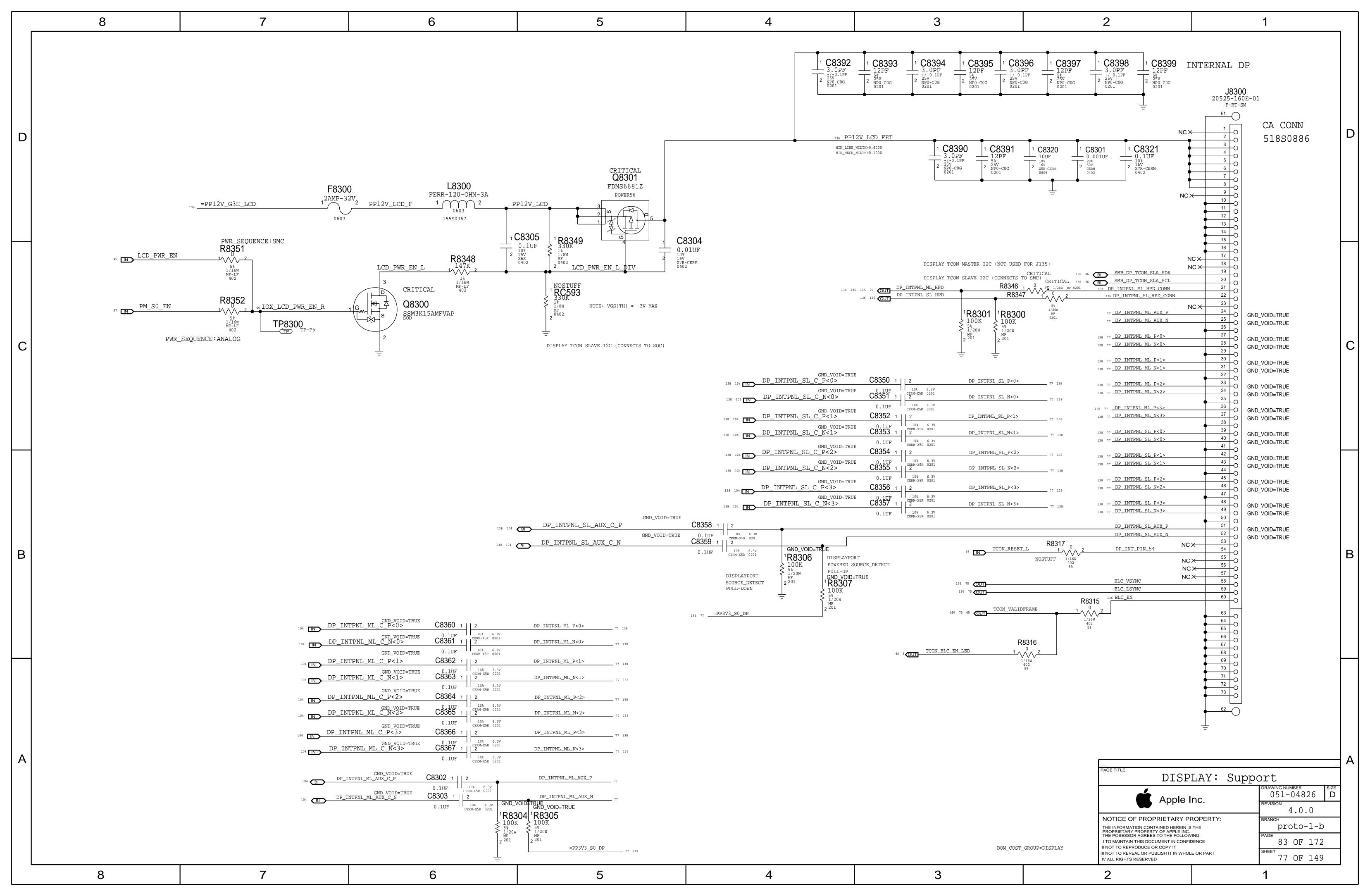


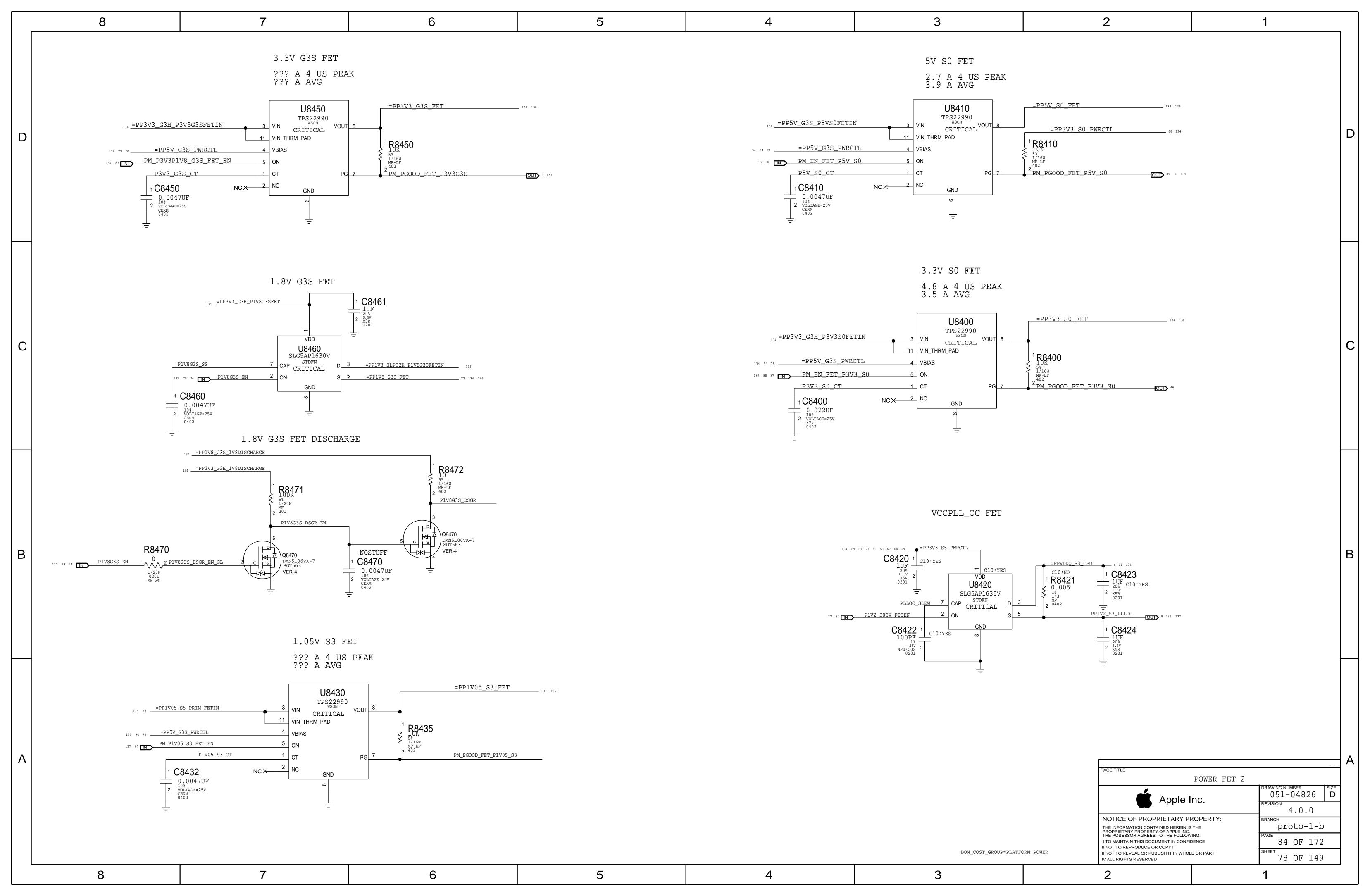


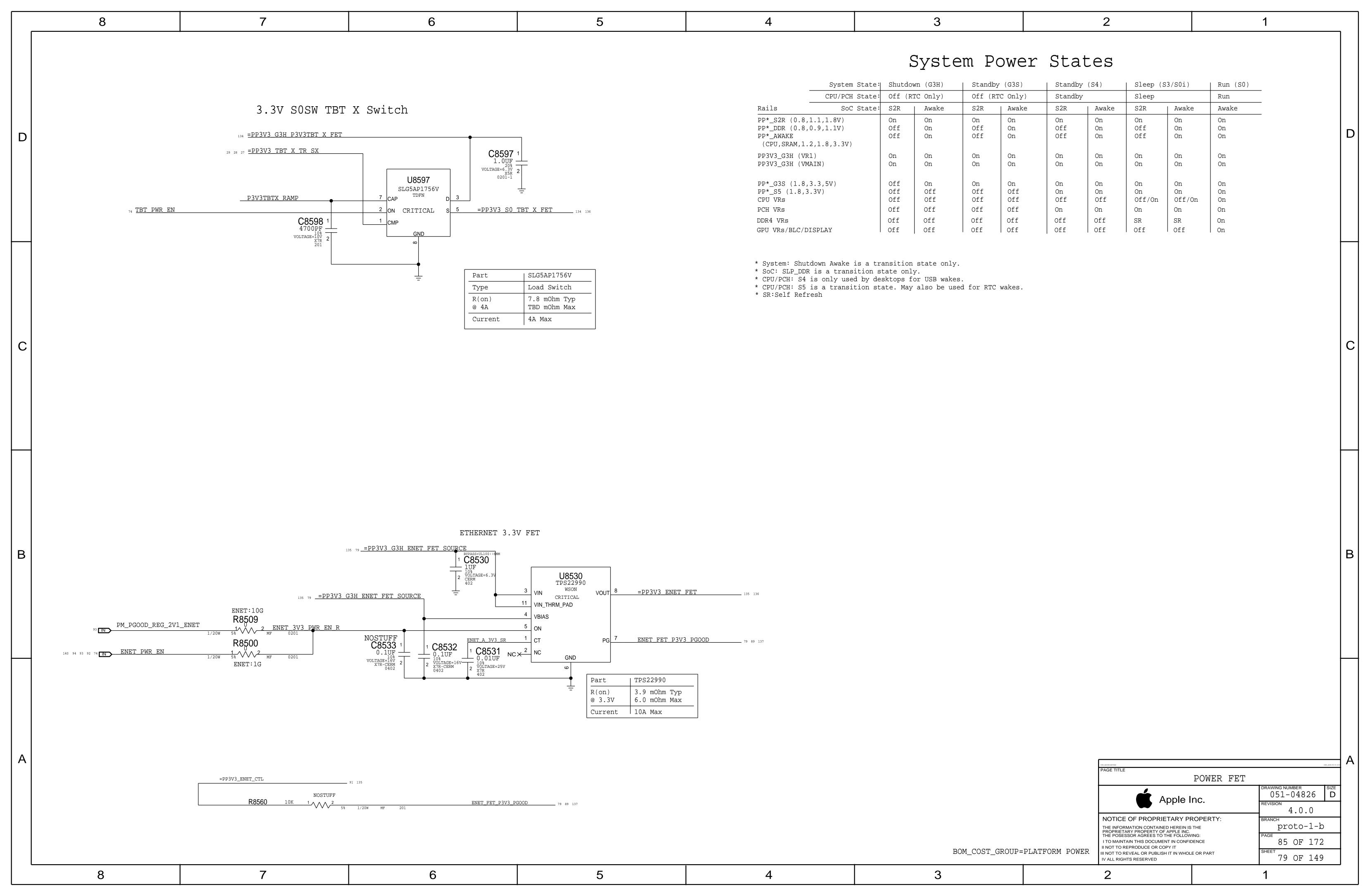


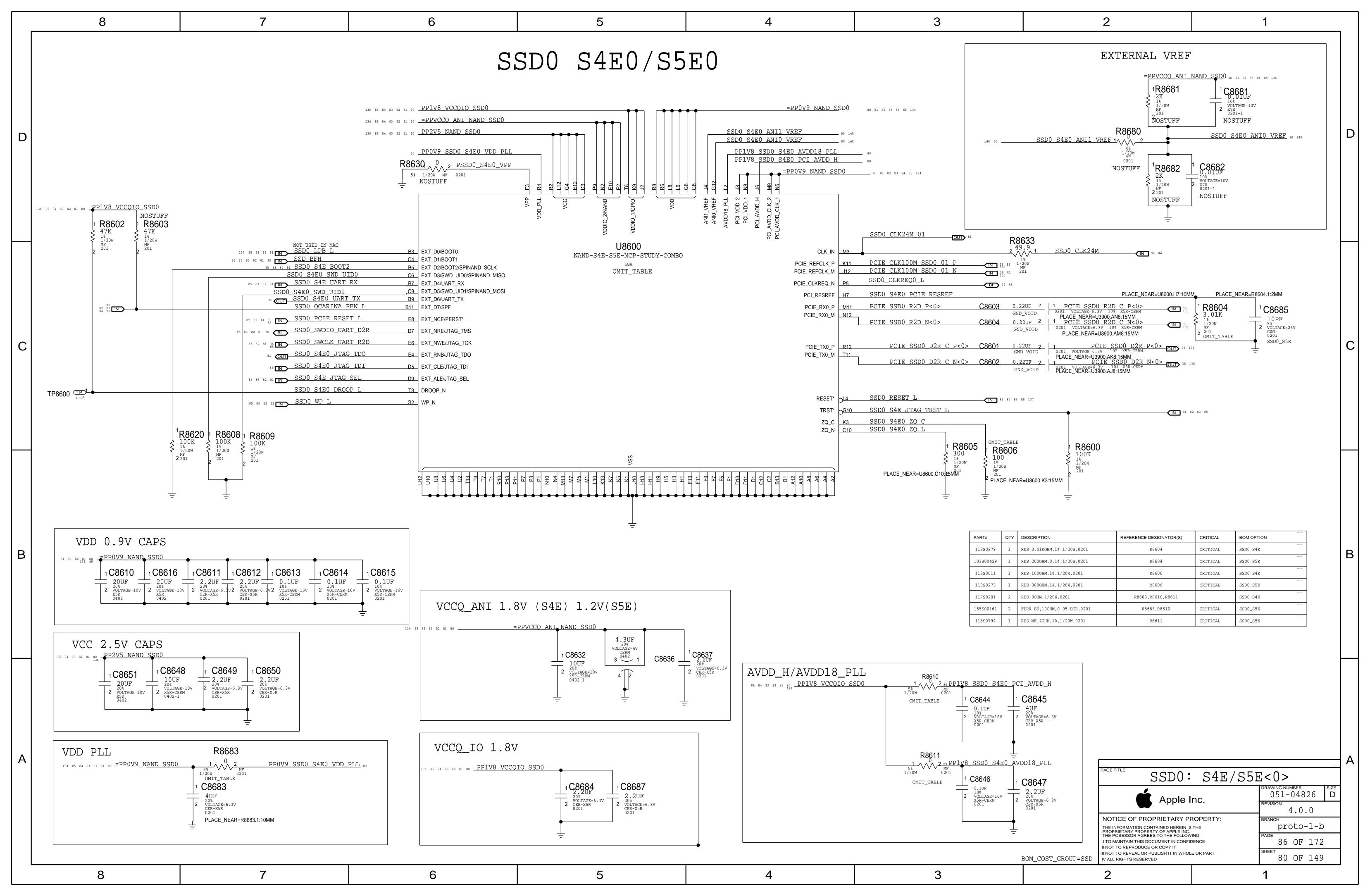


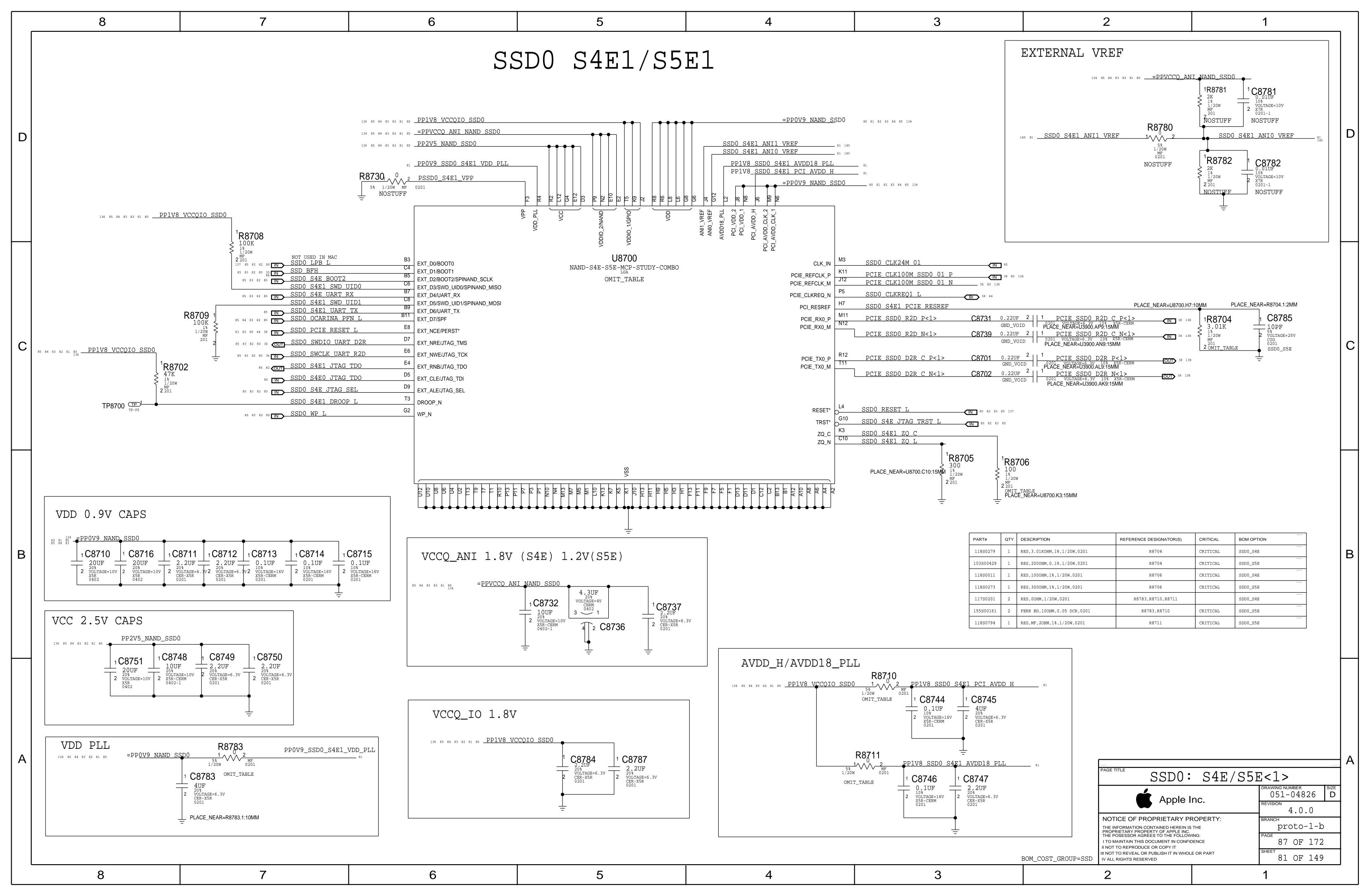


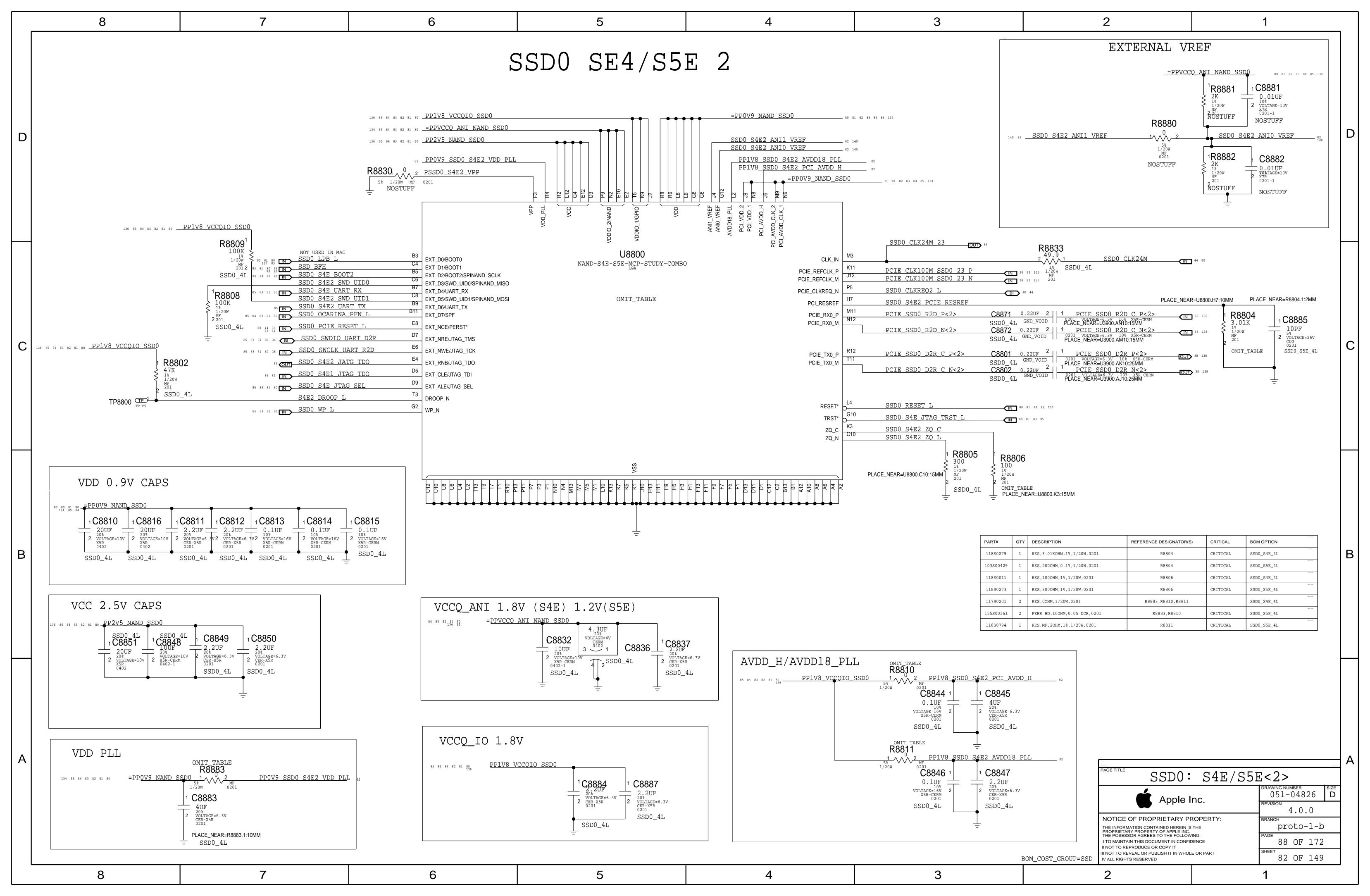


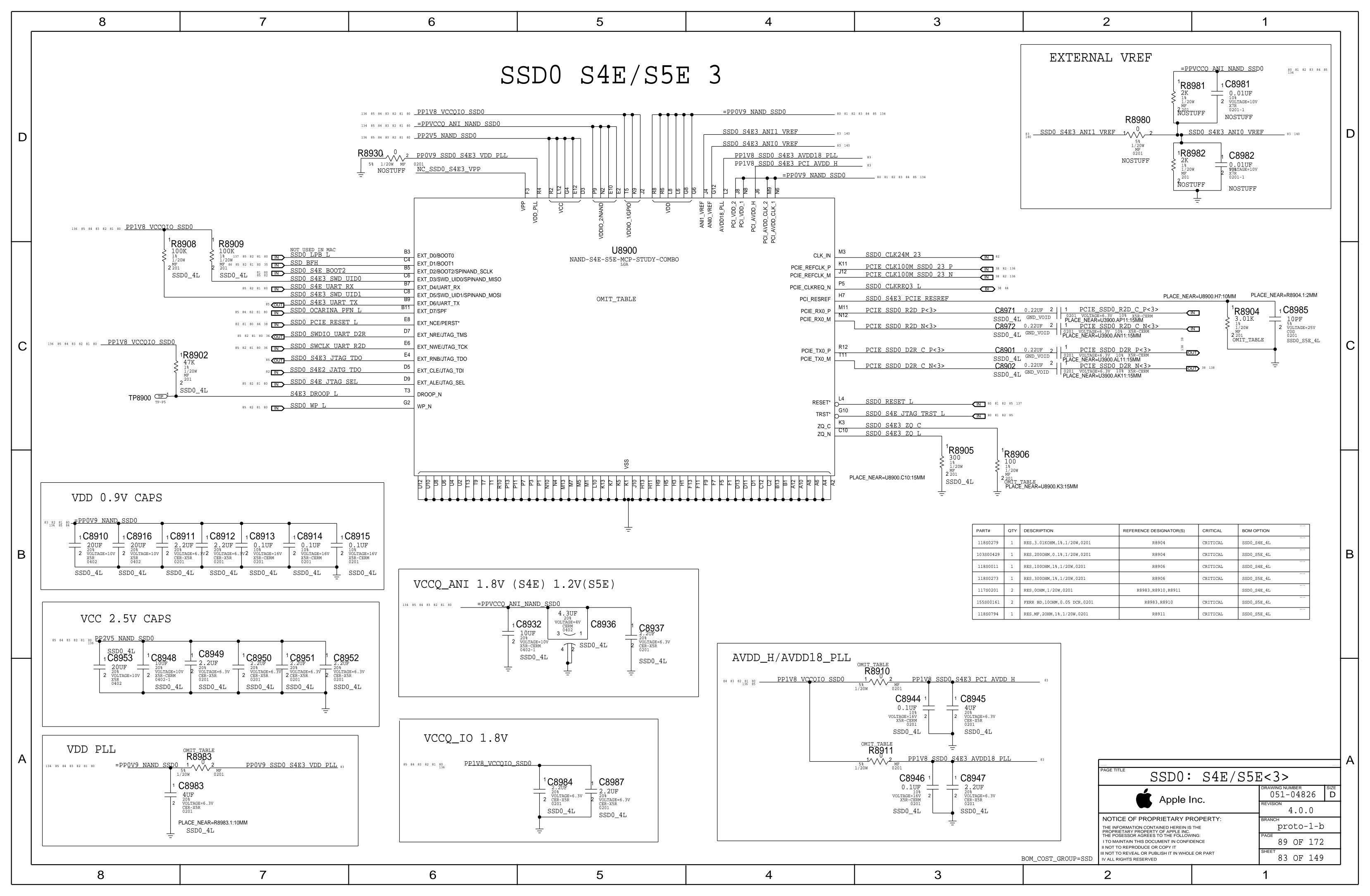


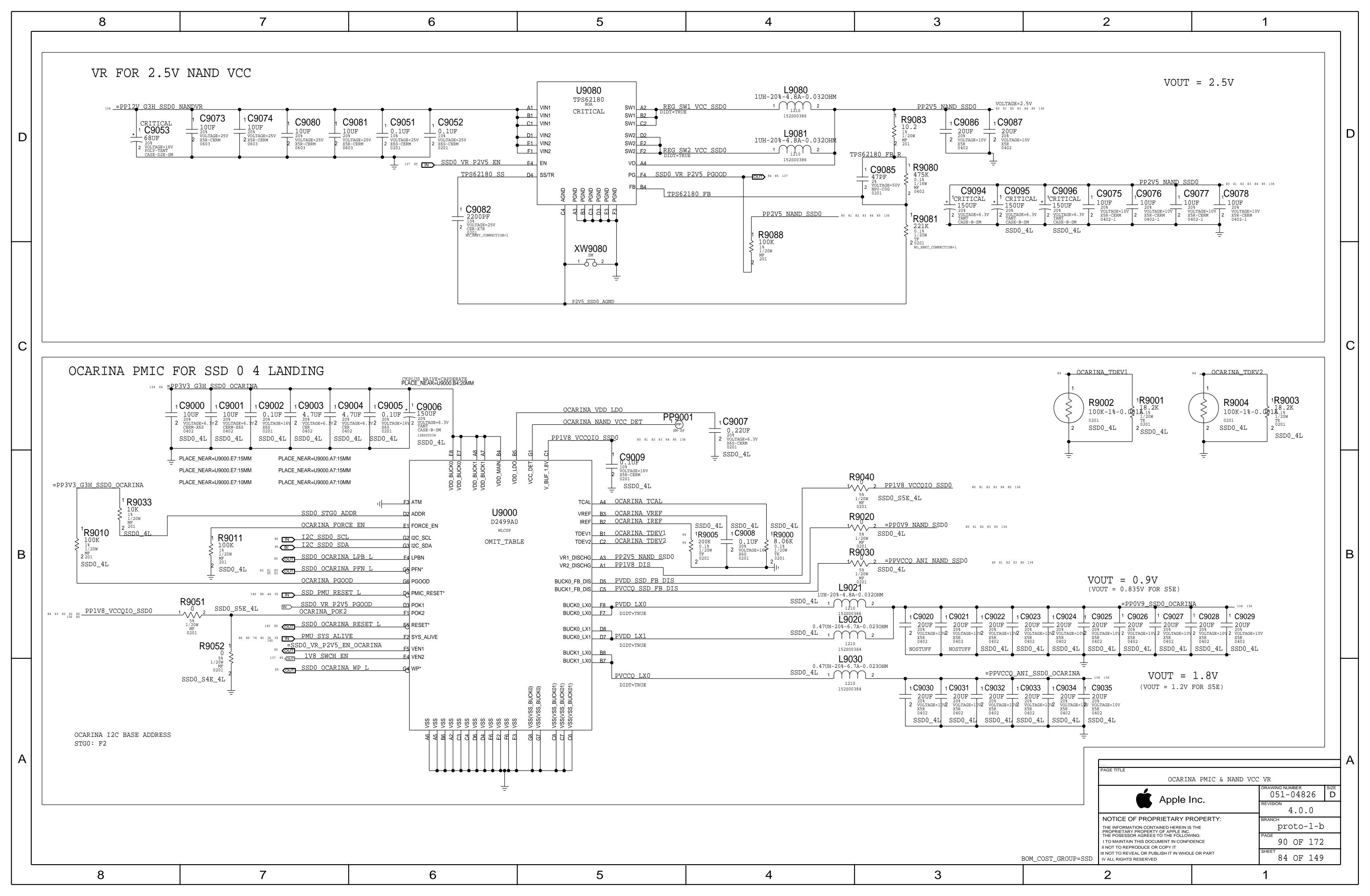


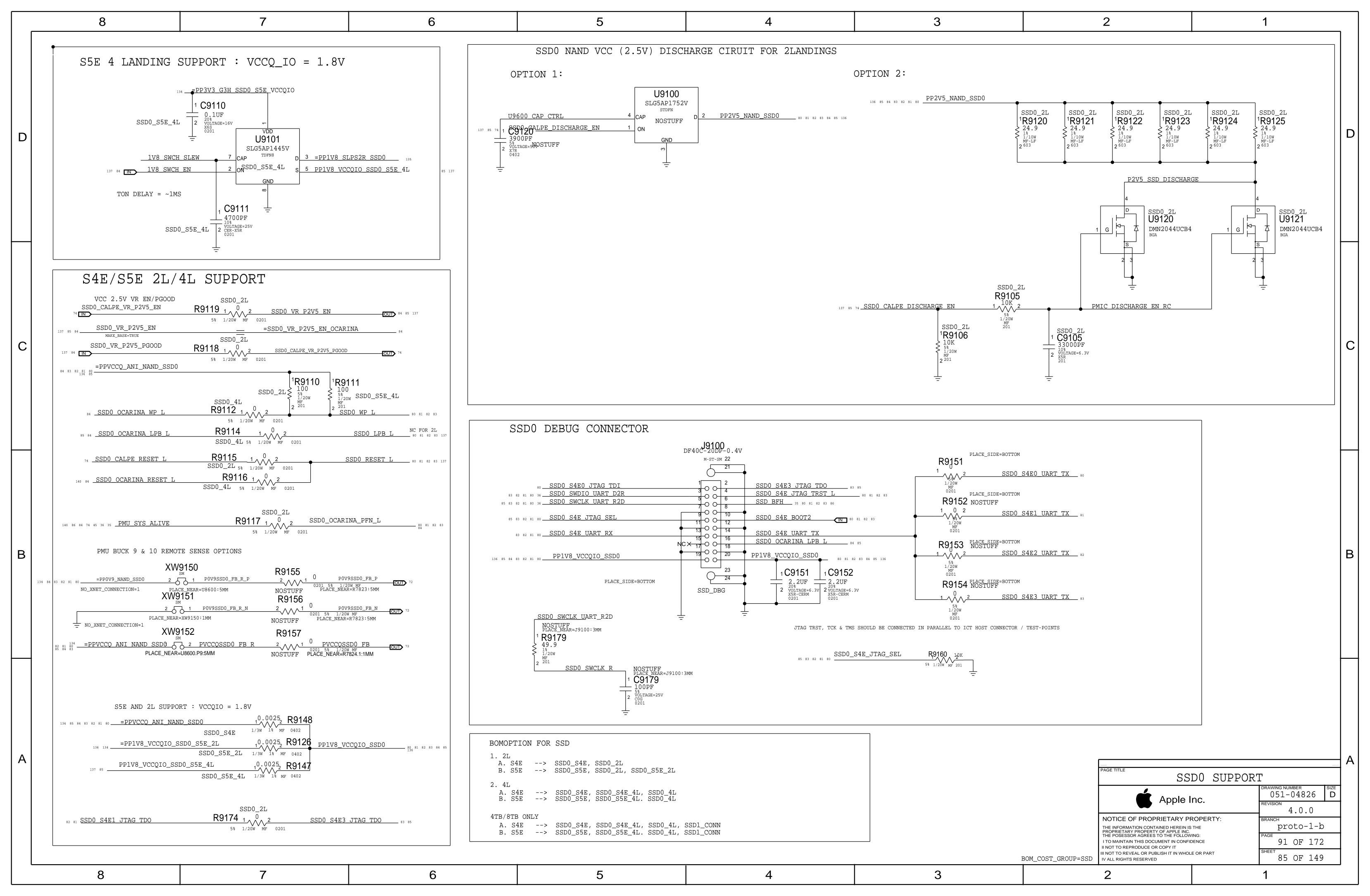


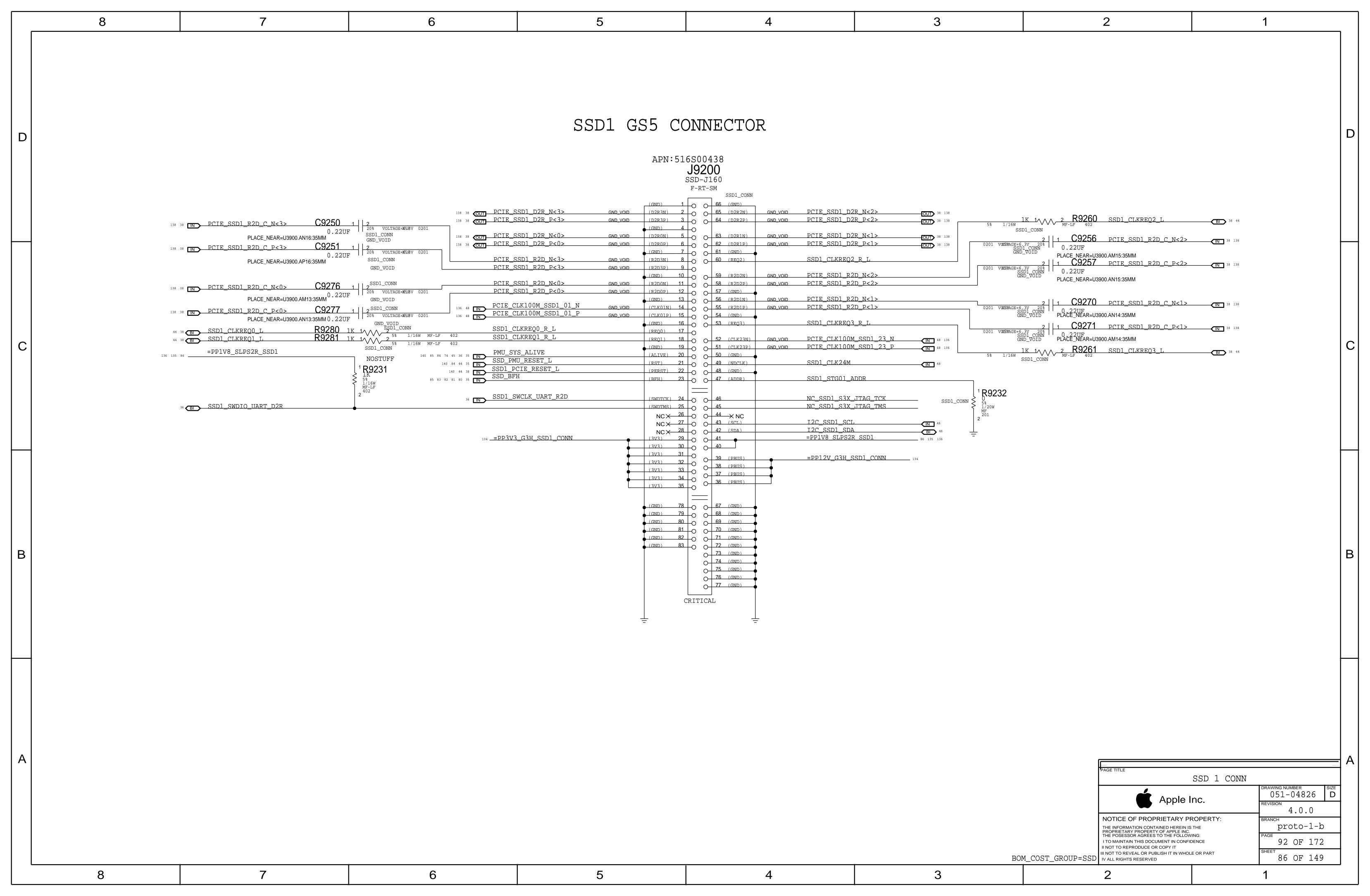


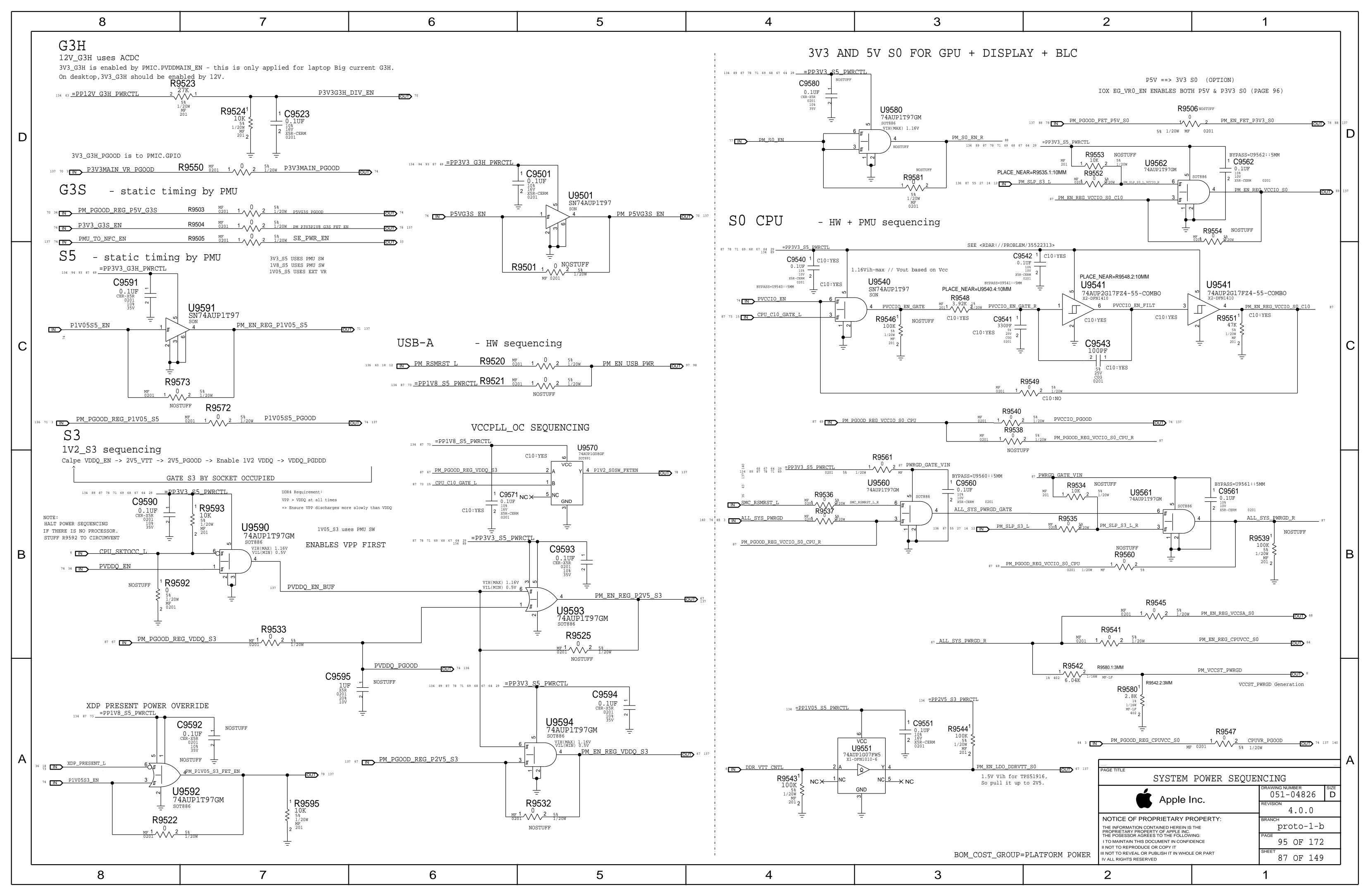


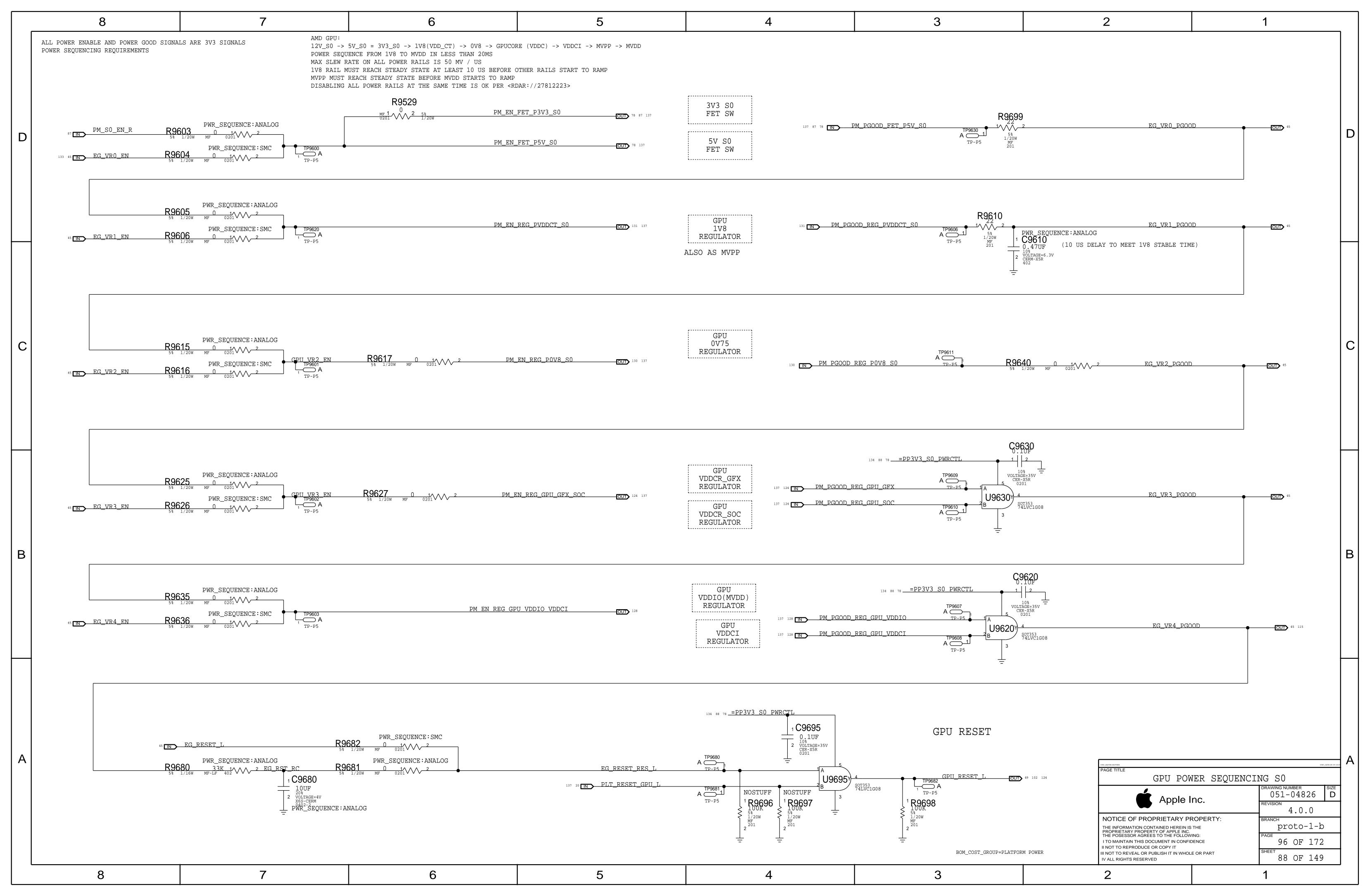


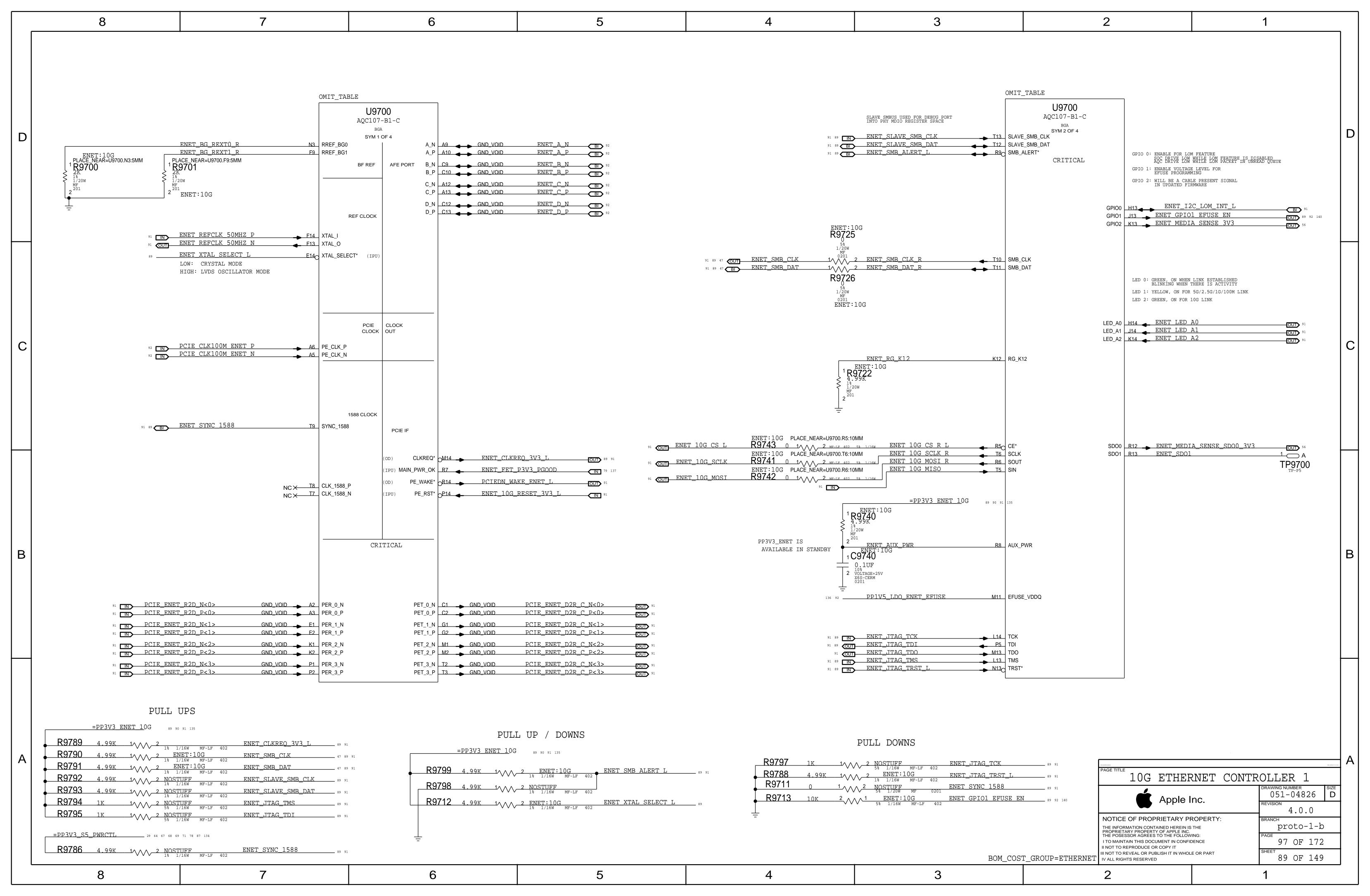


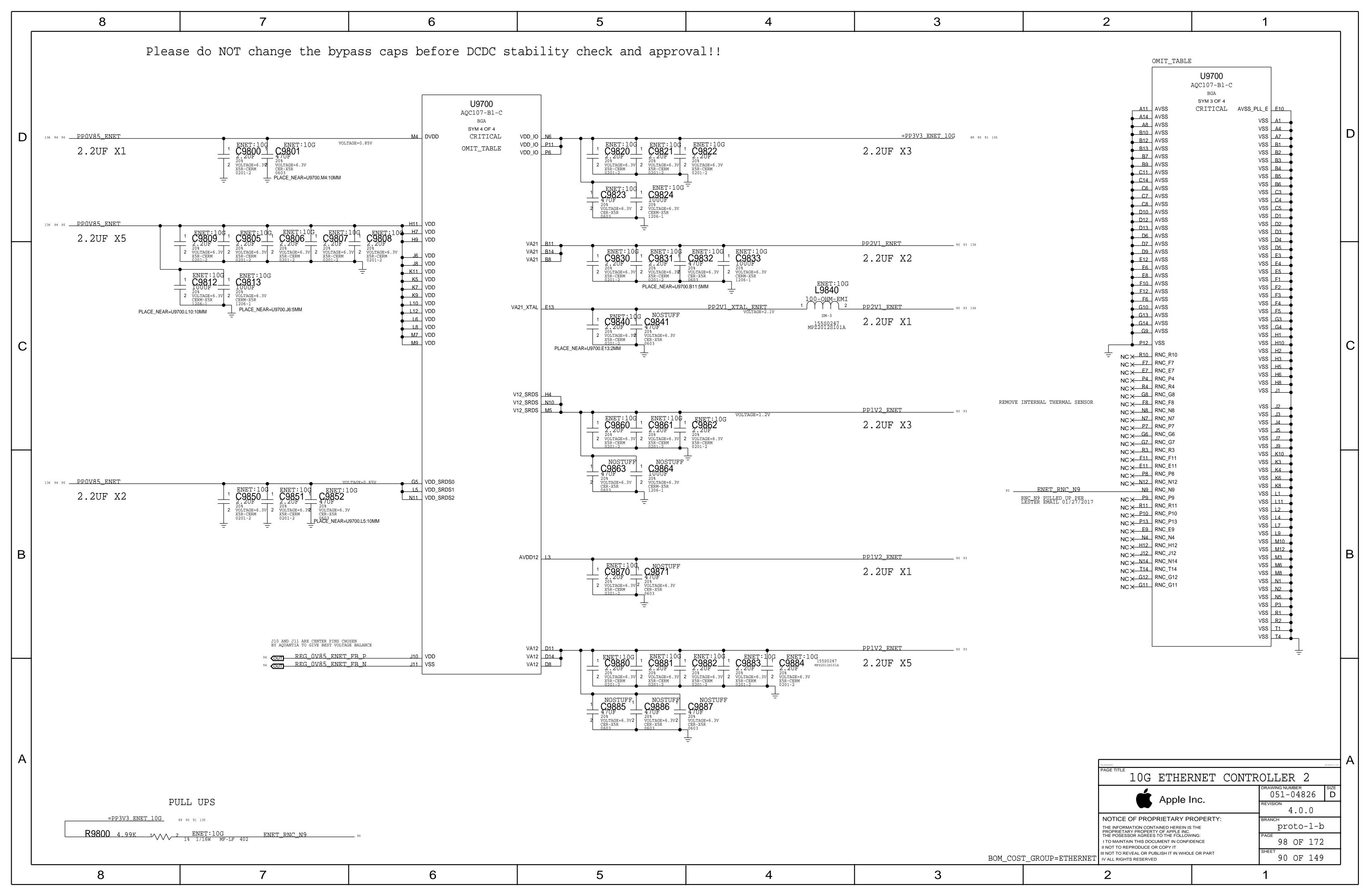


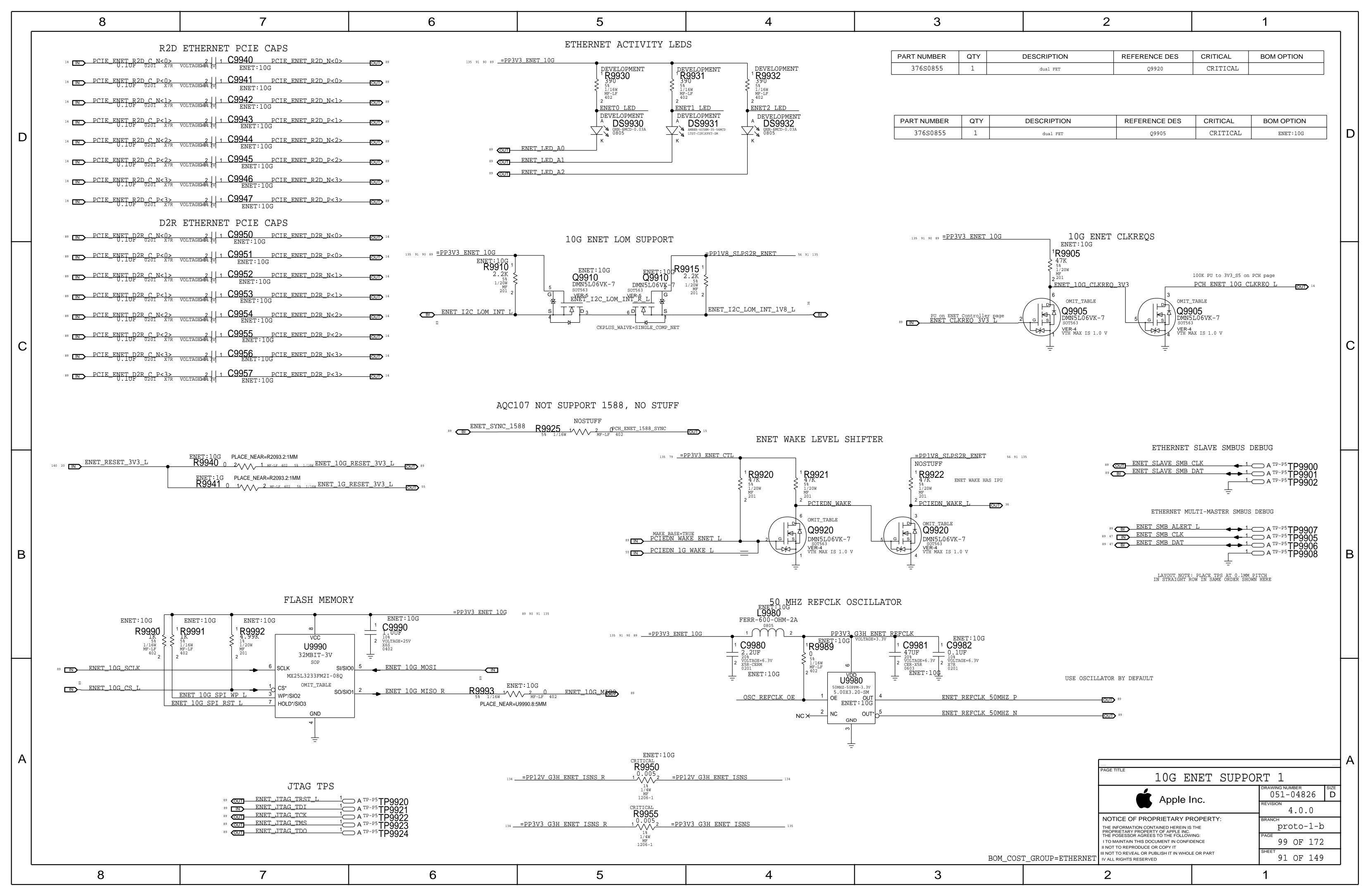


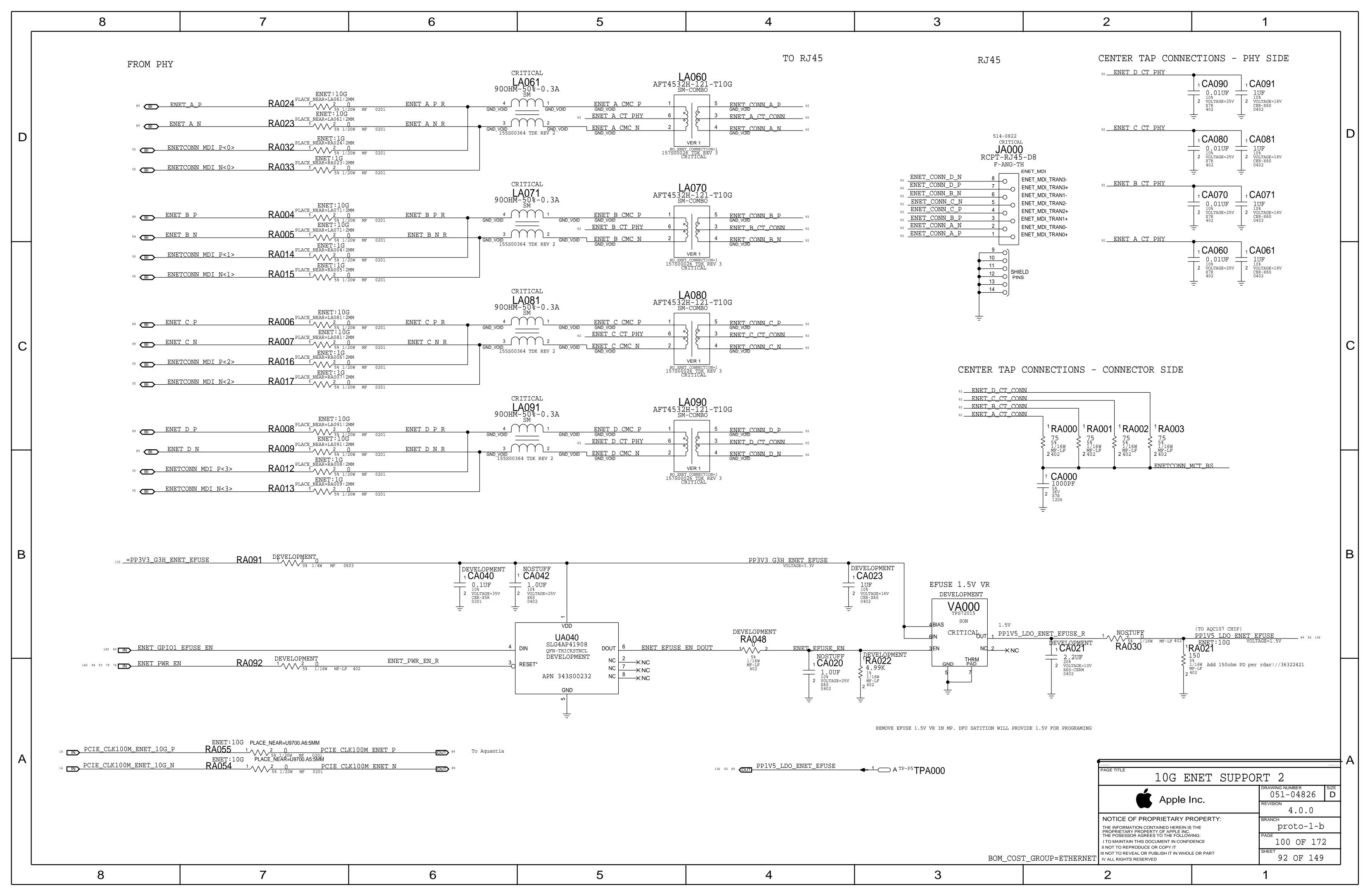


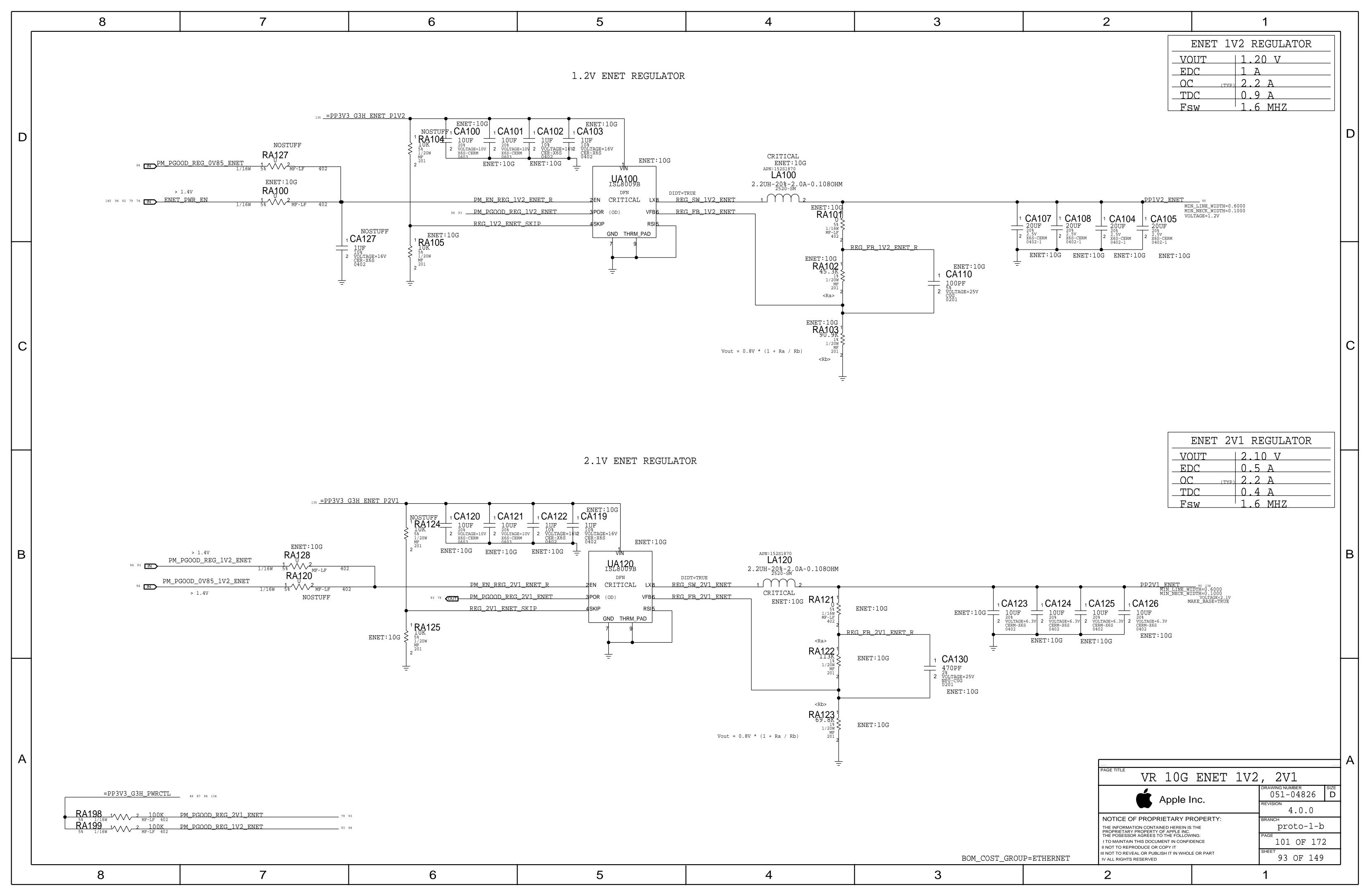


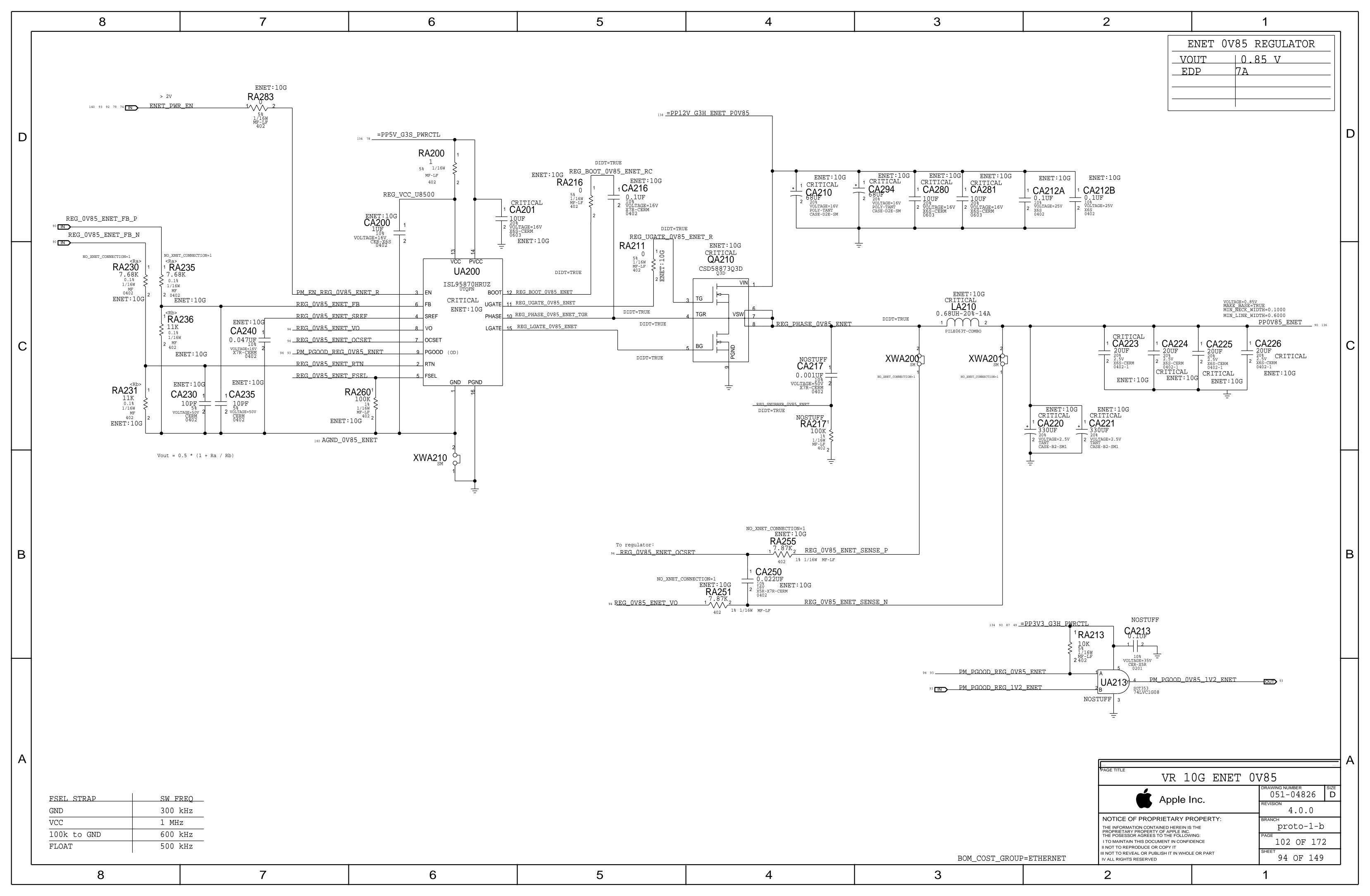


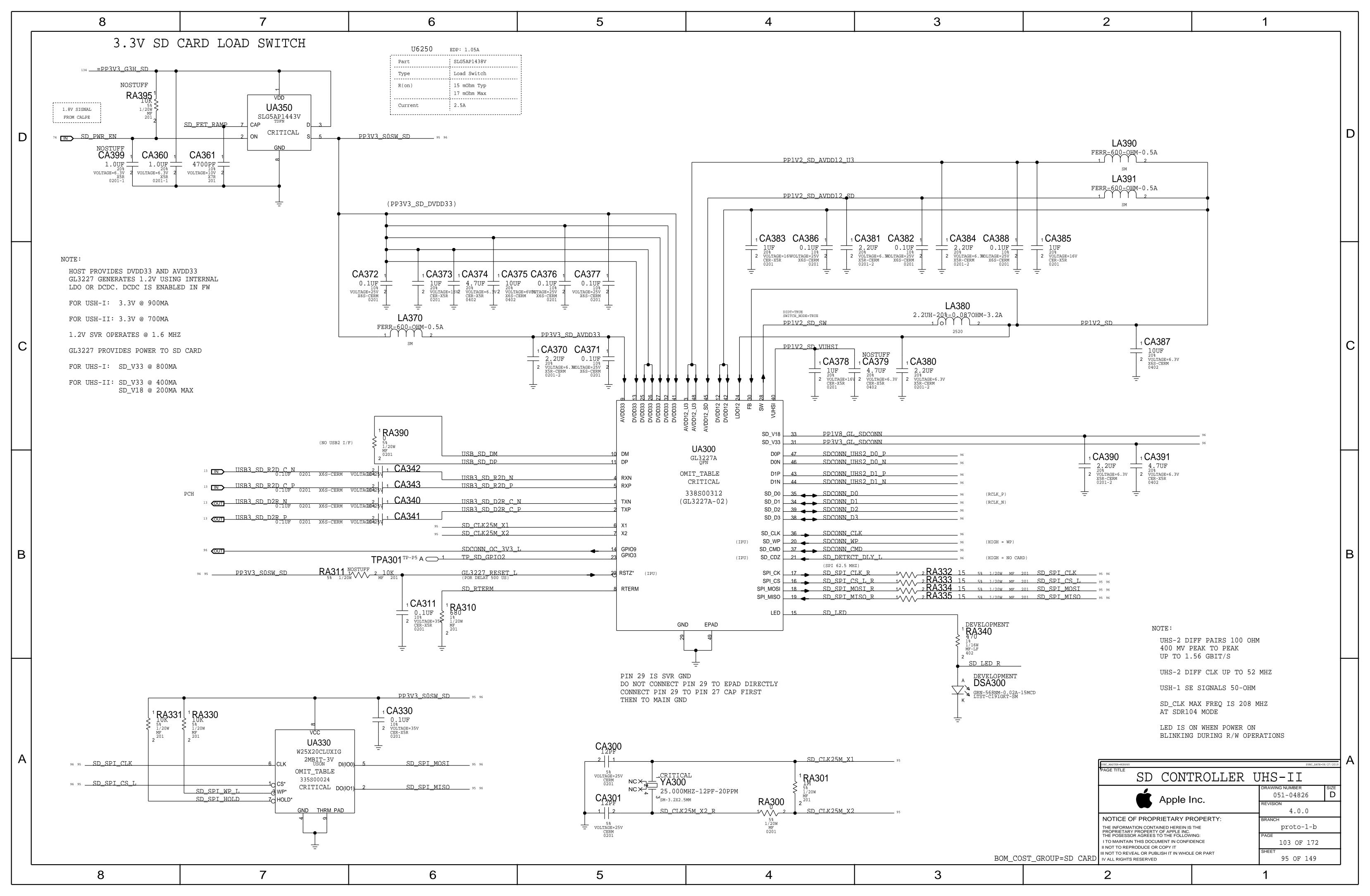


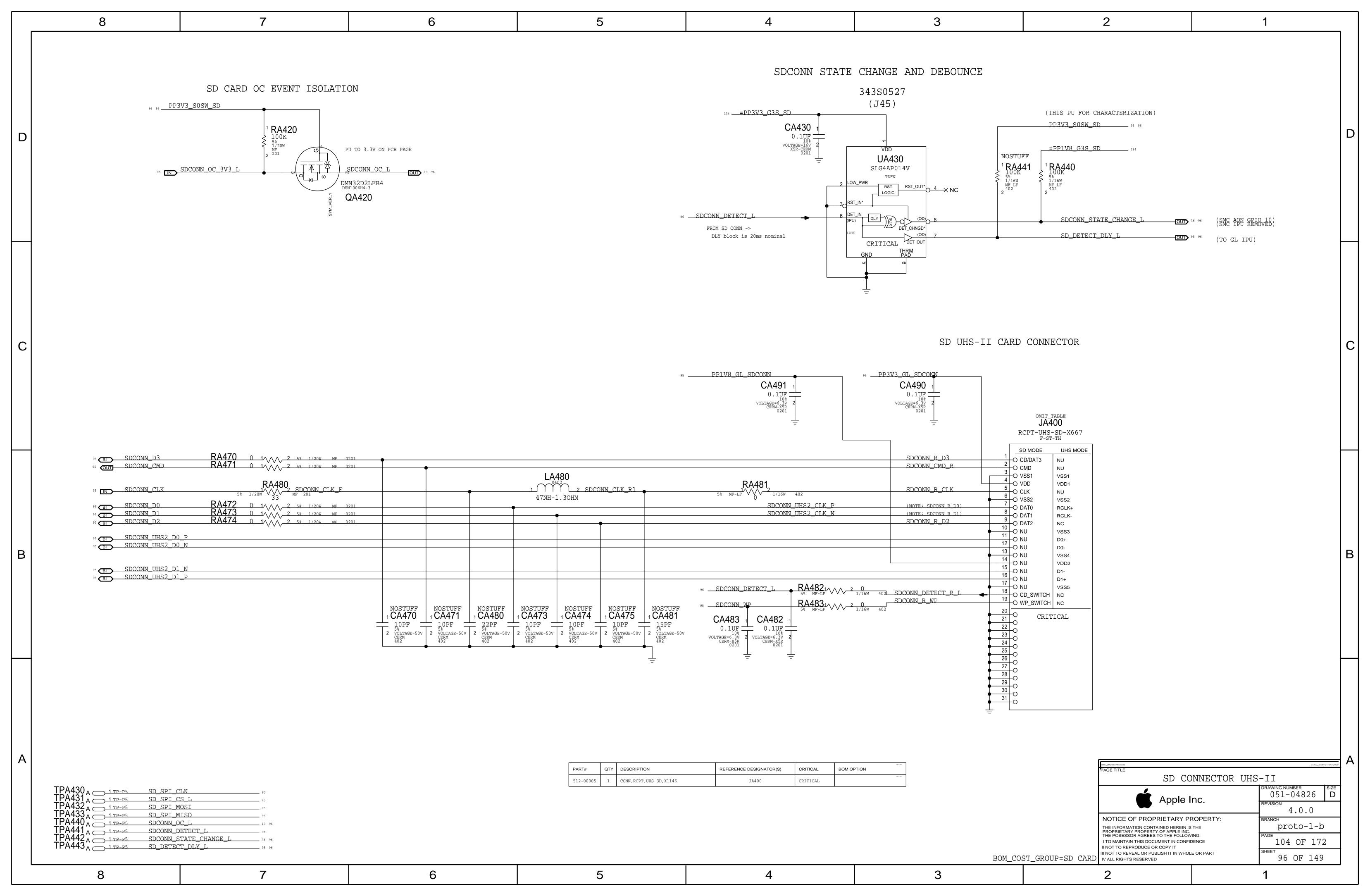


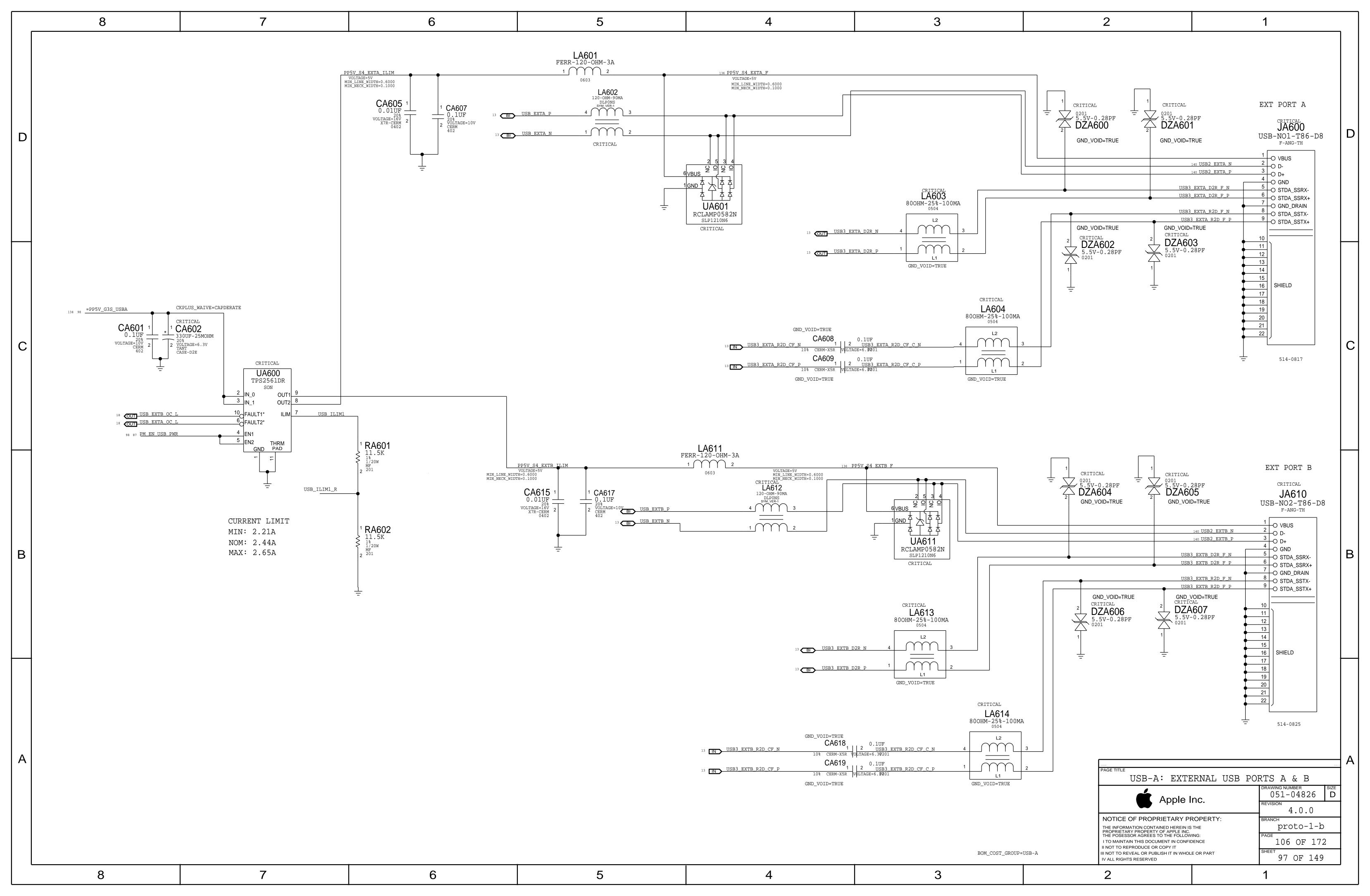


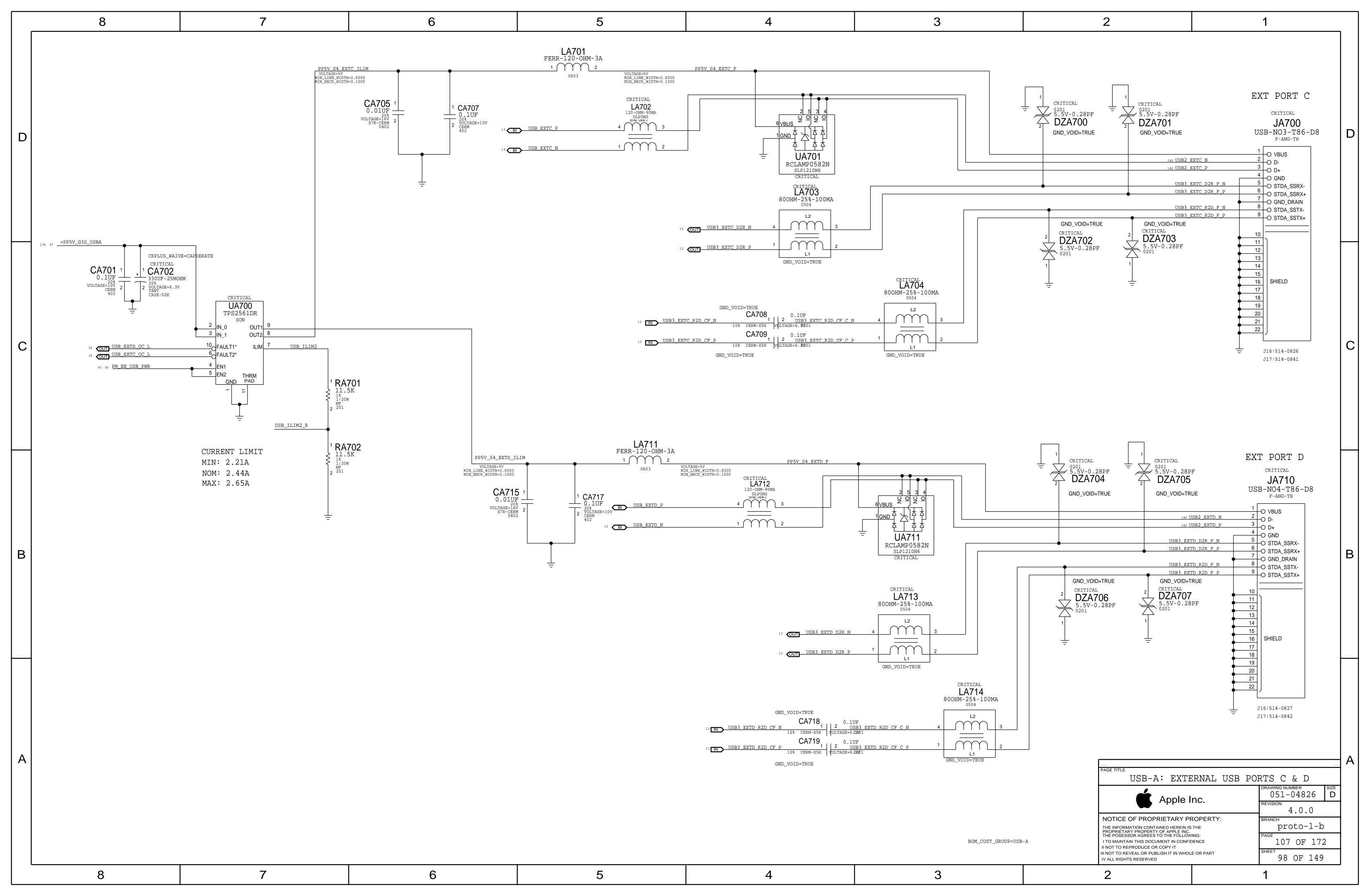


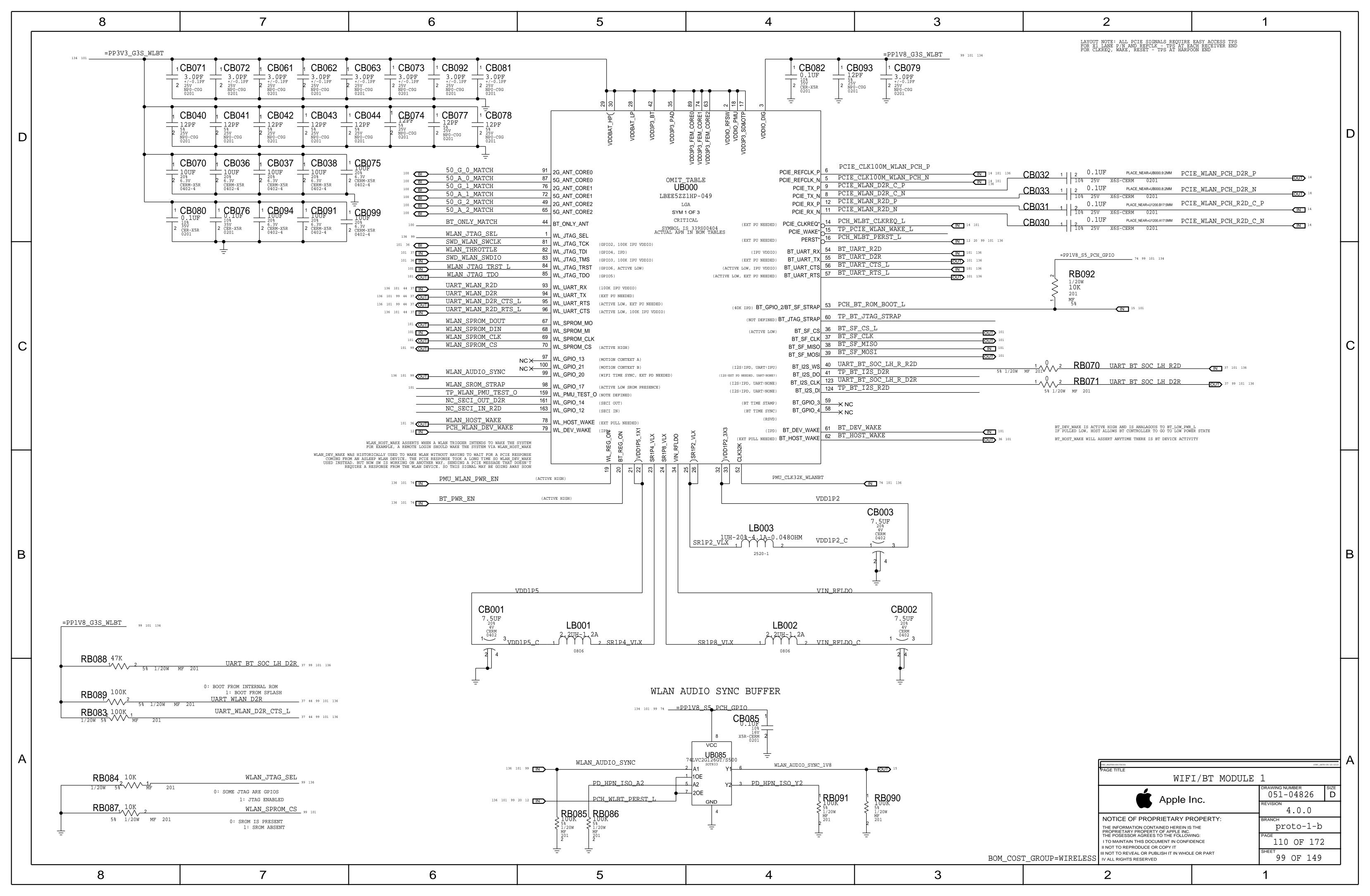


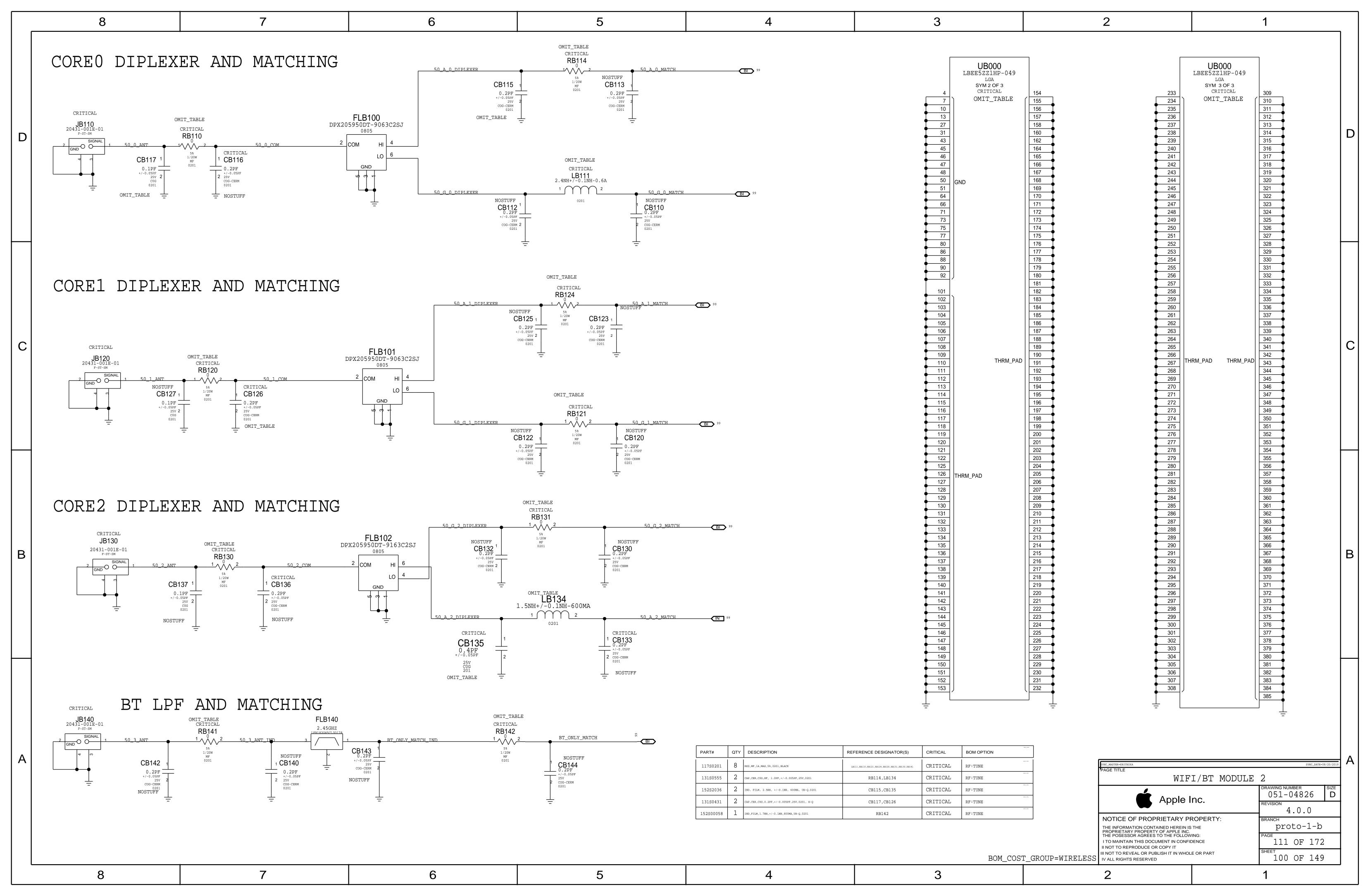


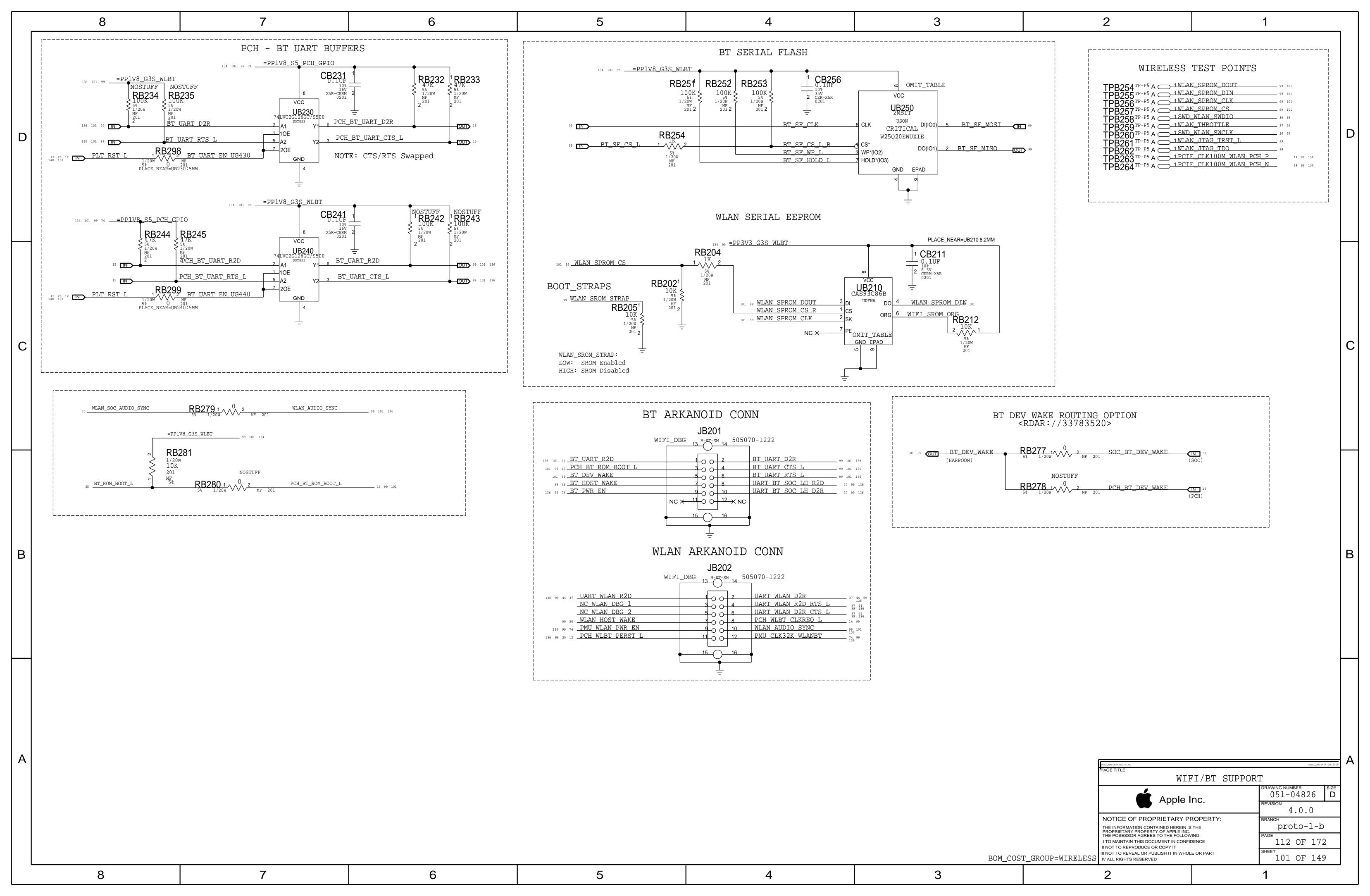


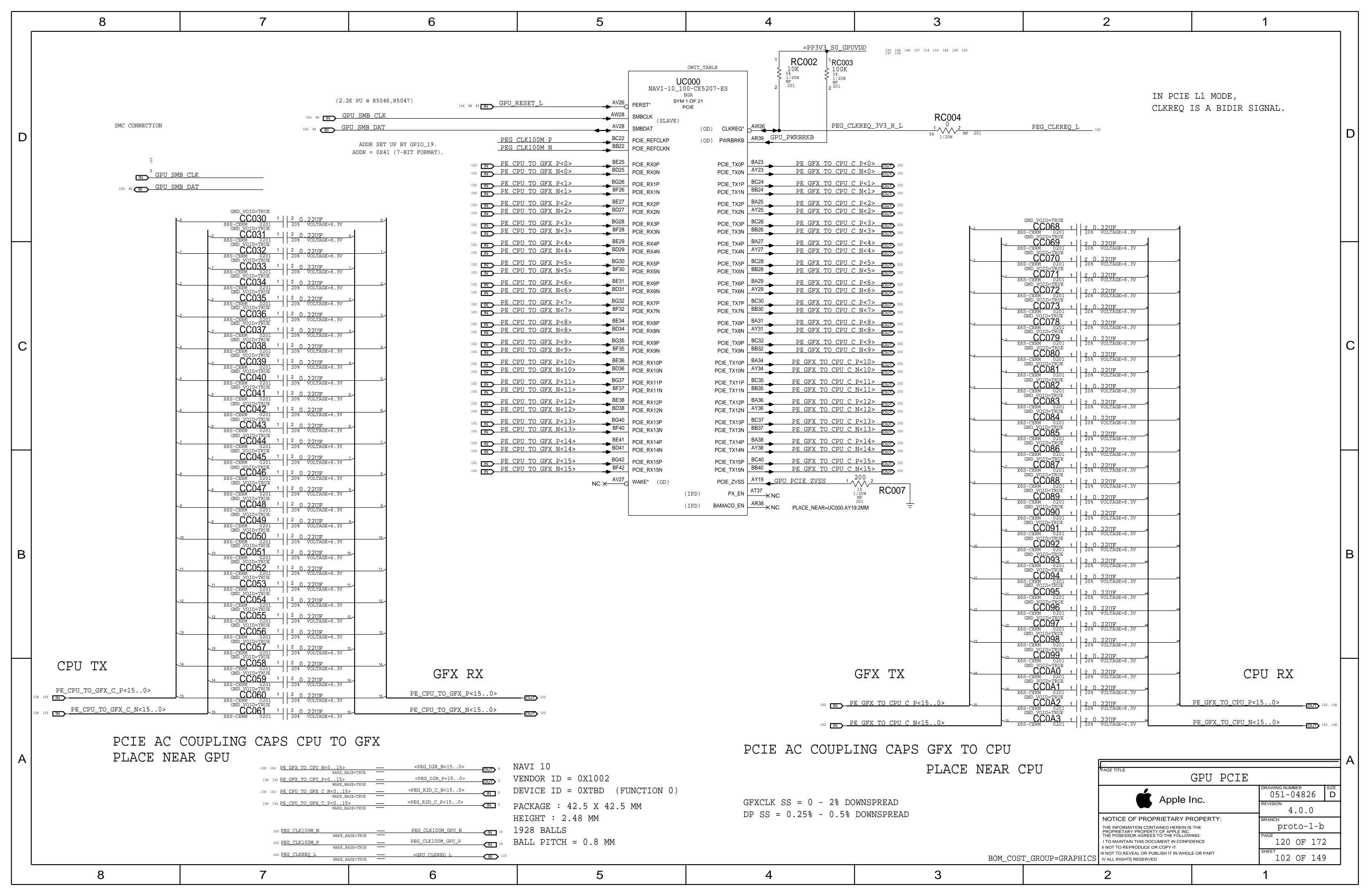


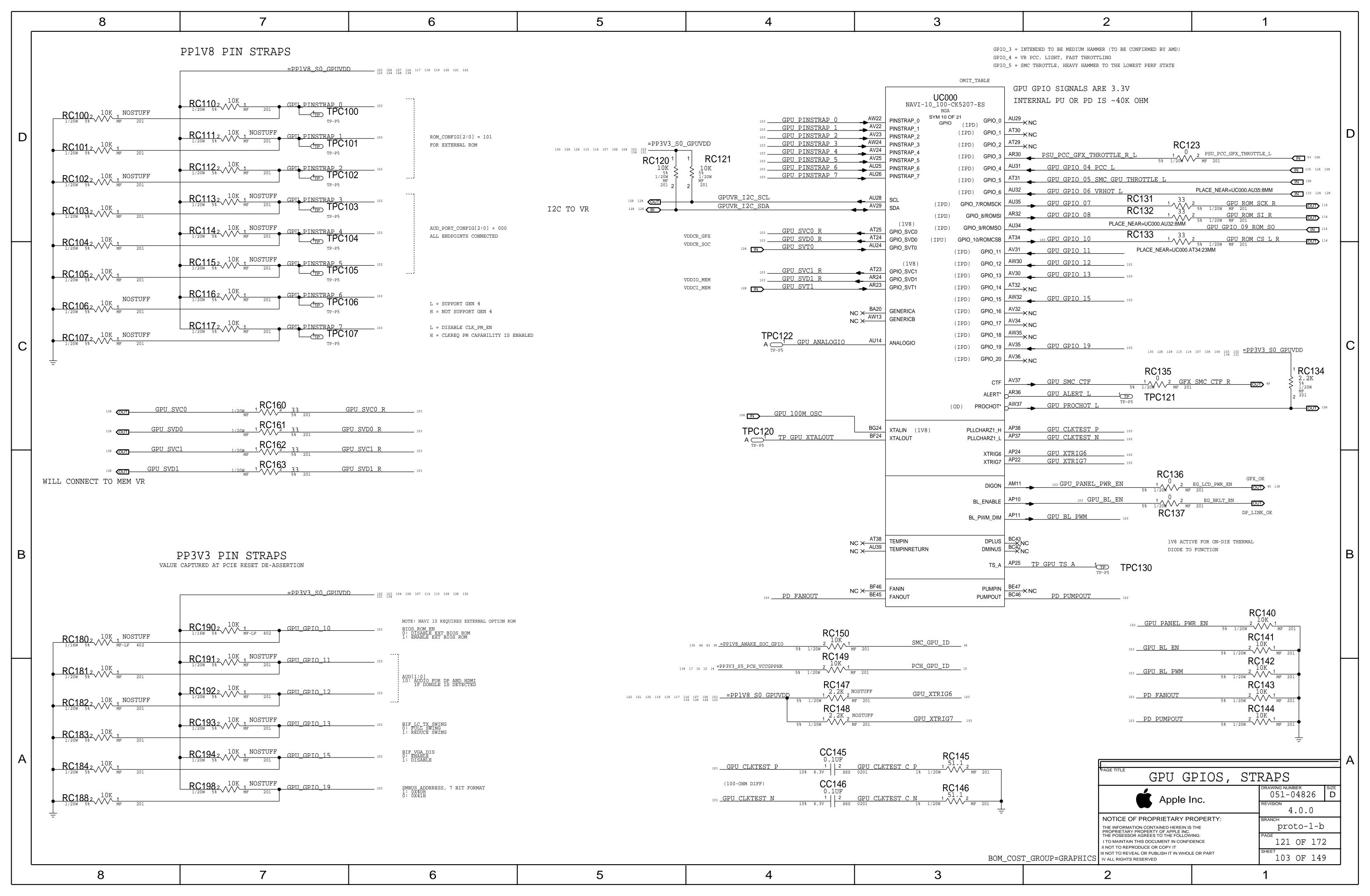


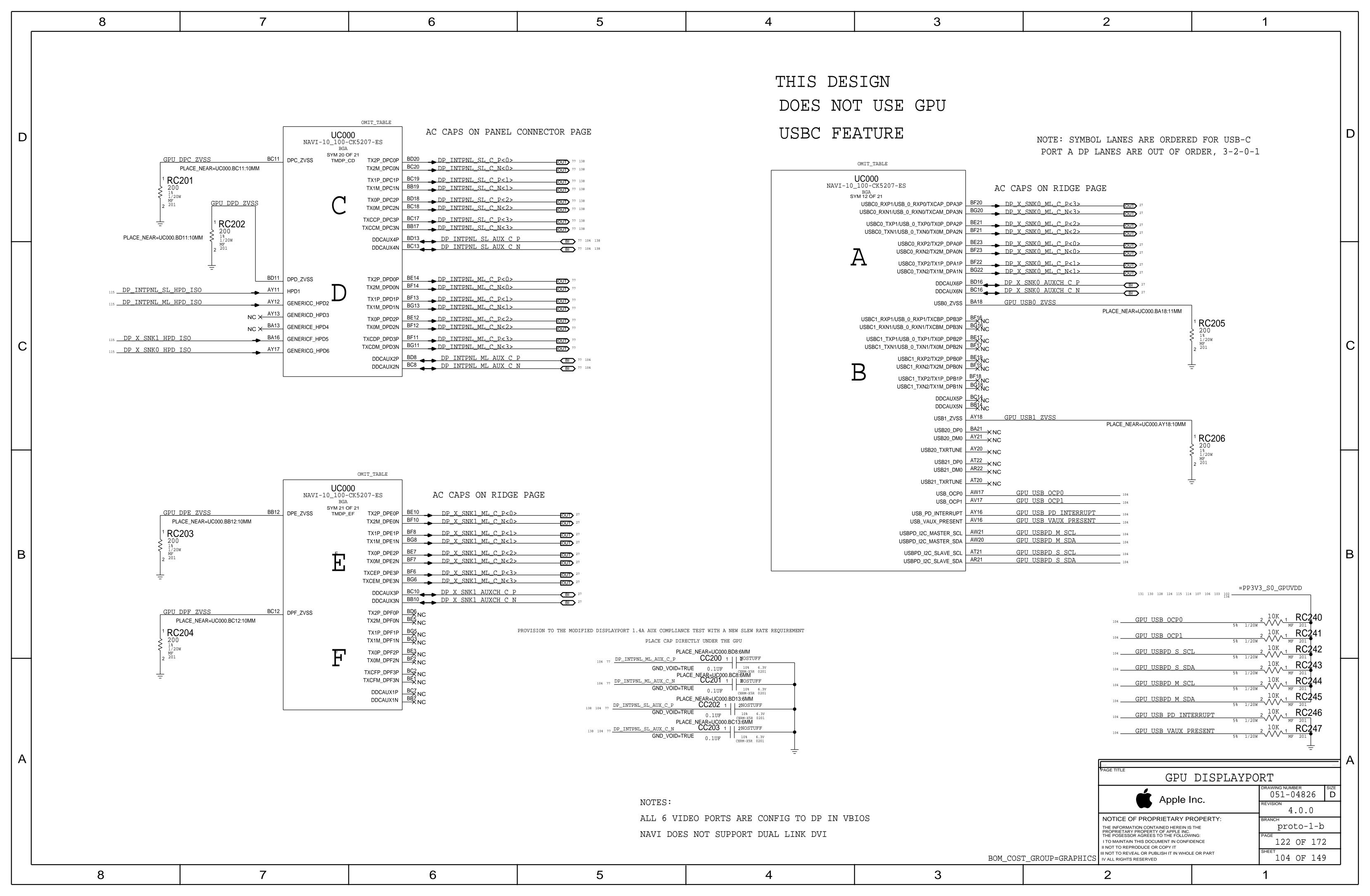


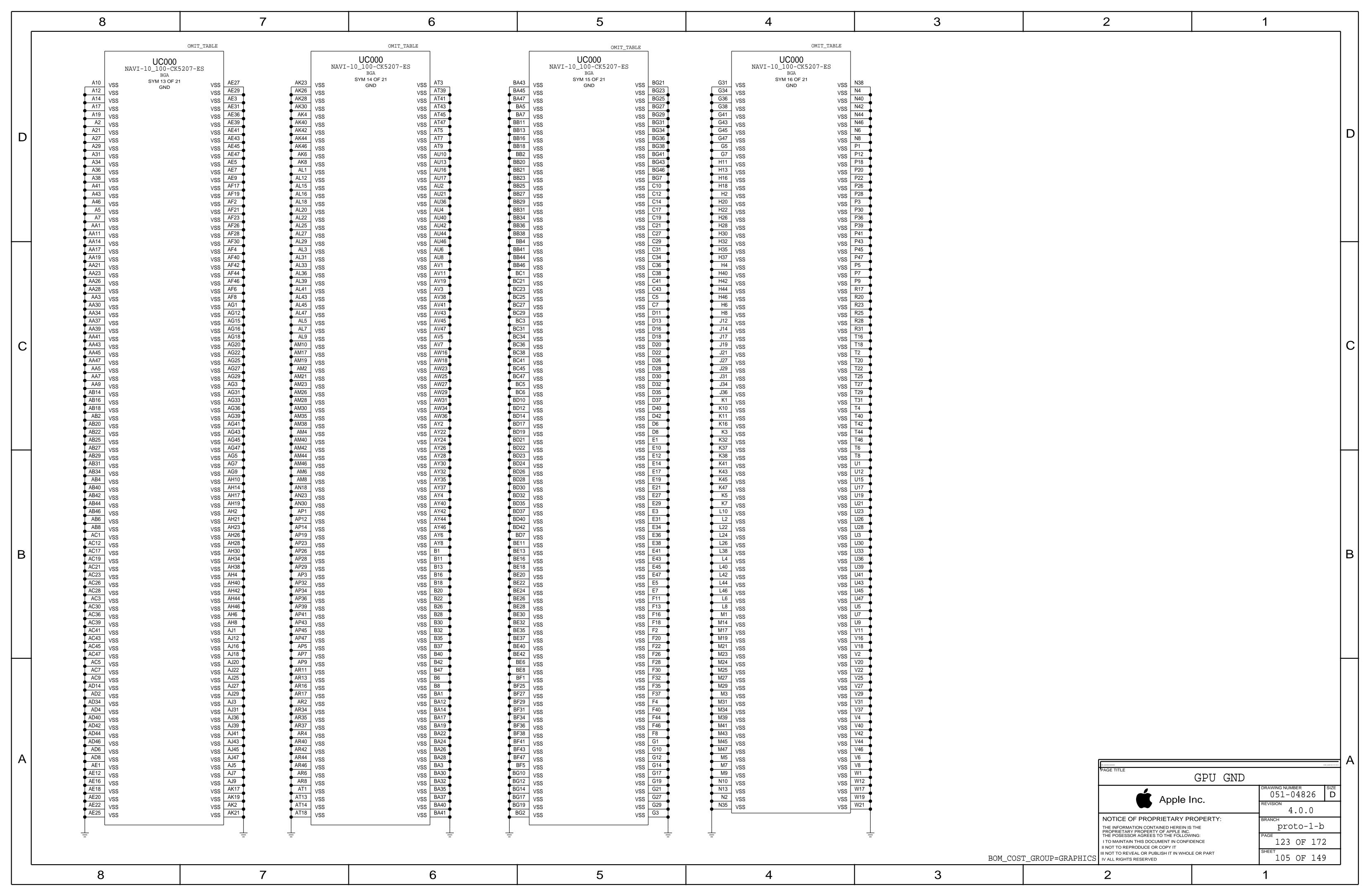


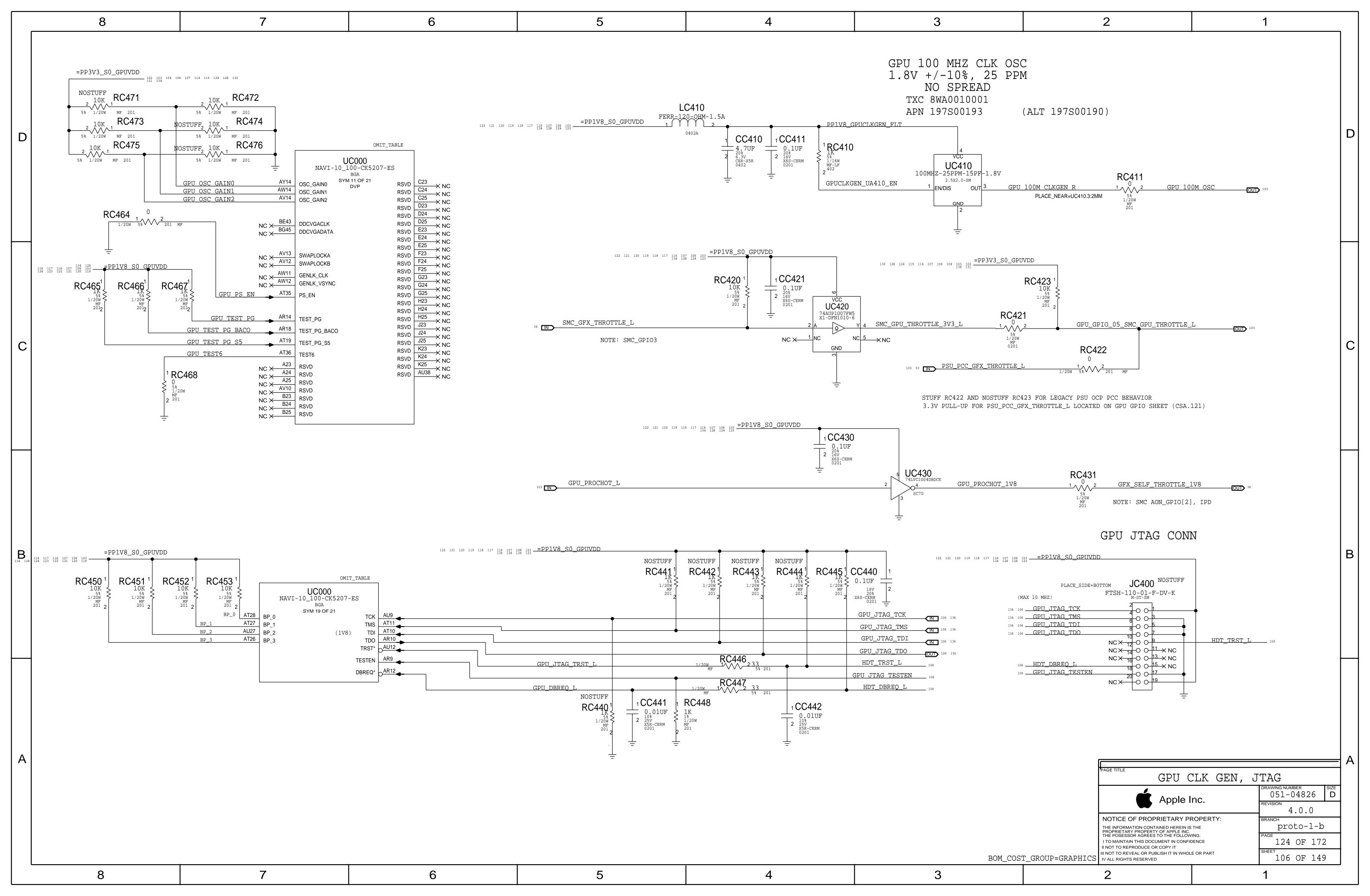


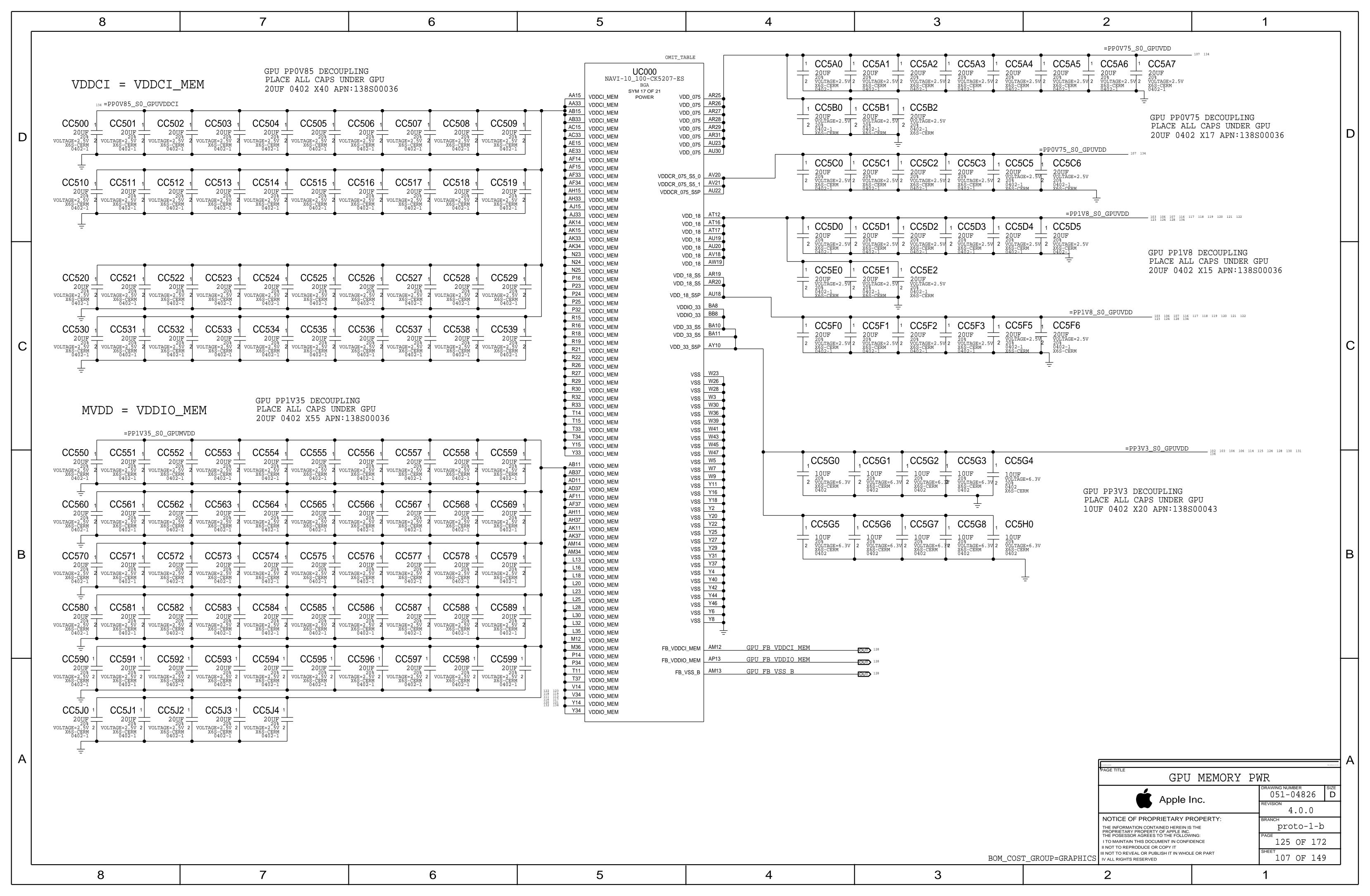


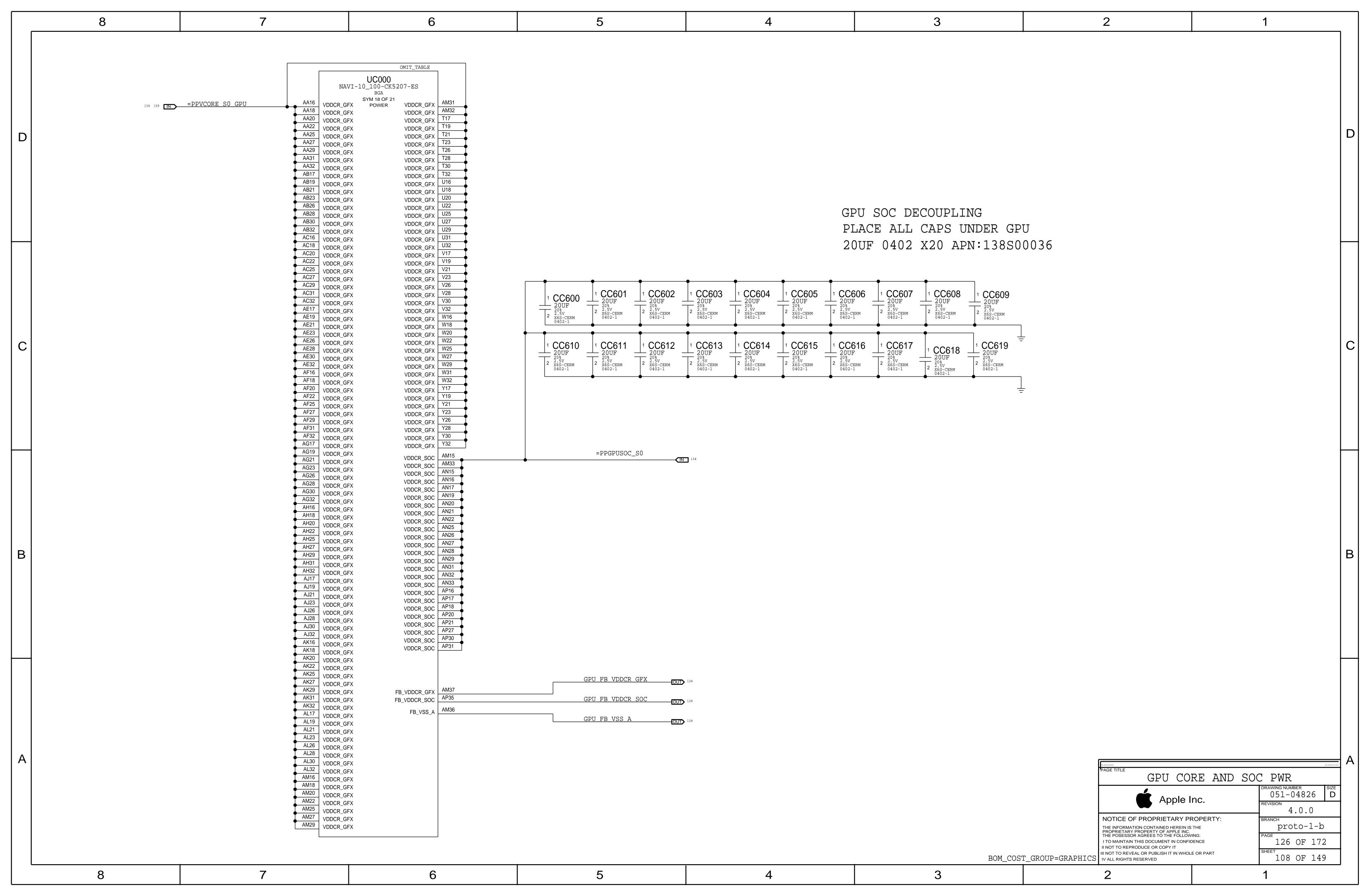


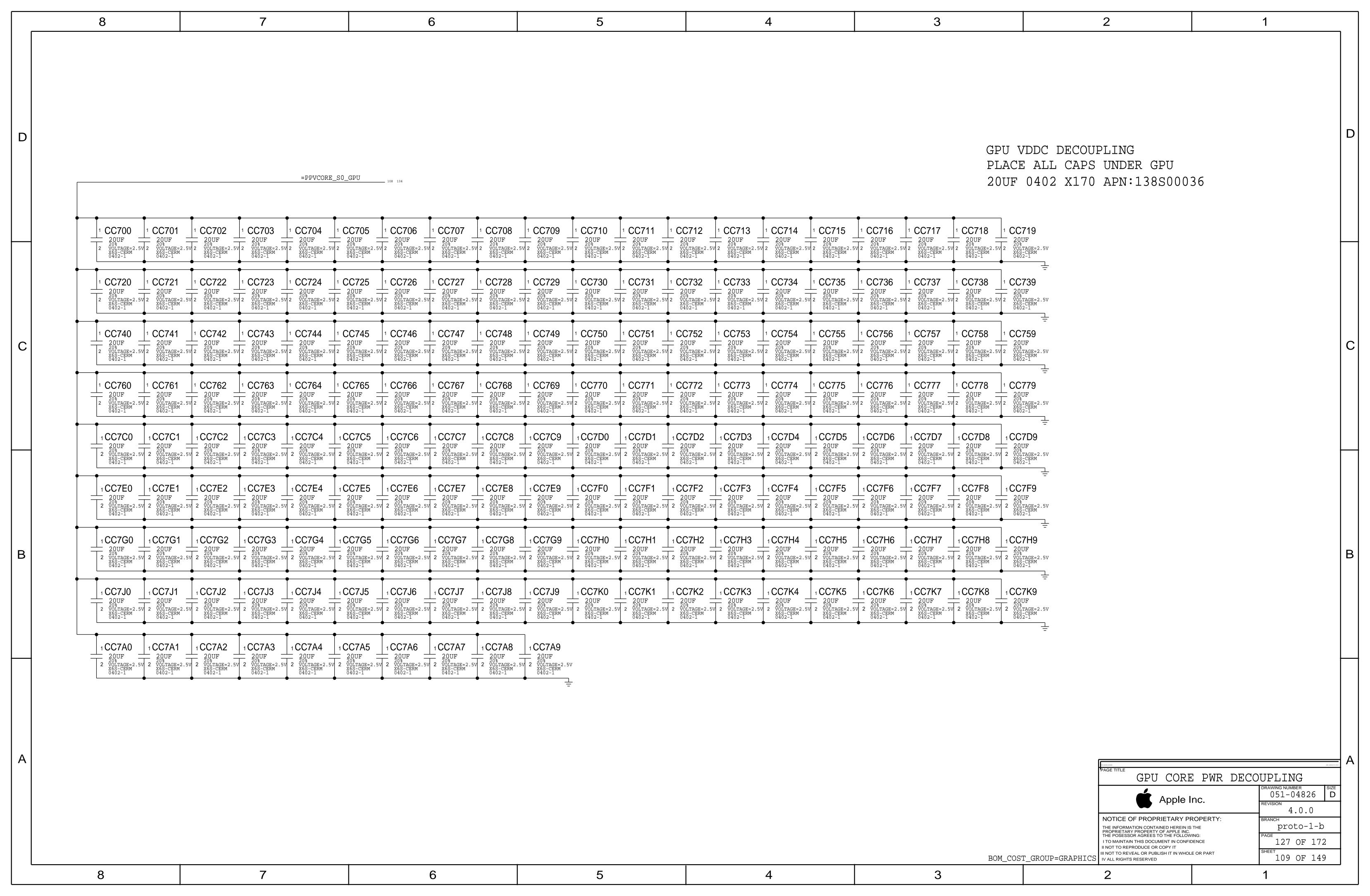


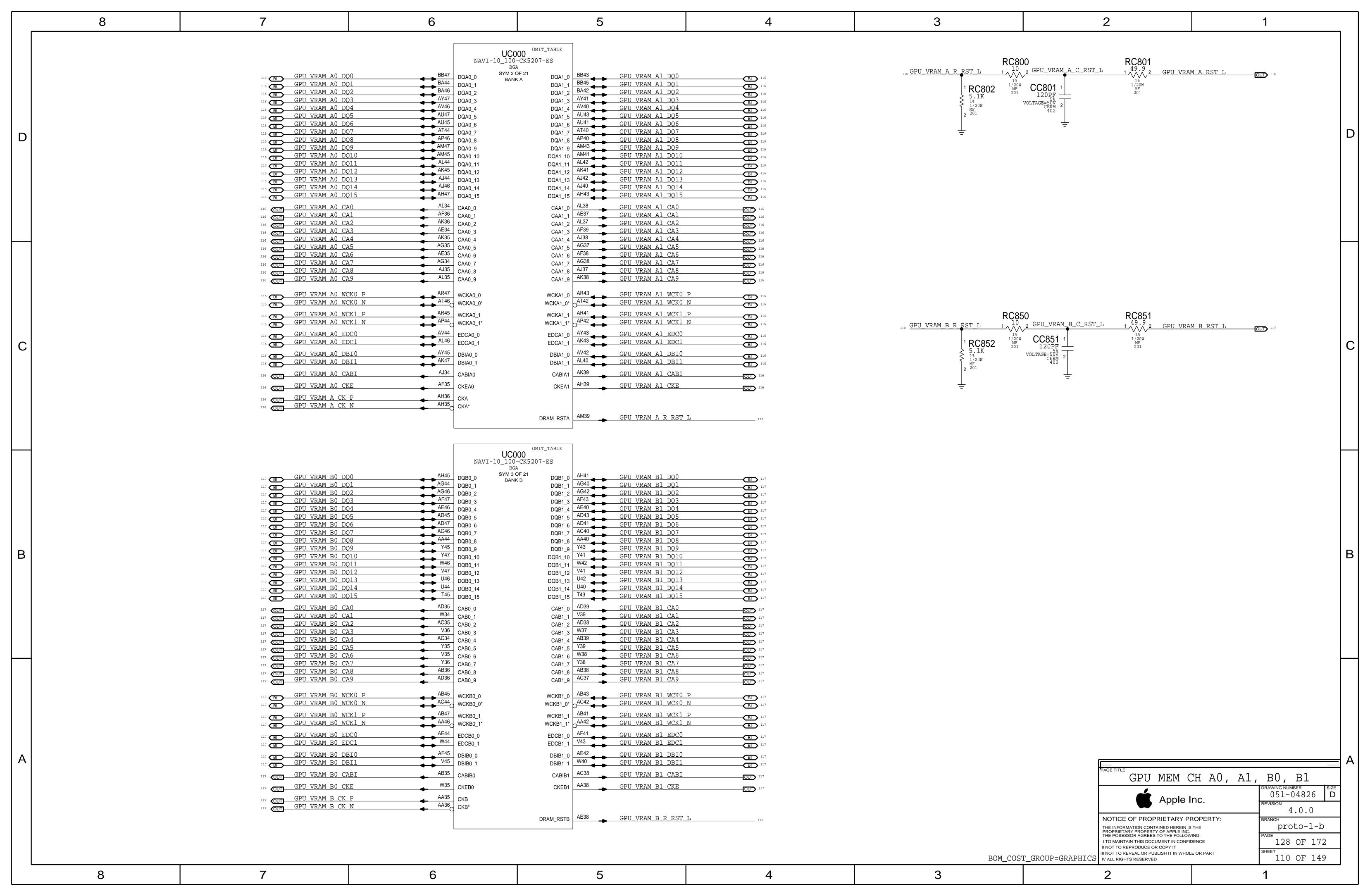


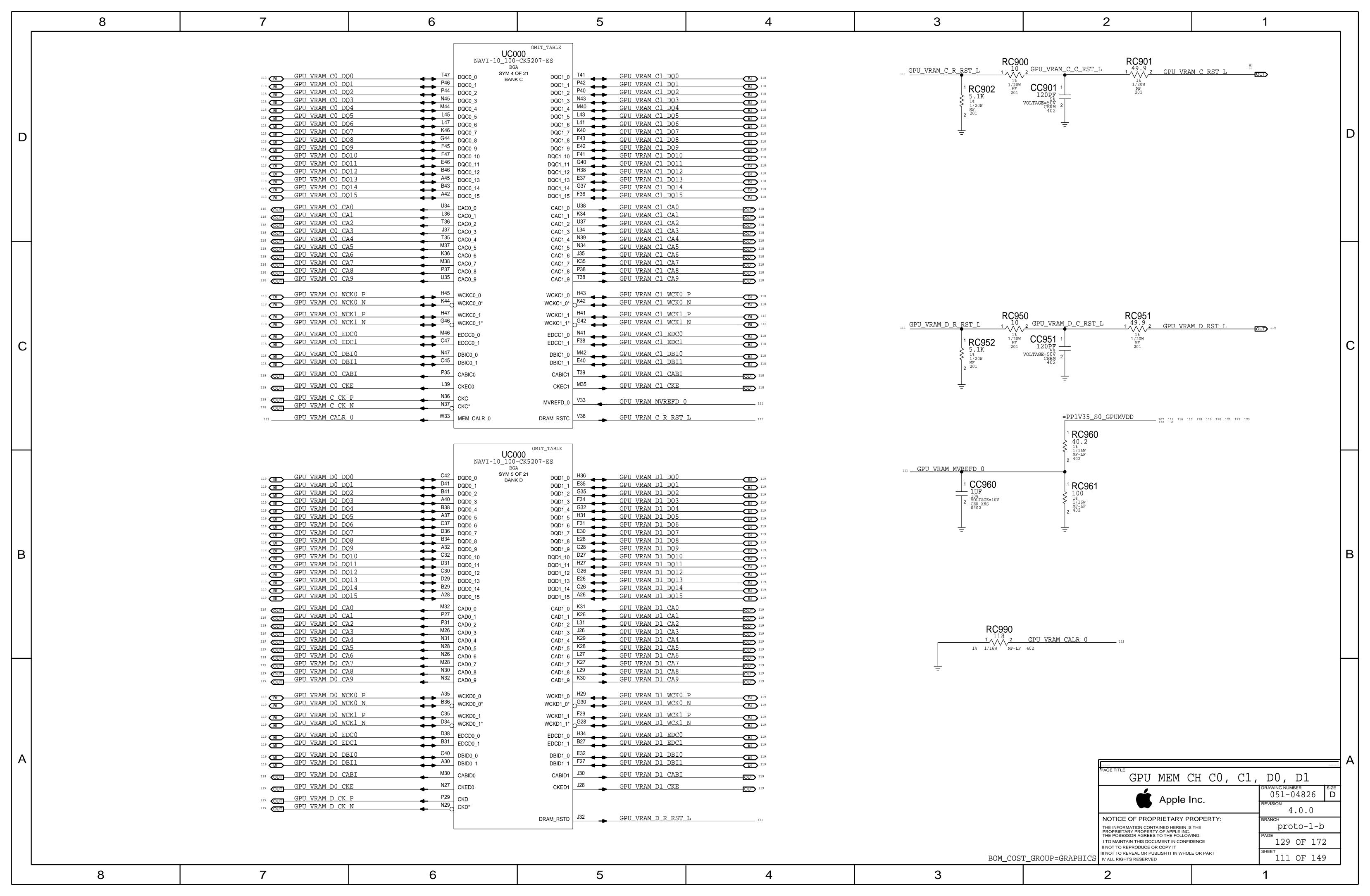


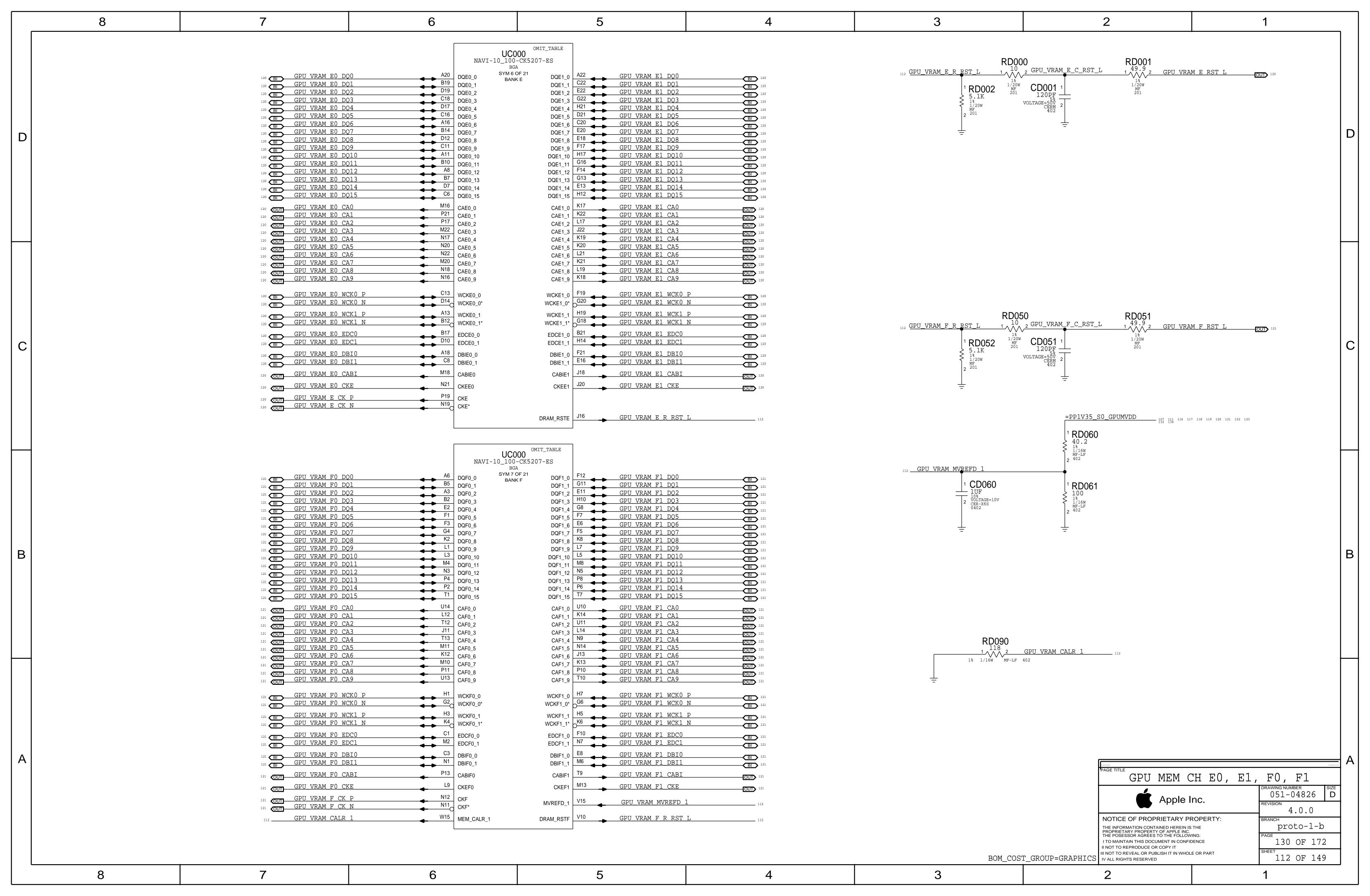


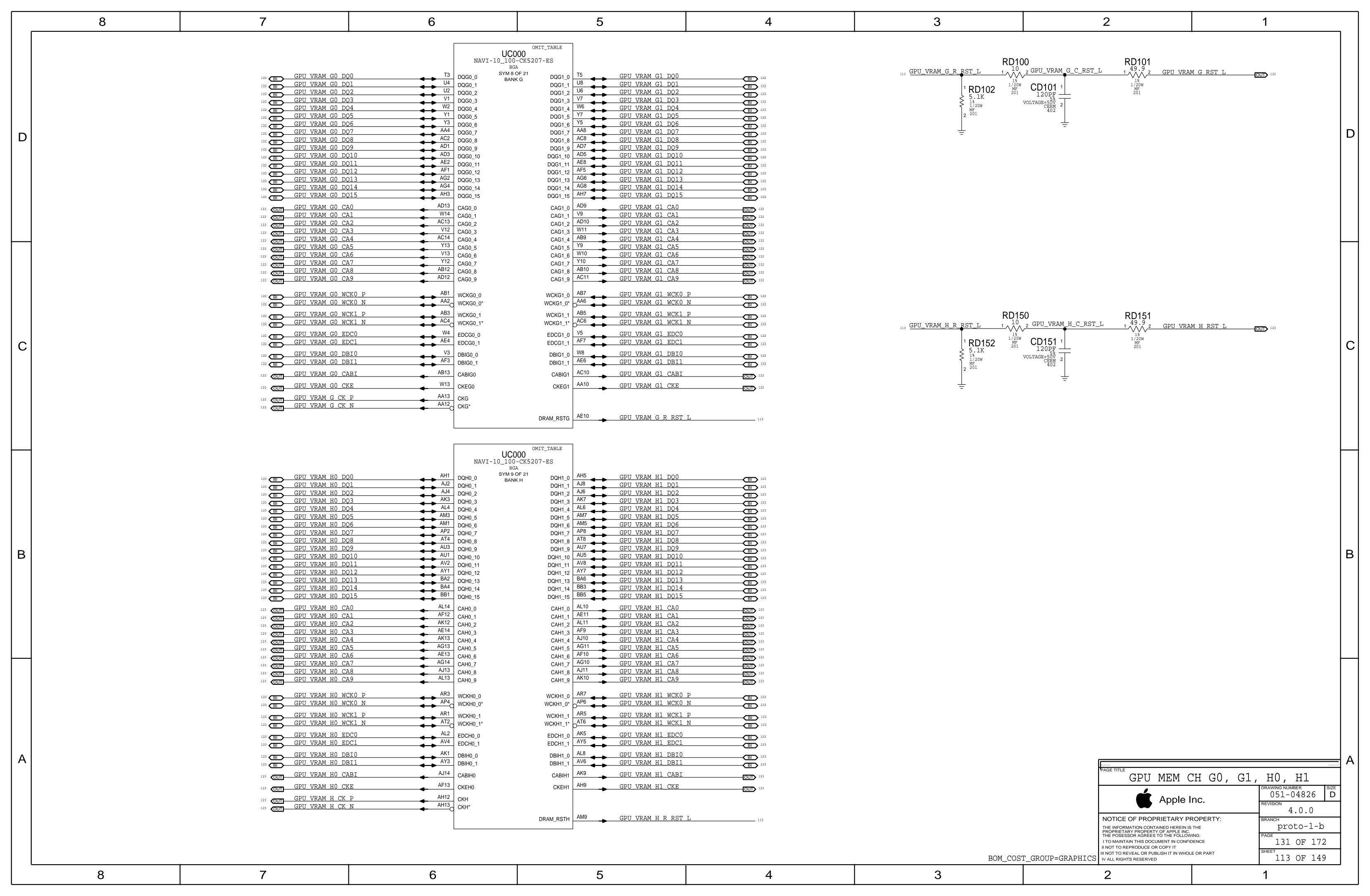


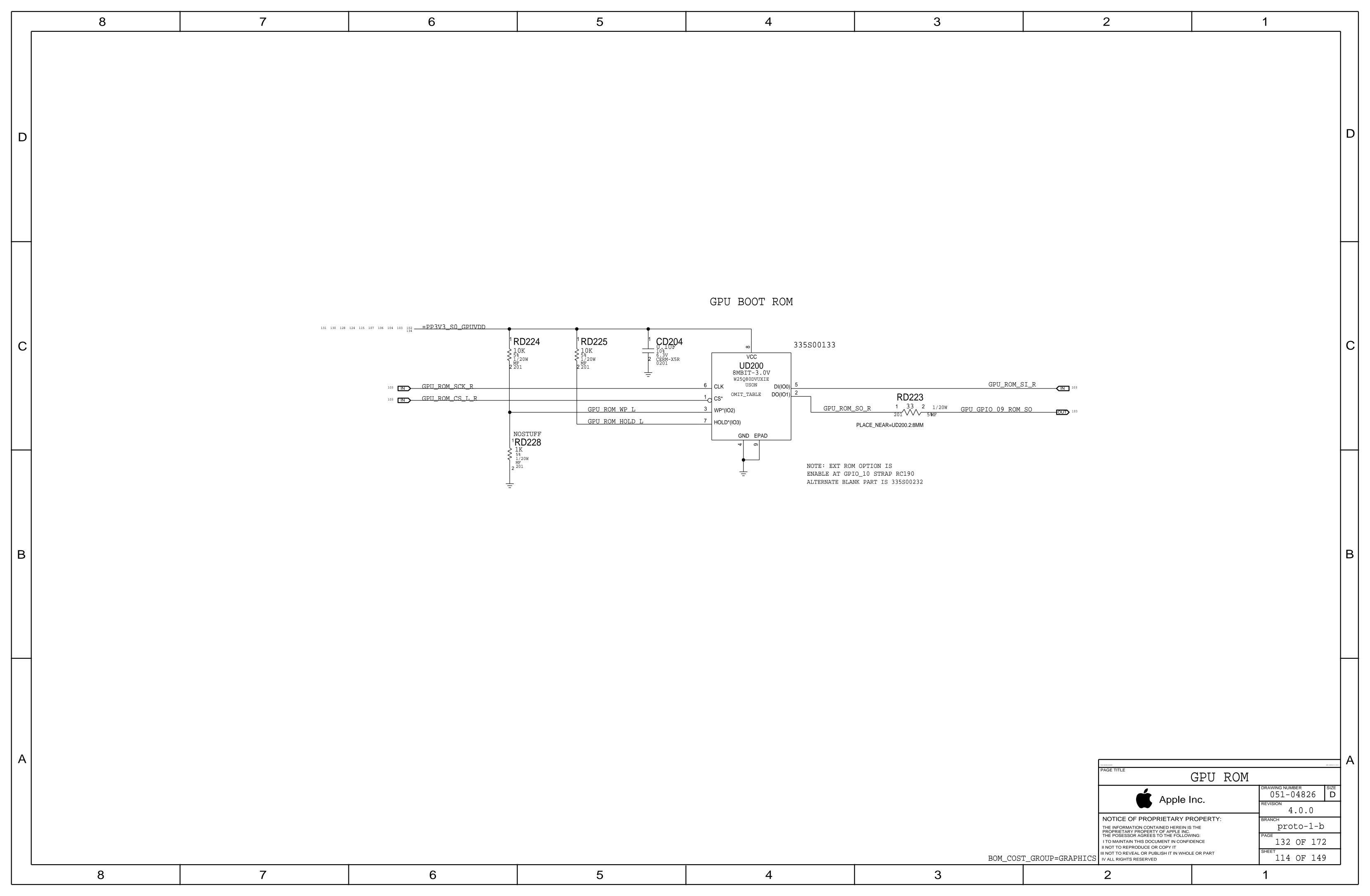


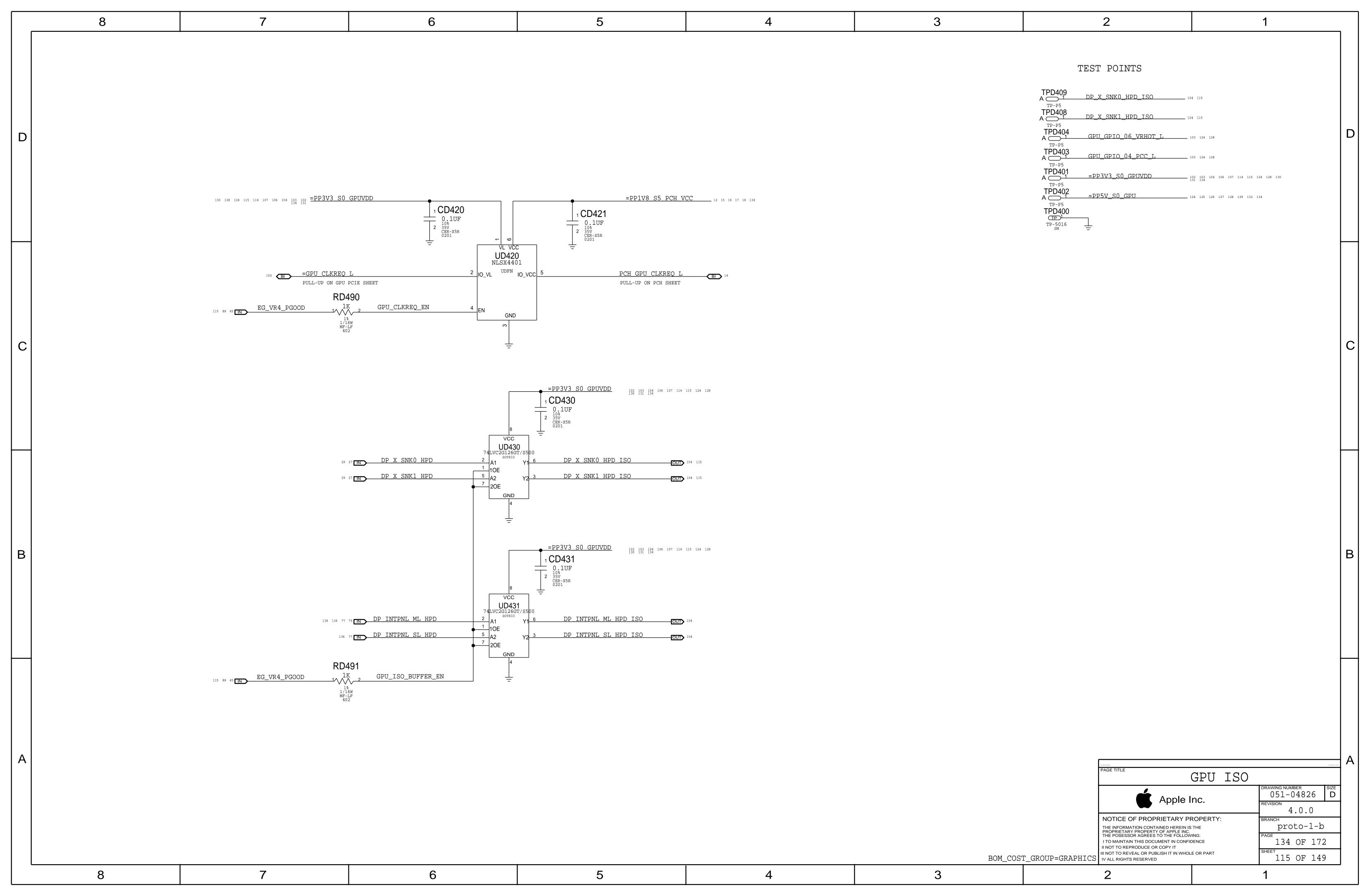


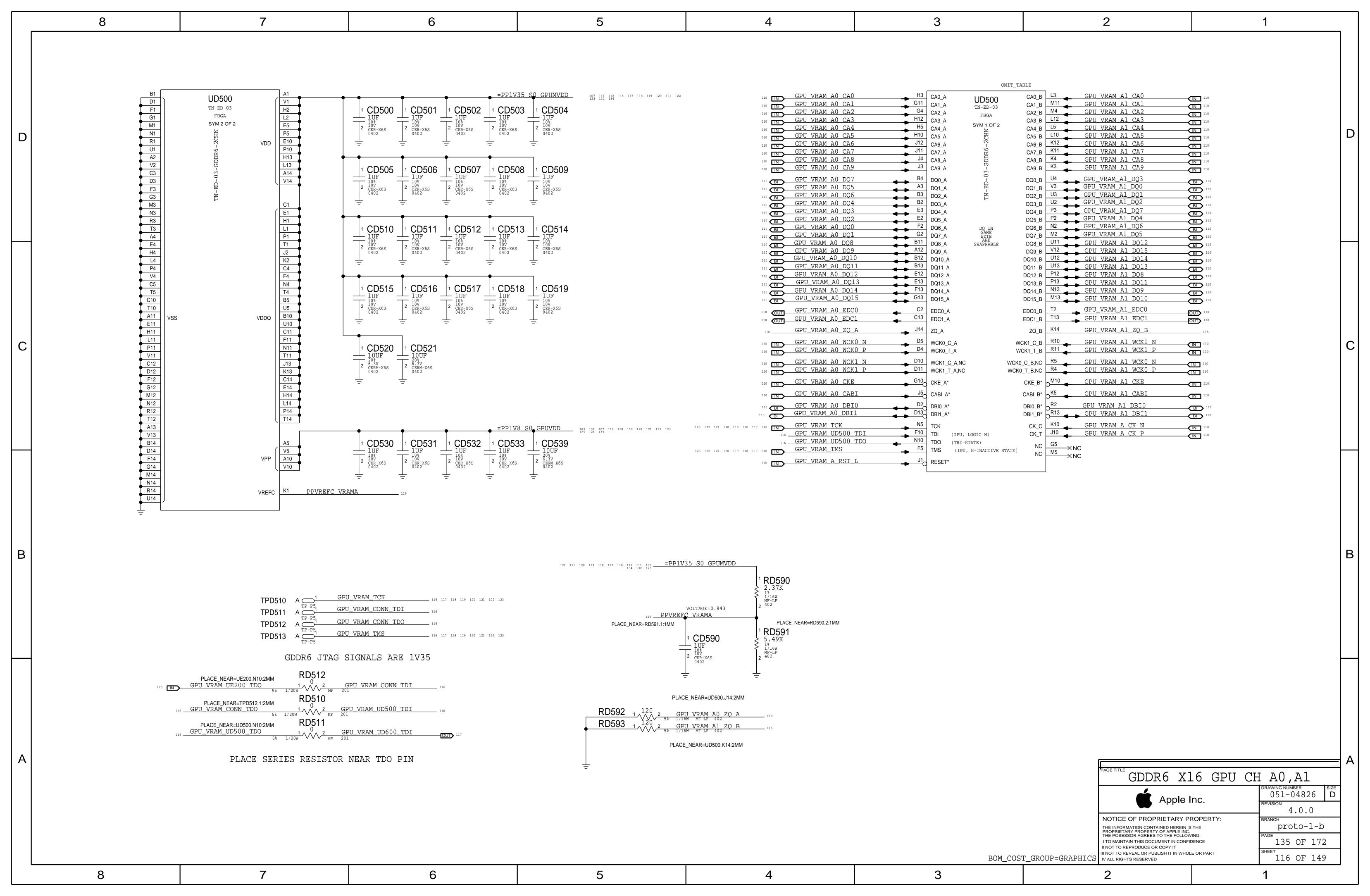


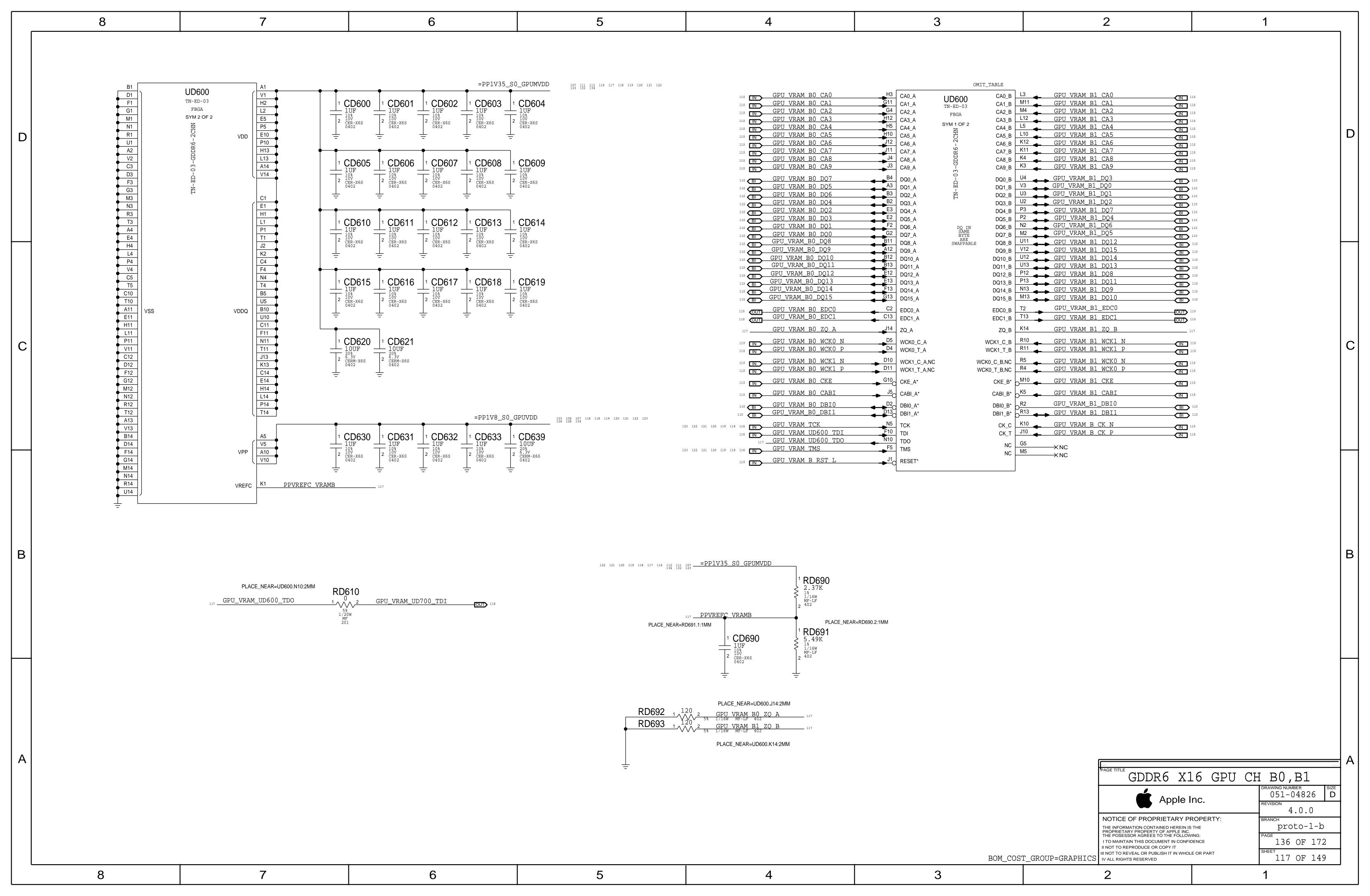


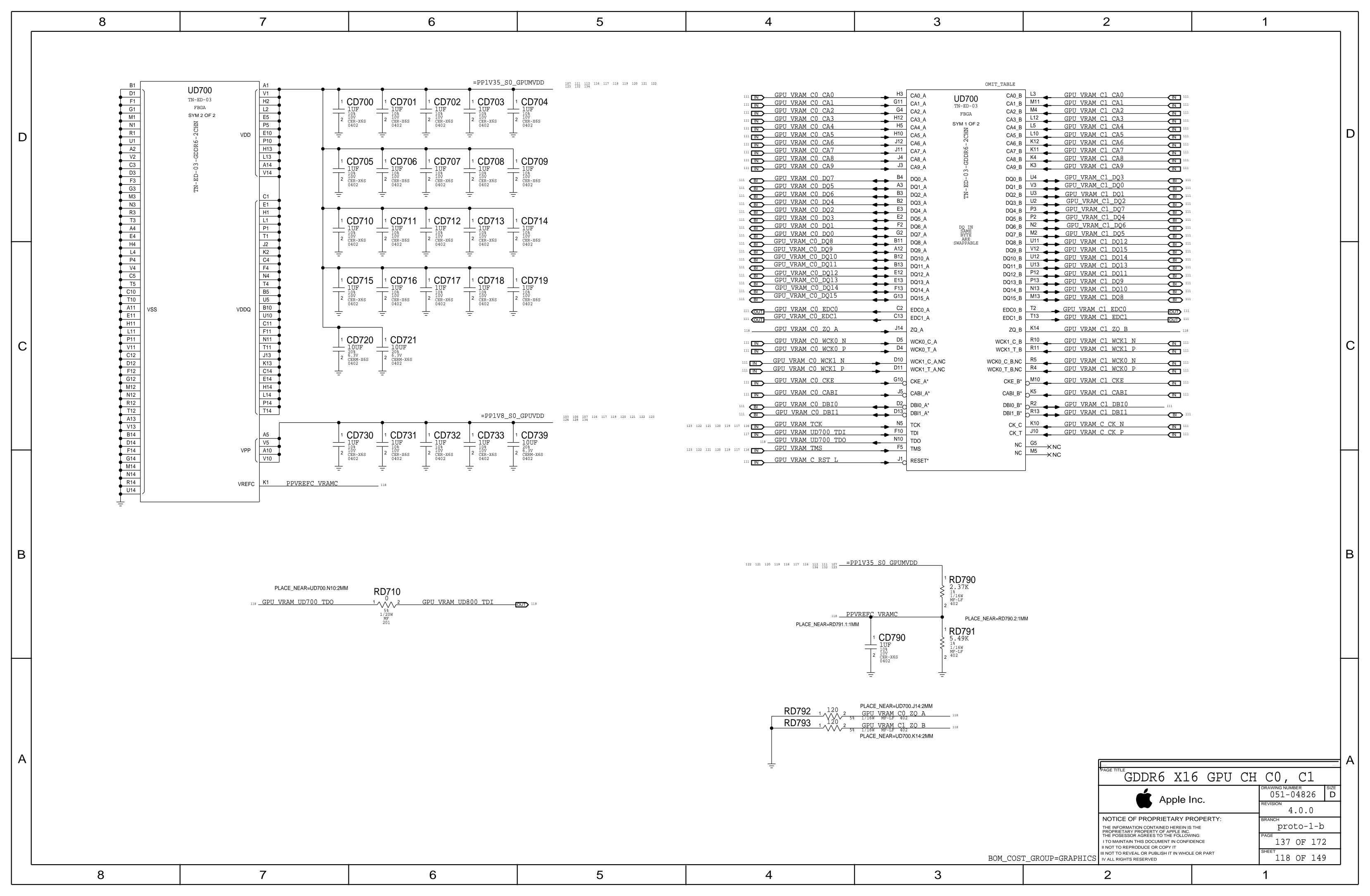


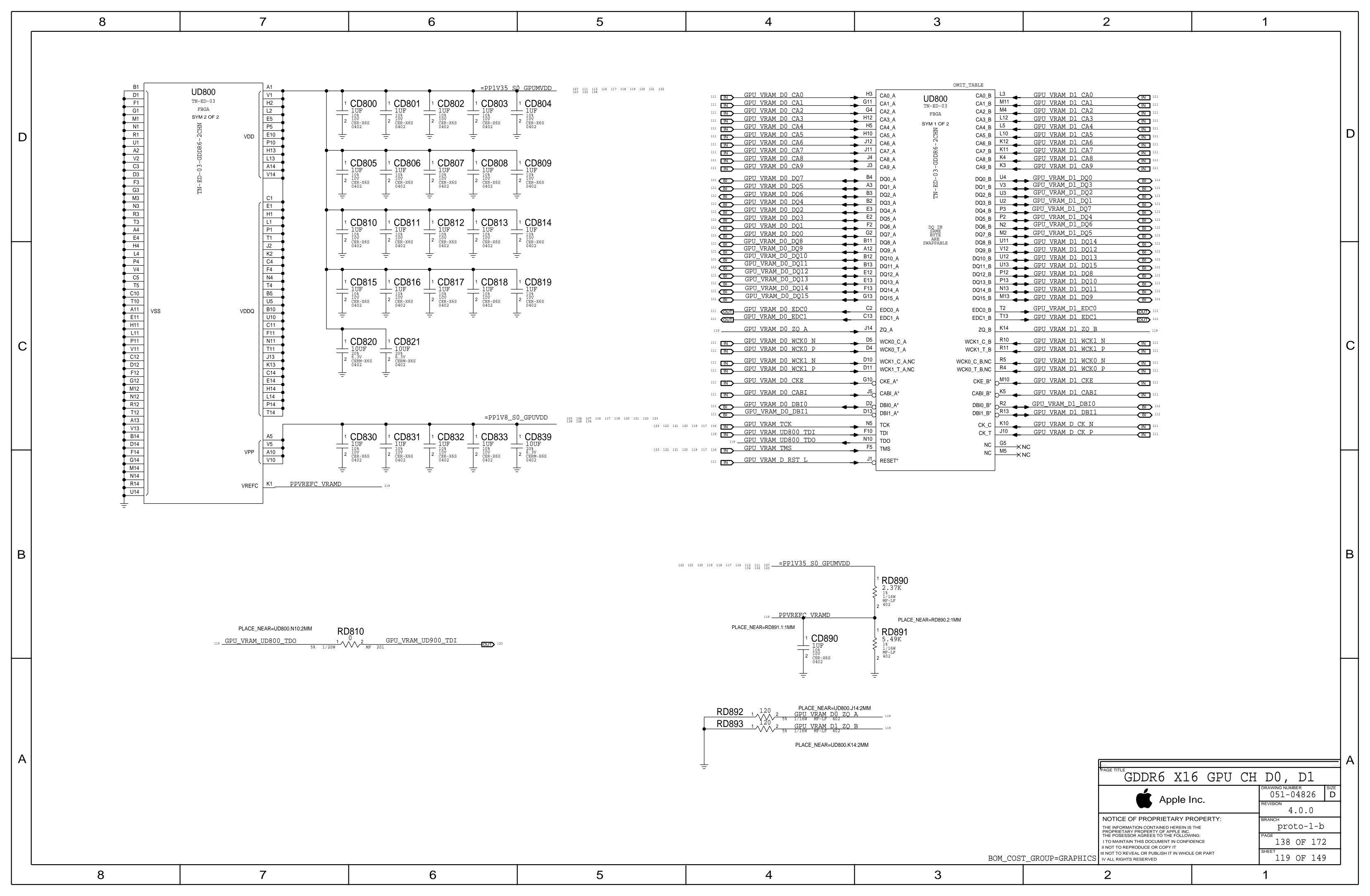


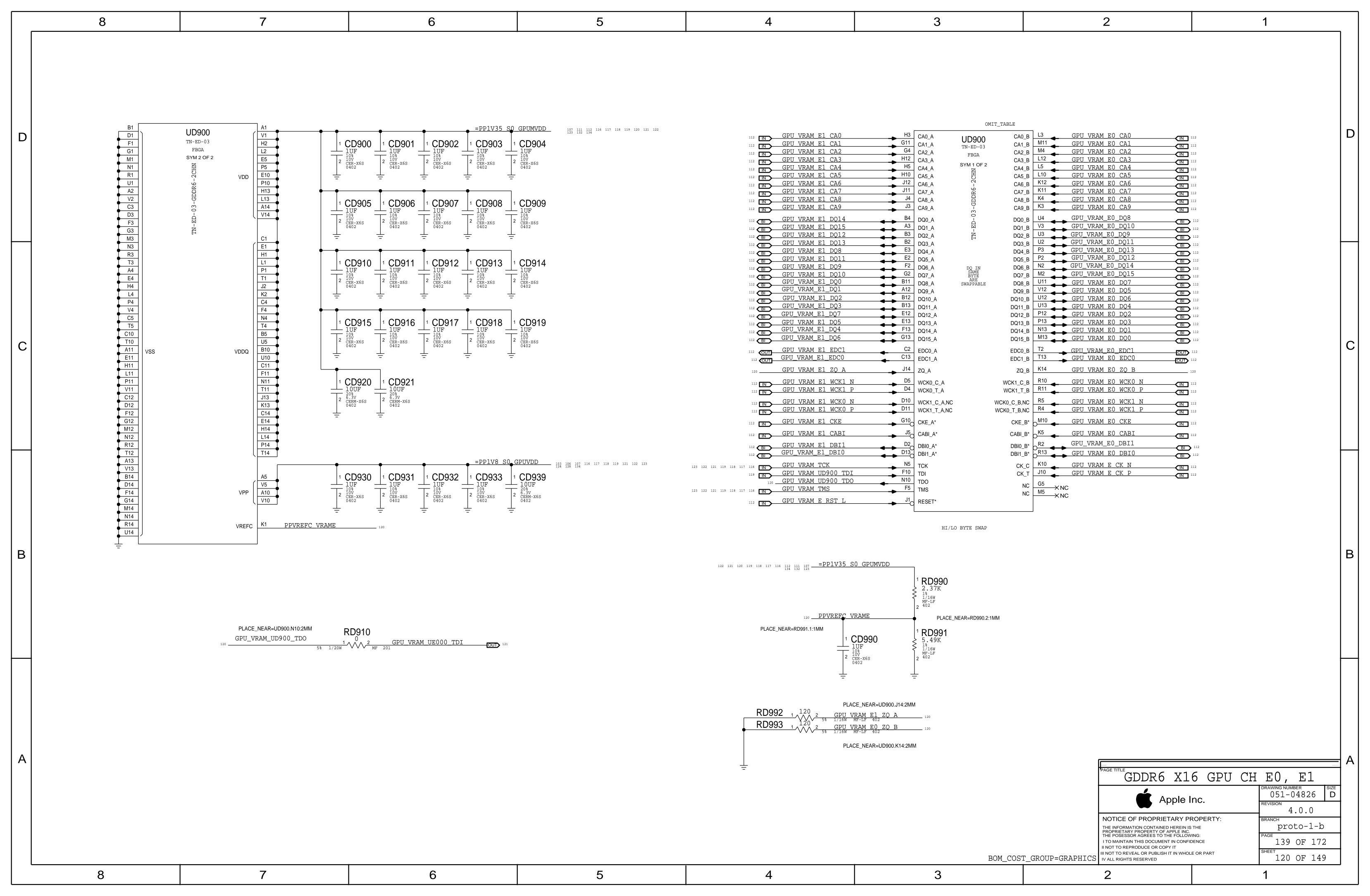


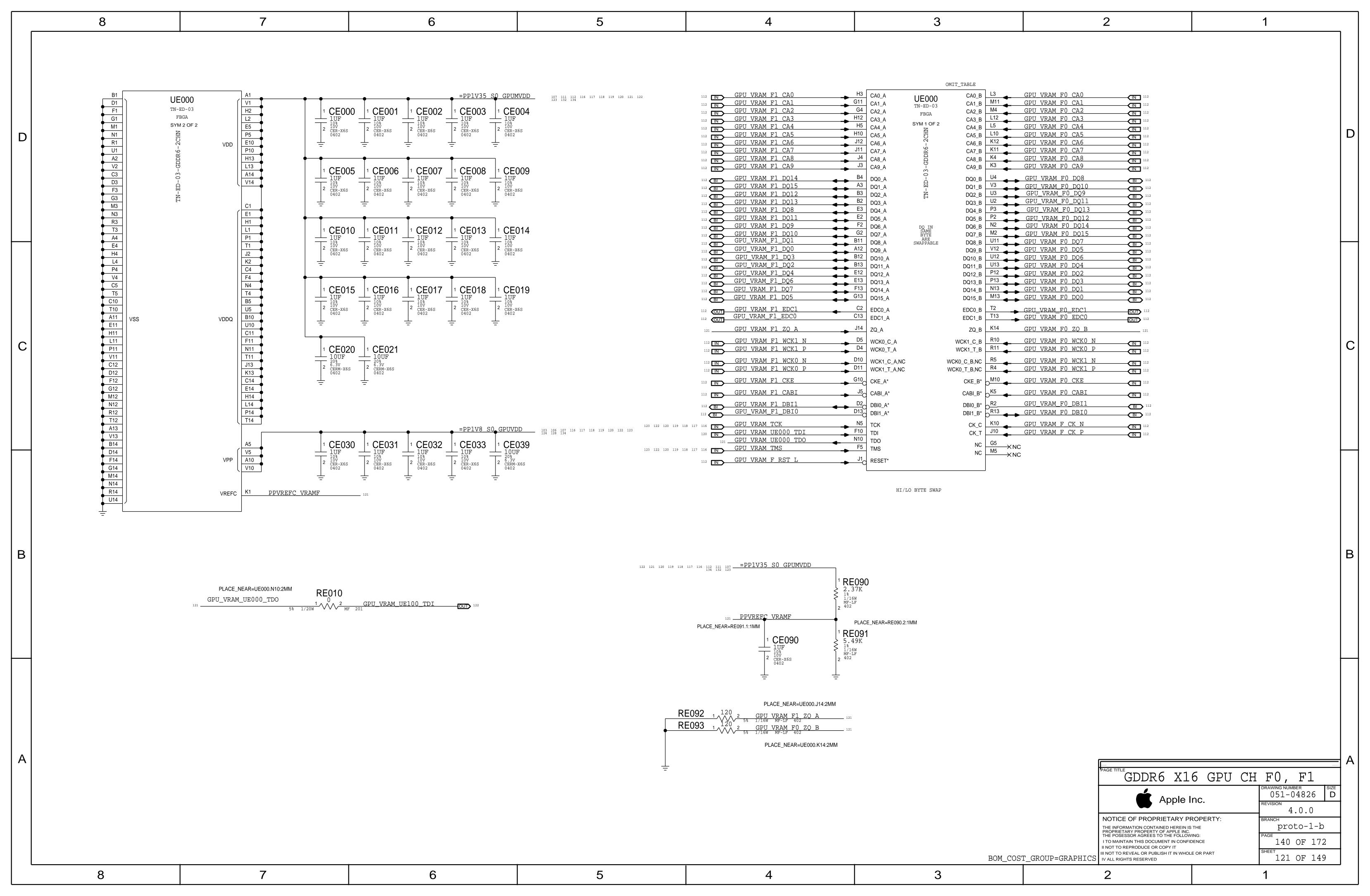


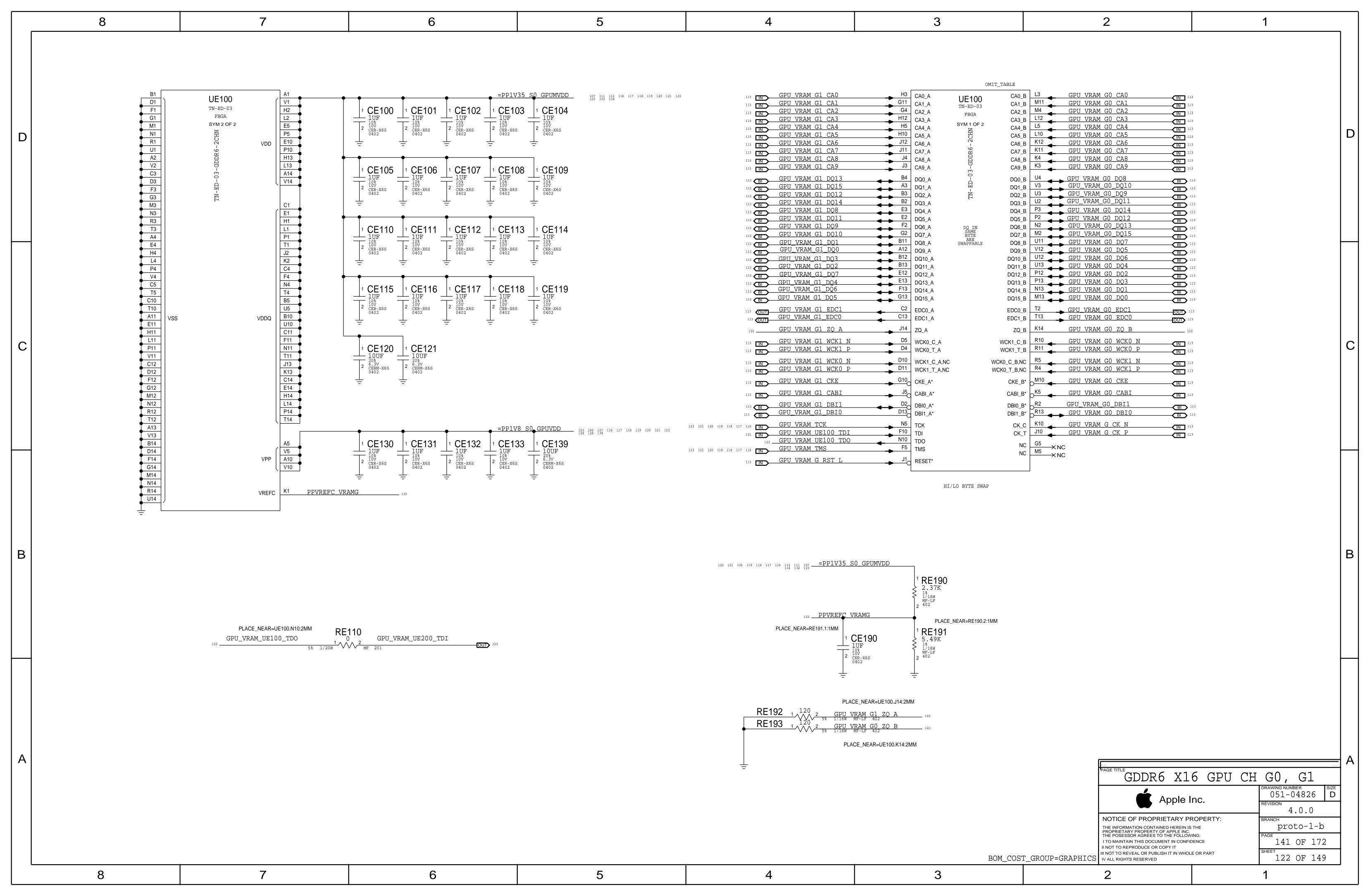


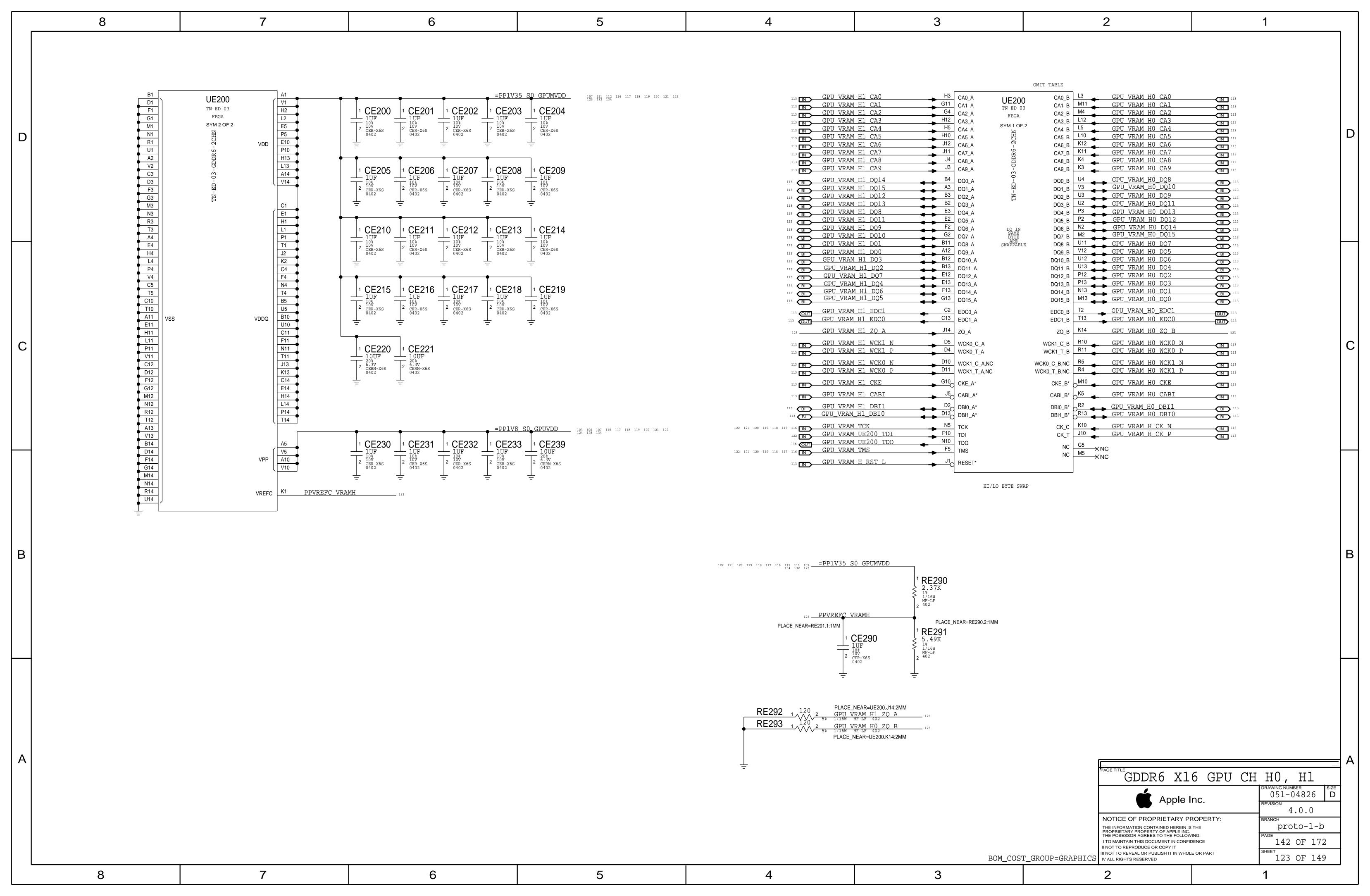


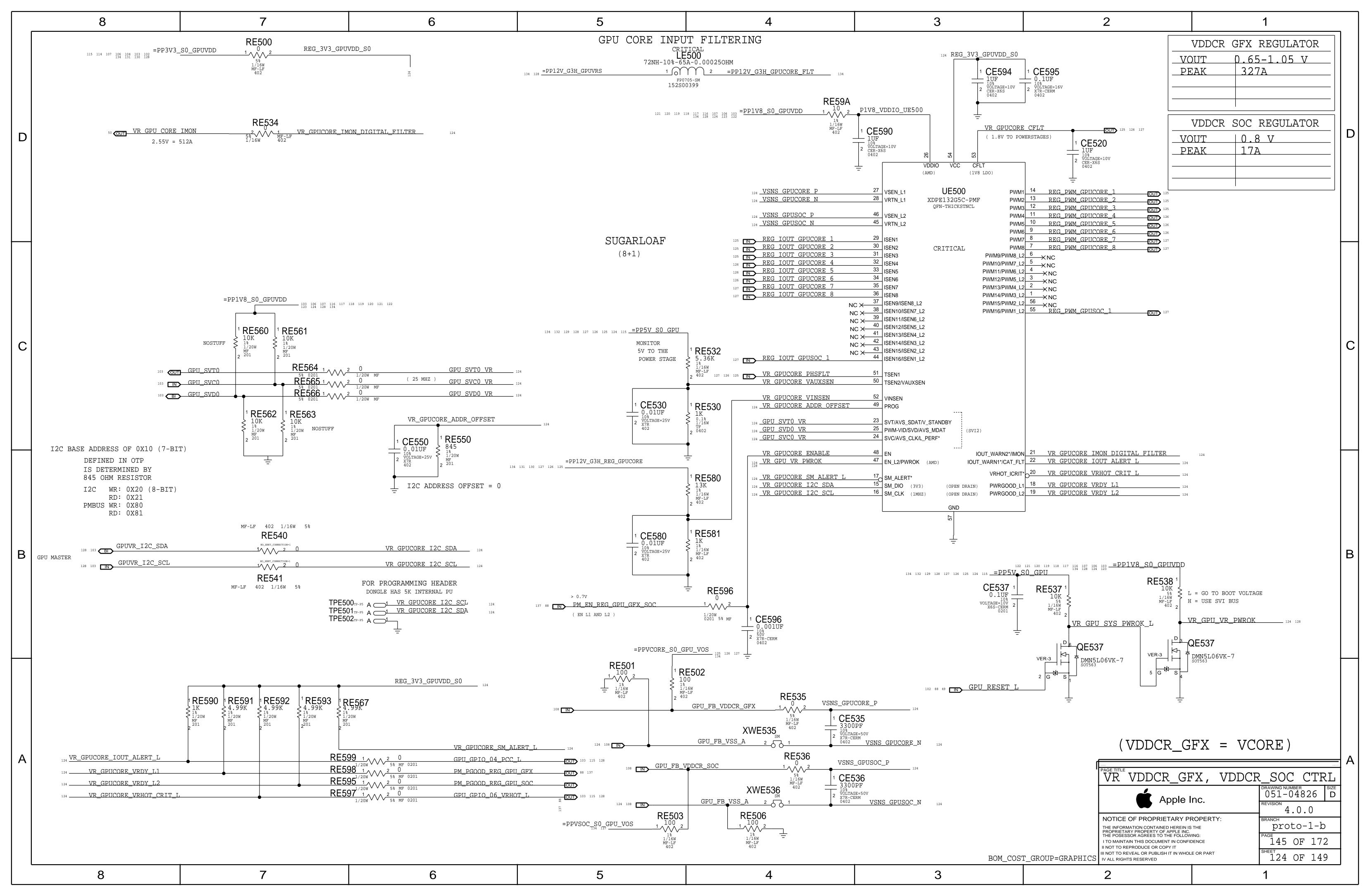


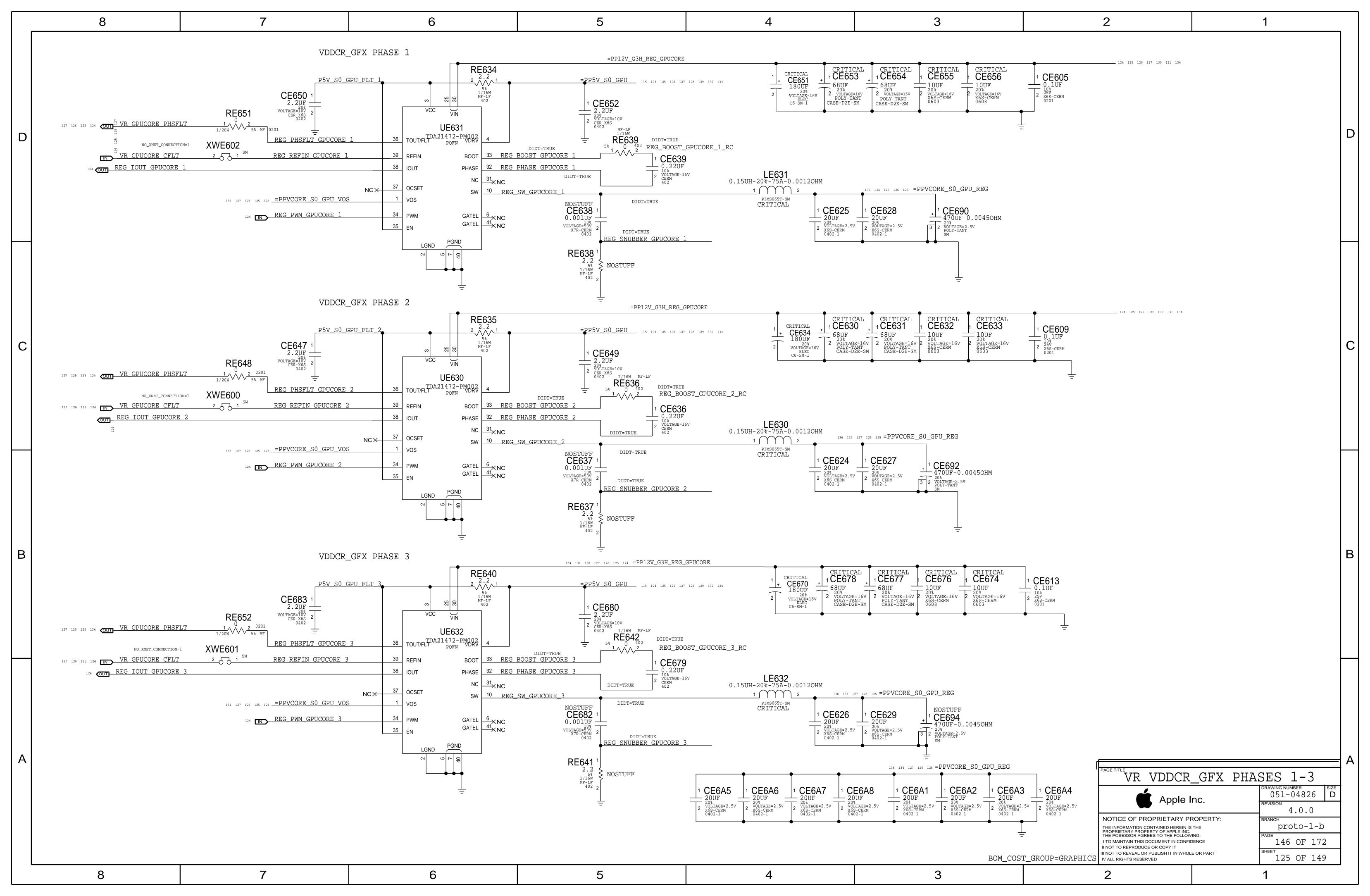


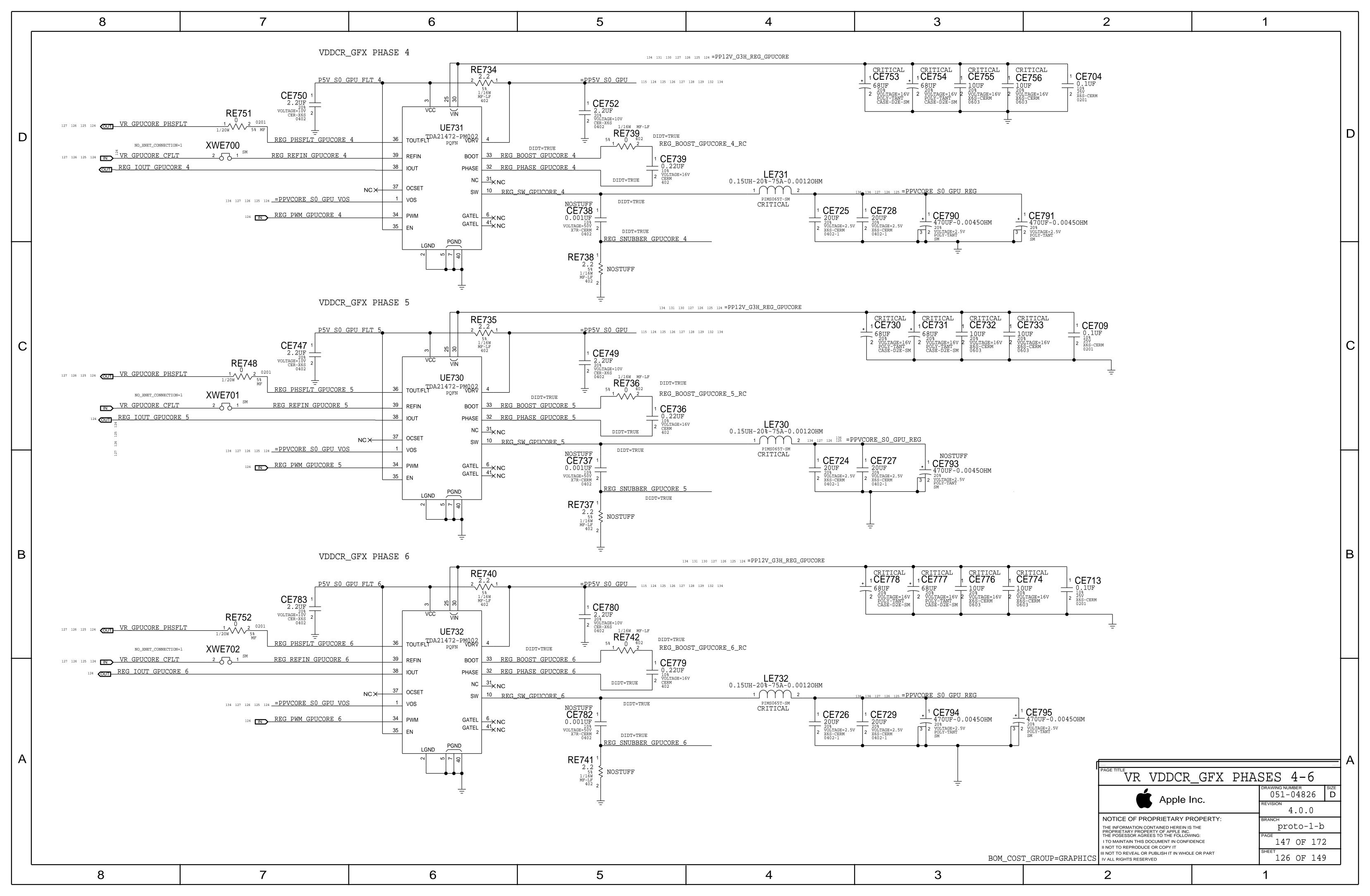


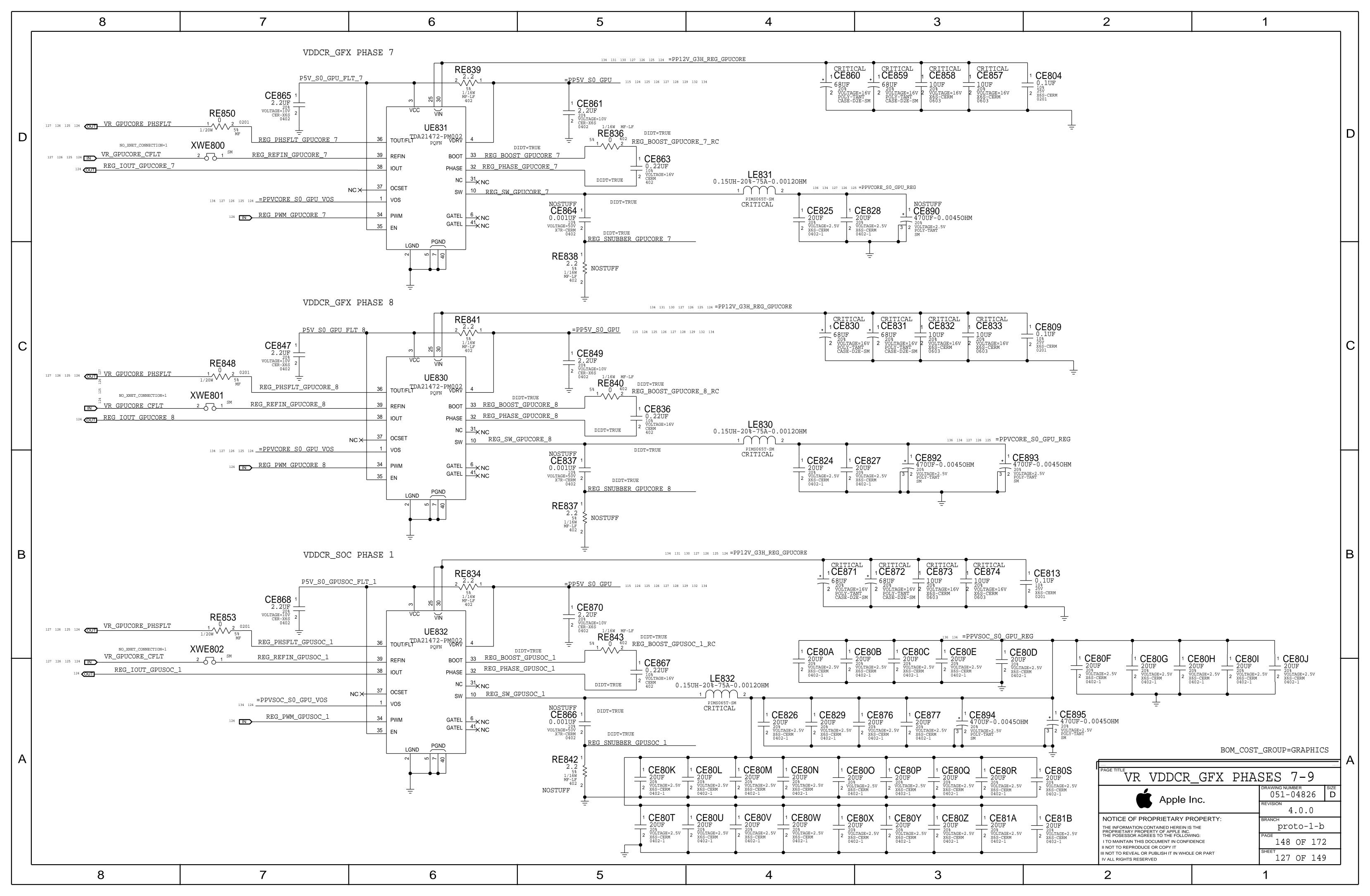


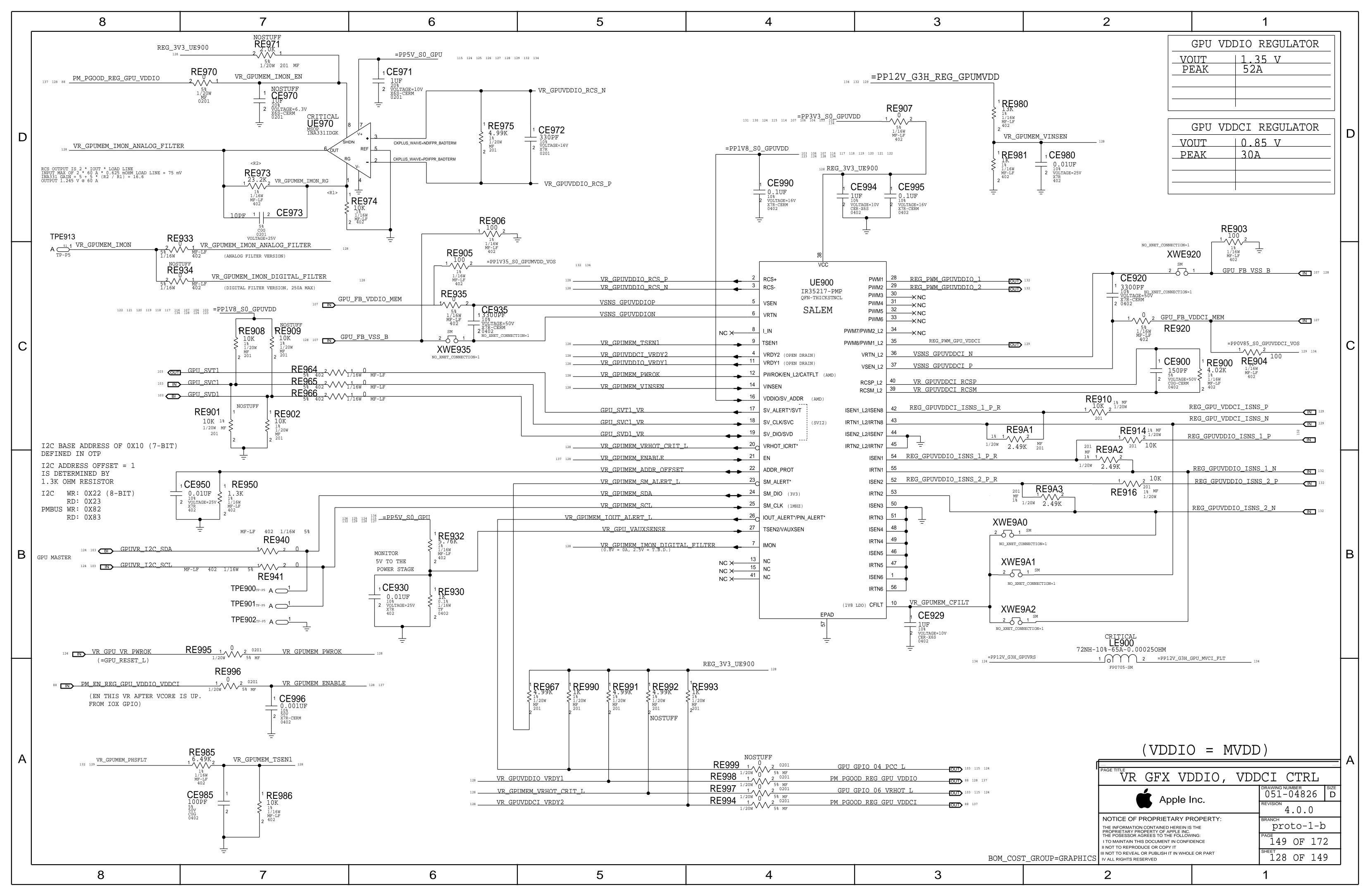


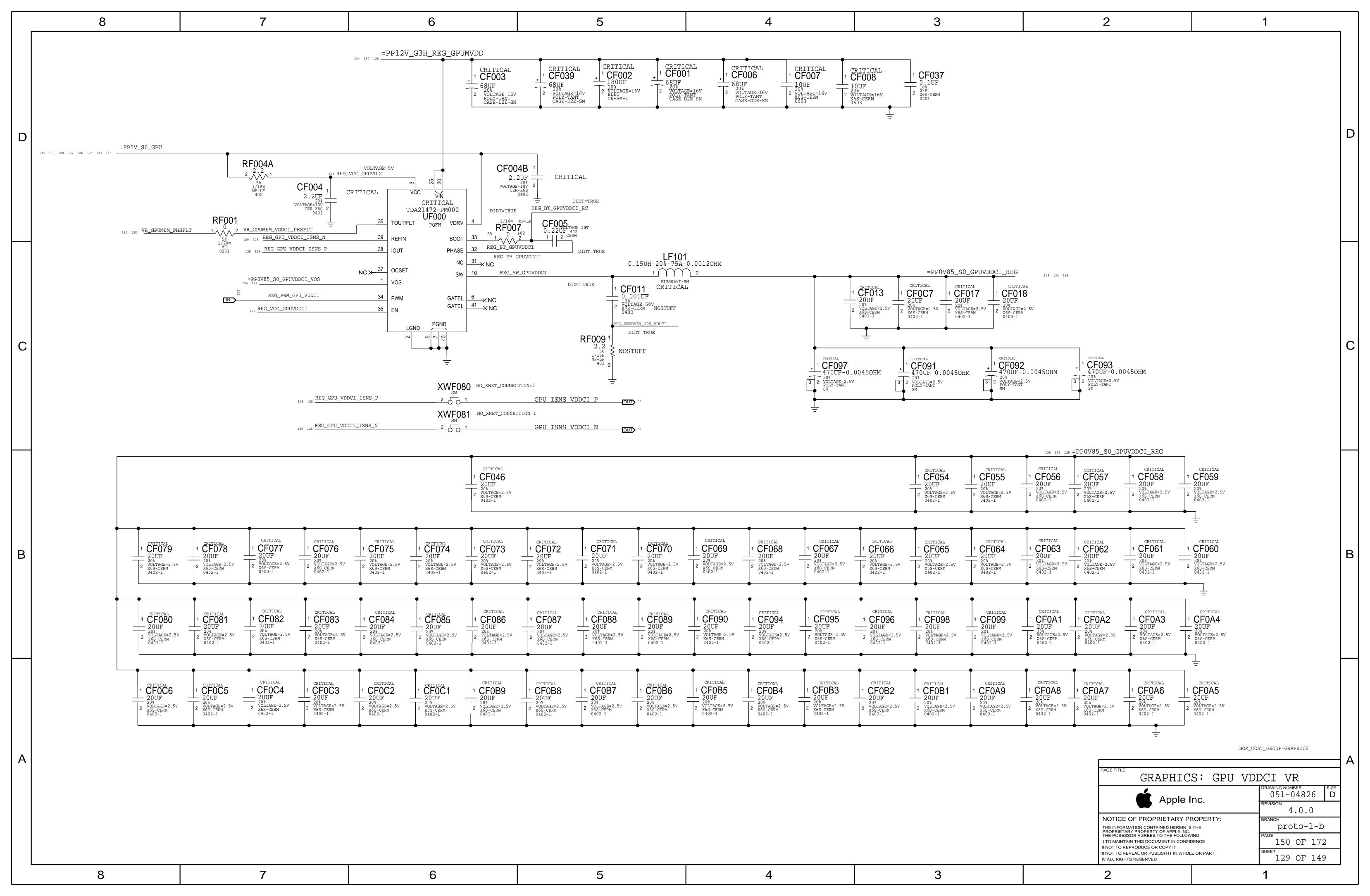


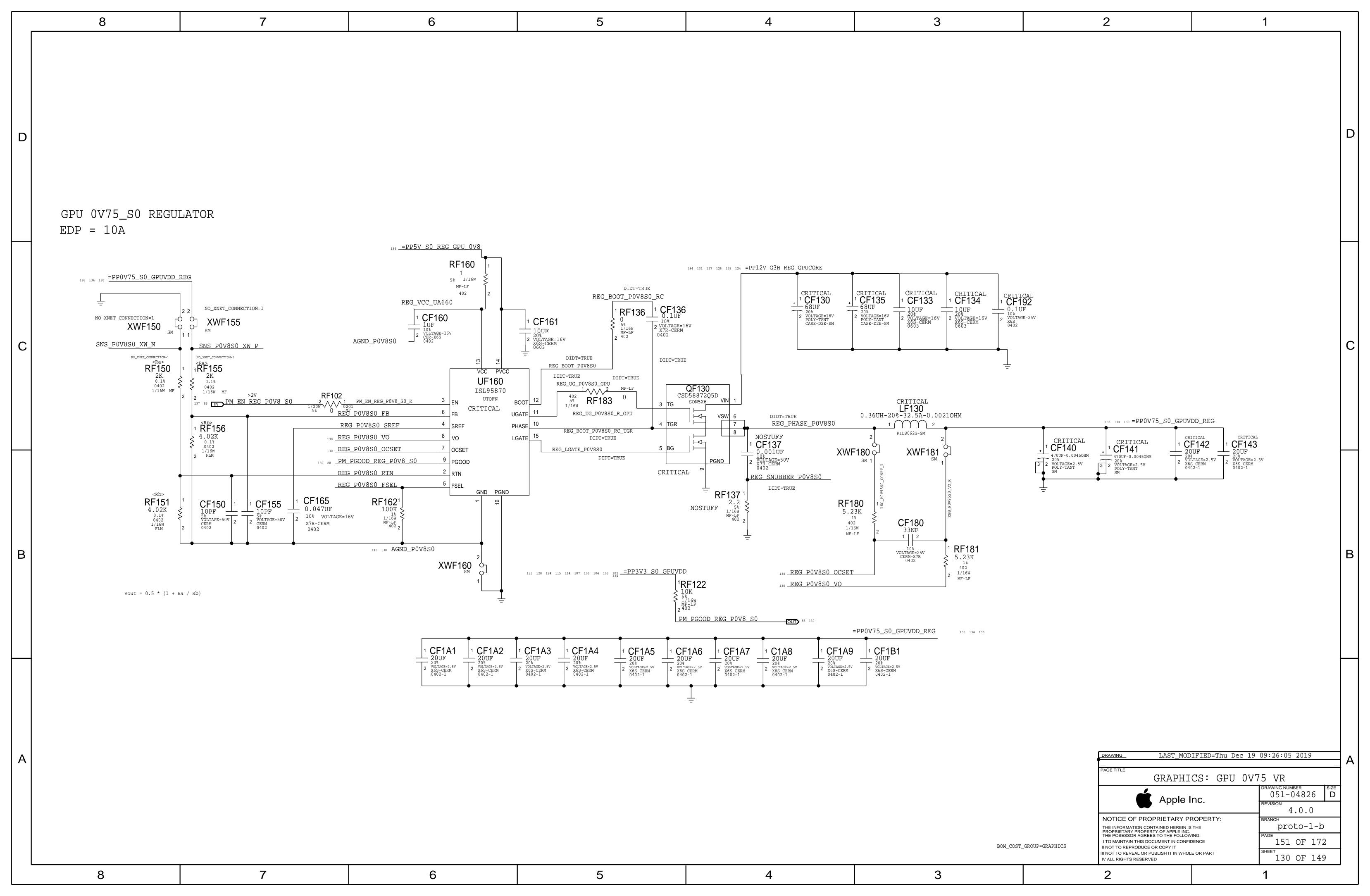


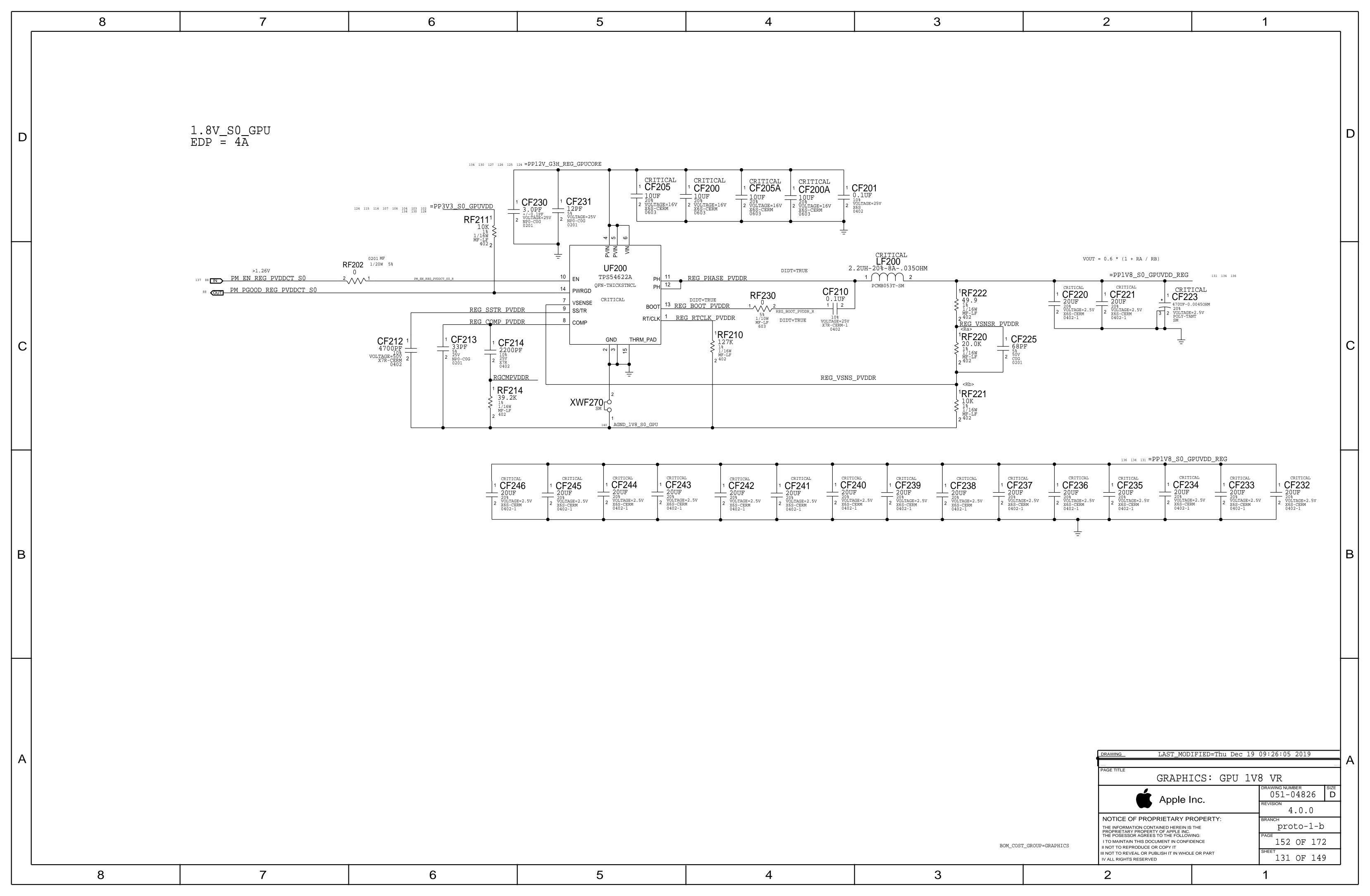


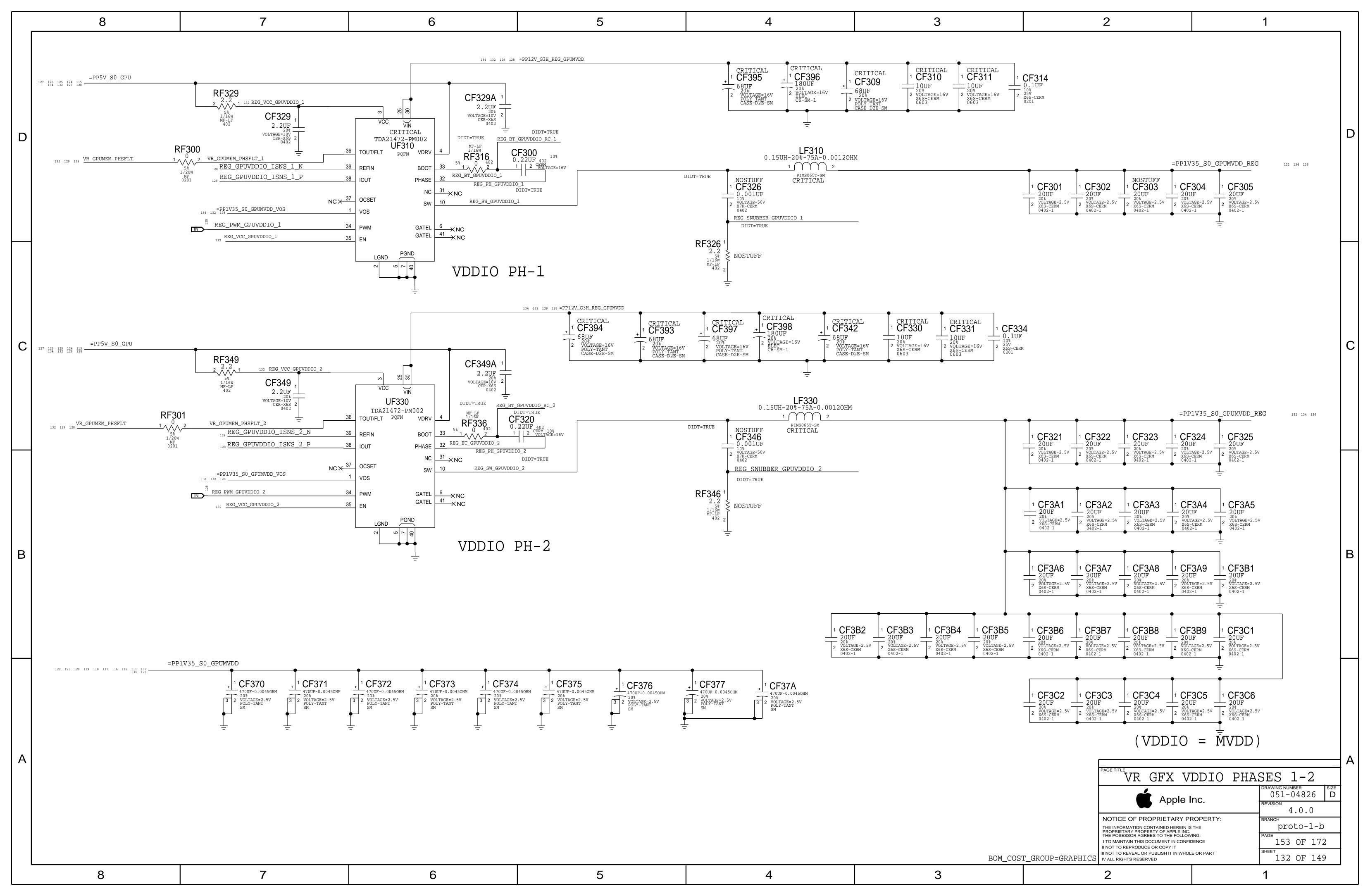


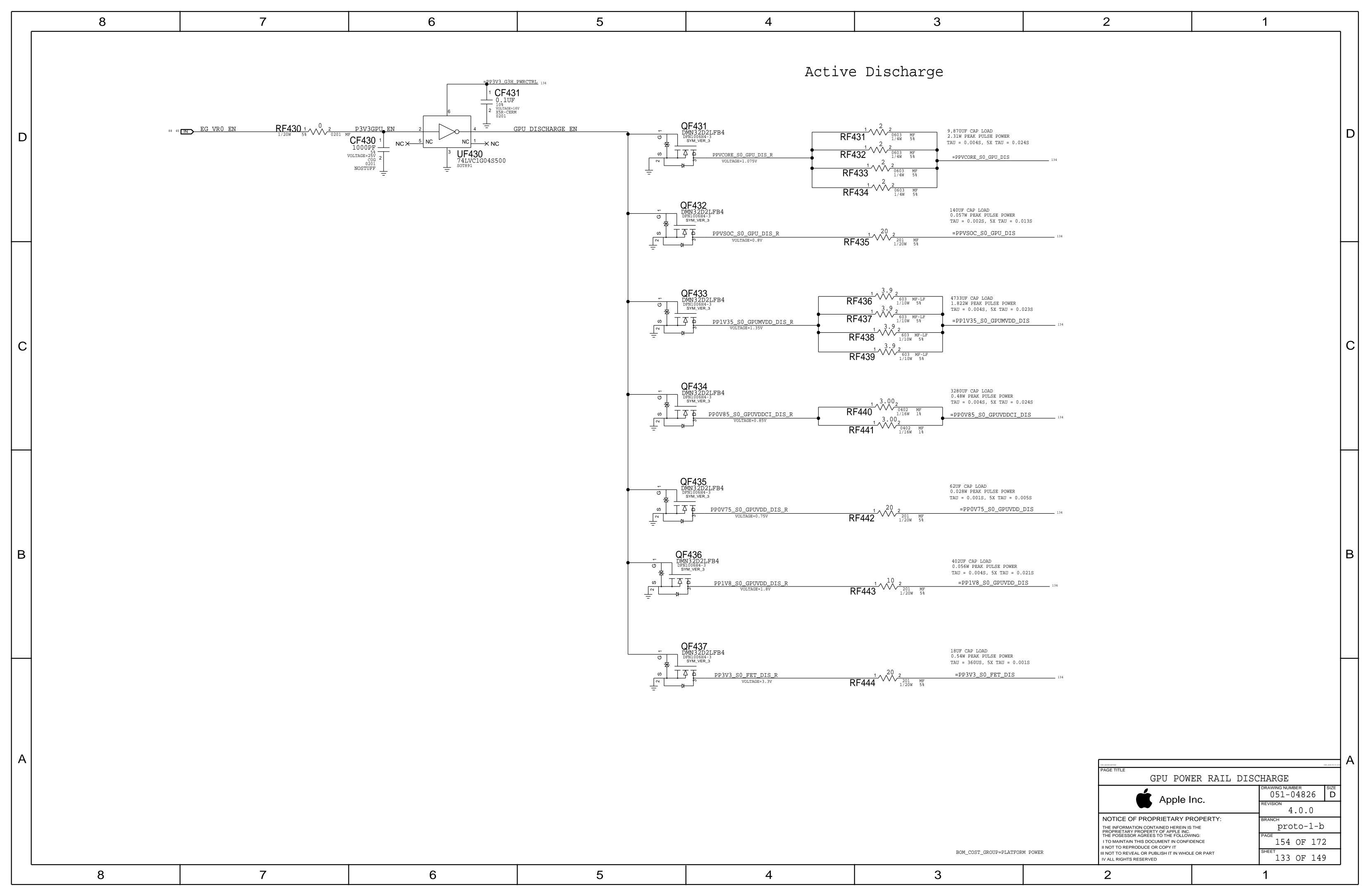


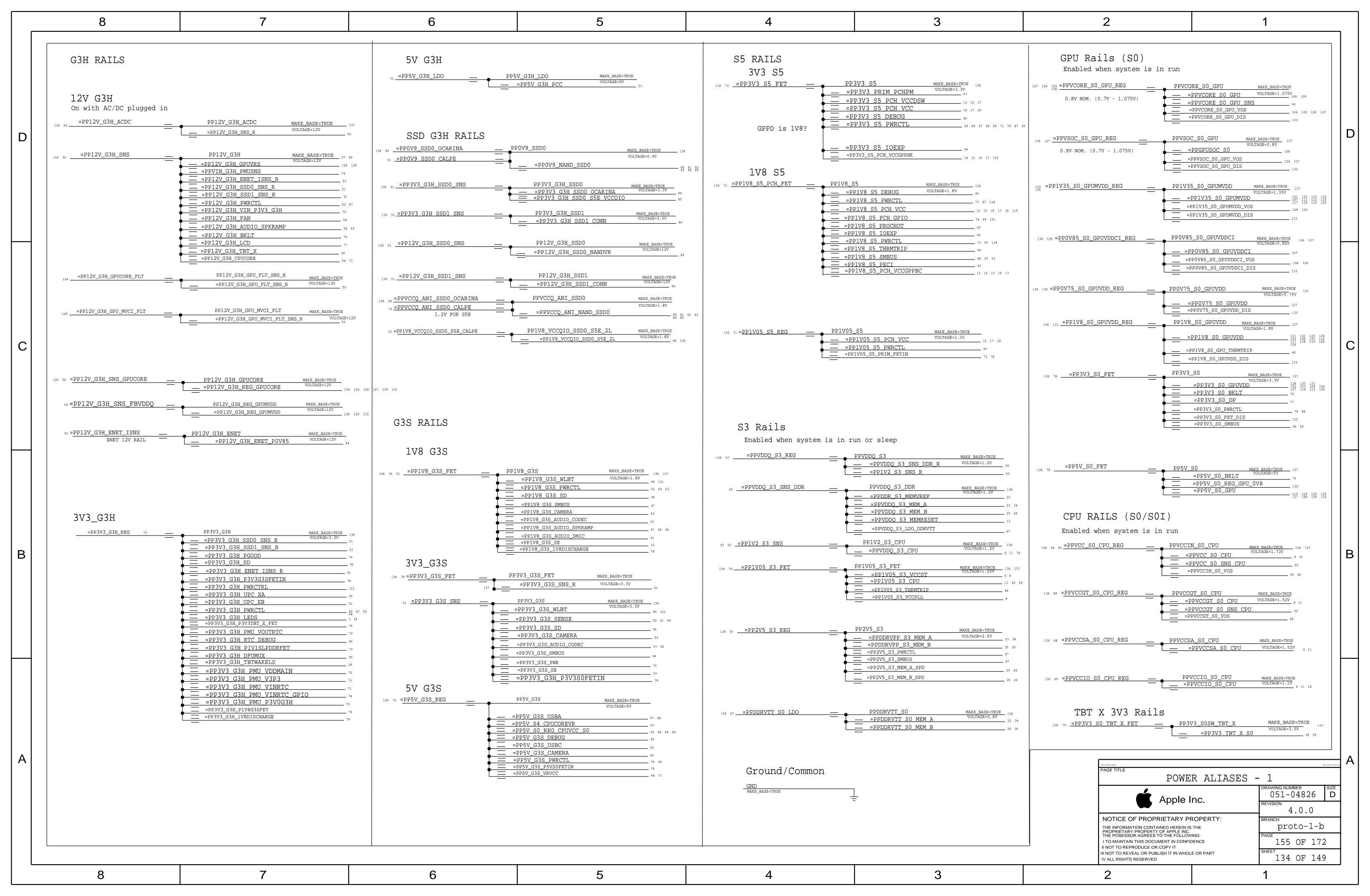


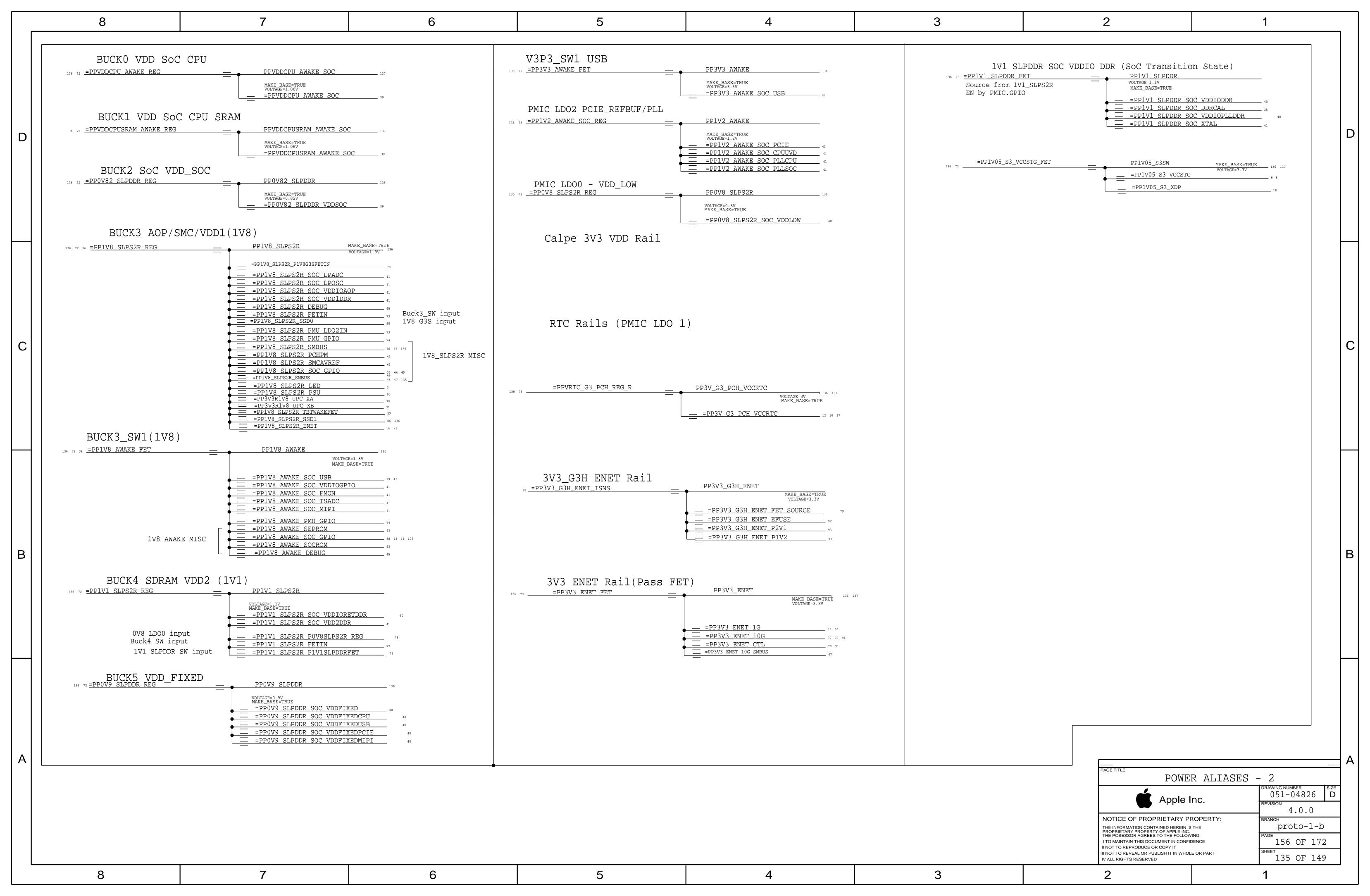


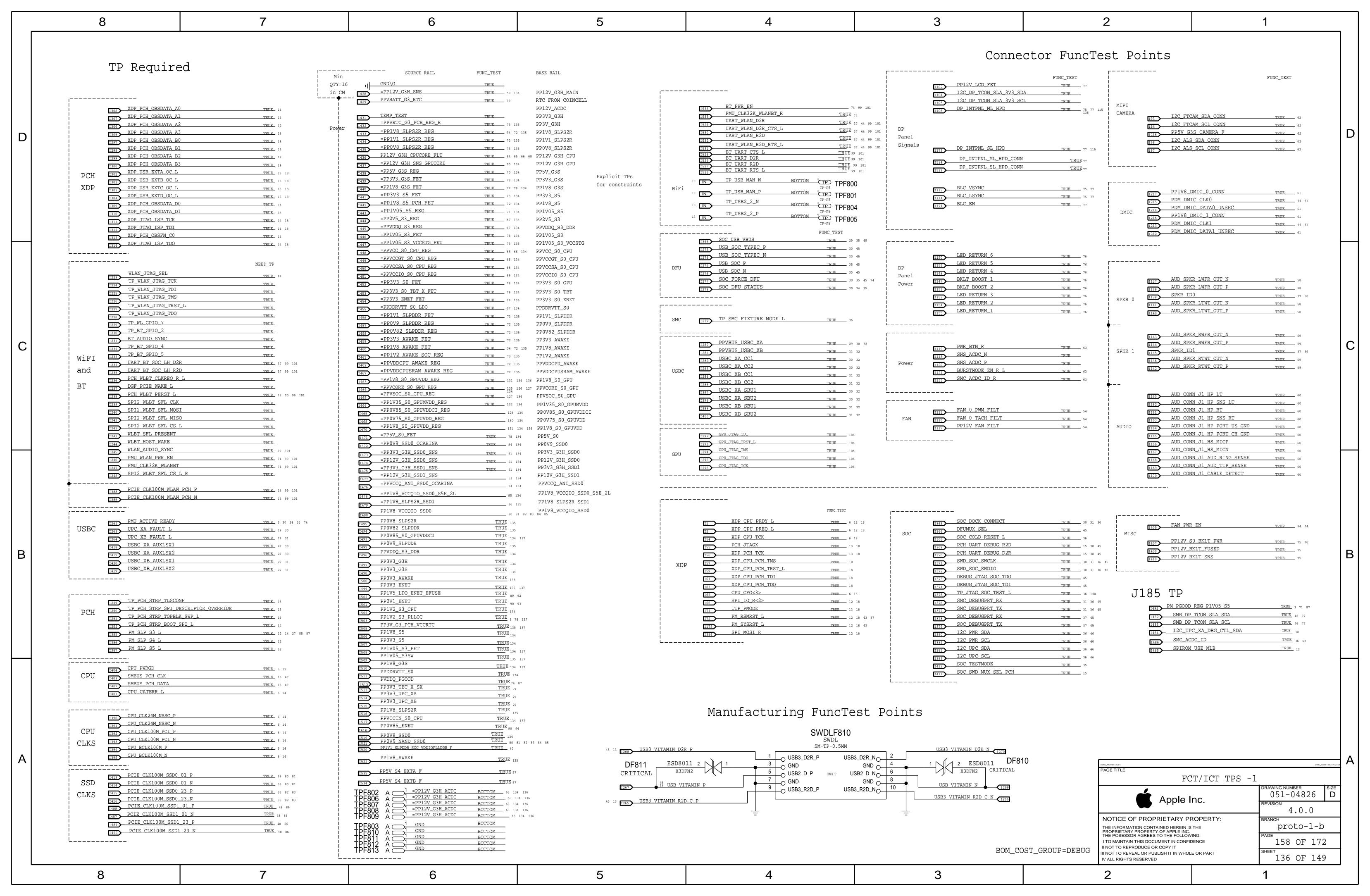




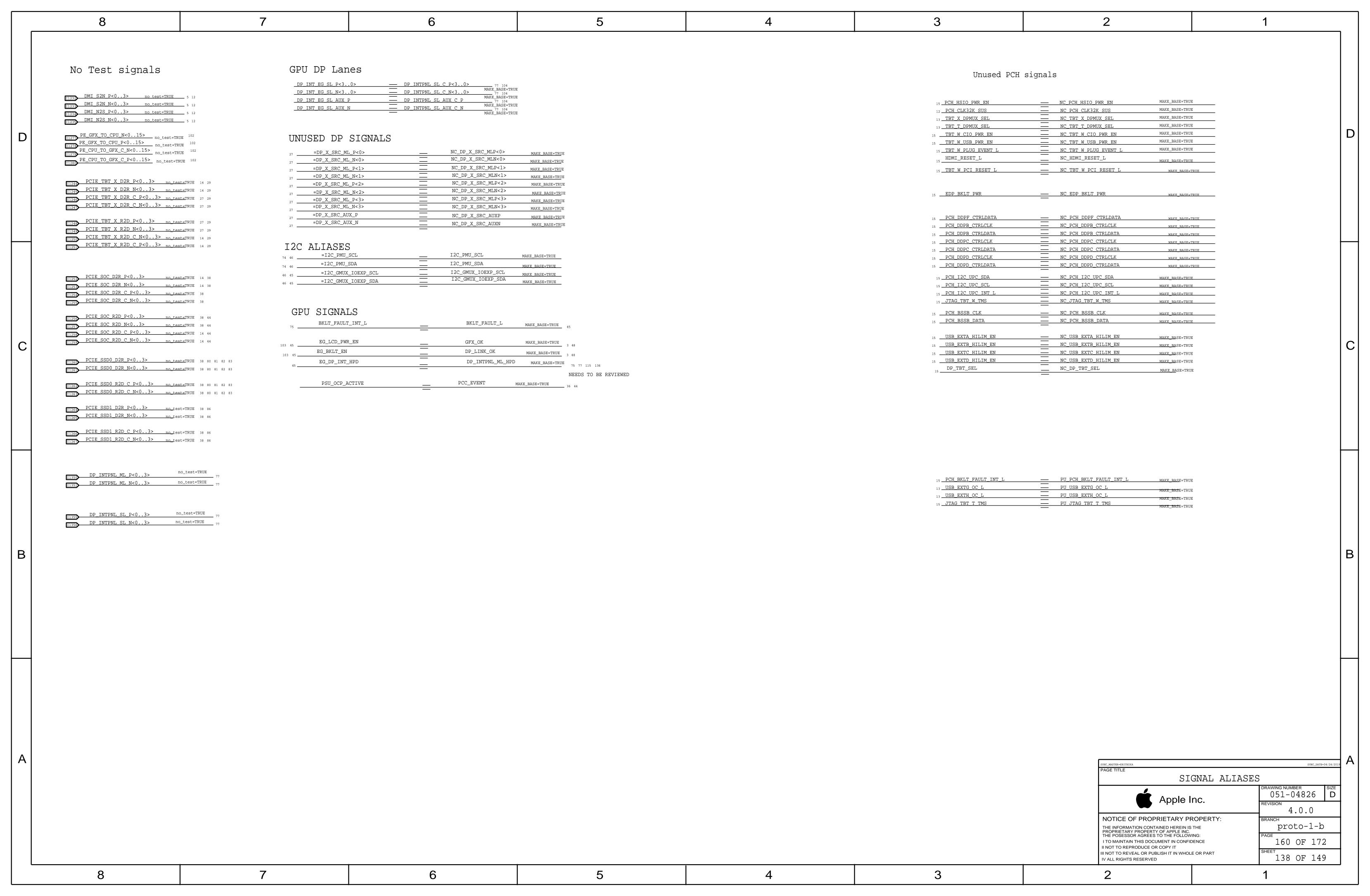


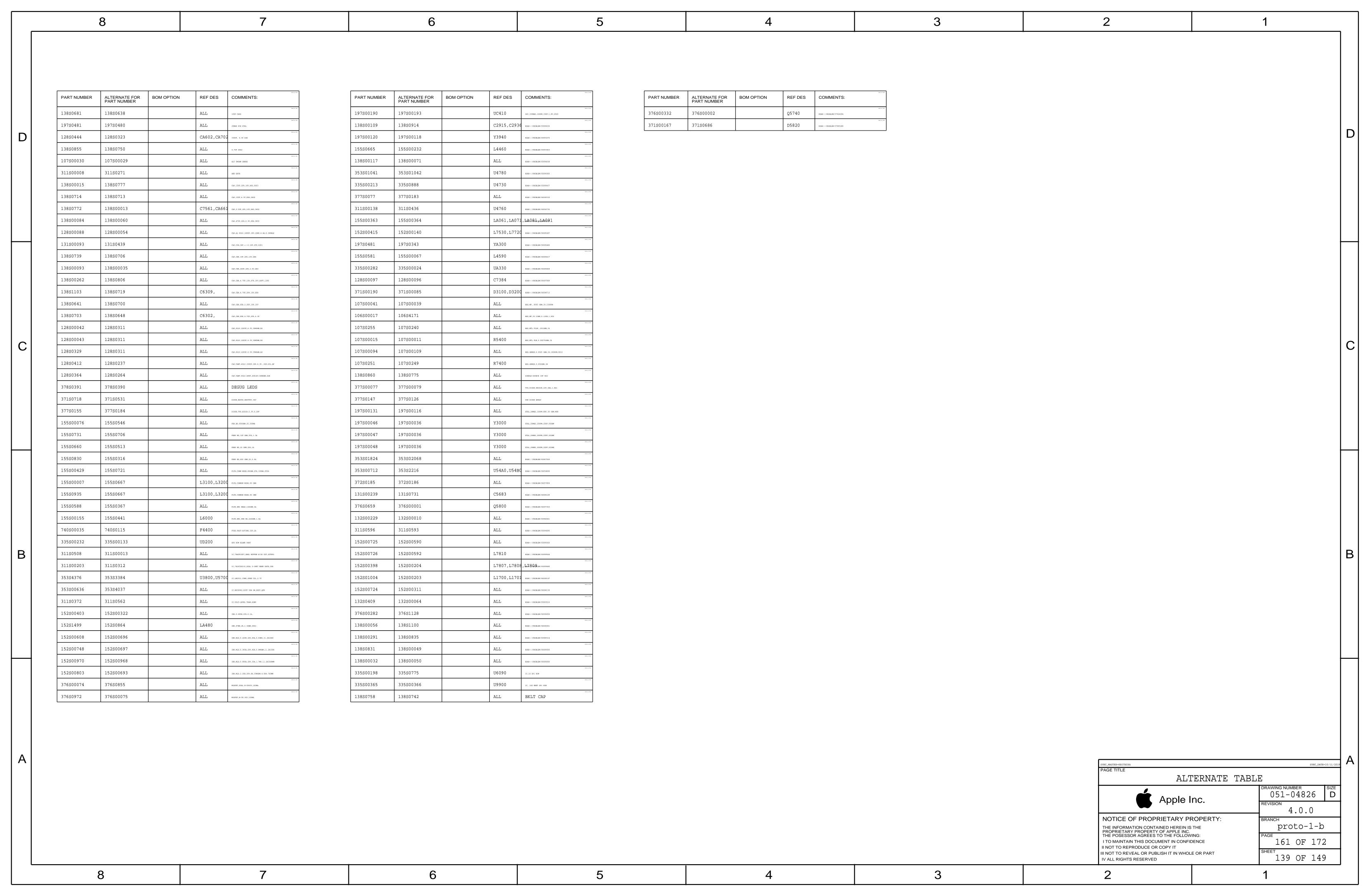


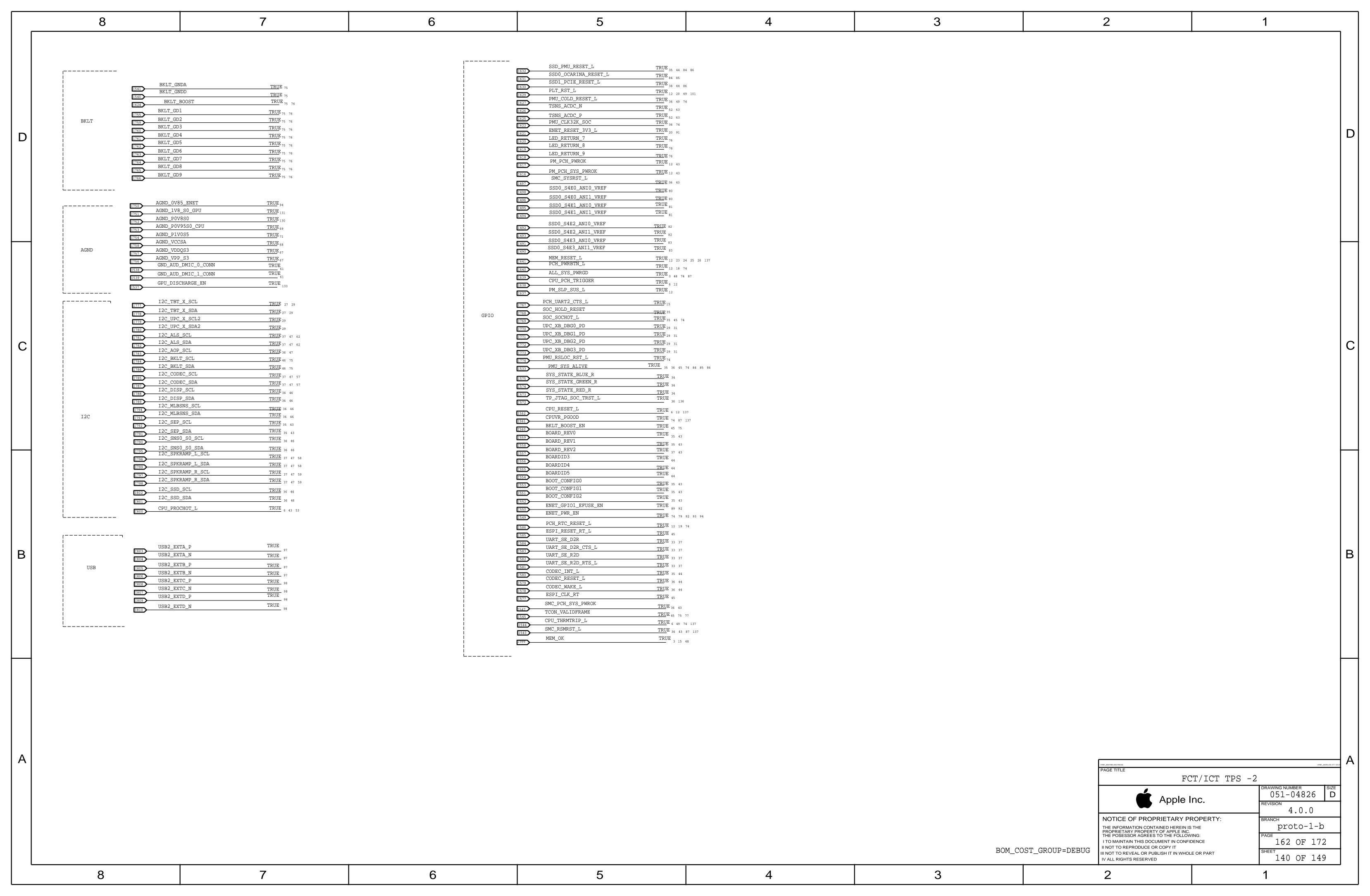












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						Т	ESTPOINTS TAB	T.F. 1		•		•			
						_									
		TE	ESTPOINTS CONFIGURAT	ΓΙΟΝ					TES	TPOINTS CONFIGURATI	ON				
	NETNAME	TYPE (ICT, FUNC, CHAR)	MIN SIZE(MM)	TOP/BOTTOM	QUANTITY PLACE	:_NEAR		NETNAME	TYPE (ICT, FUNC, CHAR)	MIN SIZE(MM)	TOP/BOTTOM QUANTITY	PLACE_NEAR			
	1V8_SWCH_EN ACDCBURST_L	CHAR	0.6	BOT	1			BOARDID5 BOARD_REV0	FCT FCT, CHAR	0.6	BOTTOM 1 BOT 1				D
	ACDC_PSU_PCC_1V8	CHAR	0.6	ВОТ	1			BOARD_REV1	FCT, CHAR	0.6	BOT 1				
	AGND_0V85_ENET	FCT	0.6	BOTTOM	1			BOARD_REV2	FCT	0.6	BOTTOM 1				
	AGND_1V8_S0_GPU AGND_P0V8S0	FCT FCT	0.6	BOTTOM	1			BOOT_CONFIG0 BOOT_CONFIG1	FCT,CHAR FCT,CHAR	0.6	BOT 1				
	AGND_P0V95S0_CPU	FCT	0.6	BOTTOM	1			BOOT_CONFIG2	FCT, CHAR	0.6	BOT 1				
	AGND_P1V0S5	FCT	0.6	BOTTOM	1			BT_AUDIO_SYNC	FCT	0.6	BOTTOM 1				
	AGND_VCCSA AGND_VDDQS3	FCT	0.6	BOTTOM	1			BURSTMODE_EN_R_L CODEC_INT_L	FCT CHAR	0.6	BOTTOM 1 BOT 1				
	AGND_VPP_S3	FCT	0.6	BOTTOM	1			CODEC_RESET_L	FCT, CHAR	0.6	BOT 1				
	ALL_SYS_PWRGD	FCT, CHAR	0.6	ВОТ	1			CODEC_WAKE_L	FCT, CHAR	0.6	BOT 1				!
	AUD_CONN_J1_AUD_RING_SENSE AUD_CONN_J1_AUD_TIP_SENSE	FCT FCT	0.6	BOTTOM	1			CPUVR_PGOOD CPU_BCLK100M_N	FCT,CHAR CHAR	0.6	BOT 1 BOT 1				
	AUD_CONN_J1_CABLE_DETECT	FCT	0.6	BOTTOM	1			CPU_BCLK100M_P	CHAR	0.6	BOT 1				
	AUD_CONN_J1_HP_LT	FCT	0.6	BOTTOM	1			CPU_C10_GATE_L	CHAR	0.6	BOT 1				
	AUD_CONN_J1_HP_PORT_CH_GND AUD_CONN_J1_HP_PORT_US_GND	FCT FCT	0.6	BOTTOM	1			CPU_CATERR_L CPU_PCH_TRIGGER	FCT	0.6	BOTTOM 1 BOTTOM 1				
c	AUD_CONN_J1_HP_RT	FCT	0.6	BOTTOM	1			CPU_PROCHOT_L	FCT	0.6	BOTTOM 1				С
	AUD_CONN_J1_HP_SNS_LT	FCT	0.6	BOTTOM	1			CPU_PWRGD	FCT, CHAR	0.6	BOT 1				
	AUD_CONN_J1_HP_SNS_RT AUD_CONN_J1_HS_MICN	FCT FCT	0.6	BOTTOM	1			CPU_RESET_L CPU_SMC_THRMTRIP_L	FCT,CHAR CHAR	0.6	BOT 1 BOT 1				
	AUD_CONN_J1_HS_MICP	FCT	0.6	BOTTOM	1			CPU_THRMTRIP_L	FCT, CHAR	0.6	BOT 1				
	AUD_SPKR_LTWT_OUT_N	FCT	0.6	BOTTOM	1			DEBUG_CLKREQ_L	CHAR	0.6	BOT 1				
	AUD_SPKR_LTWT_OUT_P AUD_SPKR_LWFR_OUT_N	FCT FCT	0.6	BOTTOM	1			DFUMUX_SEL DISP_GCON_INT_L	FCT CHAR	0.6	BOTTOM 1 BOT 1				
	AUD_SPKR_LWFR_OUT_P	FCT	0.6	BOTTOM	1			DP_DDPB_HPD	CHAR	0.6	BOT 1				
	AUD_SPKR_RTWT_OUT_N	FCT	0.6	BOTTOM	1			DP_DDPC_HPD	CHAR	0.6	BOT 1				
	AUD_SPKR_RTWT_OUT_P AUD_SPKR_RWFR_OUT_N	FCT FCT	0.6	BOTTOM	1			DP_DDPE_HPD DP_DDPE_HPD	CHAR CHAR	0.6	BOT 1 BOT 1				
	AUD_SPKR_RWFR_OUT_P	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_AUX_C_N	FCT	0.6	BOTTOM 1				
	BKLT_BOOST 1	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_AUX_C_P	FCT	0.6	BOTTOM 1				
	BKLT_BOOST_1 BKLT_BOOST_2	FCT FCT	0.6	BOTTOM	1			DP_INTPNL_ML_AUX_N DP_INTPNL_ML_AUX_P	FCT	0.6	BOTTOM 1 BOTTOM 1				
	BKLT_BOOST_EN	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_HPD	FCT	0.6	BOTTOM 1				
В	BKLT_GD1	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_HPD_CONN	FCT	0.6	BOTTOM 1				В
	BKLT_GD2 BKLT_GD3	FCT FCT	0.6	BOTTOM	1			DP_INTPNL_ML_N<0> DP_INTPNL_ML_N<1>	FCT	0.6	BOTTOM 1 BOTTOM 1				
	BKLT_GD4	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_N<2>	FCT	0.6	BOTTOM 1				
	BKLT_GD5	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_N<3>	FCT	0.6	BOTTOM 1				
	BKLT_GD6 BKLT_GD7	FCT FCT	0.6	BOTTOM	1			DP_INTPNL_ML_P<0> DP_INTPNL_ML_P<1>	FCT	0.6	BOTTOM 1 BOTTOM 1				
	BKLT_GD8	FCT	0.6	BOTTOM	1			DP_INTPNL_ML_P<2>	FCT	0.6	BOTTOM 1				
\square	BKLT_GD9 BKLT_GNDA	FCT FCT	0.6	BOTTOM	1			DP_INTPNL_ML_P<3> DP_INTPNL_SL_AUX_N	FCT	0.6	BOTTOM 1 BOTTOM 1				
	BKLT_GNDD	FCT	0.6	BOTTOM	1			DP_INTPNL_SL_AUX_N DP_INTPNL_SL_AUX_P	FCT	0.6	BOTTOM 1				
	BLC_LSYNC	FCT	0.6	BOTTOM	1			DP_INTPNL_SL_HPD	FCT	0.6	BOTTOM 1				
	BLC_VSYNC BOARDID3	FCT	0.6	BOTTOM	1			DP_INTPNL_SL_HPD_CONN DP_INTPNL_SL_N<0>	FCT	0.6	BOTTOM 1				
	BOARDID4	FCT	0.6	BOTTOM	1			DP_INTPNL_SL_N<1>	FCT	0.6	BOTTOM 1				
A															CABLE 1 DRAWING NUMBER 051-04826 D REVISION 4.0.0 BRANCH proto-1-b
								<u> </u>			_		THE POSESSOR AGREES TO THE F I TO MAINTAIN THIS DOCUMENT IN II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN IV ALL RIGHTS RESERVED	CONFIDENCE	163 OF 172 SHEET 141 OF 149
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						г	TESTPOINTS TAB	AT.F. 2						
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		т	ESTPOINTS CONFIGURA	TION			ſ		TES'	TPOINTS CONFIGURAT	ION			
	NETNAME	TYPE (ICT, FUNC, CHAR)	MIN SIZE(MM)		QUANTITY F	LACE_NEAR		NETNAME	TYPE (ICT, FUNC, CHAR)	MIN SIZE(MM)	TOP/BOTTOM QUANTITY	PLACE_NEAR		
	DP_INTPNL_SL_N<2> DP_INTPNL_SL_N<3>	FCT FCT	0.6	BOTTOM	1			I2C_AOP_SDA I2C_BKLT_SCL	CHAR FCT	0.6	BOT 1 BOTTOM 1			[
	DP_INTPNL_SL_P<0>	FCT	0.6	BOTTOM	1			I2C_BKLT_SDA	FCT	0.6	BOTTOM 1			
	DP_INTPNL_SL_P<1> DP_INTPNL_SL_P<2>	FCT FCT	0.6	BOTTOM	1			I2C_CODEC_SCL I2C_CODEC_SDA	FCT, CHAR FCT, CHAR	0.6	BOT 1 BOT 1			
	DP_INTPNL_SL_P<3>	FCT	0.6	BOTTOM	1			I2C_DISP_SCL	FCT, CHAR	0.6	BOT 1			
	DP_INT_HPD EG_RESET_RES_L	CHAR CHAR	0.6	BOT	1			I2C_DISP_SDA I2C_FTCAM_SCL	FCT, CHAR CHAR	0.6	BOT 1 1			
	ENET_3V3_PWR_EN_R	CHAR	0.6	ВОТ	1			I2C_FTCAM_SCL_CONN	FCT	0.6	BOTTOM 1			
	ENET_3V3_PWR_EN_R ENET_FET_P3V3_PGOOD	CHAR CHAR	0.6	BOT	1			I2C_FTCAM_SDA I2C_FTCAM_SDA_CONN	CHAR	0.6	BOT 1 BOTTOM 1			
	ENET_GPIO1_EFUSE_EN	FCT, CHAR	0.6	ВОТ	1			I2C_MLBSNS_SCL	FCT	0.6	BOTTOM 1			
	ENET_PWR_EN ENET_RESET_3V3_L	FCT FCT	0.6	BOTTOM	1			I2C_MLBSNS_SDA I2C_PWR_SCL	FCT CHAR	0.6	BOTTOM 1 BOT 1			
	ESPI_CLK60M_R	CHAR	0.6	BOT	1			I2C_PWR_SDA	FCT, CHAR	0.6	BOT 1			
	ESPI_CLK_RT ESPI_CS_L	FCT CHAR	0.6	BOTTOM	1			I2C_SEP_SCL I2C_SEP_SDA	FCT, CHAR	0.6	BOT 1 1			
	ESPI_IO<0>	CHAR	0.6	ВОТ	1			I2C_SNS0_S0_SCL	FCT, CHAR	0.6	BOT 1			
C	ESPI_IO<1> ESPI_IO<2>	CHAR CHAR	0.6	BOT	1			I2C_SNSO_SO_SDA I2C_SPKRAMP_L_SCL	FCT, CHAR	0.6	BOT 1 1			
	ESPI_IO<3>	CHAR	0.6	ВОТ	1			I2C_SPKRAMP_L_SDA	FCT, CHAR	0.6	BOT 1			
	ESPI_IO_RT<0> ESPI_IO_RT<1>	FCT FCT	0.6	BOTTOM	1			I2C_SPKRAMP_R_SCL I2C_SPKRAMP_R_SDA	FCT, CHAR	0.6	BOT 1 1			
	ESPI_IO_RT<2>	FCT	0.6	BOTTOM	1			I2C_SSD_SCL	FCT, CHAR	0.6	BOT 1			
	ESPI_IO_RT<3> ESPI_RESET_L	FCT CHAR	0.6	BOTTOM	1			I2C_SSD_SDA I2C_TBT_X_SCL	FCT, CHAR FCT	0.6	BOT 1 BOTTOM 1			
	ESPI_RESET_RT_L	FCT	0.6	BOTTOM	1			I2C_TBT_X_SDA	FCT	0.6	BOTTOM 1			
	FAN_0_PWM_FILT FAN_0_TACH_FILT	FCT FCT	0.6	BOTTOM	1 1			I2C_UPC_INT_L I2C_UPC_SCL	CHAR FCT	0.6	BOT 1 1 BOTTOM 1			
	FAN_PWR_EN	FCT, CHAR	0.6	ВОТ	1			I2C_UPC_SDA	FCT	0.6	BOTTOM 1			
	GFX_SELF_THROTTLE_1V8 GND	CHAR FCT	0.6	BOTTOM	40			I2C_UPC_XA_DBG_CTL_SCL I2C_UPC_XA_DBG_CTL_SDA	CHAR	0.6	BOT 1			
	GND	FCT	0.7	BOTTOM	5			I2C_UPC_XB_DBG_CTL_SCL	CHAR	0.6	BOT 1			
	GND_AUD_DMIC_0_CONN GND_AUD_DMIC_1_CONN	FCT FCT	0.6	BOTTOM	1			I2C_UPC_XB_DBG_CTL_SDA I2C_UPC_X_SCL2	CHAR	0.6	BOT 1 BOTTOM 1			
В	GPUVR_I2C_SCL	CHAR	0.6	ВОТ	1			I2C_UPC_X_SDA2	FCT	0.6	BOTTOM 1			E
	GPUVR_I2C_SDA GPU_DISCHARGE_EN	CHAR FCT	0.6	BOT	1			JTAG_TBT_X_TMS LED_RETURN_1	CHAR	0.6	BOT 1 1 1 1			
	GPU_GPIO_04_PCC_L	CHAR	0.6	вот	1			LED_RETURN_2	FCT	0.6	BOTTOM 1			
	GPU_GPIO_06_VRHOT_L GPU_GPIO_13	CHAR CHAR	0.6	BOT	1			LED_RETURN_3 LED_RETURN_4	FCT FCT	0.6	BOTTOM 1 BOTTOM 1			
	GPU_GPIO_15	CHAR	0.6	BOT	1			LED_RETURN_5	FCT	0.6	BOTTOM 1			
	GPU_GPIO_19 GPU_RESET_L	CHAR CHAR	0.6	BOT	1			LED_RETURN_6 LED_RETURN_7	FCT FCT	0.6	BOTTOM 1 BOTTOM 1			
	GPU_SMC_THRMTRIP	CHAR	0.6	BOT	1			LED_RETURN_8	FCT	0.6	BOTTOM 1 BOTTOM 1			
	I2C_ALS_SCL I2C_ALS_SCL_CONN	FCT,CHAR	0.6	BOT	1			LED_RETURN_9 MEM_OK	FCT FCT,CHAR	0.6	BOTTOM 1 BOT 1			
	I2C_ALS_SCL_CONN I2C_ALS_SDA	FCT,CHAR	0.6	BOT	1			MEM_OK MEM_RESET_L	FCT, CHAR	0.6	BOT 1			
	I2C_ALS_SDA_CONN	FCT	0.6	BOTTOM	1			MIPI_FTCAM_CLK_N	FCT	0.6	BOTTOM 1			
	I2C_AOP_SCL	FCT, CHAR	0.6	ВОТ	1			MIPI_FTCAM_C_CLK_N	FCT	0.6	BOTTOM 1			
A													PAGE TITLE TESTP	OINTS TABLE 2
														DRAWING NUMBER SIZE
													Apple	REVISION 4.0.0
													NOTICE OF PROPRIETARY PARTIES OF THE INFORMATION CONTAINED HEREIN IS PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOW	
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		1			1		Í	I		<u> </u>	_	ı	III NOT TO REVEAL OR PUBLISH IT IN WHOI IV ALL RIGHTS RESERVED	142 OF 149
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6 3 8 TESTPOINTS TABLE 3 TESTPOINTS CONFIGURATION TESTPOINTS CONFIGURATION TYPE (ICT, FUNC, CHAR) TYPE (ICT, FUNC, CHAR) TOP/BOTTOM NETNAME TOP/BOTTOM QUANTITY PLACE_NEAR NETNAME MIN SIZE(MM) QUANTITY PLACE_NEAR FCT 0.6 BOTTOM PLT_RESET_GPU_L CHAR 0.6 BOT MIPI_FTCAM_C_CLK_P MIPI_FTCAM_C_DATA_N<0> FCT 0.6 BOTTOM PLT_RST_L FCT, CHAR 0.6 MIPI_FTCAM_C_DATA_N<1> FCT 0.6 BOTTOM PMU_ACTIVE_READY FCT, CHAR 0.6 BOT FCT 0.6 0.6 BOTTOM CHAR BOT MIPI_FTCAM_C_DATA_P<0> PMU_CLK32K_PCH MIPI_FTCAM_C_DATA_P<1> FCT 0.6 BOTTOM PMU_CLK32K_SOC FCT, CHAR 0.6 BOT 0.6 BOT 0.6 CHAR CHAR BOT NAND_MODE_1V2_EN PMU_CLK32K_WLANBT NC_PCH_CLK32K_SUS CHAR 0.6 BOT PMU_CLK32K_WLANBT_R FCT 0.6 BOTTOM 0.6 BOT FCT, CHAR 0.6 BOT P1V05S5_PGOOD CHAR PMU_COLD_RESET_L P1V1_SLPDDR_SOCFET_EN 0.6 BOT PMU_ONOFF_L CHAR 0.6 BOT CHAR 0.6 BOT CHAR 0.6 BOT P1V2_S0SW_FETEN PMU_PVDDMAIN_EN CHAR 0.6 BOT FCT 0.6 P1V8G3S_EN PMU_RSLOC_RST_L BOTTOM P3V3MAIN_PGOOD CHAR 0.6 BOT FCT, CHAR 0.6 BOT PMU_SYS_ALIVE CHAR 0.6 BOT CHAR 0.6 P3V3MAIN_PGOOD BOT PMU_TO_NFC_EN P5VG3S_PGOOD CHAR 0.6 BOT CHAR 0.6 BOT PMU_VDD_HI PCH_BT_AUDIO_SYNC CHAR 0.6 BOT PMU_WLBT_PWR_EN CHAR 0.6 BOT PCH_ENETSD_CLKREQ_L 0.6 BOT PM_BATLOW_L CHAR 0.6 BOT CHAR 0.6 BOT CHAR 0.6 BOT PCH_ENETSD_RESET_L PM_EN_FET_P3V3_S0 PCH_ENET_10G_CLKREQ_L 0.6 BOT PM_EN_FET_P5V_S0 CHAR 0.6 BOT PCH_ENET_LOW_PWR CHAR 0.6 BOT PM_EN_LDO_DDRVTT_S0 CHAR 0.6 PCH_ESPI_ALERTO_L CHAR 0.6 BOT PM_EN_REG_GPU_GFX_SOC CHAR 0.6 BOT 0.6 BOT CHAR 0.6 PCH_GCON_INT_L CHAR PM_EN_REG_P0V8_S0 BOT 0.6 0.6 CHAR BOT CHAR BOT PCH_GPP_A0_PU PM_EN_REG_P1V05_S5 CHAR 0.6 BOT CHAR 0.6 BOT PCH_GPU_CLKREQ_L PM_EN_REG_P2V5_S3 CHAR BOT 0.6 CHAR 0.6 BOT PCH_GPU_ID PM_EN_REG_P3V3_G3H_R PCH_PWRBTN_L FCT, CHAR 0.6 BOT PM_EN_REG_PVDDCT_S0 CHAR 0.6 FCT, CHAR 0.6 BOT CHAR 0.6 BOT PCH_RTC_RESET_L PM_EN_REG_VCCIO_S0 CHAR 0.6 BOT 0.6 BOT PCH_SOC_SYNC PM_EN_REG_VCCSA_S0_R CHAR PCH_STRP_BSSB_SEL_GPIO CHAR 0.6 BOT PM_EN_REG_VDDQ_S3 CHAR 0.6 BOT PCH_STRP_ESPI CHAR 0.6 BOT PM_P1V05_S3_FET_EN CHAR 0.6 BOT 0.6 PCH_STRP_GPD7 CHAR BOT PM_P3V3P1V8_G3S_FET_EN CHAR 0.6 BOT CHAR 0.6 BOT CHAR 0.6 BOT PCH_STRP_GPP_H15 PM_P5VG3S_EN PCH_STRP_NO_REBOOT CHAR 0.6 BOT PM_PCH_PWROK FCT, CHAR 0.6 BOT PCH_STRP_SPIROM_SAF CHAR 0.6 BOT PM_PCH_SYS_PWROK FCT, CHAR 0.6 BOT 0.6 0.6 1 PCH_STRP_VCCPSPI_1V8 CHAR BOT PM_PGOOD_FET_P3V3G3S CHAR BOT PCH_STRP_XTAL_24MHZ CHAR 0.6 BOT PM_PGOOD_FET_P5V_S0 CHAR 0.6 BOT CHAR 0.6 BOT CHAR 0.6 PCH_SWD_SOC_CLK PM_PGOOD_REG_GPU_GFX BOT PCH_SWD_SOC_IO CHAR 0.6 BOT 1 PM_PGOOD_REG_GPU_SOC CHAR 0.6 BOT 1 PCH_UART2_CTS_L FCT, CHAR 0.6 BOT 1 PM_PGOOD_REG_GPU_VDDCI CHAR 0.6 BOT PCH_UART_DEBUG_D2R FCT, CHAR 0.6 BOT PM_PGOOD_REG_GPU_VDDIO CHAR 0.6 BOT FCT, CHAR 0.6 BOT FCT 0.6 PCH_UART_DEBUG_R2D PM_PGOOD_REG_P1V05_S5 BOTTOM PCH_WLAN_AUDIO_SYNC CHAR 0.6 BOT PM_PGOOD_REG_P2V5_S3 CHAR 0.6 BOT CHAR 0.6 BOT FCT, CHAR 0.6 BOT PCH_WLBT_CLKREQ_L PM_RSMRST_L 0.6 BOT 0.6 PCH_WLBT_PERST_L CHAR PM_SO_EN CHAR BOT 0.6 PCIEDN_WAKE_L CHAR BOT PM_SLP_S0_L CHAR 0.6 BOT FCT 0.6 PDM_DMIC_CLK0 BOTTOM PM_SLP_S3_L FCT, CHAR 0.6 BOT FCT 0.6 FCT, CHAR 0.6 PDM_DMIC_CLK1 BOTTOM PM_SLP_S4_L BOT 0.6 FCT 0.6 FCT, CHAR PDM_DMIC_DATA0_UNSEC BOTTOM PM_SLP_S5_L BOT PDM_DMIC_DATA1_UNSEC FCT 0.6 BOTTOM PM_SLP_SUS_L FCT, CHAR 0.6 BOT CHAR 0.6 BOT 0.6 BOT PD_BTI2SMUX_SEL_PCH PM_SYSRST_L FCT, CHAR 0.6 PLT_RESET_GPU_L CHAR BOT PM_VCCST_PWRGD_CPU CHAR 0.6 BOT TESTPOINTS TABLE 3 051-04826 Apple Inc. 4.0.0 NOTICE OF PROPRIETARY PROPERTY: proto-1-b THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
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8 6 3 TESTPOINTS TABLE 4 TESTPOINTS CONFIGURATION TESTPOINTS CONFIGURATION TYPE (ICT, FUNC, CHAR) TYPE (ICT, FUNC, CHAR) TOP/BOTTOM TOP/BOTTOM QUANTITY NETNAME QUANTITY PLACE_NEAR NETNAME MIN SIZE(MM) PLACE_NEAR FCT, CHAR PP0V75_S0_GPUVDD FCT, CHAR 0.6 BOT PP3V3_S5 0.6 BOT 0.6 PP0V82_SLPDDR FCT, CHAR BOT PP3V3_TBT_X_SX FCT 0.6 BOTTOM FCT PP0V85_ENET 0.6 BOTTOM PP3V3_UPC_XA FCT 0.6 BOTTOM FCT, CHAR 0.6 BOT FCT 0.6 PP0V85_S0_GPUVDDCI PP3V3_UPC_XB BOTTOM PP0V8_SLPS2R FCT, CHAR 0.6 BOT PP3V_G3_PCH_VCCRTC FCT, CHAR 0.6 BOT 0.6 BOT 0.6 BOT FCT, CHAR FCT, CHAR PP0V9_SLPDDR PP5V_G3S PP0V9_SSD0 FCT, CHAR 0.6 BOT PP5V_G3S_CAMERA_F FCT 0.6 BOTTOM FCT 0.6 FCT, CHAR 0.6 BOT PP12V_FAN_FILT BOTTOM PP5V_S0 PP12V_G3H FCT 0.6 BOTTOM PPDDRVTT_S0 FCT, CHAR 0.6 0.7 PP12V_G3H_ACDC FCT, CHAR BOT PPVBATT_G3_RTC FCT 0.6 BOTTOM FCT 0.6 CHAR 0.6 PP12V_G3H_GPUCORE BOTTOM PPVBATT_G3_RTC_R PP12V_G3H_SSD0 FCT 0.6 BOTTOM FCT 0.6 BOTTOM PPVBUS_USBC_XA FCT 0.6 FCT 0.6 PP12V_G3H_SSD1 BOTTOM PPVBUS_USBC_XB BOTTOM PP12V_LCD_FET FCT 0.6 BOTTOM PPVCCGT_S0_CPU FCT, CHAR 0.6 BOT PP12V_S0_BKLT_PWR FCT 0.6 BOTTOM PPVCCIN_SO_CPU FCT, CHAR 0.6 BOT PP1V05_S3SW FCT, CHAR 0.6 BOT PPVCCIO_SO_CPU FCT, CHAR 0.6 BOT PP1V05_S3_FET FCT, CHAR 0.6 BOT FCT, CHAR 0.6 BOT PPVCCQ_ANI_SSD0 PP1V05_S5 FCT, CHAR 0.6 BOT PPVCCSA_SO_CPU FCT, CHAR 0.6 FCT, CHAR 0.6 BOT FCT, CHAR 0.6 BOT PP1V1_SLPDDR PPVCORE_S0_GPU PP1V1_SLPDDR_SOC_VDDIOPLLDDR_F FCT 0.6 BOTTOM PPVDDCPUSRAM_AWAKE_SOC FCT, CHAR 0.6 BOT FCT, CHAR 0.6 BOT FCT, CHAR 0.6 BOT PP1V1_SLPS2R PPVDDCPU_AWAKE_SOC FCT, CHAR 0.6 FCT, CHAR 0.6 BOT BOT PP1V2_AWAKE PPVDDQ_S3 PP1V2_S3_CPU FCT 0.6 BOTTOM PPVDDQ_S3_DDR FCT 0.6 BOTTOM CHAR, CHAR, FCT, CHAR 0.6 BOT FCT, CHAR 0.6 PP1V2_S3_PLLOC BOT PPVSOC_S0_GPU PP1V2_S3_PLLOC 0.6 BOT PSU12V_PGOOD_1V8 CHAR 0.6 0.6 FCT, CHAR BOT CHAR 0.6 BOT PP1V35_S0_GPUMVDD PU_LAN_WAKE_L FCT 0.6 CHAR 0.6 BOT PP1V5_LDO_ENET_EFUSE BOTTOM PVCCIO_EN BOT PP1V8_AWAKE FCT, CHAR 0.6 BOT PVCCIO_PGOOD CHAR 0.6 PP1V8_DMIC_0_CONN FCT 0.6 BOTTOM PVDDQ_EN_BUF CHAR 0.6 BOT 0.6 FCT, CHAR 0.6 PP1V8_DMIC_1_CONN FCT BOTTOM PVDDQ_PGOOD BOT 1 PP1V8_G3S FCT, CHAR 0.6 BOT FCT 0.6 PWR_BTN_R BOTTOM REG_CPU_VCC_CORE_EN PP1V8_S0_GPUVDD FCT, CHAR 0.6 BOT CHAR 0.6 BOT PP1V8_S5 FCT, CHAR 0.6 BOT REG_CPU_VIDALERT_L_R CHAR 0.6 BOT 0.6 0.6 1 PP1V8_SLPS2R FCT, CHAR BOT REG_CPU_VIDSOUT_R CHAR BOT PP1V8_SLPS2R_PMUVDDGPIO CHAR 0.6 BOT SDCONN_OC_L CHAR 0.6 BOT PP1V8_VCCQIO_SSD0 FCT 0.6 SDCONN_STATE_CHANGE_L CHAR 0.6 BOTTOM BOT PP1V8_VCCQIO_SSD0_S5E_2L FCT 0.6 BOTTOM 1 SD_PWR_EN CHAR 0.6 BOT 1 PP1V8_VCCQIO_SSD0_S5E_4L CHAR 0.6 BOT 1 SE_CTLR_FW_DWLD CHAR 0.6 BOT PP2V1_ENET FCT 0.6 BOTTOM SE_DEV_WAKE CHAR 0.6 BOT FCT, CHAR 0.6 BOT CHAR 0.6 BOT PP2V5_NAND_SSD0 SE_GPIO0 PP2V5_S3 FCT, CHAR 0.6 BOT SMBUS_PCH_CLK FCT, CHAR 0.6 BOT PP3V3_AWAKE FCT, CHAR 0.6 BOT SMBUS_PCH_DATA FCT, CHAR 0.6 BOT PP3V3_ENET FCT, CHAR 0.6 BOT SMB_DP_TCON_SLA_SCL FCT 0.6 1 PP3V3_G3H FCT, CHAR 0.6 FCT 0.6 BOT SMB_DP_TCON_SLA_SDA BOTTOM PP3V3_G3H_SSD0 FCT 0.6 SMC_ACDC_ID CHAR 0.6 BOTTOM BOT PP3V3_G3H_SSD1 FCT 0.6 SMC_ACDC_ID_R 0.6 BOTTOM FCT BOTTOM FCT PP3V3_G3S 0.6 FCT 0.6 BOTTOM SMC_DEBUGPRT_RX BOTTOM PP3V3_G3S_FET FCT, CHAR 0.6 BOT SMC_DEBUGPRT_TX FCT 0.6 BOTTOM PP3V3_S0 FCT, CHAR 0.6 BOT SMC_GFX_THROTTLE_L CHAR 0.6 BOT CHAR 0.6 0.6 PP3V3_S0SW_TBT_X BOT SMC_GPU_ID CHAR BOT

TESTPOINTS TA	ABLE 4				
Apple Inc.	DRAWING NUMBER SIZE D				
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8 6 3 TESTPOINTS TABLE 5 TESTPOINTS CONFIGURATION TESTPOINTS CONFIGURATION TYPE (ICT, FUNC, CHAR) TYPE (ICT, FUNC, CHAR) TOP/BOTTOM NETNAME TOP/BOTTOM QUANTITY PLACE_NEAR NETNAME MIN SIZE(MM) QUANTITY PLACE_NEAR FCT SMC_GPU_THROTTLE_L CHAR 0.6 BOT SWD_SOC_SWCLK 0.6 BOTTOM SMC_PCH_SYS_PWROK FCT 0.6 BOTTOM SWD_SOC_SWDIO FCT 0.6 BOTTOM SMC_RSMRST_L FCT, CHAR 0.6 BOT SYS_STATE_BLUE_R FCT 0.6 BOTTOM CHAR 0.6 BOT FCT 0.6 SMC_SLP_S0_L BOTTOM SYS_STATE_GREEN_R SMC_SYSRST_L FCT 0.6 BOTTOM SYS_STATE_RED_R FCT 0.6 BOTTOM 0.6 BOT 0.6 BOT FCT, CHAR CHAR SML_PCH_0_CLK TBT_POC_RESET SML_PCH_0_DATA FCT, CHAR 0.6 BOT TBT_PWR_EN CHAR 0.6 BOT FCT, CHAR 0.6 BOT CHAR 0.6 BOT SML_PCH_1_CLK TBT_X_CIO_PWR_EN SML_PCH_1_DATA FCT, CHAR 0.6 BOT TBT_X_CLKREQ_L CHAR 0.6 BOT SOC_CLKREQ_L CHAR 0.6 BOT CHAR 0.6 BOT TBT_X_GPIO_0 FCT 0.6 0.6 SOC_COLD_RESET_L BOTTOM TBT_X_GPIO_1 CHAR FCT 0.6 BOTTOM TBT_X_PCI_RESET_R_L CHAR 0.6 BOT SOC_DEBUGPRT_RX FCT 0.6 TBT_X_PLUG_EVENT_L 0.6 BOT BOTTOM CHAR SOC_DEBUGPRT_TX SOC_DFU_STATUS FCT 0.6 BOTTOM TBT_X_USB_PWR_EN CHAR 0.6 BOT FCT 0.6 BOTTOM TCON_VALIDFRAME FCT 0.6 BOTTOM SOC_DOCK_CONNECT SOC_FORCE_DFU FCT 0.6 BOTTOM TP_BT_GPIO_2 CHAR 0.6 BOT SOC_HOLD_RESET FCT 0.6 BOTTOM CHAR 0.6 BOT TP_BT_GPIO_4 SOC_SOCHOT_L FCT 0.6 BOTTOM TP_BT_GPIO_5 CHAR 0.6 CHAR BOT SOC_SWD_MUX_SEL_PCH 0.6 BOT TP_EXTRA_1 CHAR 0.6 SOC_USB_VBUS FCT 0.6 BOTTOM TP_EXTRA_10 CHAR 0.6 BOT SPI2_WLBT_SFL_CLK FCT 0.6 CHAR 0.6 BOTTOM TP_EXTRA_11 BOT FCT 0.6 0.6 CHAR BOT SPI2_WLBT_SFL_CS_L BOTTOM TP_EXTRA_12 SPI2_WLBT_SFL_CS_L_R FCT 0.6 BOTTOM TP_EXTRA_13 CHAR 0.6 BOT FCT 0.6 CHAR 0.6 BOT SPI2_WLBT_SFL_MISO BOTTOM TP_EXTRA_14 SPI2_WLBT_SFL_MOSI FCT 0.6 BOTTOM TP_EXTRA_15 CHAR 0.6 CHAR 0.6 BOT CHAR 0.6 BOT SPIROM_USE_MLB TP_EXTRA_16 CHAR 0.6 BOT 0.6 BOT SPKRAMP_INT_L TP_EXTRA_17 CHAR SPKRAMP_RESET_L CHAR 0.6 BOT TP_EXTRA_18 CHAR 0.6 BOT SPKR_ID0 FCT 0.6 TP_EXTRA_2 CHAR 0.6 BOT BOTTOM 0.6 0.6 SPKR_ID1 FCT BOTTOM TP_EXTRA_3 CHAR BOT 1 0.6 BOT 0.6 BOT SSD0_CALPE_DISCHARGE_EN TP_EXTRA_4 CHAR SSD0_LPB_L CHAR 0.6 BOT TP_EXTRA_5 CHAR 0.6 BOT SSD0_OCARINA_PFN_L CHAR 0.6 BOT TP_EXTRA_6 CHAR 0.6 BOT 0.6 0.6 1 SSD0_OCARINA_PFN_L CHAR BOT TP_EXTRA_7 CHAR BOT SSD0_OCARINA_RESET_L FCT 0.6 BOTTOM TP_EXTRA_8 CHAR 0.6 BOT CHAR 0.6 BOT TP_EXTRA_9 CHAR 0.6 SSD0_RESET_L BOT SSD0_S4E0_ANI0_VREF FCT 0.6 BOTTOM 1 TP_JTAG_SOC_TRST_L FCT 0.6 BOTTOM 1 SSD0_S4E0_ANI1_VREF FCT 0.6 BOTTOM 1 TP_PCH_SLP_A_L CHAR 0.6 BOT 1 SSD0_S4E1_ANI0_VREF FCT 0.6 BOTTOM TP_PCH_STRP_TLSCONF CHAR 0.6 BOT FCT 0.6 0.6 BOT SSD0_S4E1_ANI1_VREF BOTTOM TP_PCH_STRP_TOPBLK_SWP_L CHAR SSD0_S4E2_ANI0_VREF FCT 0.6 BOTTOM TP_SD_GPI02 CHAR 0.6 BOT TP_SMC_FIXTURE_MODE_L SSD0_S4E2_ANI1_VREF FCT 0.6 BOTTOM FCT 0.6 BOTTOM 1 FCT 0.6 FCT 0.6 SSD0_S4E3_ANI0_VREF BOTTOM TP_USB_MAN_N BOTTOM FCT 0.6 FCT SSD0_S4E3_ANI1_VREF BOTTOM TP_USB_MAN_P 0.6 BOTTOM CHAR 0.6 BOT CHAR 0.6 SSD0_VR_P2V5_EN TP_WL_GPIO_7 BOT SSD0_VR_P2V5_PGOOD CHAR 0.6 BOT 0.6 TSNS_ACDC_N FCT BOTTOM 0.6 CHAR BOT FCT 0.6 SSD0_WP_L TSNS_ACDC_P BOTTOM SSD1_PCIE_RESET_L FCT 0.6 BOTTOM UART_BT_SOC_LH_D2R FCT 0.6 BOTTOM CHAR 0.6 BOT FCT SSD_BFH UART_BT_SOC_LH_R2D 0.6 BOTTOM SSD_PMU_RESET_L FCT, CHAR 0.6 BOT UART_SE_D2R FCT 0.6 BOTTOM TESTPOINTS TABLE 5 051-04826 , Apple Inc. 4.0.0 NOTICE OF PROPRIETARY PROPERTY: proto-1-b THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
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					•	TESTPOINTS TA	ABLE 6				•		
		TE	ESTPOINTS CONFIGURAT	TION				TE	ESTPOINTS CONFIGURAT	TION		7	
	NETNAME	TYPE (ICT, FUNC, CHAR)	MIN SIZE(MM)	TOP/BOTTOM	QUANTITY PLACE_NEAR		NETNAME	TYPE (ICT, FUNC, CHAR)	MIN SIZE(MM)	TOP/BOTTOM QUANTITY	PLACE_NEAR		
	UART_SE_D2R_CTS_L UART_SE_R2D	FCT	0.6	BOTTOM	1		USBC_XA_D2R_C_P<1> USBC_XA_D2R_C_P<2>	FCT	0.6	BOTTOM 1 BOTTOM 1			D
D	UART_SE_R2D_RTS_L	FCT	0.6	BOTTOM	1		USBC_XA_D2R_N<1>	FCT	0.6	BOTTOM 1		_	
	UART_WLAN_D2R	FCT	0.6	BOTTOM	1		USBC_XA_D2R_N<2>	FCT	0.6	BOTTOM 1			
	UART_WLAN_D2R_CTS_L	FCT	0.6	BOTTOM	1		USBC_XA_D2R_P<1>	FCT	0.6	BOTTOM 1		<u> </u>	
	UART_WLAN_R2D UART_WLAN_R2D_RTS_L	FCT	0.6	BOTTOM	1		USBC_XA_D2R_P<2> USBC_XA_R2D_N<1>	FCT	0.6	BOTTOM 1 BOTTOM 1			
	UPC_XA_GPIO4	CHAR	0.6	BOT	1		USBC_XA_R2D_N<2>	FCT	0.6	BOTTOM 1			
	UPC_XB_DBG0_PD	FCT	0.6	BOTTOM	1		USBC_XA_R2D_P<1>	FCT	0.6	BOTTOM 1			
	UPC_XB_DBG1_PD UPC_XB_DBG2_PD	FCT	0.6	BOTTOM	1		USBC_XA_R2D_P<2> USBC_XA_SBU1	FCT	0.6	BOTTOM 1 BOTTOM 1		<u> </u> 	
	UPC_XB_DBG3_PD	FCT	0.6	BOTTOM	1		USBC_XA_SBU2	FCT	0.6	BOTTOM 1			
	UPC_XB_GPI01	CHAR	0.6	BOT	1		USBC_XA_USB_BOT_N	FCT	0.6	BOTTOM 1			
	UPC_XB_GPI010	CHAR	0.6	BOT	1		USBC_XA_USB_BOT_P	FCT	0.6	BOTTOM 1		<u> </u>	
	UPC_XB_GPIO4 UPC_XB_GPIO9	CHAR	0.6	BOT	1		USBC_XA_USB_TOP_N USBC_XA_USB_TOP_P	FCT	0.6	BOTTOM 1 BOTTOM 1			
	USB2_EXTA_N	FCT	0.6	BOTTOM	1		USBC_XB_AUXLSX1	FCT	0.6	BOTTOM 1			
	USB2_EXTA_P	FCT	0.6	BOTTOM	1		USBC_XB_AUXLSX2	FCT	0.6	BOTTOM 1			
C	USB2_EXTB_N USB2_EXTB_P	FCT	0.6	BOTTOM	1 1		USBC_XB_CC1 USBC_XB_CC2	FCT	0.6	BOTTOM 1 BOTTOM 1		<u> </u> 	C
	USB2_EXTC_N	FCT	0.6	BOTTOM	1		USBC_XB_D2R_C_N<1>	FCT	0.6	BOTTOM 1		_	
	USB2_EXTC_P	FCT	0.6	BOTTOM	1		USBC_XB_D2R_C_N<2>	FCT	0.6	BOTTOM 1			
	USB2_EXTD_N	FCT	0.6	BOTTOM	1		USBC_XB_D2R_C_P<1>	FCT	0.6	BOTTOM 1			
	USB2_EXTD_P USB3_EXTA_D2R_F_N	FCT	0.6	BOTTOM	1		USBC_XB_D2R_C_P<2> USBC_XB_R2D_N<1>	FCT	0.6	BOTTOM 1 BOTTOM 1		<u> </u>	
	USB3_EXTA_D2R_F_P	FCT	0.6	BOTTOM	1		USBC_XB_R2D_N<2>	FCT	0.6	BOTTOM 1			
	USB3_EXTA_R2D_F_N	FCT	0.6	BOTTOM	1		USBC_XB_R2D_P<1>	FCT	0.6	BOTTOM 1			
	USB3_EXTA_R2D_F_P	FCT	0.6	BOTTOM	1		USBC_XB_R2D_P<2>	FCT	0.6	BOTTOM 1			
	USB3_EXTB_D2R_F_N USB3_EXTB_D2R_F_P	FCT	0.6	BOTTOM	1		USBC_XB_SBU1 USBC_XB_SBU2	FCT	0.6	BOTTOM 1 BOTTOM 1		<u> </u> 	
	USB3_EXTB_R2D_F_N	FCT	0.6	BOTTOM	1		USBC_XB_USB_BOT_N	FCT	0.6	BOTTOM 1			
	USB3_EXTB_R2D_F_P	FCT	0.6	BOTTOM	1		USBC_XB_USB_BOT_P	FCT	0.6	BOTTOM 1			
	USB3_EXTC_D2R_F_N	FCT	0.6	BOTTOM	1		USBC_XB_USB_TOP_N	FCT	0.6	BOTTOM 1			
	USB3_EXTC_D2R_F_P USB3_EXTC_R2D_F_N	FCT	0.6	BOTTOM	1		USBC_XB_USB_TOP_P USB_EXTE_OC_L	FCT CHAR	0.6	BOTTOM 1 BOT 1			
В	USB3_EXTC_R2D_F_P	FCT	0.6	BOTTOM	1		USB_EXTF_OC_L	CHAR	0.6	BOT 1			В
	USB3_EXTD_D2R_F_N	FCT	0.6	BOTTOM	1		USB_SOC_N	FCT	0.6	BOTTOM 1			
	USB3_EXTD_D2R_F_P	FCT	0.6	BOTTOM	1		USB_SOC_P	FCT	0.6	BOTTOM 1		<u> </u>	
	USB3_EXTD_R2D_F_N USB3_EXTD_R2D_F_P	FCT	0.6	BOTTOM	1		USB_SOC_TYPEC_N USB_SOC_TYPEC_P	FCT	0.6	BOTTOM 1 BOTTOM 1			
	USB3_VITAMIN_D2R_N	FCT	0.6	BOTTOM	1		VR_GPUMEM_ENABLE	CHAR	0.6	BOT 1			
	USB3_VITAMIN_D2R_P	FCT	0.6	BOTTOM	1		WLAN_AUDIO_SYNC_1V8	CHAR	0.6	BOT 1			
	USB3_VITAMIN_R2D_C_N USB3_VITAMIN_R2D_C_P	FCT	0.6	BOTTOM	1 1		WLBT_HOST_WAKE XDP_JTAG_ISP_TCK	CHAR CHAR	0.6	BOT 1			
\vdash	USBC_XA_AUXLSX1	FCT	0.6	BOTTOM	1		XDP_JTAG_ISP_TCK XDP_JTAG_ISP_TDI	CHAR	0.6	BOT 1		-	
	USBC_XA_AUXLSX2	FCT	0.6	BOTTOM	1		XDP_JTAG_ISP_TDO	CHAR	0.6	BOT 1			
	USBC_XA_CC1	FCT	0.6	BOTTOM	1		XDP_PRESENT_L	CHAR	0.6	BOT 1			
	USBC_XA_CC2 USBC_XA_D2R_C_N<1>	FCT	0.6	BOTTOM	1		XDP_USB_EXTA_OC_L XDP_USB_EXTB_OC_L	CHAR	0.6	BOT 1		<u> </u>	
	USBC_XA_D2R_C_N<2>	FCT	0.6	BOTTOM	1		XDP_USB_EXTC_OC_L	CHAR	0.6	BOT 1			
							XDP_USB_EXTD_OC_L	CHAR	0.6	BOT 1			
A												NOTICE OF PROPRIETARY P THE INFORMATION CONTAINED HEREIN I PROPRIETARY PROPERTY OF APPLE INC THE POSESSOR AGREES TO THE FOLLOW I TO MAINTAIN THIS DOCUMENT IN CONF II NOT TO REPRODUCE OR COPY IT	PROPERTY: US THE Proto-1-b PAGE FIDENCE 4.0.0 BRANCH Proto-1-b PAGE 168 OF 172
					1	1						III NOT TO REVEAL OR PUBLISH IT IN WHO IV ALL RIGHTS RESERVED	SHEET 146 OF 149
	8		7		6	5		4		3		2	1

	8	7			6		5		4			3	2	1
	<u>\</u>												!	
	SSD BOM GROUPS						Programmable P	arts						
	BOM GROUP		ВО	M OPTIONS		NAA JANSOO PAID	PART# QTY DESCRIPTION		REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION			
	STG_256GB_WD			E_256GB_2L_WD,SOC		Tele 4, Alles Marco 2, Flori Walk 4, Alles Marco 2, Flori Walk 4, Milles 10, Flori	341S01498 1 IC,TBT TBT-X (VX	X) POC,X1647	U2890	CRITICAL	Take_(TTIN			
	STG_256GB_TO STG_512GB_HY			!E_256GB_2L_TO,SOC !E_512GB_4L_HY,SOC		THE AMERICAN PIN	335S00133	8MBIT,50MHZ,USON8	U2890 U6090	CRITICAL CRITICAL	Table, 5, 17Thi	-		
	STG_512GB_TO			E_512GB_4L_TO,SOC		NAA, ARABOO JOS	335S00198 1 1c,SPI SERIAL FLASH,		U6090	CRITICAL	Table, s./Thi			
	STG_1TB_HY			E_1TB_4L_HY,SOC:20		THE AMERICAN PRO-		V (V39) DVT-2,X1294	UB250	CRITICAL	Take COTIN			D
	STG_1TB_TO STG_2TB_WD			E_1TB_4L_TO,SOC:20 E_2TB_4L_WD,SOC:20		NALAMOND FINE	335S00255	SH,2MBIT,1.8V,DFN8	UB250 U9990	CRITICAL CRITICAL	Také, (, TIN			
	STG_2TB_HY			E_2TB_4L_HY,SOC:20		Make, and control of the	335S00365 1 IC, SPI SERIAL FLASH,		U9990	CRITICAL	Sale_C/IRV	_		
	STG_4TB_WD		4L_S4E,S4E_4TB_4	L_WD,SOC:2G,SSD1_	CONN,SSD:2TB_WD_ITLC	160,40000,70	341S01502 1 IC,SDCARD CTL,GL3227	\(V7A09),POC,X1647	UA330	CRITICAL	SD_ROM:PROG			
	STG_4TB_HY				CONN,SSD:2TB_HY_ITLC	THE AMERICAN PINS		,3V,8-USON,2X3X,6MM	UA330 UB210	CRITICAL	1844,5,019			
	STG_8TB_WD STG_8TB_HY				CONN, SSD: 4TB_WD_ITLC CONN, SSD: 4TB_HY_ITLC	964,50000770	341S00725 1 WIFI ROM (V01) WW1,3 335S00214 1 IC,EEPROM,SER,UWIRE		UB210	CRITICAL CRITICAL	WIFI_ROM: PROG WIFI_ROM: BLANK	_		
	GOG GDOUDG								-		,			
	SOC GROUPS BOM GROUP		POI	M OPTIONS		164,350000-100								
	SOC:1G			SOC:DEV_1G		1163,00000770								
	SOC:2G		Ç	SOC:DEV_2G		1862, 30000007, 700	ASICs							
							PART# QTY DESCRIPTION		REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION			
	BOARD REV GROUPS					VALL ASSESSMENT AND	337S00821 1 IC, PCH-H, CML, QRL8, QS	A-0,BGA874	U1200	CRITICAL	3664,500 5664,500			
	BOM GROUP BOARDREV_POC		ВС	OM OPTIONS		Nata protection of the	338S00441		U2800 U7800	CRITICAL CRITICAL	Shark J. Princ			
	BOARDREV_P1			BOARDREV0		Nata pilannia yna	353S01961 2 IC,CD3218,ACE2,B2,US		U3100,U3200	CRITICAL	NA.6.3/No.			C
	BOARDREV_EVT		BOARDREV1			THE ASSESSED FOR	338S00332 1 IC,ENET CONTROLLER, A	C107,B1,BGA224	U9700	CRITICAL	Takit 5,100e			
	BOARDREV_PVT		BOARDREV1,	BOARDREV0			343S0616 I IC, CAESAR IV, GBIT, EN 338S00312 I IC, GL3227A, USB3 3.0	T CTRL,QFN64 O SD CARD READER,QFN48	U6000 UA300	CRITICAL CRITICAL	1G_ENET			
	GS5 ASSEMBLIES						338S00410 1 ic,pmu,ocarina,d	499A0,OTP-AG,WLCSP56	П9000	CRITICAL	SSD0_S4E_4L			
		DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION			499A0,OTP-AG,WLCSP56	U9000	CRITICAL	SSD0_S5E_4L	<- Placeholder APN		
	555 0410	WD,4L,16DP,GS5,ITLC,X1318	SSD	CRITICAL	SSD:2TB_WD_ITLC			I,B3,M,ES7.9,LGA385	UB000	CRITICAL CRITICAL	WIFI:MURATA WIFI:USI			
		HY,4L,16DP,GS5,ITLC,X1318	SSD	CRITICAL	SSD: 2TB_HY_ITLC					1		J		
	474 0404	WD,4L,16DP,GS5,ITLC,X1318 HY,4L,16DP,GS5,ITLC,X1318	SSD SSD	CRITICAL CRITICAL	SSD:4TB_WD_ITLC SSD:4TB_HY_ITLC									
		'					Н9М							
		://50926379&50926402>					PART# QTY DESCRIPTION		REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION			
	SSD BOM Groups <rdar <<="" description="" part#="" qty="" td=""><td></td><td>CRITICAL BOM OPTION</td><td>MAZ, MA</td><td></td><td></td><td>339S00386 1 pop,gibraltar_l+1gb,20N 339S00388 1 pop,gibraltar_l+2gb,20N</td><td></td><td>+</td><td>CRITICAL CRITICAL</td><td>SOC:DEV_1G SOC:DEV_2G</td><td></td><td></td><td></td></rdar>		CRITICAL BOM OPTION	MAZ, MA			339S00386 1 pop,gibraltar_l+1gb,20N 339S00388 1 pop,gibraltar_l+2gb,20N		+	CRITICAL CRITICAL	SOC:DEV_1G SOC:DEV_2G			
	998-16396 2 NAND, 3DV4, 128GBT, S4e, 256GB, T, SLGA110		CRITICAL S4E_256GB_2L	1_TO			339S00601 1 pop,gibraltar_l+1gb,16N			CRITICAL	SOC:PRD_1G			
	335S00378 2 NAND,3DV4,128GBT,S4E,256G,H,SLGA110	U8600,U8700 CE	CRITICAL S4E_256GB_2L	256GB			339S00605 1 pop,gibraltar_l+2gb,16N	I,M,B0,SCK,CSP1122	U3900	CRITICAL	SOC:PRD_2G			
В	335S00395 2 NAND, 3DV4, 192GBT, 21.1, S4E, 256G, T, SLGA110	U8600,U8700 CF	CRITICAL S4E_512GB_4L	_TO										l _B
	998-16396 2 NAND, 3DV4, 128GBT, S4E, 256G, T, SUBX, SLGA110		CRITICAL S4E_512GB_4L	512GB			Н9М							
	335S00398 2 NAND, 3DV4, 192GBT, 21.1, S4E, 256G, H, SLGA110 335S00378 2 NAND, 3DV4, 128GBT, S4E, 256G, H, SLGA110	·	CRITICAL S4E_512GB_4L CRITICAL S4E_512GB_4L	TANALIÇUTEM			PART NUMBER ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES COMMENTS:	Tabe jet jedi				
	335S00397 2 NAND, 3DV4, 320GBT, S4e, 256GB, T, SLGA110	<u></u>	CRITICAL S4E_1TB_4L_TC	VARA, COM			339S00387 339S00386	SOC:DEV_1G	ALL <rdar: 41988491=""></rdar:>	POP,	RON SCK PRIMARY, HYNIX SCK ALT GIBRALTAR+1GB,20NM,M,DEV,SCK,CSP112 RON SCK PRIMARY, MICRON ATK ALT	2		
	335S00397 2 NAND, 3DV4, 320GBT, S4e, 256GB, T, SLGA110 335S00396 2 NAND, 3DV4, 256GBT, S4e, 256GB, T, SLGA110		CRITICAL S4E_1TB_4L_TO	TARKE, K, IDM			339S00390 339S00386 339S00391 339S00386	SOC:DEV_1G SOC:DEV_1G	ALL <rdar: 41988491=""> ALL <rdar: 41988491=""></rdar:></rdar:>	POP,	GIBRALTAR+1GB,20NM,M,DEV,SCK,CSP112 RON SCK PRIMARY, HYNIX ATK ALT GIBRALTAR+1GB,20NM,M,DEV,SCK,CSP112			
	335S00399 2 NAND,3DV4,320GBT,21.1,S4E,256G,H,SLGA110		CRITICAL S4E_1TB_4L_H	Takel, (,The			339800389 339800388	SOC:DEV_2G	ALL <rdar: 41988491=""></rdar:>	MICR POP,	RON SCK PRIMARY, HYNIX SCK ALT GIBRALTAR+2GB,20NM,M,DEV,SCK,CSP112			
	335S00379 2 NAND,3DV4,256GBT,S4E,256G,H,SLGA110		CRITICAL S4E_1TB_4L_H	1662,5,694			339S00392 339S00388	SOC: DEV_2G	ALL <rdar: 41988491=""></rdar:>	POP,	RON SCK PRIMARY, MICRON ATK ALT GIBRALTAR+2GB,20NM,M,DEV,SCK,CSP112 RON SCK PRIMARY, HYNIX ATK ALT			
\vdash	335S00391 4 NAND, 3DV4, 512GBT, S4E, 256GB, SD, SLGA110 335S00380 4 NAND, 3DV4, 512GBT, S4E, 256G, H, SLGA110		CRITICAL S4E_2TB_4L_WI	TABLE, CITA			339S00393 339S00388 339S00602 339S00601	SOC:DEV_2G SOC:PROD_1G	ALL <rdar: 41988491=""> ALL <rdar: 41988491=""></rdar:></rdar:>	POP,	GIBRALTAR+2GB,20NM,M,DEV,SCK,CSP112 RON SCK PRIMARY, HYNIX SCK ALT GIBRALTAR_L+1GB,16NM,M,B0,SCK,C1122			\vdash
	335S00391 4 NAND, 3DV4, 512GBT, XXX, S4E, 256G, H, SLGA110		CRITICAL S4E_21B_4L_WI	1866,6/86			339S00602 339S00601 339S00603 339S00601	SOC:PROD_IG	ALL <rdar: 41988491=""></rdar:>	Table, ALZ, OTHE MICR	RON SCK PRIMARY, MICRON ATK ALT GIBRALTAR_L+1GB,16NM,M,B0,SCK,C1122			
	335S00380 4 NAND, 3DV4, 512GBT, S4E, 256G, H, SLGA110		CRITICAL S4E_4TB_4L_H	4TB			339S00604 339S00601	SOC:PROD_1G	ALL <rdar: 41988491=""></rdar:>	POP,	RON SCK PRIMARY, HYNIX ATK ALT GIBRALTAR_L+1GB,16NM,M,B0,SCK,C1122 RON SCK PRIMARY, HYNIX SCK ALT			
	335S00433 4 NAND, 3DV4, 1TBT, XXX, S4E, 512G, SD, SLGA110	U8600,U8700,U8800,U8900 CI	CRITICAL S4E_8TB_4L_W	ID 8TR			339S00606 339S00605 339S00607 339S00605	SOC:PROD_2G SOC:PROD_2G	ALL <rdar: 41988491=""> ALL <rdar: 41988491=""></rdar:></rdar:>	POP,	GIBRALTAR_L+2GB,16NM,M,B0,SCK,C1122 RON SCK PRIMARY, MICRON ATK ALT GIBRALTAR_L+2GB,16NM,M,B0,SCK,C1122			
	335S00444 4 NAND,3DV5,1024GBT,S4E,512G,H,SLGA110	U8600,U8700,U8800,U8900 CI	CRITICAL S4E_8TB_4L_H	100 A A A A A A A A A A A A A A A A A A			339800608 339800605	SOC: PROD_2G	ALL <rdar: 41988491=""></rdar:>	Table, ALZ, Olive MICR	CON SCK PRIMARY, HYNIX ATK ALT GIBRALTAR_L+2GB,16NM,M,B0,SCK,C1122			
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													PAGE TITLE BOM Configui	ration sync_date=09/26/2019
	SOCKET& CONNECTOR													DRAWING NUMBER SIZE 051-04826 D
	PART# QTY DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL BOM OPTION	Mac () Mac									Apple Inc.	REVISION 4.0.0
	511S00012 1 CONN, CPU, SOCKET, LGA1200, HF		CRITICAL	1684, 4, 700 1684, 4, 700									NOTICE OF PROPRIETARY PROPERTY:	BRANCH proto-1-b
	514-00118 1 CONN,RCPT,USB-C,DUAL,X1221	J3300 C	CRITICAL										THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE	PAGE 170 OF 172
													II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	170 OF 172 SHEET 147 OF 149
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