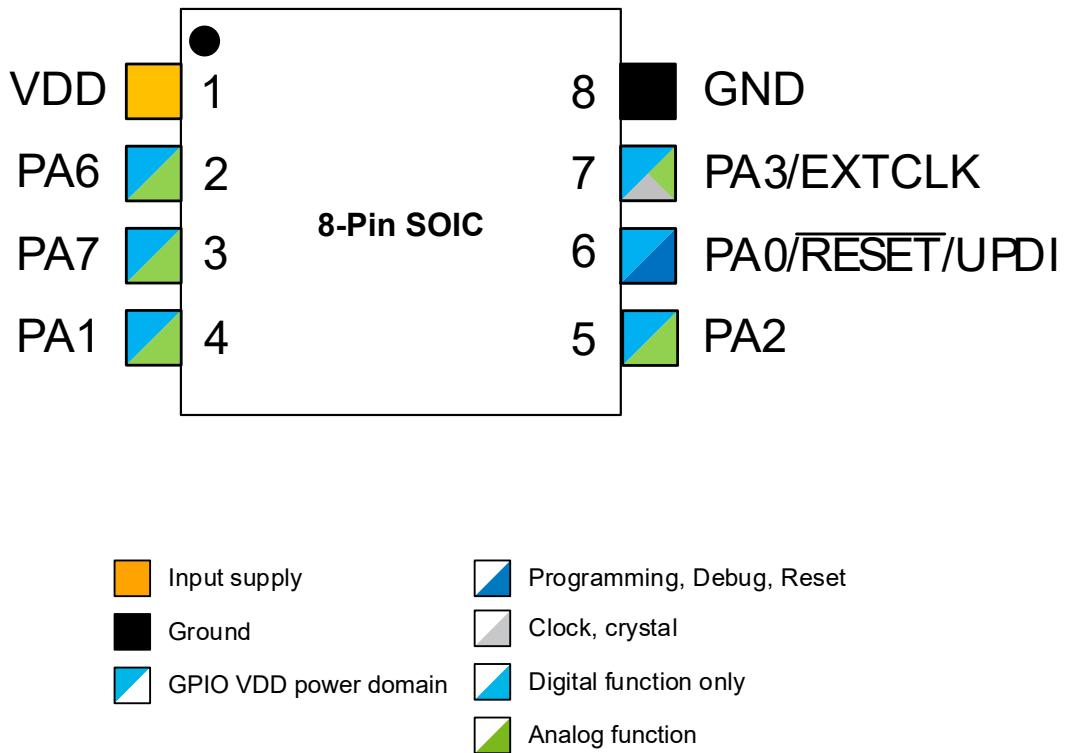


抵抗カラーコード

0	黒	1	黒い礼服	
1	茶	10	小林一茶	1
2	赤	100	赤い人参	2
3	橙	1K	みかんはだいだい	
4	黄	10K	四季の色	
5	緑	1M	五月みどり	
6	青	10M	青二才のろくでなし	
7	紫	100M	紫七部	
8	灰	1G	ハイヤー	
9	白	10G	ホワイトクリスマス	
金				5
銀				10
				20

E3

1M		2.2M		4.7M	
100K		220K		470K	
10K		22K		47K	
1K		2.2K		4.7K	
100		220		470	
10		22		47	
1		2			



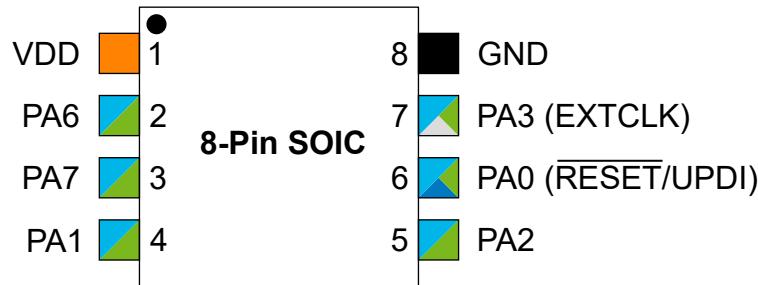
5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

SOIC 8-pin	Pin Name (1,2)	Other/Special	ADC0	AC0	USART0	SPI0	TWI0	TCA0	TCB0	CCL
6	PA0	RESET/UPDI	AIN0		XDIR	SS				LUT0-IN0
4	PA1		AIN1		TxD ⁽³⁾	MOSI	SDA	WO1		LUT0-IN1
5	PA2	EVOUT0	AIN2		RxD ⁽³⁾	MISO	SCL	WO2		LUT0-IN2
7	PA3	EXTCLK	AIN3	OUT	XCK	SCK		WO0/WO3		
8	GND									
1	VDD									
2	PA6		AIN6	AINN0	TxD	MOSI ⁽³⁾			WO0	LUT0-OUT
3	PA7		AIN7	AINP0	RxD	MISO ⁽³⁾		WO0 ⁽³⁾		LUT1-OUT

Note:

1. Pin names are of type Pxn , with x being the PORT instance (A, B) and n the pin number. Notation for signals is $\text{PORT}x_PINn$. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins $Px2$ and $Px6$ of each port have full asynchronous detection.
3. Alternate pin positions. For selecting the alternate positions, refer to the PORTMUX documentation.



Power	Functionality
Power Supply	Programming/Debug
Ground	Clock/Crystal
Pin on VDD Power Domain	Digital Function Only
	Analog Function

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing, 14 and 20 Pins

VQFN 20-Pin	SOIC 20-Pin	SOIC 14-Pin	Pin Name (1,2)	Other/Special	ADC0	AC0	DAC0	USART0	SPI0	TWI0	TCA0	TCB0	TCD0	CCL
19	16	10	PA0	RESET/ UPDI	AIN0									LUT0-IN0
20	17	11	PA1		AIN1			TxD(3)	MOSI	SDA(3)				LUT0-IN1
1	18	12	PA2	EVOUT0	AIN2			RxD(3)	MISO	SCL(3)				LUT0-IN2
2	19	13	PA3	EXTCLK	AIN3			XCK(3)	SCK		WO3			
3	20	14	GND											
4	1	1	VDD											
5	2	2	PA4		AIN4			XDIR(3)	SS		WO4		WOA	LUT0-OUT
6	3	3	PA5		AIN5	OUT					WO5	WO	WOB	
7	4	4	PA6		AIN6	AINN0	OUT		MOSI(3)(4)					
8	5	5	PA7		AIN7	AINP0			MISO(3)(4)					LUT1-OUT
9	6	PB5	CLKOUT		AIN8	AINP1					WO2(3)			
10	7	PB4			AIN9	AINN1					WO1(3)			LUT0-OUT(3)
11	8	PB3	TOSC1					RxD			WO0(3)			
12	9	PB2	TOSC2, EVOUT1					TxD			WO2			
13	10	PB1			AIN10			XCK		SDA	WO1			
14	11	PB0			AIN11			XDIR		SCL	WO0			
15	12	PC0							SCK(3)			WO(3)	WOC	
16	13	PC1							MISO(3)(4)			WOD		LUT1-OUT(3)
17	14	PC2	EVOUT2						MOSI(3)(4)					
18	15	PC3							SS(3)		WO3(3)			LUT1-IN0

Notes:

1. Pin names are of type Pxn , with x being the PORT instance (A, B) and n the pin number. The notation for signals is $\text{PORT}_x\text{-PIN}_n$. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.
3. Alternate pin positions. For selecting the alternate positions, refer to section 15. PORTMUX - Port Multiplexer.
4. Alternate pins for SPI MISO and MOSI are respectively at PA7 and PA6 for 14-pin devices and PC1 and PC2 for 20-pin devices.

Table 5-2. PORT Function Multiplexing, Eight Pins

SOIC 8-Pin	Pin Name (1,2)	Other/Special	ADC0	AC0	DAC0	USART0	SPI0	TWI0	TCA0	TCB0	TCD0	CCL
6	PA0	RESET/UPDI	AIN0			XDIR	SS					LUT0-IN0
4	PA1		AIN1			TxD(3)	MOSI	SDA	WO1			LUT0-IN1
5	PA2	EVOUT0	AIN2			RxD(3)	MISO	SCL	WO2			LUT0-IN2
7	PA3	EXTCLK	AIN3	OUT		XCK	SCK		WO0/WO3			
8	GND											
1	VDD											
2	PA6		AIN6	AINN0	OUT	TxD	MOSI(3)			WO0	WOA	LUT0-OUT
3	PA7		AIN7	AINP0		RxD	MISO(3)		WO0(3)		WOB	LUT1-OUT

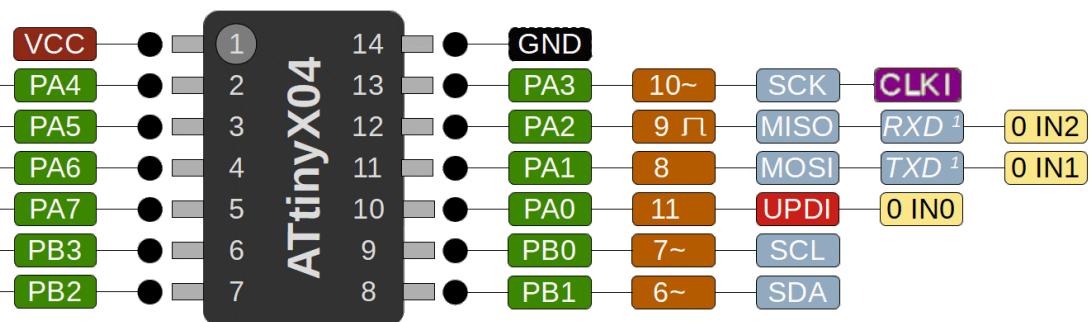
tinyAVR0 ATTiny1604



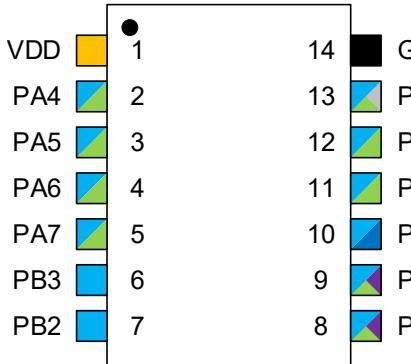
* ~ PWM
 Δ ASYNC INTERRUPT
¹ PERIPHERAL ALTERNATE LOCATION

megaTinyCore

https://github.com/SpenceKonde/megaTinyCore/blob/master/megaavr/extras/ATTiny_x04.md



14-pin SOIC150



Power

Input supply

Ground

GPIO on VDD power domain

Functionality

Reset, Programming

Clock, crystal

TWI

Digital function only

Analog function

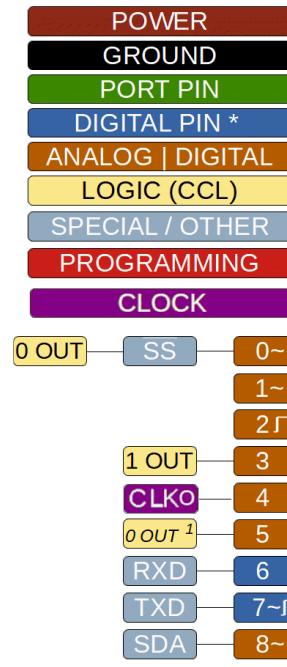
Note:

1. Pins names are of type Px_n, with x being the PORT instance (A, B) and n the pin number. Notation for signals is PORTx_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

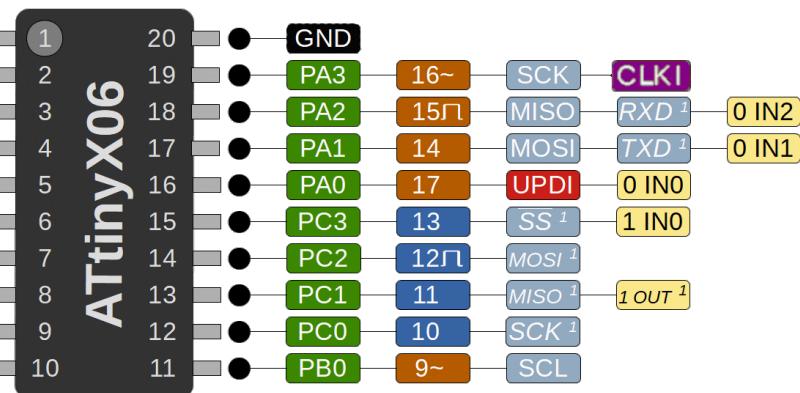
SOIC 14-pin	Pin Name ^(1,2)	Special	EXTINT _x	ADC ₀	AC ₀	USART ₀	SPI ₀	TWI ₀	TCA ₀	TCB ₀	Other	CCL	Scan
10	PA0	RESET, UPDI	S	AIN0								LUTO-IN0	RESET
11	PA1		S	AIN1		TXD	MOSI				BREAK	LUTO-IN1	
12	PA2		A	AIN2		RXD	MISO				EVOUT	LUTO-IN2	ENABLE
13	PA3	CLKI	S	AIN3		XCK	SCK		W03				CLOCK
14	GND												
1	VCC												
2	PA4		S	AIN4		XDIR	SS		W04			LUTO-OUT	SO2
3	PA5		S	AIN5	OUT				W05	W00			SO3
4	PA6		A	AIN6	AINN0								SI0/SER
5	PA7		S	AIN7	AINP0							LUT1-OUT	SO0/SER
	PB7		S										
	PB6		A										
	PB5		S	AIN8	AINP1				W02		CLKOUT		
	PB4		S	AIN9	AINN1				W01			LUT0-OUT	
6	PB3		S			RXD			W00				SO1/SER
7	PB2		A			TXD			W02		EVOUT		SI1/SER
8	PB1	I2C	S	AIN10		XCK	SDA	W01					S12
9	PB0	I2C	S	AIN11		XDIR	SCL	W00					S13
	PC0		S				SCK		W00				
	PC1		S				MISO					LUT1-OUT	
	PC2		A				MOSI				EVOUT		
	PC3		S				SS		W03			LUT1-IN0	
	PC4		S						W04			LUT1-IN1	
	PC5		S						W05			LUT1-IN2	



* ~ PWM
 ↳ ASYNC INTERRUPT
¹ PERIPHERAL ALTERNATE LOCATION

megaTinyCore

https://github.com/SpenceKonde/megaTinyCore/blob/master/megaavr/extras/ATTiny_x06.md



20-pin SOIC300

VDD	1	20	GND
PA4	2	19	PA3 (EXTCLK)
PA5	3	18	PA2
PA6	4	17	PA1
PA7	5	16	PA0 (RESET/UPDI)
PB5	6	15	PC3
PB4	7	14	PC2
PB3	8	13	PC1
PB2	9	12	PC0
PB1	10	11	PB0

Functionality

- Reset, Programming
- Clock, crystal
- TWI
- Digital function only
- Analog function

Power

- Input supply
- Ground
- GPIO on VDD power domain

5.1 Multiplexed Signals

Table 5-1. PORT Function Multiplexing

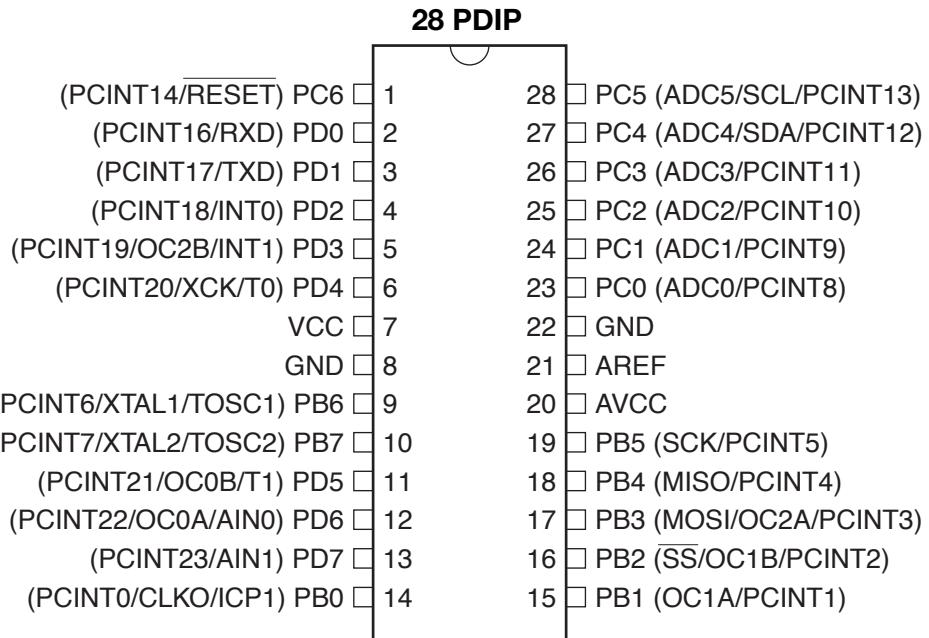
QFN20-Pin	SOIC20-Pin	Pin Name ^(1,2)	Special	ADC0	AC0	USART0	SPI0	TWI0	TCA0	TCB0	CCL
19	16	PA0	RESET / UPDI	AIN0							LUTO-IN0
20	17	PA1		AIN1		TxD ⁽³⁾	MOSI				LUTO-IN1
1	18	PA2	EVOUT	AIN2		RxD ⁽³⁾	MISO				LUTO-IN2
2	19	PA3	CLKI	AIN3		XCK ⁽³⁾	SCK		WO3		
3	20	GND									
4	1	VCC									
5	2	PA4		AIN4		XDIR ⁽³⁾	SS		WO4		LUTO-OUT
6	3	PA5		AIN5	OUT				WO5	WO0	
7	4	PA6		AIN6	AINN0						
8	5	PA7		AIN7	AINP0						LUT1-OUT
9	6	PB5	CLKOUT	AIN8	AINP1				WO2 ⁽³⁾		
10	7	PB4		AIN9	AINN1				WO1 ⁽³⁾		LUT0-OUT ⁽³⁾
11	8	PB3				RxD			WO0 ⁽³⁾		
12	9	PB2	EVOUT			TxD			WO2		
13	10	PB1		AIN10		XCK			WO1		
14	11	PB0		AIN11		XDIR		SDA	WO0		
15	12	PC0					SCK ⁽³⁾			WO0 ⁽³⁾	
16	13	PC1					MISO ⁽³⁾				LUT1-OUT ⁽³⁾
17	14	PC2	EVOUT				MOSI ⁽³⁾				
18	15	PC3					SS ⁽³⁾		WO3 ⁽³⁾		LUT1-IN0

Note:

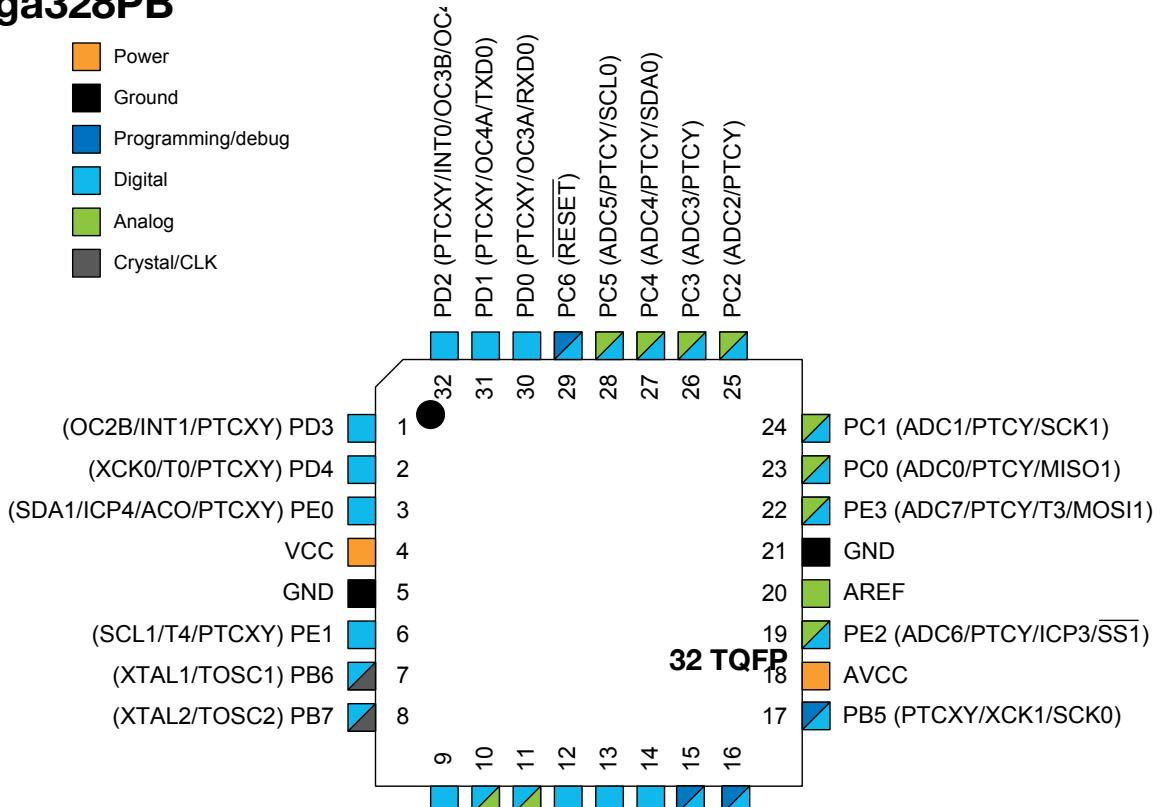
- Pins names are of type Px_n, with x being the PORT instance (A, B) and n the pin number. Notation for signals is PORTx_PINn. All pins can be used as event input.
- All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.
- Alternate pin positions. For selecting the alternate positions, refer to the PORTMUX documentation.

ATmega ATmega328P, PB

ATmega48A/PA/88A/PA/168A/PA/328/P

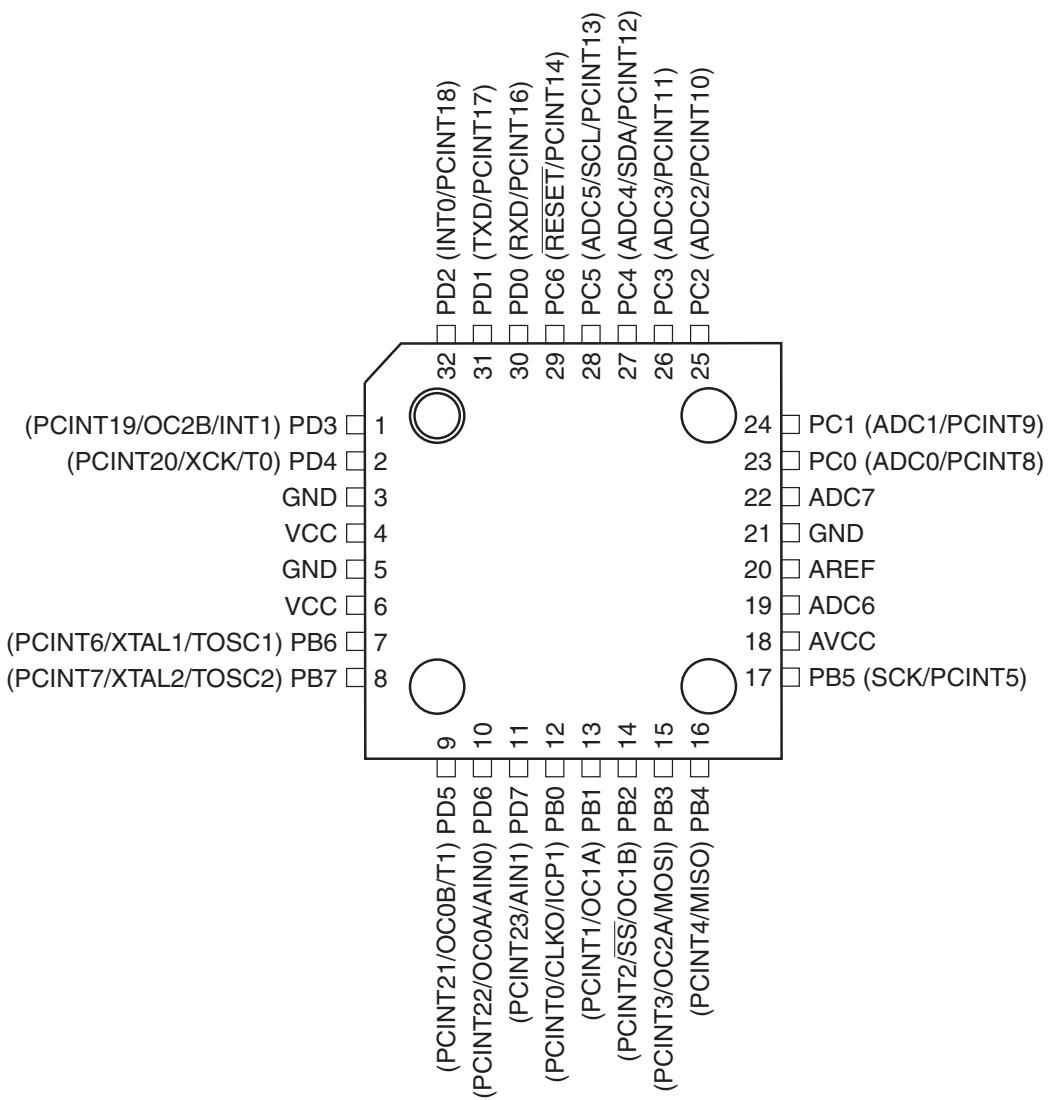


ATmega328PB



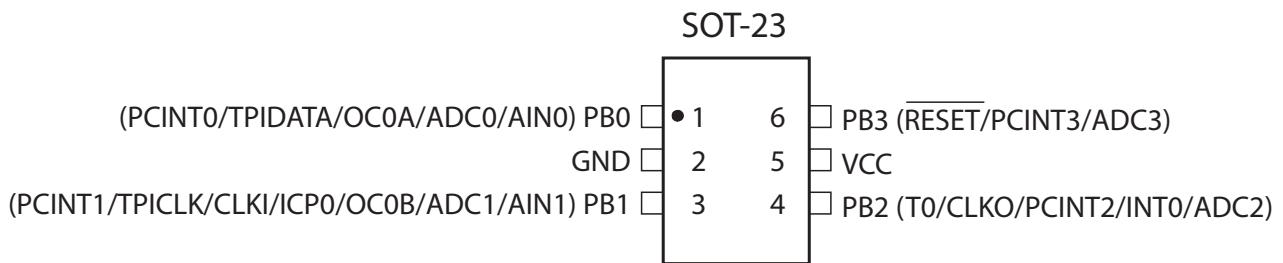
ATmega ATmega48

32 TQFP

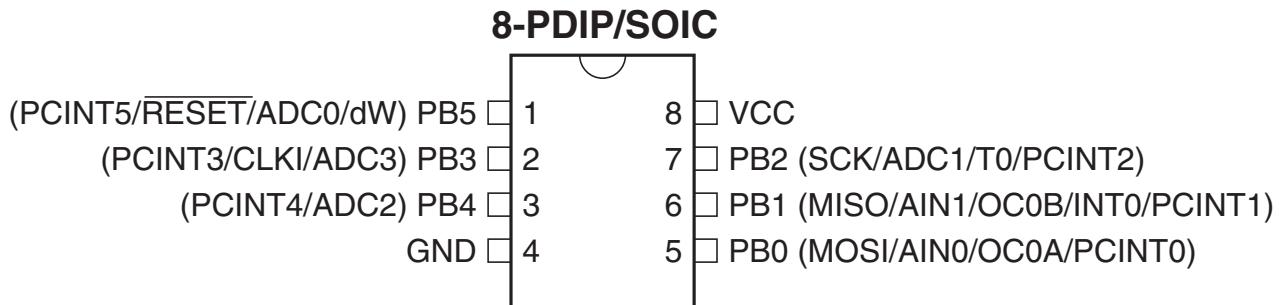


ATtiny

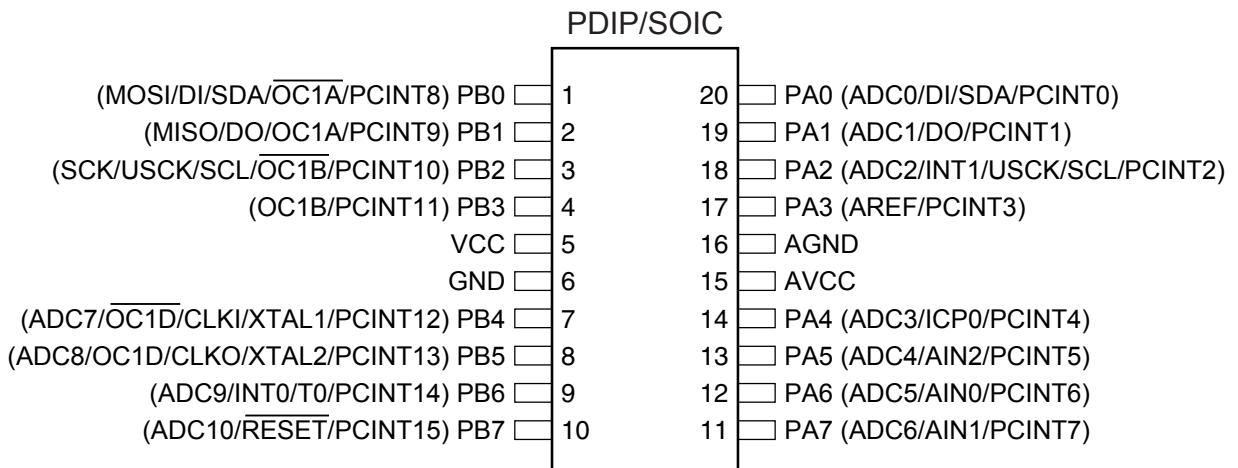
ATtiny4/5/9/10



ATtiny13A

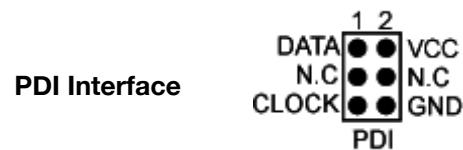
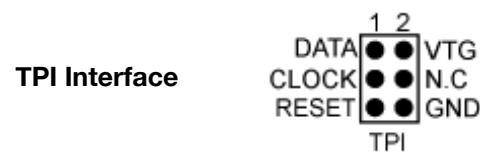


ATtiny261/461/861, ATtiny261V/461V/861V



AVRISPmk2

ターゲット側のピンを上から見た状態、AVRISPmk2の赤い線が1番ピン側

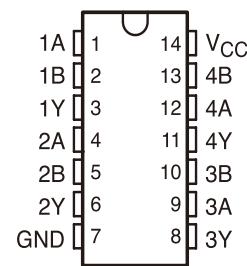


SN74HC00**QUADRUPLE 2-INPUT POSITIVE-NAND GATES****FUNCTION TABLE
(each gate)**

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H



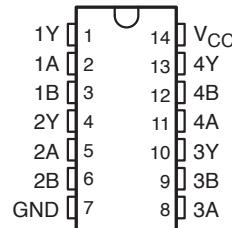
SN54HC00 . . . J OR W PACKAGE
SN74HC00 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

**SN74HC02****QUADRUPLE 2-INPUT POSITIVE-NOR GATES****FUNCTION TABLE
(each gate)**

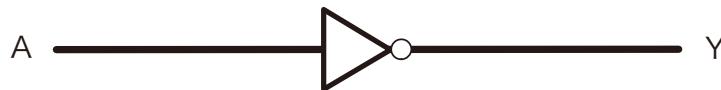
INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H



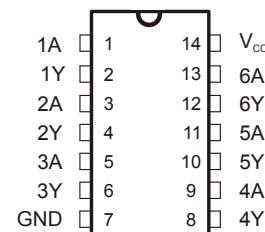
SN54HC02 . . . J OR W PACKAGE
SN74HC02 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

**SN74HC04****HEX INVERTERS****FUNCTION TABLE
(EACH INVERTER)**

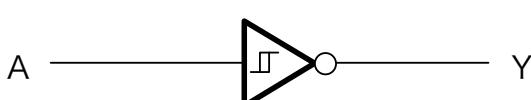
INPUT A	OUTPUT Y
H	L
L	H



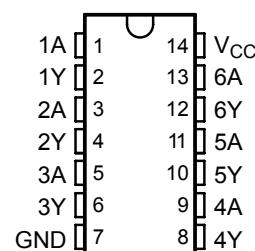
SN54HC04 . . . J OR W PACKAGE
SN74HC04 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

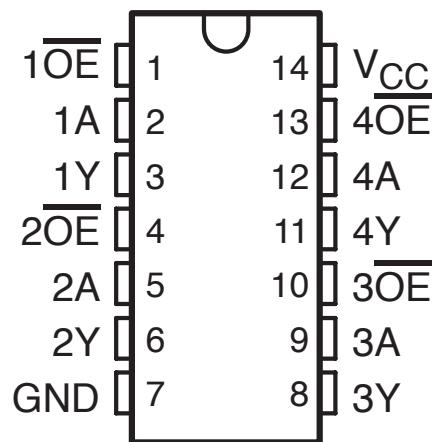
**SN74HC14****Hex Schmitt-Trigger Inverters****Function Table
(Each Inverter)**

INPUTS A	OUTPUT Y
H	L
L	H



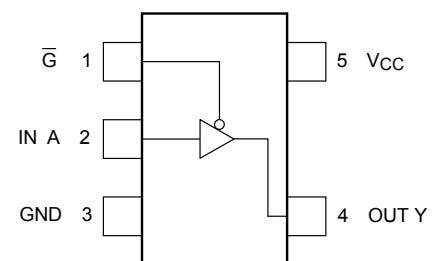
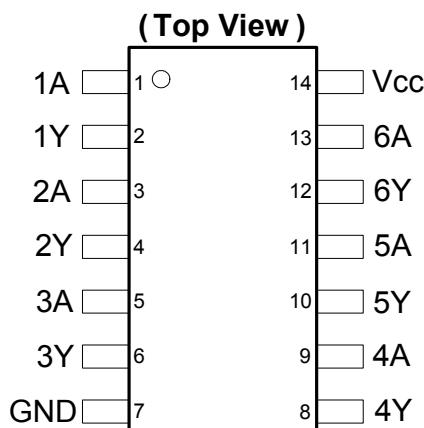
SN54HC14 . . . J OR W PACKAGE
SN74HC14 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



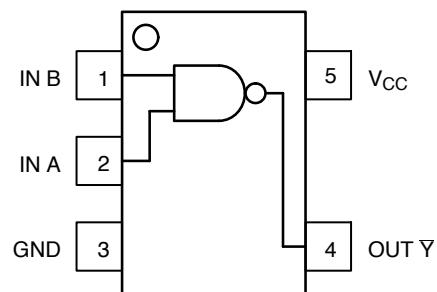
SN74HC125
**QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS**
**TC7SZ125F**
Bus Buffer 3-State Output
真理値表

Input		Output
A	\bar{G}	Y
X	H	Z
L	L	L
H	L	H

X: Don't Care
Z: High Impedance

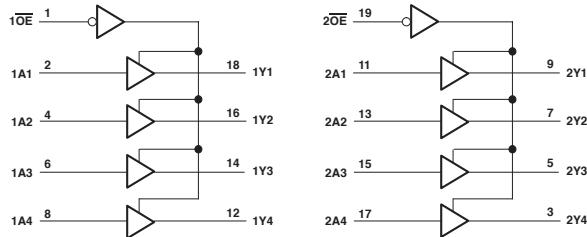
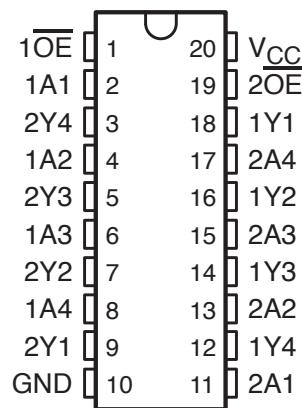
ピン接続図 (top view)
**74AHCU04****MC74VHC1G00**
UNBUFFERD HEX INVERTERS
Single 2-Input NAND Gate


SO-14 / TSSOP-14

**Figure 1. Pinout (Top View)**

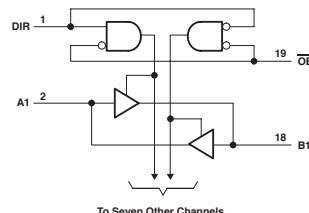
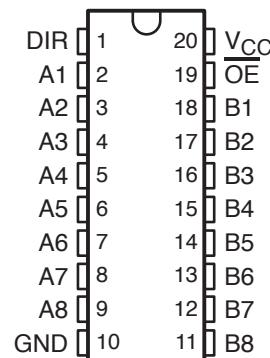
SN74HC244**OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS**FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

SN54HC244 . . . J OR W PACKAGE
SN74HC244 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)**SN74HC245****OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

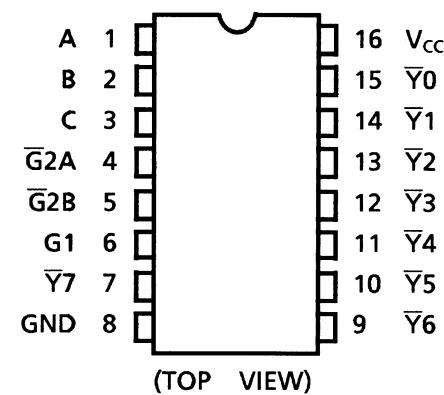
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54HC245 . . . J OR W PACKAGE
SN74HC245 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)**TC74HC138AP****3-to-8 Line Decoder**

Inputs			Outputs								Selected Output	
Enable		Select		\overline{Y}_0	\overline{Y}_1	\overline{Y}_2	\overline{Y}_3	\overline{Y}_4	\overline{Y}_5	\overline{Y}_6	\overline{Y}_7	
G1	$\overline{G}2A$	$\overline{G}2B$	C	B	A							
L	X	X	X	X	X	H	H	H	H	H	H	None
X	H	X	X	X	X	H	H	H	H	H	H	None
X	X	H	X	X	X	H	H	H	H	H	H	None
H	L	L	L	L	L	H	H	H	H	H	H	\overline{Y}_0
H	L	L	L	L	H	H	L	H	H	H	H	\overline{Y}_1
H	L	L	L	H	H	H	H	L	H	H	H	\overline{Y}_2
H	L	L	L	H	H	H	H	L	H	H	H	\overline{Y}_3
H	L	L	H	L	H	H	H	H	L	H	H	\overline{Y}_4
H	L	L	H	H	H	H	H	H	H	L	H	\overline{Y}_5
H	L	L	H	H	H	H	H	H	H	H	L	\overline{Y}_6
H	L	L	H	H	H	H	H	H	H	H	L	\overline{Y}_7

X: Don't care



(TOP VIEW)

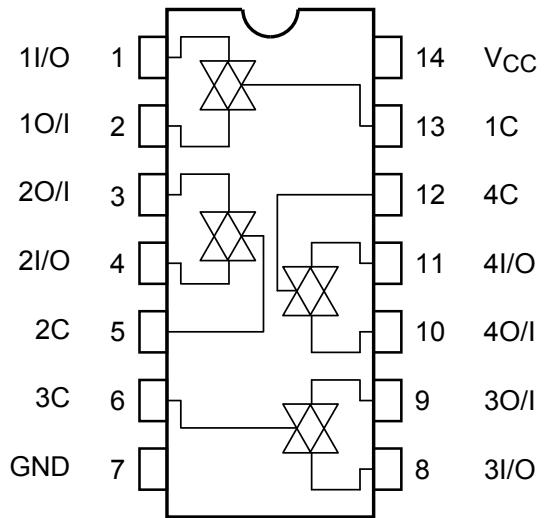
アナログスイッチ

TC74HC4066AP

Quad Bilateral Switch

真理値表

Control	Switch Function
H	On
L	Off



(top view)

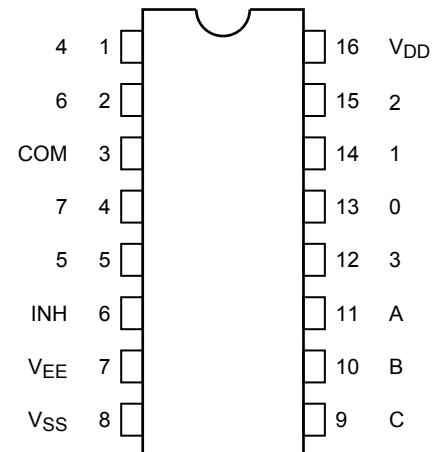
TC4051BP

Single 8-Channel Multiplexer/Demultiplexer

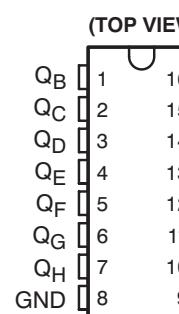
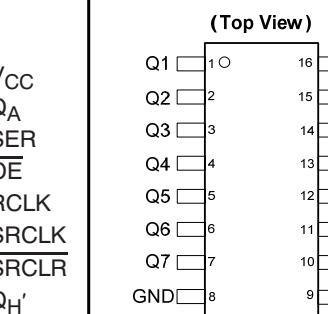
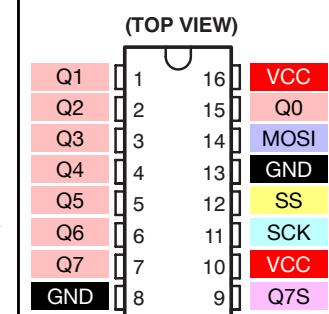
真理値表

Control Inputs				"ON" Channel		
Inhibit	C Δ	B	A	TC4051B	TC4052B	TC4053B
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	*	*	*	None	None	None

*: Don't care, Δ : Except TC4052B



- ・3本の出力を8本に増やす
- ・Q_{H'}, Q_{7S}から別のQ_A, Q₁に入れると出力をさらに増やすことができる
- ・ArduinoのSPIなどからコントロールできる

		74HC595		ATmegaへの接続(SPI)
ピン番号	Texas Instruments	NXP他		
	SN74HC595	74HC595		
ピンレイアウト	(TOP VIEW) 	(Top View) 	(TOP VIEW) 	
データ	14	SER	DS	MOSI
出力有効(負論理)	13	/OE	/OE	GND
クロック	11	SRCLK	SHCP	SCK(SRCK)
SSクロック	12	RCLK	STCP	SS
クリア(負論理)	10	/SRCLR	/MR	VCC

SN74HC164**8Bit Parallel-Out Shift Registers**

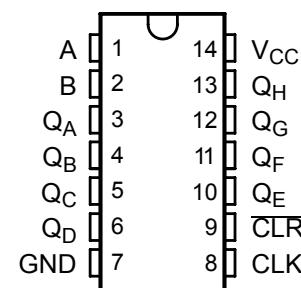
74HC595とは異なり、ストレージレジスタが搭載されていないため、変換中の状態が出力される。

FUNCTION TABLE⁽¹⁾⁽²⁾

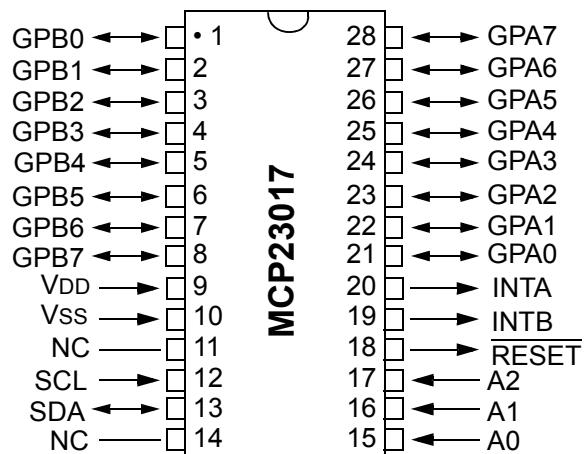
INPUTS				OUTPUTS			
CLR	CLK	A	B	Q _A	Q _B	...	Q _H
L	X	X	X	L	L	...	L
H	L	X	X	Q _{A0}	Q _{B0}	...	Q _{H0}
H	↑	H	H	H	Q _{An}	...	Q _{Gn}
H	↑	L	X	L	Q _{An}	...	Q _{Gn}
H	↑	X	L	L	Q _{An}	...	Q _{Gn}

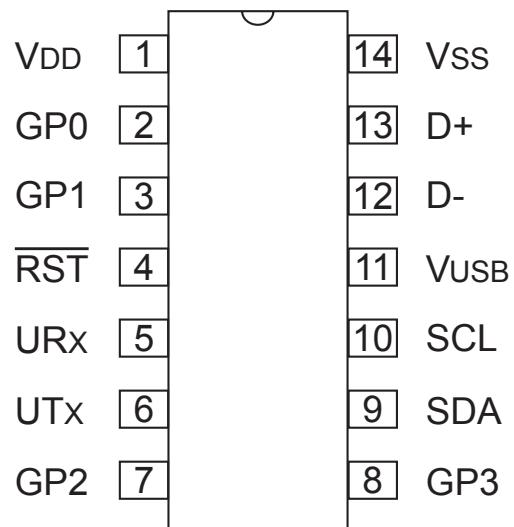
(1) Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

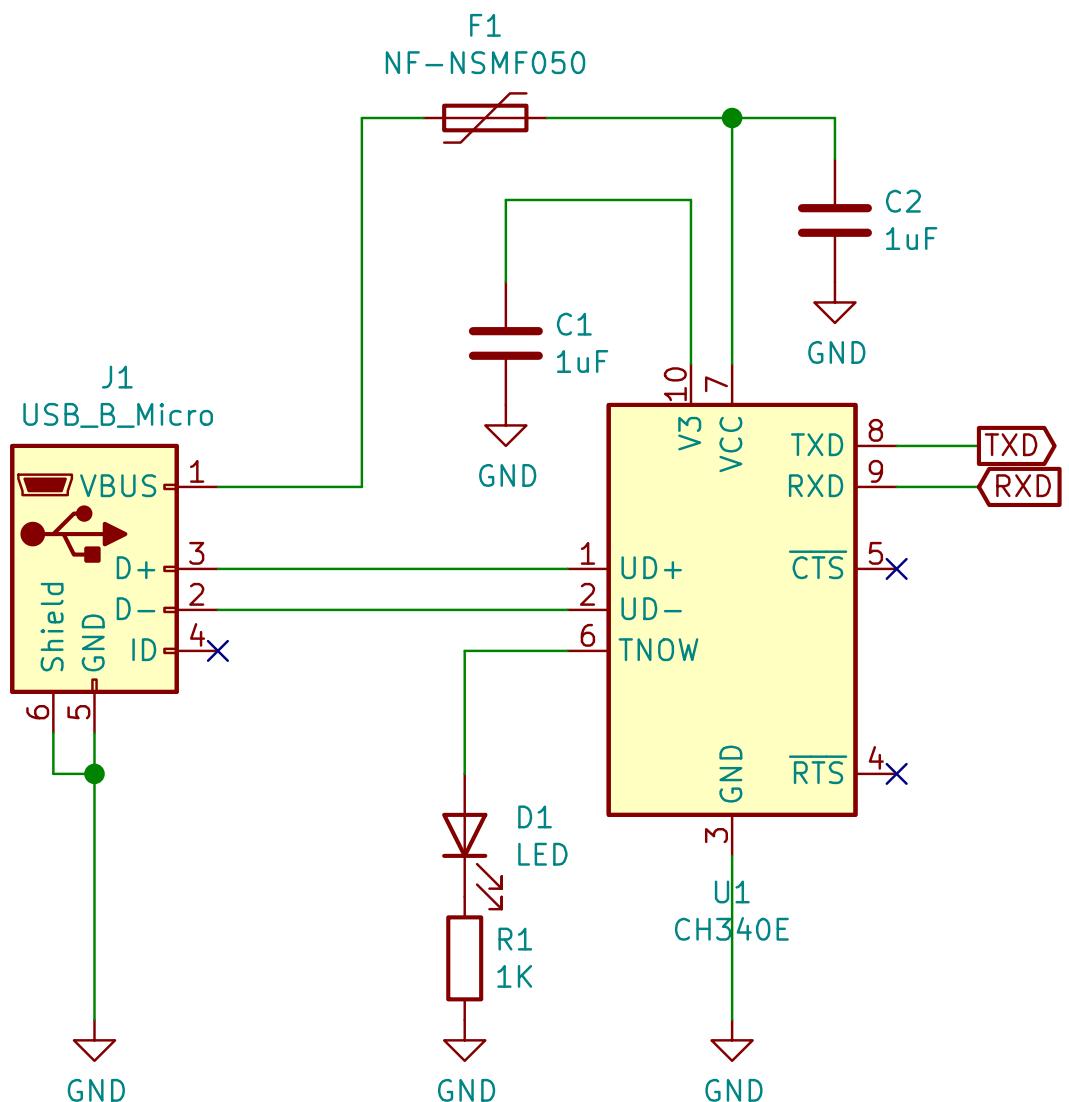
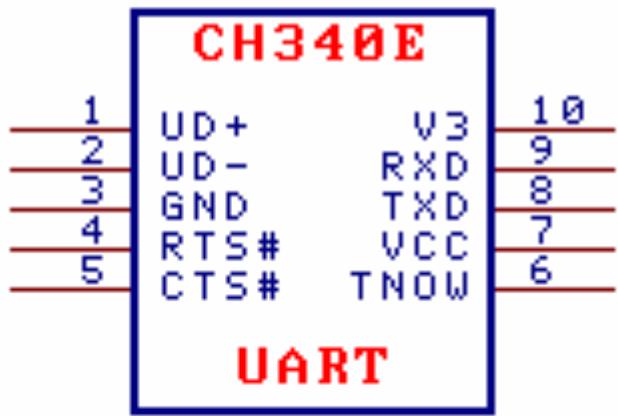
(2) Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of CLK: indicates a 1-bit shift.



SN54HC164...J OR W PACKAGE
SN74HC164...D, N, NS, OR PW PACKAGE
(TOP VIEW)



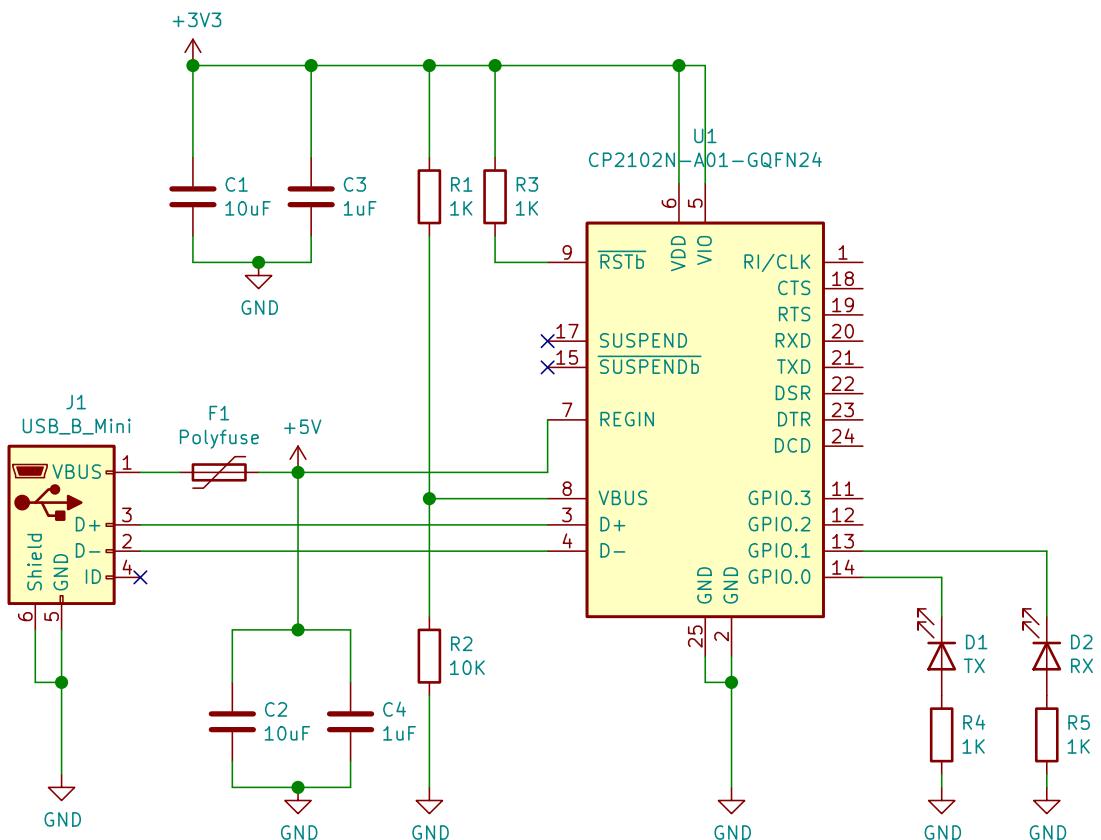
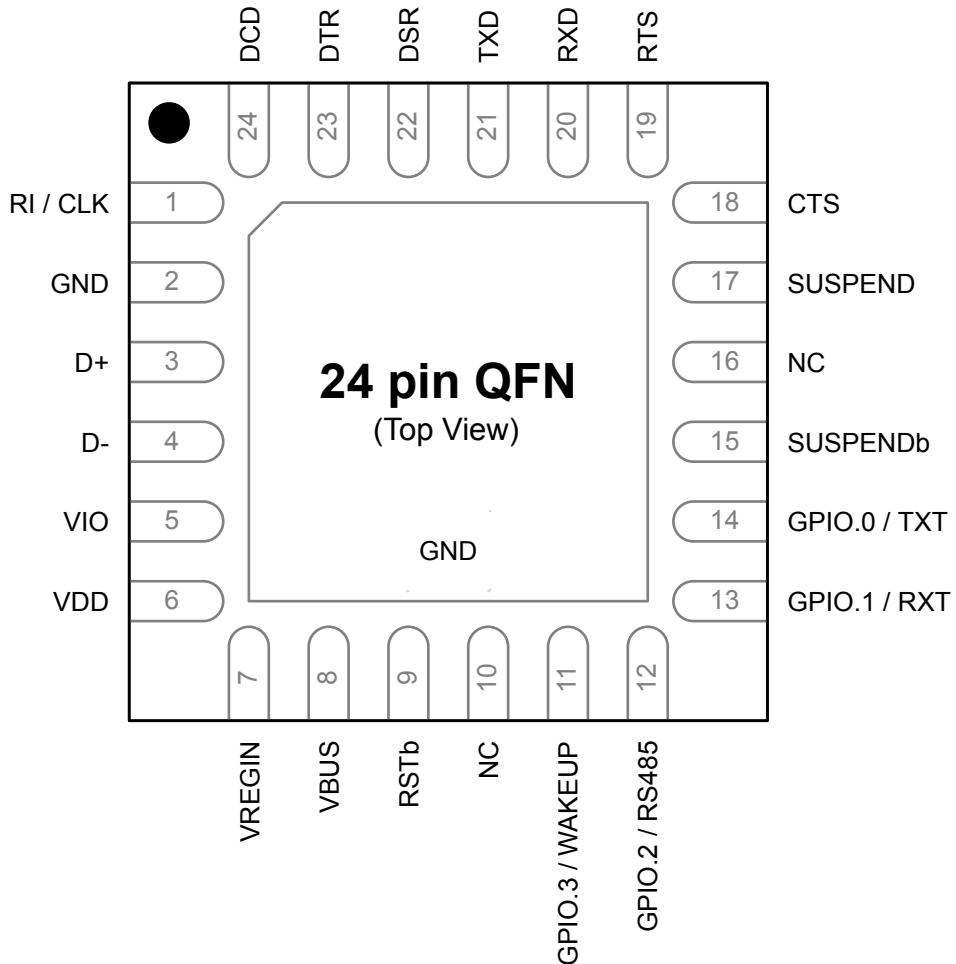




3.3Vで使用する場合はV3を3.3Vに接続すること

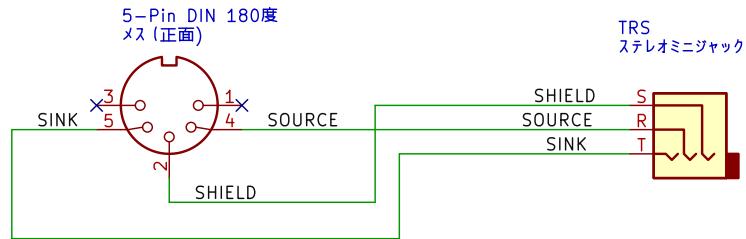
CP2102N-QFN24

QFN24



MIDI

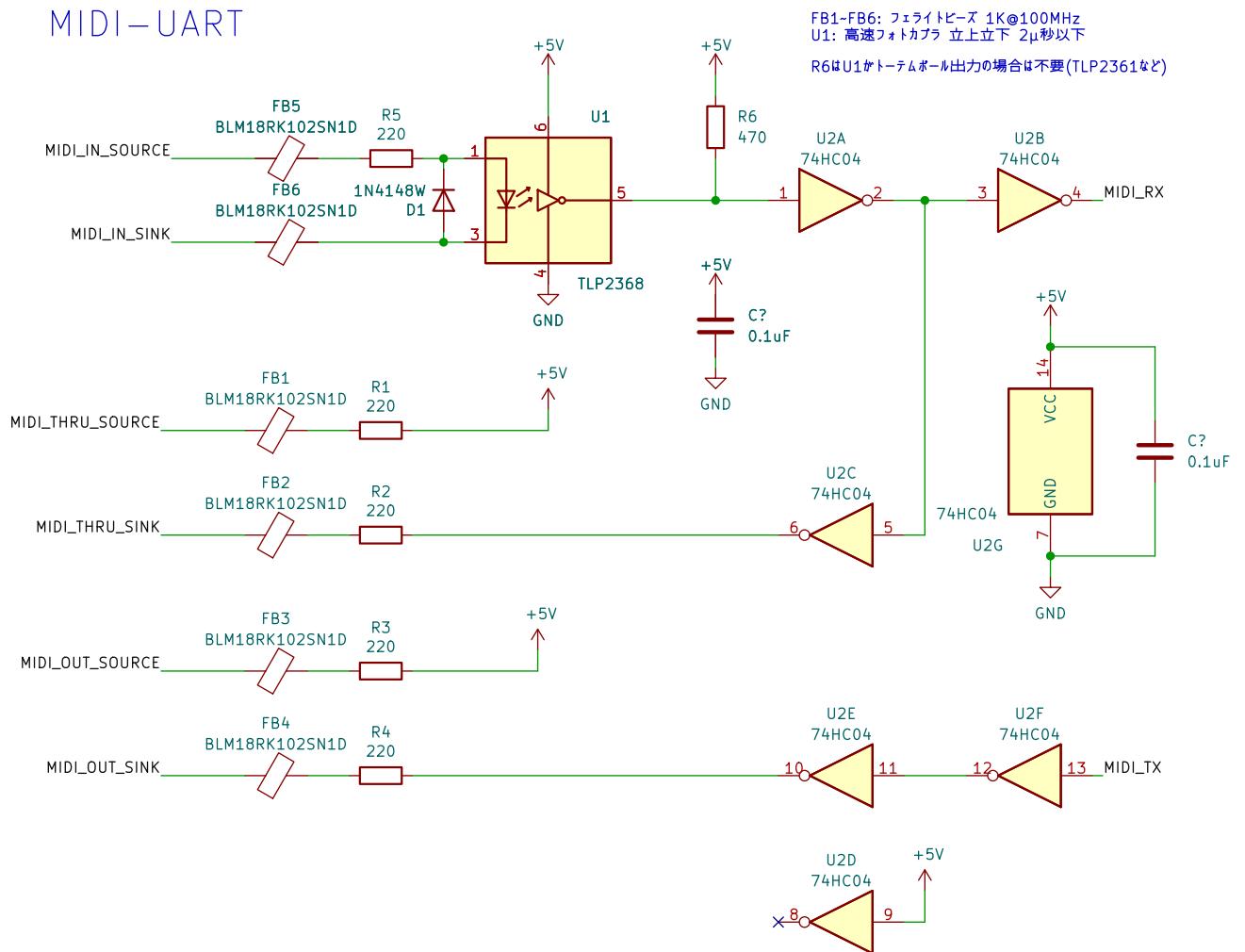
MIDI-TRS



	TRS	DIN
SINK	TIP	PIN 5
SOURCE	RING	PIN 4
SHIELD	SLEEVE	PIN 2

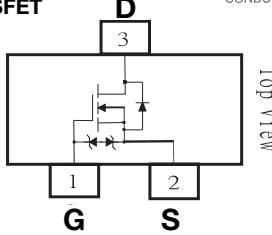
RP-054 TRS Connectors with MIDI Devices
(MIDI TRS Type-A)

MIDI-UART

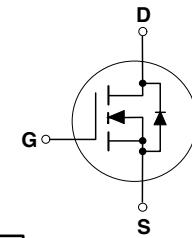
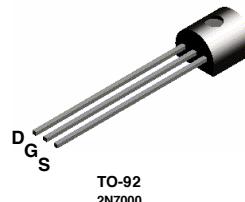


2N7002K**PANJIT**
SEMI
CONDUCTOR

Nch MOSFET

**2N7000****FAIRCHILD**
SEMICONDUCTOR™

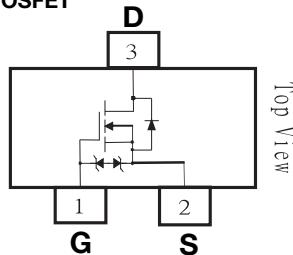
Nch MOSFET



Vds	60V
Vgs	+20V
Is	300mA
Vgs(th)	2.5V(max)
Rds(on)	4Ω(max)

BSS138**PANJIT**
SEMI
CONDUCTOR

Nch MOSFET

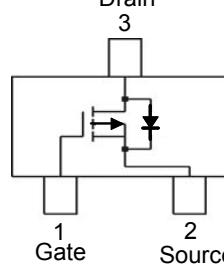


Vds	50V
Vgs	+20V
Is	300mA
Vgs(th)	0.8V ~ 1.5V
Rds(on)	2.8Ω(typ) 6Ω(max) 2.5V

BSS84**PANJIT**
SEMI
CONDUCTOR

Pch MOSFET

Drain

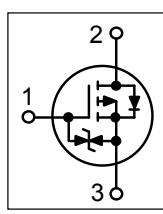
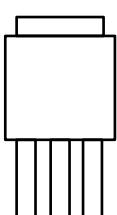


Vds	-50V
Idr	-130mA
Vgs(th)	-0.8V ~ -2.0V
Rds(on)	3.8Ω(typ) 10Ω(max)

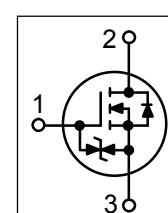
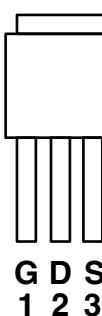
2SJ681**TOSHIBA**

Pch MOSFET

生産終了品

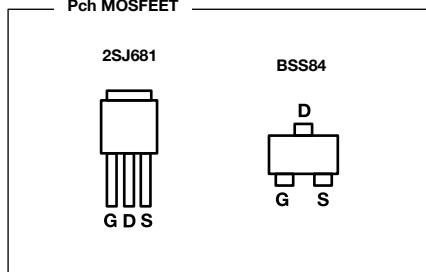
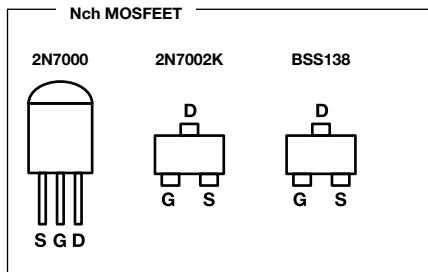
G D S
1 2 3**2SK4017****TOSHIBA**

Nch MOSFET

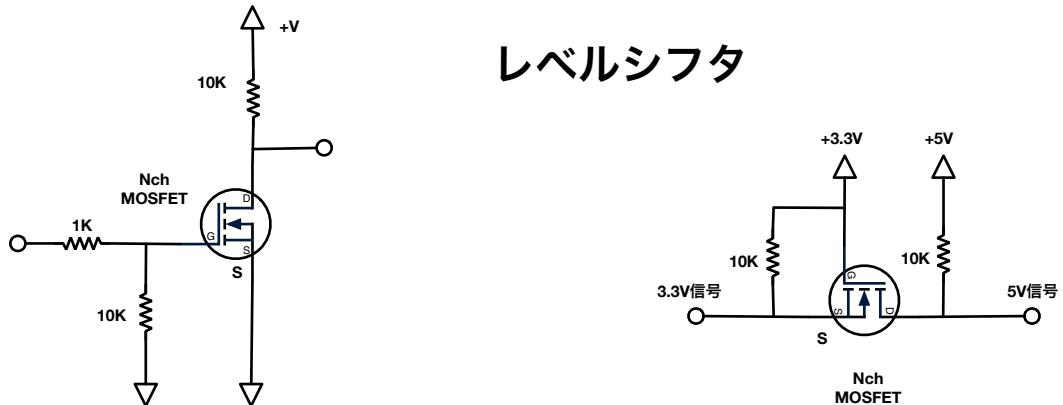
G D S
1 2 3

Vds	-60V
Idr	-5A
Vgs(th)	-0.8V ~ -2.0V
Rds(on)	0.25Ω(max)

Vds	60V
Id	5A
Vth	1.5V ~ -2.5V
Rds(on)	0.15Ω(max)



論理反転(NOT)



I²Cバス用レベルシフタ

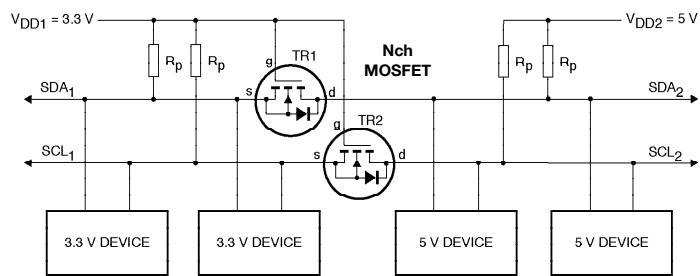
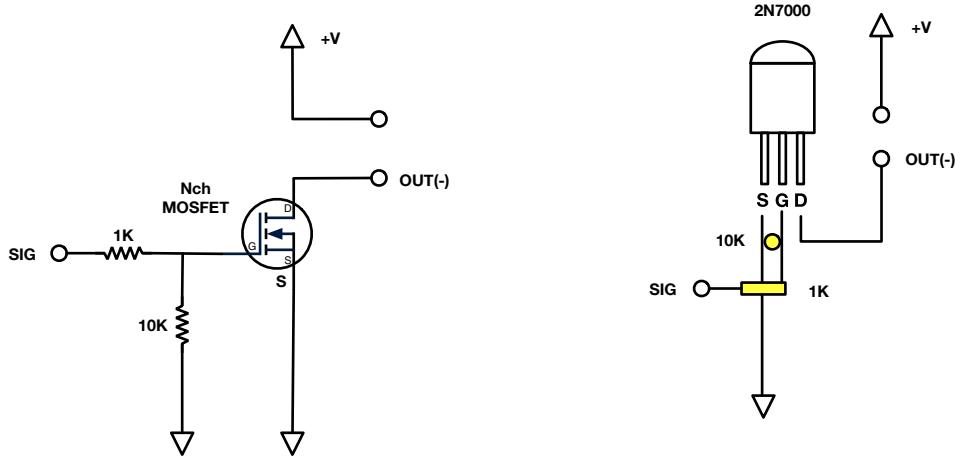


図45 I²Cバス・システム内の2箇所の異なった電源電圧に接続された双方向性レベル・シフタ回路

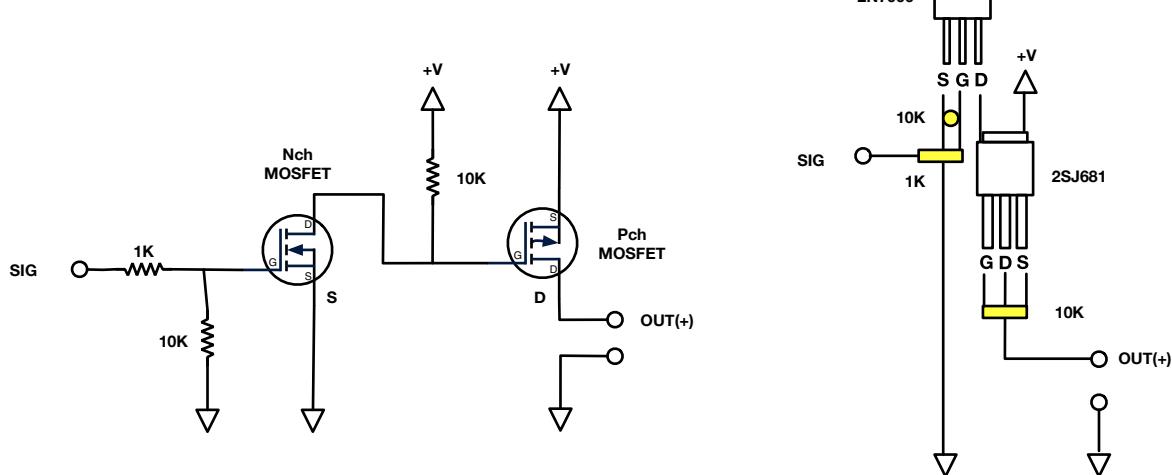
Philips セミコンダクタ i2c仕様書 Ver 2.1

ローサイドスイッチ



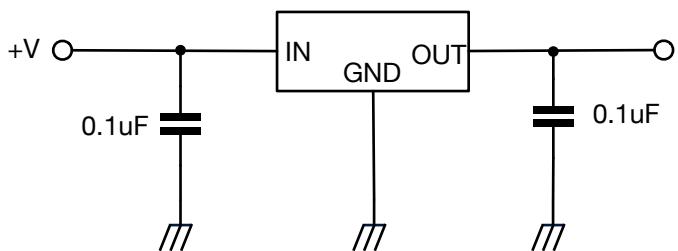
ブレッドボードでの配線

ハイサイドスイッチ



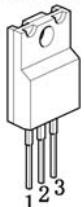
ブレッドボードでの配線

正電源用三端子レギュレータ



NJM7800FA

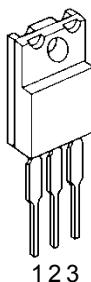
(TO-220F)



NJM7805FA	
最大入力	+35V
出力	+5V
電流	1.5A max.
ドロップ	だいたい3V

1.IN / 2.GND / 3.OUT

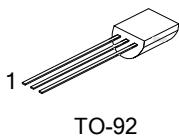
NJU7223



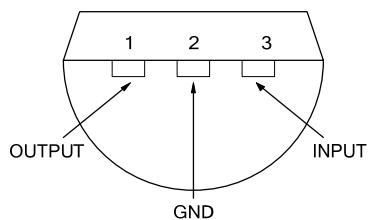
NJU7223F33	
最大入力	+18V
出力	+3.3V
電流	500mA max.
ドロップ	0.4V

1.OUT / 2.IN / 3.GND

LP2950



TO-92

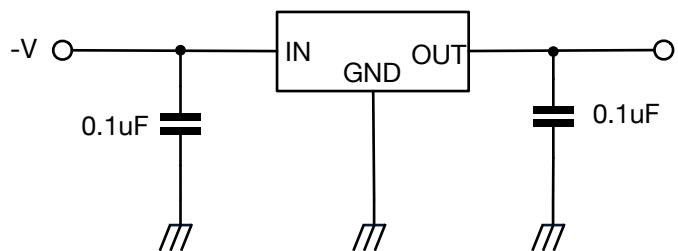


TO-92 Plastic Package Bottom View

LP2950L-3.3

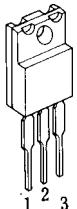
最大入力	+30V
出力	+3.3V
電流	100mA max.
ドロップ	0.45V

負電源用 三端子レギュレータ



NJM7900FA

(TO-220F)



NJM7905FA	
最大入力	-35V
出力	-5V
電流	1.5A max.
ドロップ	だいたい3V

1.COMMON / 2.IN / 3.OUT

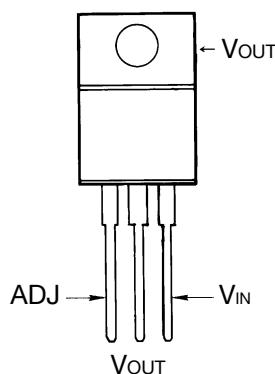
LM317, LM337 可変三端子レギュレータ

LM317, LM337	
最大入力	40V
出力	可変
電流	1.5A max.

LM317

正電源用

TO-220 (T)
Plastic Package

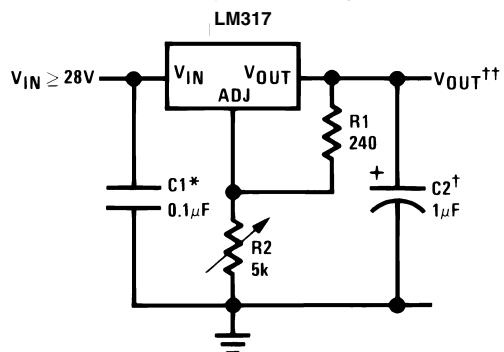


固定抵抗で
それっぽい電圧にする

V _{OUT}	R ₁	R ₂
1.5	330	68
1.6	240	68
2.5	470	470
3.03	330	470
3.37	330	560
5.05	370	820
9.06	240	1500
11.83	390	3300
15.31	240	2700

代表的なアプリケーション

1.2V-25V Adjustable Regulator



入出力の電圧差が大きい場合には出力電流を最大限にまで活用できません。

* 平滑フィルタが IC から 6 インチ以上離れている時に必要。

† トランジエント応答改善用コンデンサ。1 ~ 1000μF の電解またはタンタルコンデンサを追加すると出力インピーダンスとトランジエントを改善できる。

$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ}(R_2)$$

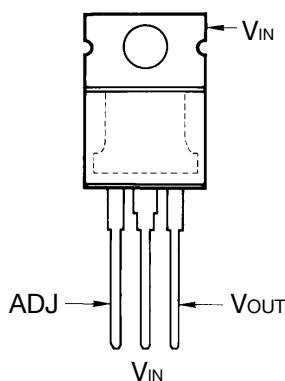
$$V_{OUT} = 1.25 \times (1 + R_2 / R_1)$$

$$(I_{ADJ} = 100\mu A)$$

LM337

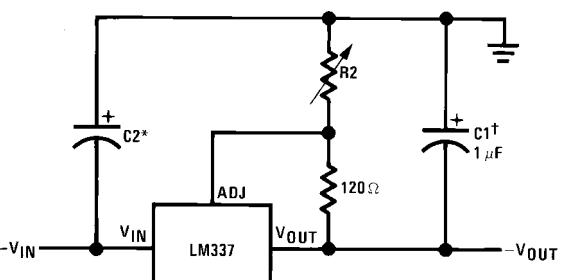
負電源用

TO-220
Plastic Package



代表的なアプリケーション

Adjustable Negative Voltage Regulator



入出力の電圧差が大きい場合には出力電流を最大限にまで活用できません。

$$-V_{OUT} = -1.25V \left(1 + \frac{R_2}{120} \right) + (-I_{ADJ} \times R_2)$$

† C1 = 1μF のタンタルまたは 10μF の電解コンデンサは安定を保つため必要です。

* C2 = 1μF のタンタルコンデンサは平滑フィルタが IC から 4 インチ (約 10cm) 以上離れている時に必要です。

出力側コンデンサには、タンタルまたは電解コンデンサ (1 ~ 1000μF) を出力インピーダンスとトランジエント改善のため使用してください。