Data mining

Chapter-3(II) (1)

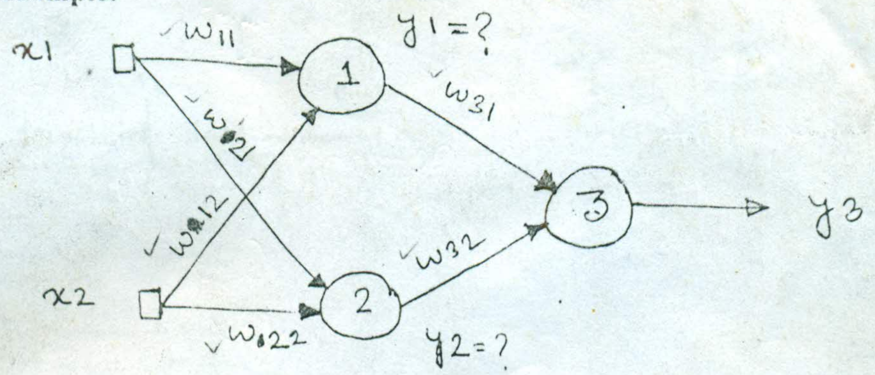
IT-08050

14-12-07

4 AI

ICT-4/2

Math Example:



Given, Synaptic Weight: W11=2, W12=1, ~~W21~~=-3, W22=4, W31=2, W32=-5 $W_{21} = -3$

Input: X1= 1

X2= 0

Transfer Function: Hard limiter or step φ(n) = 1 if n>=0

= 0 otherwise

Output: y=?

Solution:

Calculating the weight sum in first hidden layer: W_{12}

V1= W11*X1 + W12*X2 = 2*1 + 1*0 = 2

V2= W21*X1 + W22*X2 = -3*1 + 4*0 = -3

Applying transfer function:

Y1 = φ(2) = 1

Y2 = φ(-3) = 0

Hence, the input to the output layer (Node 3) is (1,0). Now, **calculating** the weighted sum of node 3

V3 = W31* Y1 + W32 * Y2 = 2*1 + (-5)*0 = 2

Applying transfer function: The output is

Y3 = φ(2) = 1

Problem1: The input to single input neuron is 2.0, its weight is 2.3 and its bias is -3.

i) What is the net input to the transfer function? (Ans: 1.6)

ii) What is the neuron output for the following Transfer function:

i) Hardlimit (1.0) ii) Linear (1.6) iii) Long-sigmoid (0.8320) $\equiv \left(\frac{1}{1+e^{-n\alpha}} \right.$, here, $\left. \alpha = 1 \right)$

Problem 2: Given a Two-input neuron with the following parameters: b= 1.2, W=[3 2] and Input p= [-5 6]', Calculate the neuron output for the following transfer function.

i) A symmetric hard limit transfer function. (Ans: -1)

ii) A saturating linear transfer function. (Ans: 0)

iii) A hyperbolic tangent sigmoid transfer function. (Ans: -0.9468)

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⏭ N.B. Try to solve using MATLAB.
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Neural networks as directed graphs:

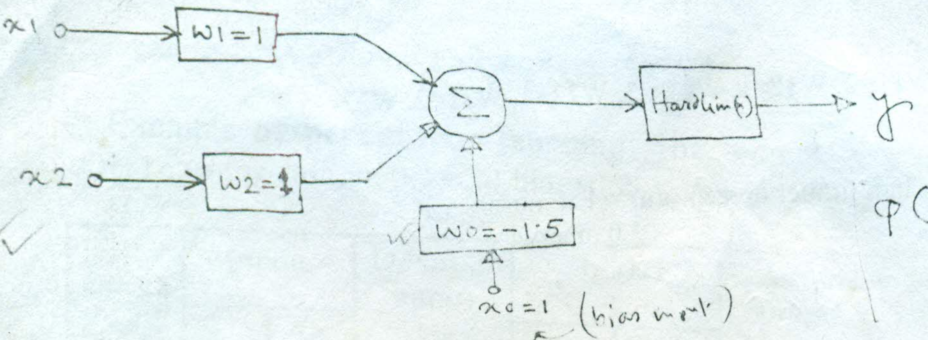
Kawsar Ahmed.

Design of ANN for logical operation AND/OR/NOT.

Logical AND:

$x1$	$x2$	$y = x1 . x2$
0	0	0
0	1	0
1	0	0
1	1	1

N.B. - Remember that *[bias input = −1.5]



$$\varphi(n) = 1 \quad ; n \geq 0$$
$$= 0 \quad n < 0$$

Now, input $x1=0$ and $x2=0$

$n = 0\times1 + 0\times1 - 1.5\times1 = -1.5$ $\quad [\therefore \varphi(-1.5) = 0]$

input $x1=0$ and $x2=1$

$n = 0\times1 + 1\times1 - 1.5\times1 = -0.5$ $\quad \therefore \varphi(-0.5) = 0$

input $x1=1$ and $x2=0$

$n = 1\times1 + 0\times1 - 1.5\times1 = -0.5$ $\quad \therefore \varphi(-0.5) = 0$

Finally, input $x1=1$ and $x2=1$

$n = 1\times1 + 1\times1 - 1.5\times1 = 0.5$ $\quad \therefore \varphi(0.5) = 1$

That is, this neural Network satisfies the truth table of logic AND gate.

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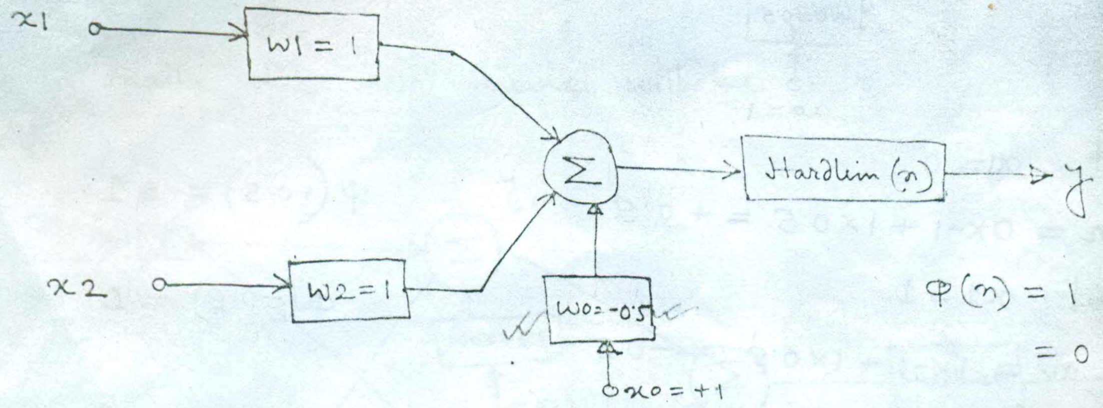
logical OR:

$x1$	$x2$	$y = x1 \oplus x2$
0	0	0
0	1	1
1	0	1
1	1	1

N.B) **bias input = −0.5**



$\varphi(n) = 1 \;;\; n \geq 0$

$\quad\;\; = 0 \;;\; n < 0$

Now . Input $x1 = 0$ and $x2 = 0$

$n = 0 \times 1 + 0 \times 1 - 0.5 \times 1 = -0.5$ $\qquad \varphi(-0.5) = 0$

Input $x1 = 0$ and $x2 = 1$

$n = 0 \times 1 + 1 \times 1 - 0.5 \times 1 = 0.5$ $\qquad \varphi(0.5) = 1$

Input $x1 = 1$ and $x2 = 0$

$n = 1 \times 1 + 0 \times 1 - 0.5 \times 1 = 0.5$ $\qquad \varphi(0.5) = 1$

Finally, Input $x1 = 1$ and $x2 = 1$

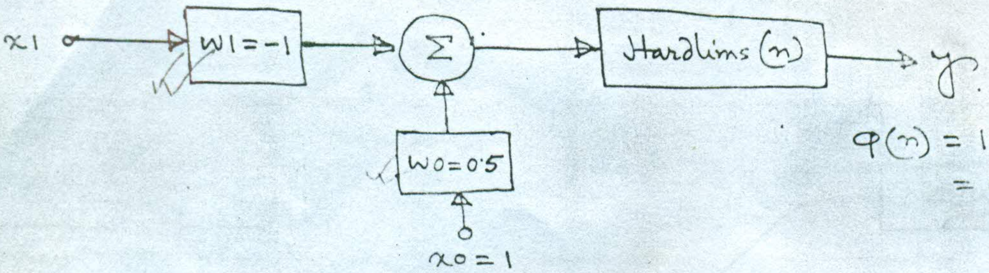
$n = 1 \times 1 + 1 \times 1 - 0.5 \times 1 = 1.5$ $\qquad \varphi(1.5) = 1$

It is found that the abone artificial Neural Network satifies The logical OR gate truth table

☒ Logical NOT:

N.B **bias input 0.5** **

x_1	$y = \bar{x}_1$
0	1
1	0



$\varphi(n) = 1 \quad ; \quad n \geq 0$
$\quad\;\; = 0 \quad ; \quad n < 0$

Input $x_1 = 0$.

$n = 0 \times -1 + 1 \times 0.5 = +0.5$

$\varphi(+0.5) = 1$

Input $x_1 = 1$

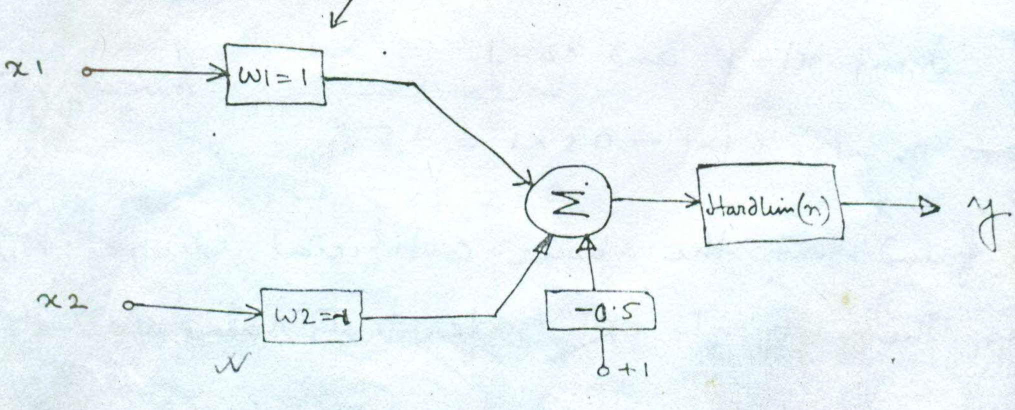
$n = 1 \times -1 + 1 \times 0.5 = -0.5$

$\varphi(-0.5) = 0$

☒ Logical XOR:

a	b	$\bar{a}$	$\bar{b}$	$y_1 = \bar{a}.b$	$y_2 = a.\bar{b}$	$y = \bar{a}.b + a.\bar{b}$
0	0	1	1	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0

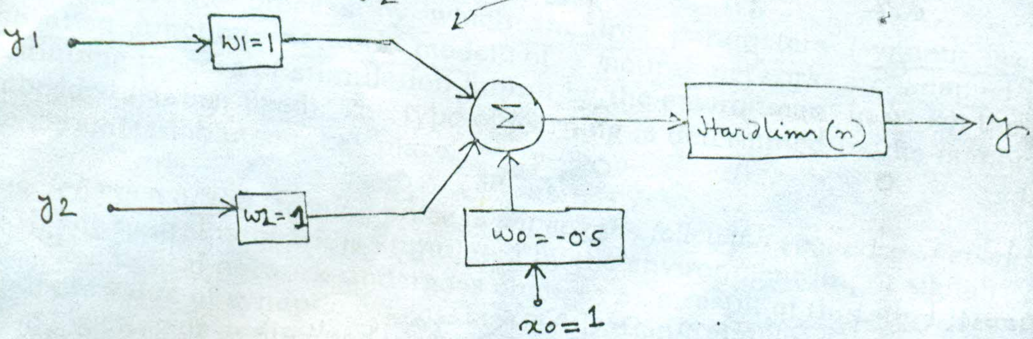
Now, $\boxed{y_1 = \bar{a}.b \quad \text{and} \quad y_2 = a.\bar{b}}$



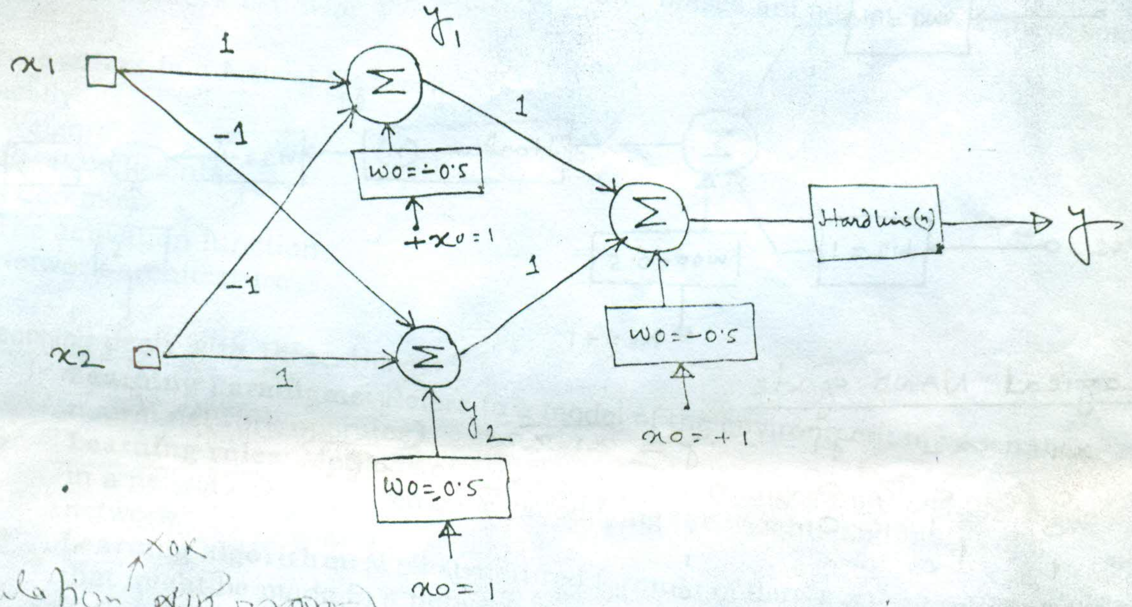
N:B XOR and OR [illegible] $\boxed{\text{bias input} = -0.5}$ **

$$y = \bar{a}.b + a.\bar{b}$$
$$= y_1 + y_2$$

that means simple OR circuit



Finally, the ANN model will be:



N.B → (Calculation $\overset{XOR}{\uparrow}$ [illegible] [illegible])

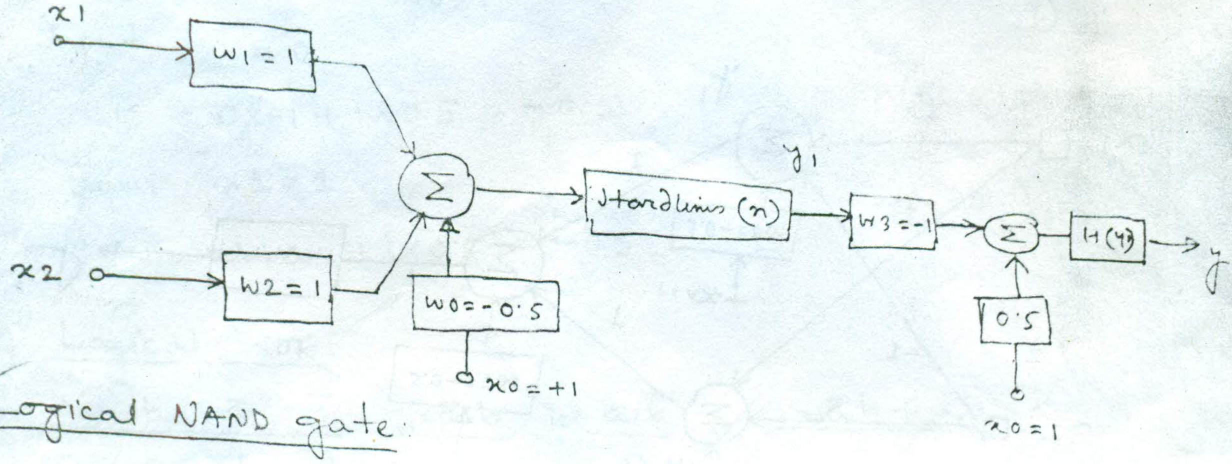
Question: Design ANN to perform the logical operation AND, OR, NOT and XOR.

Question: Design a ANN to perform the following logical operation
1) AND 2) OR 3) NOT 4) XOR 5) NOR 6) NAND.

logical NOR Gate:

x_1	x_2	y_1	$y = \overline{x_1 + x_2}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

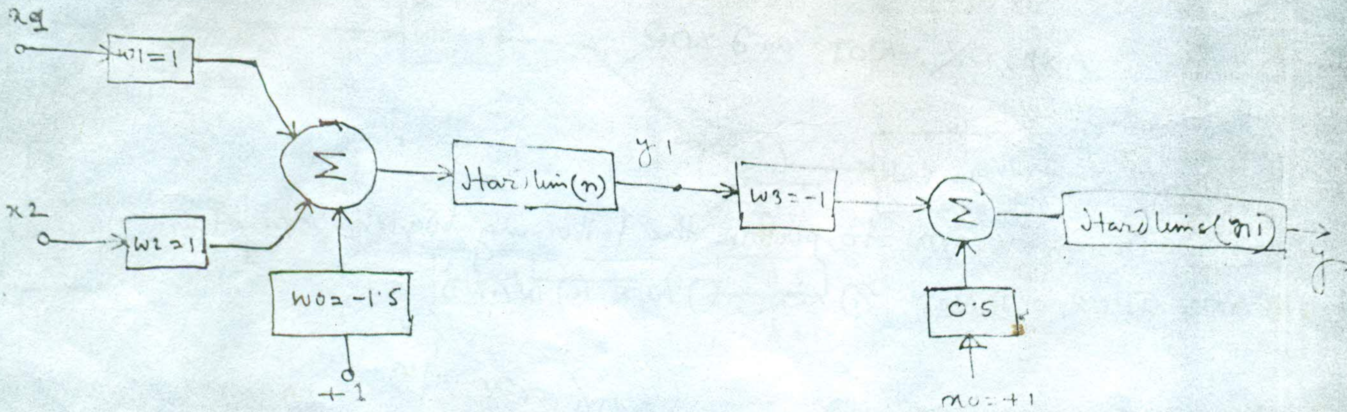
It is possible to design a NOR gate using OR and a NOT gate.



Logical NAND gate:

x_1	x_2	y_1	$y = \overline{x_1 . x_2}$
0	0	0	1
0	1	0	1
1	0	0	1.
1	1	1	0

It is possible to design a NAND gate using AND and a NOT gate.



Fig(a) - Logical NAND.