Novel Low-Power Multiplexer-Based 1-Bit Full Adder Circuit (MBA-12T)

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ABSTRACT

This paper introduces a novel low-power multiplexer-based 1-bit full adder circuit, MBA-12T, which utilizes 12 transistors. The circuit exhibits reduced transition activity and charge recycling capability, resulting in a significant reduction in short-current power consumption. Simulation results demonstrate that the MBA-12T consumes 26% less power than conventional 28-transistor CMOS adders and 23% less power than other 10-transistor adders, while operating 64% faster. These findings highlight the potential of the MBA-12T for building larger low-power high-performance VLSI systems. The performance evaluation of the MBA-12T adder suggests its suitability for applications requiring low-power consumption and high-speed operation in VLSI systems.

Keywords: Full adder, low power, multiplexer, very large-scale integrated (VLSI) circuit

I. INTRODUCTION

The introduction of the paper presents a novel low-power multiplexer-based 1-bit full adder circuit, referred to as MBA-12T, which utilizes 12 transistors. The circuit is designed to exhibit reduced transition activity and charge recycling capability, resulting in a significant reduction in short-current power consumption. The introduction highlights the simulation results, which indicate that the MBA-12T consumes 26% less power than conventional 28-transistor CMOS adders and 23% less power than other 10-transistor adders, while also operating 64% faster. Additionally, the introduction emphasizes the potential of the MBA-12T for building larger low-power high-performance VLSI systems.

II. METHODS

The methods used in the paper involved the proposal and simulation of the novel low-power multiplexer-based 1-bit full adder circuit, MBA-12T. The circuit was constructed using six identical multiplexers and a total of 12 transistors. HSPICE simulations were performed to evaluate the MBA-12T and compare it with five other adders, including the 28-transistor complementary CMOS, SERF, and 10T adders. The simulations were carried out using a comprehensive input signal pattern to cover every possible transition for a 1-bit full adder. The technology used for the simulations was 0.35-um CMOS digital technology with a 3.3-V supply voltage.

The testing results showed that the MBA-12T consumes 26% less power than conventional 28-transistor CMOS adders and 23% less power than the most power-efficient 10-transistor adders. Additionally, the MBA-12T was found to be 64% speedier than the fastest of all other tested adders. These findings suggest that the MBA-12T is suitable for building larger low-power high-performance VLSI systems.

III. SCHEMATIC, OUTPUT WAVEFORM AND LAYOUT OVER CADENCE VIRTUOSO

A. New MBA(Multiplexer Based Full Adder)-12 Transistor Full Adder (20200105196)

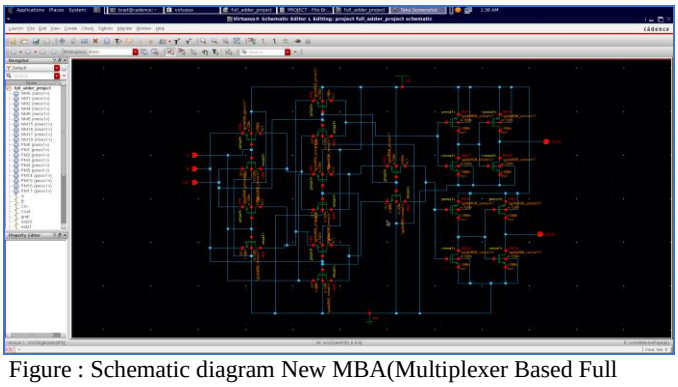

Figure : Schematic diagram New MBA(Multiplexer Based Full Adder)-12 Transistor Full Adder

Figure : Output waveshape New MBA(Multiplexer Based Full Adder)-12 Transistor Full Adder without buffer.

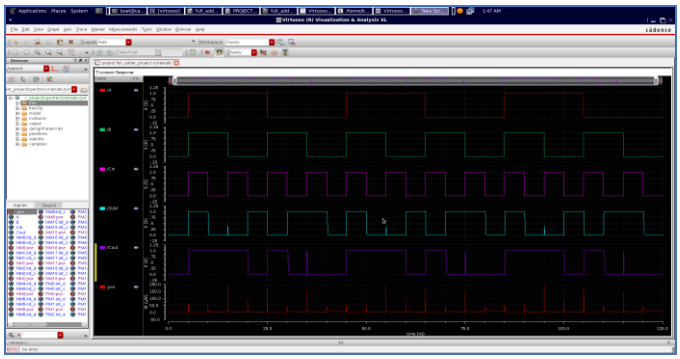

Figure : Output waveshape of New MBA(Multiplexer Based Full Adder)-12 Transistor Full Adder MBA with buffer.

Figure : Layout for 12-T MBA

SIMULATION RESULT	
Propagation Delay	40.67E-12 s
Avg. Power Without Buffer	13.11E-3 W
Average Power with Buffer	5.202E-6 W
Power Delay Product	2.114E-16 Ws
Cell Area	52.446E-6 μm^2
No. of Transistor without Buffer	12
No. of Transistor with Buffer	20
No. of DRC Error	0
No. of LVS Error	0

B. Full Adder using intermediate XNOR (A,B) Signal-I. (20200105201)

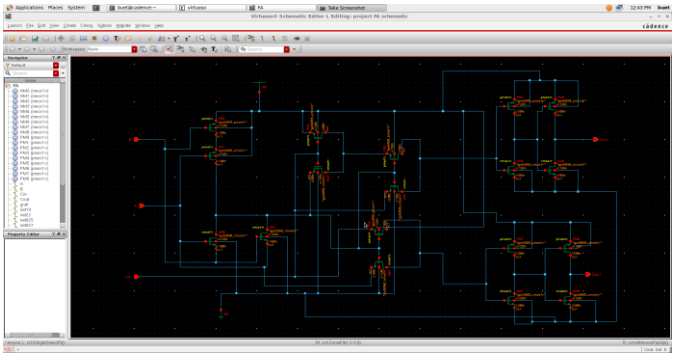

Figure : Schematic diagram of Full Adder using intermediate XNOR (A,B) Signal-I

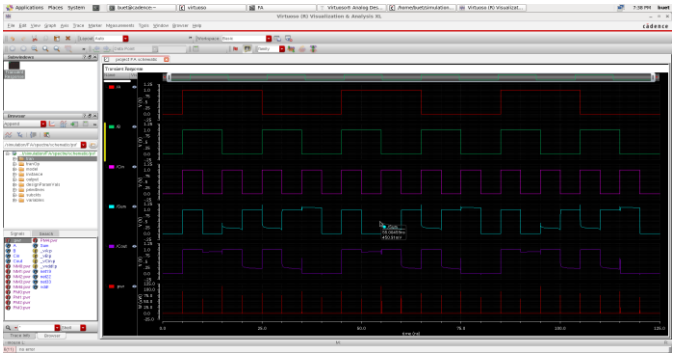

Figure : Output waveshape Full Adder using intermediate XNOR (A,B) Signal-I without buffer.

Figure : Output waveshape Full Adder using intermediate XNOR (A,B) Signal-I with buffer.

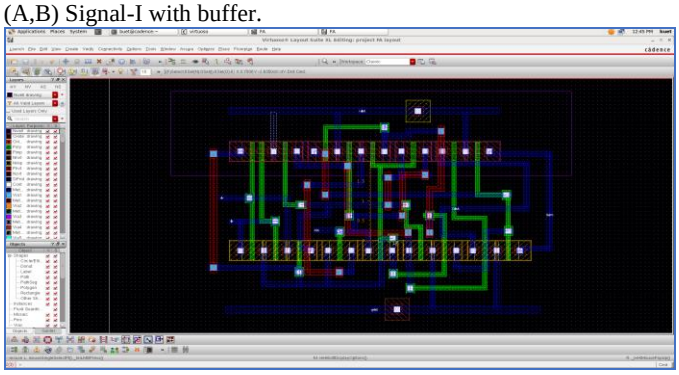

Figure : Layout of Full Adder using intermediate XNOR (A,B) Signal-I

IV. RESULT COMPARISON

Result Comparison		
	12-T MBA	Intermediate X-NOR-I
Propagation Delay	40.67E-12 s	51.32E-12 s
Avg. Power Without Buffer	13.11E-3 W	168.4E-9 W
Average Power with Buffer	5.202E-6 W	2.44E-6 W
Power Delay Product	2.114E-16 Ws	1.973E-16 Ws
Cell Area	52.446E-6 μm^2	38.677E-6 μm^2
No. of Transistor without Buffer	12	10
No. of Transistor with Buffer	20	18
No. of DRC Error	0	0
No. of LVS Error	0	0

V. CONCLUSION

The novel low-power multiplexer-based 1-bit full adder circuit, MBA-12T, utilizing 12 transistors, demonstrates reduced transition activity and charge recycling capability, resulting in a significant reduction in short-current power consumption. Simulation results indicate that the MBA-12T consumes 26% less power than conventional 28-transistor CMOS adders and 23% less power than other 10-transistor adders, while operating 64% faster. These findings highlight the potential of the MBA-12T for building larger low-power high-performance VLSI systems, making it a promising advancement in the field of circuit design.

VI. REFERENCES

[1] R. Shalem, E. John, and L. K. John, "A novel low-power energy recovery full adder cell," in Proc. Great Lakes Symp. VLSI, Feb. 1999, pp. 380–383.

[2] A. P. Chandrakasan, S. Sheng, and R. W. Broderson, "Low-power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp. 473–483, Apr. 1992.

[3] R. Pedram and M. Pedram, Low Power Design Methodologies. Norwell, MA: Kluwer, 1996.

[4] H. T. Bui, A. K. Al-Sheraidah, and Y. Wang, "Design and analysis of 10-transistor full adders using novel XOR-XNOR gates," in Proc. Int. Conf. Signal Processing 2000 (Wold Computer Congress), Beijing, China, Aug. 2000.

[5] J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J. Solid-State Circuits, vol. 29, pp. 780–786, July 1994.

[6] N. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A System Perspective. Reading, MA: Addison-Wesley, 1993.

[7] R. Zimmermannn and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, pp. 1079–1090, July 1997.

[8] Y. Jiang, Y. Wang, and J. Wu, "Comprehensive Power Evaluation of Full Adders," Florida Atlantic Univ., Boca Raton, Tech. Rep., 2000. [9] Meta-Software, HSPICE User's Manual Version H9002, 1992