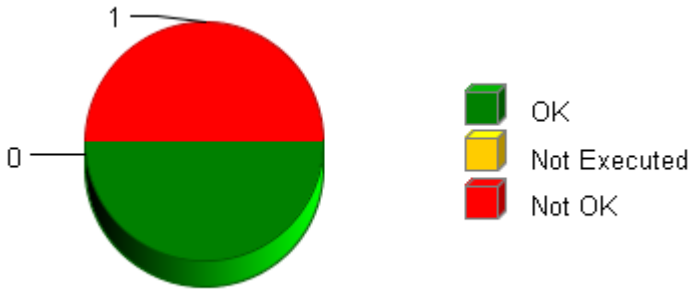
Summary

Total Test Objects:	2
Successful:	1
Failed:	1
Not Executed:	0
Date:	2015-09-01
Time:	17:22:46+0530

Overall Test Object Results (including Coverage)



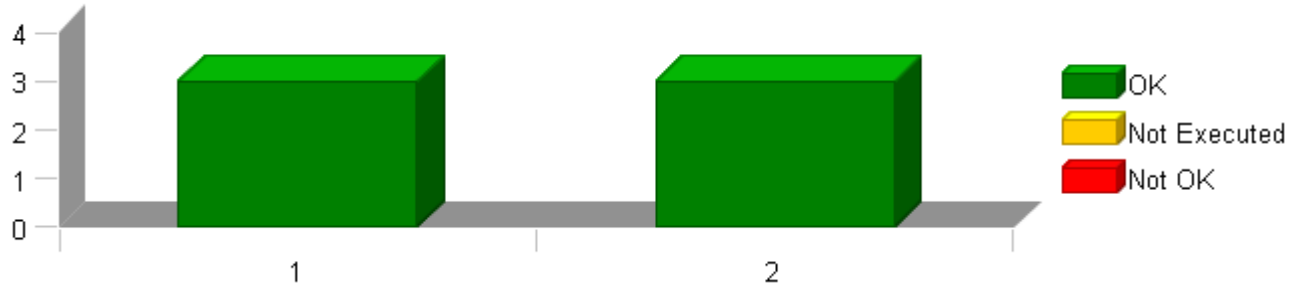
Selected Project Items

Test Object "CBD_UnitTest/StOpCtrl/StOpCtrl_Per1"
Test Object "CBD_UnitTest/StOpCtrl/TargetSelection"

Used Test Environments

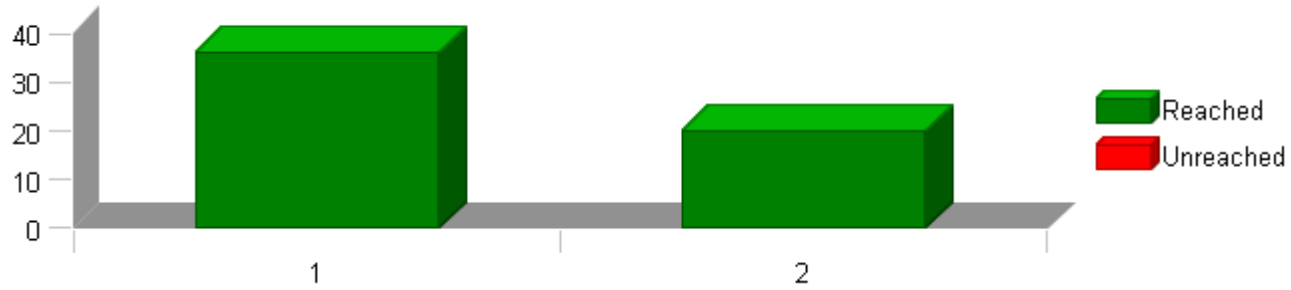
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



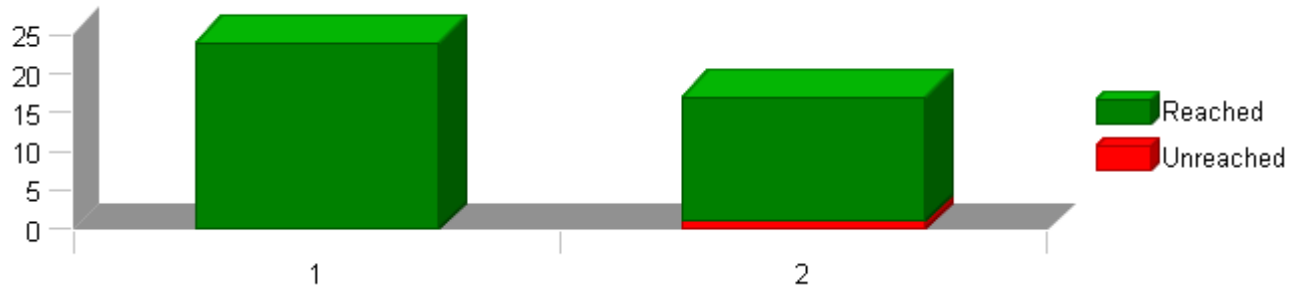
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



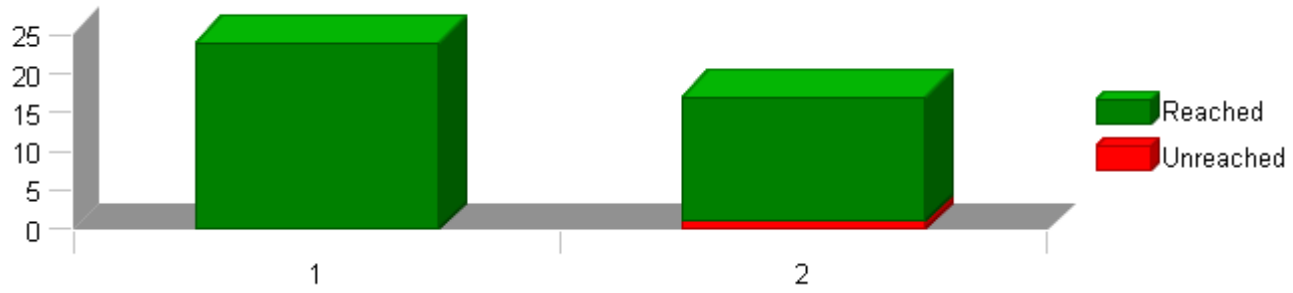
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

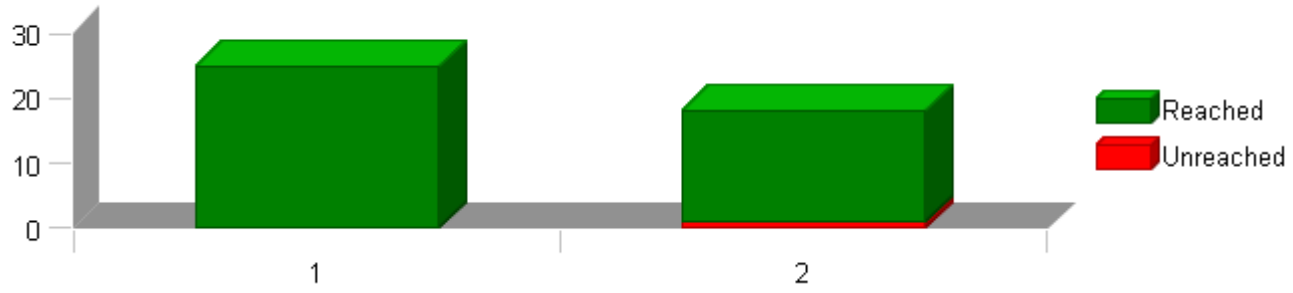
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

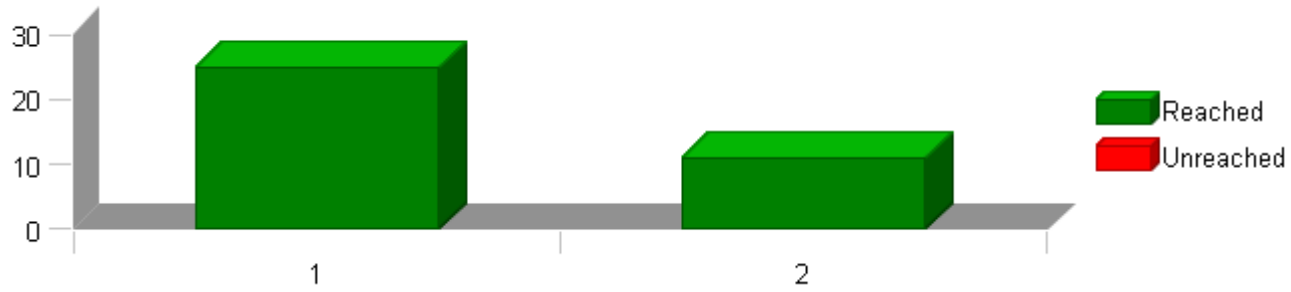
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	StOpCtrl	100 %	97.56 %	97.56 %	97.67 %	100 %	6 of 6 passed	✗
	CBD_UnitTest	100 %	97.56 %	97.56 %	97.67 %	100 %	6 of 6 passed	✗
	StOpCtrl	100 %	97.56 %	97.56 %	97.67 %	100 %	6 of 6 passed	✗
1	StOpCtrl_Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✓
2	TargetSelection	100 %	94.11 %	94.11 %	94.44 %	100 %	3 of 3 passed	✗

TEST DETAILS REPORT

TargetSelection

2015-09-01, 17:22:17+0530

Project	StOpCtrl
Module	StOpCtrl
Test Object	TargetSelection

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	94.11 %
Branch (C1) Coverage	94.11 %
MCC Coverage	100 %
MC/DC Coverage	94.44 %

Statistics

Total Testcases	3
Successful	3 ✔
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_Research_StOpCtrl
Configuration File	D:\Synergy_Work_Area\FORD_Research_StOpCtrl\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\StOpCtrl\src\Ap_StOpCtrl.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\StOpCtrl\utp\contract -I$(PROJECTROOT)\StOpCtrl\utp\contract\Ap_StOpCtrl -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470\include

Comments/Description/Specification

Name	Text
Module 'StOpCtrl'	**********Unit Test Information********** Name of Tester:Spoorti Mali Code File(s) Under Test:Ap_StOpCtrl.c Code File(s) Version:24 Module Design Document:State_Output_Control_MDD Module Design Document Version:8 Data Dictionary Version:9.1.1 Unit Test Plan Version:6 Optimization Level:Level 2 Compiler (CodeGen) Version: TMS470 _ 4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):632 Total RAM Used (Bytes):14 Total CALS Used (Bytes):0 Special Test Requirements: Test Date:9/01/2015 Comments:""NOTE1: Inline function defined in ""GlobalMacro.h"" are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map"" map file is embedded for reference. NOTE3: 100% coverage cannot be achieved in ""TargetSelection"" function as default case of ""switch (StOpCtrl_State_Cnt_M_u08)"" can not be covered." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl

Attributes

Name	Value
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\FORD_Research_StOpCtrl\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)

CPU Cycles:

TS1.1 52.00 Cycles
TS1.2 59.00 Cycles
```

Description

Vector Description:

TS1.1 "Longest Execution Path==>
if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32)) ==> False
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32))==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>True
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False"
TS1.2 "Shortest Execution Path==>
if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>True
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>True
"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0399999991
LoaScaleFctr_Uls_T_f32	0.0299999993
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0.0599999987
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0900000036
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0399999991
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0399999991	0.0399999991	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 2: Boundary Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)

CPU Cycles:

TS2.1 52.00 Cycles
TS2.2 52.00 Cycles
TS2.3 52.00 Cycles
TS2.4 59.00 Cycles
TS2.5 53.00 Cycles
TS2.6 52.00 Cycles
TS2.7 52.00 Cycles
TS2.8 52.00 Cycles
TS2.9 62.00 Cycles
TS2.10 55.00 Cycles
TS2.11 55.00 Cycles
TS2.12 59.00 Cycles
TS2.13 57.00 Cycles
TS2.14 55.00 Cycles
TS2.15 56.00 Cycles
TS2.16 54.00 Cycles
TS2.17 52.00 Cycles
TS2.18 52.00 Cycles
TS2.19 52.00 Cycles
TS2.20 55.00 Cycles
TS2.21 51.00 Cycles
TS2.22 58.00 Cycles
TS2.23 58.00 Cycles
TS2.24 56.00 Cycles
TS2.25 56.00 Cycles
TS2.26 54.00 Cycles
TS2.27 51.00 Cycles
TS2.28 54.00 Cycles
TS2.29 52.00 Cycles
```

Description

Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3OperScaleFctr_Uls_T_f32==>Min
TS2.4OperScaleFctr_Uls_T_f32==>Max
TS2.5OperScaleFctr_Uls_T_f32==>Pos
TS2.6LoaScaleFctr_Uls_T_f32==>Min
TS2.7LoaScaleFctr_Uls_T_f32==>Max
TS2.8LoaScaleFctr_Uls_T_f32==>Pos
TS2.9StrtStopScaleFctr_Uls_T_f32==>Min
TS2.10StrtStopScaleFctr_Uls_T_f32==>Max
TS2.11StrtStopScaleFctr_Uls_T_f32==>Pos
TS2.12OperRateLimit_UlspS_T_f32==>Min
TS2.13OperRateLimit_UlspS_T_f32==>Max
TS2.14OperRateLimit_UlspS_T_f32==>Pos
TS2.15LoaRateLimit_UlspS_T_f32==>Min
TS2.16LoaRateLimit_UlspS_T_f32==>Max
TS2.17LoaRateLimit_UlspS_T_f32==>Pos
TS2.18StrtStopRateLimit_UlspS_T_f32==>Min
TS2.19StrtStopRateLimit_UlspS_T_f32==>Max
TS2.20StrtStopRateLimit_UlspS_T_f32==>Pos
TS2.21StOpCtrl_ScaleSV_Uls_M_f32==>Min
TS2.22StOpCtrl_ScaleSV_Uls_M_f32==>Max
TS2.23StOpCtrl_ScaleSV_Uls_M_f32==>Pos
TS2.24StOpCtrl_RateSource_Cnt_M_u08==>Min
TS2.25StOpCtrl_RateSource_Cnt_M_u08==>Max
TS2.26StOpCtrl_RateSource_Cnt_M_u08==>Pos
TS2.27StOpCtrl_State_Cnt_M_u08==>Min
TS2.28StOpCtrl_State_Cnt_M_u08==>Max
TS2.29StOpCtrl_State_Cnt_M_u08==>Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	500
LoaScaleFctr_Uls_T_f32	1
OperRateLimit_UlspS_T_f32	5
OperScaleFctr_Uls_T_f32	1
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	1
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	500
StrtStopScaleFctr_Uls_T_f32	1

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	5	5	✔
target_SelRampValue_Uls_T_f32	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0500000007
LoaScaleFctr_Uls_T_f32	0.600000024
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.0500000007
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.4 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0599999987
LoaScaleFctr_Uls_T_f32	0.600000024
OperRateLimit_UlspS_T_f32	2
OperScaleFctr_Uls_T_f32	1
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.00999999978
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.0599999987
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.0599999987	0.0599999987	✔
target_SelRampValue_Uls_T_f32	0.600000024	0.600000024	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.5 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0700000003
LoaScaleFctr_Uls_T_f32	0.600000024
OperRateLimit_UlspS_T_f32	0.200000003
OperScaleFctr_Uls_T_f32	0.5
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.0199999996
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.0700000003
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.0700000003	0.0700000003	✔
target_SelRampValue_Uls_T_f32	0.5	0.5	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.6 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0799999982
LoaScaleFctr_Uls_T_f32	0
OperRateLimit_UlspS_T_f32	2.0999999
OperScaleFctr_Uls_T_f32	0
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.0299999993
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.0799999982
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	2.0999999	2.0999999	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0900000036
LoaScaleFctr_Uls_T_f32	1
OperRateLimit_UlspS_T_f32	0.300000012
OperScaleFctr_Uls_T_f32	0.00999999978
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0399999991
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	0.0900000036
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.300000012	0.300000012	✔
target_SelRampValue_Uls_T_f32	0.00999999978	0.00999999978	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.100000001
LoaScaleFctr_Uls_T_f32	0.5
OperRateLimit_UlspS_T_f32	2.20000005
OperScaleFctr_Uls_T_f32	0.0199999996
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.0500000007
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.100000001
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	2.20000005	2.20000005	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.9 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0
OperRateLimit_UlspS_T_f32	0.400000006
OperScaleFctr_Uls_T_f32	0.0299999993
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0599999987
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.00999999978	0.00999999978	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.10 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0199999996
LoaScaleFctr_Uls_T_f32	0.00999999978
OperRateLimit_UlspS_T_f32	2.29999995
OperScaleFctr_Uls_T_f32	0.0399999991
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.0700000003
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.0199999996
StrtStopScaleFctr_Uls_T_f32	1

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.0199999996	0.0199999996	✔
target_SelRampValue_Uls_T_f32	0.00999999978	0.00999999978	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.11 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0299999993
LoaScaleFctr_Uls_T_f32	0.0199999996
OperRateLimit_UlspS_T_f32	0.5
OperScaleFctr_Uls_T_f32	0.0500000007
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0799999982
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0299999993
StrtStopScaleFctr_Uls_T_f32	0.5

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.0299999993	0.0299999993	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0399999991
LoaScaleFctr_Uls_T_f32	0.0299999993
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0.0599999987
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0900000036
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0399999991
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0399999991	0.0399999991	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	1
LoaScaleFctr_Uls_T_f32	0.0399999991
OperRateLimit_UlspS_T_f32	5
OperScaleFctr_Uls_T_f32	0.0700000003
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.100000001
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.0900000036
StrtStopScaleFctr_Uls_T_f32	0.00999999978

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0900000036	0.0900000036	✔
target_SelRampValue_Uls_T_f32	0.00999999978	0.00999999978	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.14 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	1
LoaScaleFctr_Uls_T_f32	0.0500000007
OperRateLimit_UlspS_T_f32	2.0000999
OperScaleFctr_Uls_T_f32	0.0799999982
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.00999999978
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.100000001
StrtStopScaleFctr_Uls_T_f32	0.0199999996

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.15 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0.0599999987
OperRateLimit_UlspS_T_f32	0.200000003
OperScaleFctr_Uls_T_f32	0.0900000036
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0199999996
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0.0299999993

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	4	4	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.00999999978	0.00999999978	✔
target_SelRampValue_Uls_T_f32	0.0299999993	0.0299999993	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.16 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	500
LoaScaleFctr_Uls_T_f32	0.0700000003
OperRateLimit_UlspS_T_f32	2.0999999
OperScaleFctr_Uls_T_f32	0.100000001
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.0299999993
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.0199999996
StrtStopScaleFctr_Uls_T_f32	0.0399999991

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	2.0999999	2.0999999	✔
target_SelRampValue_Uls_T_f32	0.0399999991	0.0399999991	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	100.000099
LoaScaleFctr_Uls_T_f32	0.0799999982
OperRateLimit_UlspS_T_f32	0.300000012
OperScaleFctr_Uls_T_f32	0.00999999978
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.0399999991
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	1
StrtStopScaleFctr_Uls_T_f32	0.0500000007

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.300000012	0.300000012	✔
target_SelRampValue_Uls_T_f32	0.00999999978	0.00999999978	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	1
LoaScaleFctr_Uls_T_f32	0.0900000036
OperRateLimit_UlspS_T_f32	2.20000005
OperScaleFctr_Uls_T_f32	0.0199999996
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0500000007
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0.0599999987

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	2.20000005	2.20000005	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.19 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	150
LoaScaleFctr_Uls_T_f32	0.100000001
OperRateLimit_UlspS_T_f32	0.400000006
OperScaleFctr_Uls_T_f32	0.0299999993
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0599999987
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	500
StrtStopScaleFctr_Uls_T_f32	0.0700000003

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.400000006	0.400000006	✔
target_SelRampValue_Uls_T_f32	0.0299999993	0.0299999993	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.20 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	153
LoaScaleFctr_Uls_T_f32	0.00999999978
OperRateLimit_UlspS_T_f32	2.29999995
OperScaleFctr_Uls_T_f32	0.0399999991
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0700000003
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	100.000099
StrtStopScaleFctr_Uls_T_f32	0.0799999982

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	153	153	✔
target_SelRampValue_Uls_T_f32	0.00999999978	0.00999999978	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.21 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	200
LoaScaleFctr_Uls_T_f32	0.0399999991
OperRateLimit_UlspS_T_f32	0.170000002
OperScaleFctr_Uls_T_f32	0.0700000003
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0399999991
StrtStopScaleFctr_Uls_T_f32	0.00999999978

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	200	200	✔
target_SelRampValue_Uls_T_f32	0.00999999978	0.00999999978	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	250
LoaScaleFctr_Uls_T_f32	0.0500000007
OperRateLimit_UlspS_T_f32	2.16000009
OperScaleFctr_Uls_T_f32	0.0799999982
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	1
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.0900000036
StrtStopScaleFctr_Uls_T_f32	0.0199999996

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0900000036	0.0900000036	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	269
LoaScaleFctr_Uls_T_f32	0.0599999987
OperRateLimit_UlspS_T_f32	0.180000007
OperScaleFctr_Uls_T_f32	0.0900000036
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.5
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.100000001
StrtStopScaleFctr_Uls_T_f32	0.0299999993

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0.0299999993	0.0299999993	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	300
LoaScaleFctr_Uls_T_f32	0.0700000003
OperRateLimit_UlspS_T_f32	2.17000008
OperScaleFctr_Uls_T_f32	0.100000001
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.0299999993
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0.0399999991

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	2.17000008	2.17000008	✔
target_SelRampValue_Uls_T_f32	0.0399999991	0.0399999991	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	358
LoaScaleFctr_Uls_T_f32	0.0799999982
OperRateLimit_UlspS_T_f32	0.189999998
OperScaleFctr_Uls_T_f32	0.600000024
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0399999991
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	0.0199999996
StrtStopScaleFctr_Uls_T_f32	0.0500000007

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	4	4	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0199999996	0.0199999996	✔
target_SelRampValue_Uls_T_f32	0.0500000007	0.0500000007	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.26 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	489
LoaScaleFctr_Uls_T_f32	0.0900000036
OperRateLimit_UlspS_T_f32	2.18000007
OperScaleFctr_Uls_T_f32	0.600000024
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0500000007
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0.0599999987

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	489	489	✔
target_SelRampValue_Uls_T_f32	0.0599999987	0.0599999987	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.27 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	426
LoaScaleFctr_Uls_T_f32	0.100000001
OperRateLimit_UlspS_T_f32	0.200000003
OperScaleFctr_Uls_T_f32	0.600000024
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.0599999987
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0199999996
StrtStopScaleFctr_Uls_T_f32	0.0700000003

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.200000003	0.200000003	✔
target_SelRampValue_Uls_T_f32	0.0700000003	0.0700000003	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	436
LoaScaleFctr_Uls_T_f32	0.600000024
OperRateLimit_UlspS_T_f32	2.19000006
OperScaleFctr_Uls_T_f32	0.600000024
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.0700000003
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.0299999993
StrtStopScaleFctr_Uls_T_f32	0.0799999982

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	2.19000006	2.19000006	✔
target_SelRampValue_Uls_T_f32	0.0799999982	0.0799999982	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.29 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	247
LoaScaleFctr_Uls_T_f32	0.600000024
OperRateLimit_UlspS_T_f32	0.209999993
OperScaleFctr_Uls_T_f32	0.600000024
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0799999982
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.0399999991
StrtStopScaleFctr_Uls_T_f32	0.0900000036

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	4	4	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0399999991	0.0399999991	✔
target_SelRampValue_Uls_T_f32	0.0900000036	0.0900000036	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 3: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)

CPU Cycles:

TS3.1 52.00 Cycles
TS3.2 59.00 Cycles
TS3.3 57.00 Cycles
TS3.4 51.00 Cycles
TS3.5 57.00 Cycles
TS3.6 60.00 Cycles
TS3.7 57.00 Cycles
```

Description

Vector Description:

TS3.1" if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32)) ==> False
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32))==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>True
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False"
TS3.2"if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>True
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>True
"
TS3.3"else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>True
if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False

"
TS3.4"if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>False
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
"
TS3.5"if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>True
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
"
TS3.6"if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>False
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>True
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>True
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False"
TS3.7"if ((StrtStopScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32) &&
(StrtStopScaleFctr_Uls_T_f32 < LoaScaleFctr_Uls_T_f32))==>True
else if (LoaScaleFctr_Uls_T_f32 < OperScaleFctr_Uls_T_f32)==>False
if (OperScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (LoaScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False
if (StrtStopScaleFctr_Uls_T_f32 <= StOpCtrl_ScaleSV_Uls_M_f32)==>False"

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.2 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0399999991
LoaScaleFctr_Uls_T_f32	0.0299999993
OperRateLimit_UlspS_T_f32	0.100000001
OperScaleFctr_Uls_T_f32	0.0599999987
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0900000036
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0399999991
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.0399999991	0.0399999991	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.3 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0599999987
LoaScaleFctr_Uls_T_f32	0.600000024
OperRateLimit_UlspS_T_f32	2
OperScaleFctr_Uls_T_f32	1
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.00999999978
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.0599999987
StrtStopScaleFctr_Uls_T_f32	0.600000024

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.0599999987	0.0599999987	✔
target_SelRampValue_Uls_T_f32	0.600000024	0.600000024	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.4 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.0299999993
LoaScaleFctr_Uls_T_f32	0.0199999996
OperRateLimit_UlspS_T_f32	0.5
OperScaleFctr_Uls_T_f32	0.0500000007
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0799999982
StOpCtrl_State_Cnt_M_u08	1
StrtStopRateLimit_UlspS_T_f32	0.0299999993
StrtStopScaleFctr_Uls_T_f32	0.5

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.0299999993	0.0299999993	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	1
LoaScaleFctr_Uls_T_f32	0.0500000007
OperRateLimit_UlspS_T_f32	2.0000999
OperScaleFctr_Uls_T_f32	0.0799999982
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.00999999978
StOpCtrl_State_Cnt_M_u08	2
StrtStopRateLimit_UlspS_T_f32	0.100000001
StrtStopScaleFctr_Uls_T_f32	0.0199999996

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.100000001	0.100000001	✔
target_SelRampValue_Uls_T_f32	0.0199999996	0.0199999996	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.6 (Repeat Count = 1) ✔

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0
OperRateLimit_UlspS_T_f32	0.400000006
OperScaleFctr_Uls_T_f32	0.0299999993
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0599999987
StOpCtrl_State_Cnt_M_u08	3
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_SelRampRate_UlspS_T_f32	0.00999999978	0.00999999978	✔
target_SelRampValue_Uls_T_f32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.7 (Repeat Count = 1)

Name	Input Value
LoaRateLimit_UlspS_T_f32	0.00999999978
LoaScaleFctr_Uls_T_f32	0.0599999987
OperRateLimit_UlspS_T_f32	0.200000003
OperScaleFctr_Uls_T_f32	0.0900000036
SelRampRate_UlspS_T_f32	target_SelRampRate_UlspS_T_f32
SelRampValue_Uls_T_f32	target_SelRampValue_Uls_T_f32
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.0199999996
StOpCtrl_State_Cnt_M_u08	4
StrtStopRateLimit_UlspS_T_f32	0.00999999978
StrtStopScaleFctr_Uls_T_f32	0.0299999993

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	4	4	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_SelRampRate_UlspS_T_f32	0.00999999978	0.00999999978	✔
target_SelRampValue_Uls_T_f32	0.0299999993	0.0299999993	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

TEST DETAILS REPORT

StOpCtrl_Per1

2015-09-01, 17:18:07+0530

Project	StOpCtrl
Module	StOpCtrl
Test Object	StOpCtrl_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3 ✔
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FORD_Research_StOpCtrl
Configuration File	D:\Synergy_Work_Area\FORD_Research_StOpCtrl\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\StOpCtrl\src\Ap_StOpCtrl.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\StOpCtrl\utp\contract -I$(PROJECTROOT)\StOpCtrl\utp\contract\Ap_StOpCtrl -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470\include

Comments/Description/Specification

Name	Text
Module 'StOpCtrl'	**********Unit Test Information********** Name of Tester:Spoorti Mali Code File(s) Under Test:Ap_StOpCtrl.c Code File(s) Version:24 Module Design Document:State_Output_Control_MDD Module Design Document Version:8 Data Dictionary Version:9.1.1 Unit Test Plan Version:6 Optimization Level:Level 2 Compiler (CodeGen) Version: TMS470 _ 4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):632 Total RAM Used (Bytes):14 Total CALS Used (Bytes):0 Special Test Requirements: Test Date:9/01/2015 Comments:""NOTE1: Inline function defined in ""GlobalMacro.h"" are not unit tested. NOTE2: ""CBD_Sandbox_dbg.map"" map file is embedded for reference. NOTE3: 100% coverage cannot be achieved in ""TargetSelection"" function as default case of ""switch (StOpCtrl_State_Cnt_M_u08)"" can not be covered." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl

Attributes

Name	Value
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
Timer Unit	Cycles
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\FORD_Research_StOpCtrl\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

StOpCtrl_Per1

2015-09-01, 17:18:07+0530

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)

CPU Cycles:

TS1.1 167.00 Cycles
TS1.2 195.00 Cycles
```

Description

Vector Description:

TS1.1 "Shortest Execution Path==>(if (D_TRUE_CNT_LGC == DiagStsDiagRmpActive_Cnt_T_lgc)==>true
if(Abs_f32_m(Scale_Uls_T_f32) > D_EPSILON_ULS_F32)==>True
if((ArbdSt_Cnt_T_u08 == D_OPER_CNT_U08)||
(ArbdSt_Cnt_T_u08 == D_DIAG_CNT_U08))==>True)"
TS1.2 "Longest Execution Path==>(if (D_FALSE_CNT_LGC != RampSrlComSvcDft_Cnt_T_lgc)==>False
if((ArbdSt_Cnt_T_u08 == D_OPER_CNT_U08)||
(ArbdSt_Cnt_T_u08 == D_DIAG_CNT_U08))==>True)"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	1
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00499999989
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	1

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	4	4	✔
StOpCtrl_ScaleSV_Uls_M_f32	1	1 ± 0.000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	1	1 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32

TEST DETAILS REPORT

StOpCtrl_Per1

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Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0	0 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0	0 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Case 2: Boundary Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)

CPU Cycles:

TS2.1 193.00 Cycles
TS2.2 177.00 Cycles
TS2.3 193.00 Cycles
TS2.4 182.00 Cycles
TS2.5 193.00 Cycles
TS2.6 197.00 Cycles
TS2.7 193.00 Cycles
TS2.8 198.00 Cycles
TS2.9 195.00 Cycles
TS2.10 181.00 Cycles
TS2.11 202.00 Cycles
TS2.12 185.00 Cycles
TS2.13 191.00 Cycles
TS2.14 193.00 Cycles
TS2.15 201.00 Cycles
TS2.16 186.00 Cycles
TS2.17 194.00 Cycles
TS2.18 180.00 Cycles
TS2.19 193.00 Cycles
TS2.20 182.00 Cycles
TS2.21 196.00 Cycles
TS2.22 196.00 Cycles
TS2.23 180.00 Cycles
TS2.24 180.00 Cycles
TS2.25 180.00 Cycles
TS2.26 192.00 Cycles
TS2.27 180.00 Cycles
TS2.28 190.00 Cycles
TS2.29 193.00 Cycles
TS2.30 180.00 Cycles
TS2.31 180.00 Cycles
TS2.32 193.00 Cycles
TS2.33 180.00 Cycles
TS2.34 182.00 Cycles
TS2.35 193.00 Cycles
TS2.36 180.00 Cycles
TS2.37 180.00 Cycles
TS2.38 180.00 Cycles
TS2.39 190.00 Cycles
```

Description

Vector Description:

TS2.1All Min
TS2.2All Max
TS2.3DiagRampRate_XpmS_f32==>Min
TS2.4DiagRampRate_XpmS_f32==>Max
TS2.5DiagRampRate_XpmS_f32==>Pos
TS2.6DiagRampValue_Uls_f32==>Min
TS2.7DiagRampValue_Uls_f32==>Max
TS2.8DiagRampValue_Uls_f32==>Pos
TS2.9OperRampRate_XpmS_f32==>Min
TS2.10OperRampRate_XpmS_f32==>Max
TS2.11OperRampRate_XpmS_f32==>Pos
TS2.12OperRampValue_Uls_f32==>Min
TS2.13OperRampValue_Uls_f32==>Max
TS2.14OperRampValue_Uls_f32==>Pos
TS2.15RampSrlComSvcDft_Cnt_lgc==>Min
TS2.16RampSrlComSvcDft_Cnt_lgc==>Max
TS2.17DiagStsDiagRmpActive_Cnt_lgc==>Min
TS2.18DiagStsDiagRmpActive_Cnt_lgc==>Max
TS2.19LoaRateLimit_UlspS_f32==>Min
TS2.20LoaRateLimit_UlspS_f32==>Max
TS2.21LoaRateLimit_UlspS_f32==>Pos
TS2.22LoaScaleFctr_Uls_f32==>Min
TS2.23LoaScaleFctr_Uls_f32==>Max
TS2.24LoaScaleFctr_Uls_f32==>Pos
TS2.25StrtStopRateLimit_UlspS_f32==>Min
TS2.26StrtStopRateLimit_UlspS_f32==>Max
TS2.27StrtStopRateLimit_UlspS_f32==>Pos
TS2.28StrtStopScaleFctr_Uls_f32==>Min
TS2.29StrtStopScaleFctr_Uls_f32==>Max
TS2.30StrtStopScaleFctr_Uls_f32==>Pos
TS2.31StOpCtrl_RateSource_Cnt_M_u08==>Min
TS2.32StOpCtrl_RateSource_Cnt_M_u08==>Max
TS2.33StOpCtrl_RateSource_Cnt_M_u08==>Pos
TS2.34StOpCtrl_ScaleSV_Uls_M_f32==>Min
TS2.35StOpCtrl_ScaleSV_Uls_M_f32==>Max
TS2.36StOpCtrl_ScaleSV_Uls_M_f32==>Pos
TS2.37StOpCtrl_State_Cnt_M_u08==>Min
TS2.38StOpCtrl_State_Cnt_M_u08==>Max
TS2.39StOpCtrl_State_Cnt_M_u08==>Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0	0 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0	0 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	1
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.5
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	1
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00499999989
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	1

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	1	1 ± 0.000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	1	1 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.302492708
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.278027028
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	467.263367
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.913472593
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00184350228
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.229679927
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	12.2960091
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.437346101

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.298805714	0.298805714 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.298805714	0.298805714 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.874079227
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.5
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.125087604
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	400.319458
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.783863902
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00437599793
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.430418581
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	98.6420746
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.511585534

Name	Actual Value	Expected Value	Result
			✔

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	
StOpCtrl_ScaleSV_Uls_M_f32	0.125087604	0.125087604 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.125087604	0.125087604 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.795848608
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.100000001
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.248467639
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	19.4142303
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.890313745
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.000856229686
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.178747743
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	347.215179
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.912165463

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.794136167	0.794136167 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.794136167	0.794136167 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.549617529
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.302972317
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	470.055634
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.345170826
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00453384453
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.285311997
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	230.531555
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.0534599125

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_ScaleSV_Uls_M_f32	0	0 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0	0 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.978491127
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.0630179122
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	355.155426
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.37968564
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00150193088
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.313731551
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	499.605286
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.774366021

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.975487292	0.975487292 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.975487292	0.975487292 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.491835803

Name	Input Value
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.109179109
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.5
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	62.8037148
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.0365810841
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00349366385
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.376354158
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	400.485138
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.805990219

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.366228372	0.366228372 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.366228372	0.366228372 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.903346658
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.401654392
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.417788565
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	255.977127
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.889059067
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.356350482
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	104.680313
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.372262955

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.417788565	0.417788565 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.417788565	0.417788565 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.912750721
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.43549338
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.341149598
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	174.657196
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.247193187
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00499999989
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.0995012149
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	270.846985
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.271981448

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.341149598	0.341149598 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.341149598	0.341149598 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.374679446
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.250740886
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.450032115
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	120.650238
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.102508686
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00200000009

Name	Input Value
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.309367985
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	351.57251
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.254598081

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.450032115	0.450032115 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.450032115	0.450032115 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.302492708
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.17081669
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.332862049
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	224.334244
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.883540571
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00277462602
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	472.720032
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.912750721

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0	0 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0	0 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.874079227
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.149735615
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.496800482
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	337.882721
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.605523407
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00274528307
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	399.68866
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.374679446

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.496800482	0.496800482 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.496800482	0.496800482 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.795848608
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.227583542
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.114147879
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	237.553909
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.770338356
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00141481787
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.5
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	141.127426
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.809498906

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.793018997	0.793018997 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.793018997	0.793018997 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.15 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.912750721
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.450168639
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.0773187354
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.47720623
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00453384453
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.313731551
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	75.9448013
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.874079227

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.0773187354	0.0773187354 ± 0.00000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.0773187354	0.0773187354 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.16 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.978491127
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.4540025
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.369179547
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	378.217407
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.137388721
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00184350228
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.430418581
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	179.716095
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.532755435

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.369179547	0.369179547 ± 0.0000009	✔

Name	Actual Value	Expected Value	Result
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.369179547	0.369179547 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.491835803
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.324026555
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.14401643
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	235.665161
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.196203798
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00437599793
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.178747743
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	483.425446
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.601612389

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.483083814	0.483083814 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.483083814	0.483083814 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.903346658
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.300142467

Name	Input Value
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.0840428099
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	428.495758
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.522839844
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.000856229686
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.285311997
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	401.115234
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.302492708

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.0840428099	0.0840428099 ± 0.00000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.0840428099	0.0840428099 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.912750721
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.450168639
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.0773187354
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.47720623
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00453384453
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.313731551
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	75.9448013
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.874079227

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.0773187354	0.0773187354 ± 0.00000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.0773187354	0.0773187354 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.20 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.374679446
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.347135067
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.133428857
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.919257522
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00150193088
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.376354158
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	437.837311
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.795848608

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.133428857	0.133428857 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.133428857	0.133428857 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.271981448
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.118045613
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.300215781
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	499.035156
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.185756475
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00349366385
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.356350482
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	339.307495
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.549617529

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.185756475	0.185756475 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.185756475	0.185756475 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.254598081
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.214068949
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.477190673
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	321.016907
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.000249681034
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.0995012149
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	393.866913
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.978491127

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.477190673	0.477190673 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.477190673	0.477190673 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.912750721
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.161929607
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.378751665
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	58.9904594
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	1
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00313205272

Name	Input Value
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.309367985
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	47.5237427
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.491835803

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.378751665	0.378751665 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.378751665	0.378751665 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.374679446
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.17084749
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.469484001
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	499.035156
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.554514825
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00466732867
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.139226139
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	154.503677
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.589655042

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.469484001	0.469484001 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.469484001	0.469484001 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.809498906
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.304135561
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.433613509
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	14.4784288
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.554514825
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.003329559
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.212471202
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.903346658

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.433613509	0.433613509 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.433613509	0.433613509 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.26 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.0608705021
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.229989052
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.499736607
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	426.140442
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.756111026
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00455480907
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.201671615
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.616394937

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.201671615	0.201671615 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.201671615	0.201671615 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.27 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.532755435
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.316572487
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.487465203
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	243.069336
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.986927152
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00370065309
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.190872014
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	33.1765671
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.241738513

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.487465203	0.487465203 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.487465203	0.487465203 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.601612389
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.0594032705
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.285156995
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	350.683502
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.362691522
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00178843865
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.180072427
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	75.9448013
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.285156995	0.285156995 ± 0.0000009	✔

Name	Actual Value	Expected Value	Result
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.285156995	0.285156995 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.29 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.302492708
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.411022067
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.345914781
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	188.372864
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.70142132
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00191088545
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.16927284
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	437.837311
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	1

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.298670948	0.298670948 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.298670948	0.298670948 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.30 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.874079227
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.442060322

Name	Input Value
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.080007121
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	367.200684
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.70142132
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00391925359
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.158473238
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	339.307495
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.241738513

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.080007121	0.080007121 ± 0.00000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.080007121	0.080007121 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.31 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.795848608
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.0594032705
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.285156995
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	350.683502
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.362691522
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00178843865
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.180072427
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	75.9448013
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.302492708

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.285156995	0.285156995 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.285156995	0.285156995 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.32 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.549617529
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.411022067
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.345914781
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	188.372864
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.70142132
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00191088545
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.16927284
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	437.837311
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.874079227

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.545795739	0.545795739 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.545795739	0.545795739 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.33 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.978491127
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.442060322
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.080007121
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	367.200684
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.70142132
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00391925359
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.158473238
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	339.307495
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.795848608

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.080007121	0.080007121 ± 0.00000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.080007121	0.080007121 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.34 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.455319345
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.331167996
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	350.683502
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.362691522
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00333907246
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.229679927
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	75.9448013
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.549617529

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.331167996	0.331167996 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.331167996	0.331167996 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.35 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	1
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.4540025
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.369179547
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	188.372864
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.70142132
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00184350228

Name	Input Value
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.430418581
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	437.837311
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.978491127

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.996312976	0.996312976 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.996312976	0.996312976 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.36 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	0.503346682
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.324026555
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.14401643
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	367.200684
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.70142132
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00437599793
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.178747743
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	339.307495
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.491835803

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.14401643	0.14401643 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.14401643	0.14401643 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.37 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.302492708
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.300142467
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.0840428099
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	350.683502
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.362691522
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.000856229686
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.285311997
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	75.9448013
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.903346658

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.0840428099	0.0840428099 ± 0.00000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.0840428099	0.0840428099 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.38 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.874079227
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.450168639
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.0773187354
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	224.334244
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.883540571
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00453384453
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.313731551
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	472.720032
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.912750721

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.313731551	0.313731551 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.313731551	0.313731551 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 2.39 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.903346658
StOpCtrl_State_Cnt_M_u08	3
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.347135067
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.133428857
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	337.882721
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.605523407
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00150193088
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.376354158
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	399.68866
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.374679446

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	3	3	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.133428857	0.133428857 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	3	3	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.133428857	0.133428857 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Case 3: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)

CPU Cycles:

TS3.1 187.00 Cycles
TS3.2 193.00 Cycles
TS3.3 177.00 Cycles
TS3.4 193.00 Cycles
TS3.5 199.00 Cycles
TS3.6 195.00 Cycles
TS3.7 209.00 Cycles
```

Description

Vector Description:

TS3.1(ArbdTarSca_Uls_T_f32 >= (StOpCtrl_ScaleSV_Uls_M_f32 + StepLimit_Uls_T_f32)) ==> True
TS3.2"(D_TRUE_CNT_LGC == DiagStsDiagRmpActive_Cnt_T_lgc) ==>False
(ArbdTarSca_Uls_T_f32 >=D_TARGETSCALEHI_ULS_F32) ==> False
(ArbdTarSca_Uls_T_f32 <=D_TARGETSCALELO_ULS_F32) ==> True
(D_FALSE_CNT_LGC != RampSrlComSvcDft_Cnt_T_lgc) ==> False
(ArbdRate_UlspS_T_f32>=D_RATELIMITHI_ULSPS_F32)==> False
(ArbdRate_UlspS_T_f32<=D_RATELIMITLO_ULSPS_F32)==> False
(ArbdTarSca_Uls_T_f32 >= (StOpCtrl_ScaleSV_Uls_M_f32 + StepLimit_Uls_T_f32)) ==> False
(ArbdTarSca_Uls_T_f32 <= (StOpCtrl_ScaleSV_Uls_M_f32 -StepLimit_Uls_T_f32)) ==> False
(Abs_f32_m(Scale_Uls_T_f32) > D_EPSILON_ULS_F32)==> False
(Scale_Uls_T_f32>=D_TARGETSCALEHI_ULS_F32)==>False
(Scale_Uls_T_f32<=D_TARGETSCALELO_ULS_F32)==>True
(ArbdSt_Cnt_T_u08 == D_DIAG_CNT_U08) ==> True"
TS3.3"(D_TRUE_CNT_LGC == DiagStsDiagRmpActive_Cnt_T_lgc) ==>True
(ArbdTarSca_Uls_T_f32 >=D_TARGETSCALEHI_ULS_F32) ==> True
(D_FALSE_CNT_LGC != RampSrlComSvcDft_Cnt_T_lgc) ==> True
(Abs_f32_m(Scale_Uls_T_f32) > D_EPSILON_ULS_F32)==>True
(Scale_Uls_T_f32>=D_TARGETSCALEHI_ULS_F32)==>True
(ArbdSt_Cnt_T_u08 == D_DIAG_CNT_U08) ==>True
(ArbdSt_Cnt_T_u08 == D_OPER_CNT_U08)==> False"
TS3.4"(ArbdTarSca_Uls_T_f32 <=D_TARGETSCALELO_ULS_F32) ==> False
(ArbdTarSca_Uls_T_f32 <= (StOpCtrl_ScaleSV_Uls_M_f32 -StepLimit_Uls_T_f32)) ==> True
(Scale_Uls_T_f32<=D_TARGETSCALELO_ULS_F32)==>False"
TS3.5"(ArbdSt_Cnt_T_u08 == D_DIAG_CNT_U08) ==>False
(ArbdSt_Cnt_T_u08 == D_OPER_CNT_U08)==> False"
TS3.6"if (D_TRUE_CNT_LGC == DiagStsDiagRmpActive_Cnt_T_lgc)==> True
if (D_FALSE_CNT_LGC != RampSrlComSvcDft_Cnt_T_lgc)==>False
if((ArbdSt_Cnt_T_u08 == D_OPER_CNT_U08)||
  (ArbdSt_Cnt_T_u08 == D_DIAG_CNT_U08))==>True"
TS3.7"if (D_FALSE_CNT_LGC != RampSrlComSvcDft_Cnt_T_lgc)==>False
if(Abs_f32_m(Scale_Uls_T_f32) > D_EPSILON_ULS_F32)==>True"

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.000199999995	0.000199999995 ± 0.0000000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.000199999995	0.000199999995 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0	0 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0	0 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 3.3 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	4
StOpCtrl_ScaleSV_Uls_M_f32	1
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.5
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	1
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00499999989

Name	Input Value
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	1
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	500
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	1

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	1	1 ± 0.000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	1	1 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 3.4 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0.302492708
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.278027028
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	467.263367
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.913472593
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00184350228
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.229679927
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	12.2960091
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.437346101

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.298805714	0.298805714 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.298805714	0.298805714 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	2
StOpCtrl_ScaleSV_Uls_M_f32	0.491835803
StOpCtrl_State_Cnt_M_u08	4
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32

Name	Input Value
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.109179109
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.5
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	62.8037148
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0.0365810841
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00349366385
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0.376354158
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	400.485138
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.805990219

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.366228372	0.366228372 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.366228372	0.366228372 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 3.6 (Repeat Count = 1) ✔

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	1
StOpCtrl_ScaleSV_Uls_M_f32	0
StOpCtrl_State_Cnt_M_u08	1
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.5
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	1
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	9.99999975e-005
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	0
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	1	1	✔
StOpCtrl_ScaleSV_Uls_M_f32	0	0 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	1	1	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0	0 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔

Test Step 3.7 (Repeat Count = 1)

Name	Input Value
Rte_Inst_Ap_StOpCtrl	target_Rte_Inst_Ap_StOpCtrl
StOpCtrl_RateSource_Cnt_M_u08	3
StOpCtrl_ScaleSV_Uls_M_f32	0.874079227
StOpCtrl_State_Cnt_M_u08	2
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampRate_XpmS_f32	target_StOpCtrl_Per1_DiagRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagRampValue_Uls_f32	target_StOpCtrl_Per1_DiagRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc	target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaRateLimit_UlspS_f32	target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_LoaScaleFctr_Uls_f32	target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampRate_XpmS_f32	target_StOpCtrl_Per1_OperRampRate_XpmS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OperRampValue_Uls_f32	target_StOpCtrl_Per1_OperRampValue_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_OutputRampMult_Uls_f32	target_StOpCtrl_Per1_OutputRampMult_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc	target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32	target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32	target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32
target_Rte_Inst_Ap_StOpCtrl.StOpCtrl_Per1_SysStReqDi_Cnt_lgc	target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc
target_StOpCtrl_Per1_DiagRampRate_XpmS_f32.value	0.149735615
target_StOpCtrl_Per1_DiagRampValue_Uls_f32.value	0.496800482
target_StOpCtrl_Per1_DiagStsDiagRmpActive_Cnt_lgc.value	0
target_StOpCtrl_Per1_LoaRateLimit_UlspS_f32.value	0.00999999978
target_StOpCtrl_Per1_LoaScaleFctr_Uls_f32.value	0
target_StOpCtrl_Per1_OperRampRate_XpmS_f32.value	0.00274528307
target_StOpCtrl_Per1_OperRampValue_Uls_f32.value	1
target_StOpCtrl_Per1_RampSrlComSvcDft_Cnt_lgc.value	0
target_StOpCtrl_Per1_StrtStopRateLimit_UlspS_f32.value	0.100000001
target_StOpCtrl_Per1_StrtStopScaleFctr_Uls_f32.value	0.374679446

Name	Actual Value	Expected Value	Result
StOpCtrl_RateSource_Cnt_M_u08	2	2	✔
StOpCtrl_ScaleSV_Uls_M_f32	0.8740592	0.8740592 ± 0.0000009	✔
StOpCtrl_State_Cnt_M_u08	2	2	✔
target_StOpCtrl_Per1_OutputRampMult_Uls_f32.value	0.8740592	0.8740592 ± 0.004	✔
target_StOpCtrl_Per1_SysStReqDi_Cnt_lgc.value	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
TargetSelection	1	TargetSelection	1	✔