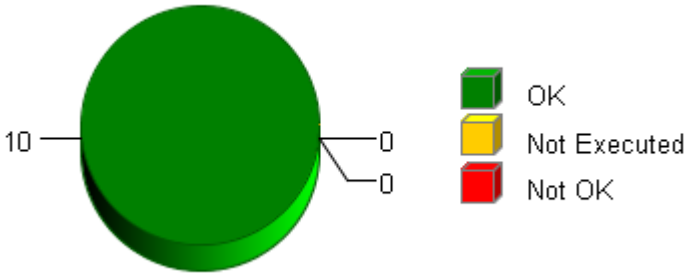
Summary

Total Test Objects:	10
Successful:	10
Failed:	0
Not Executed:	0
Date:	2018-04-10
Time:	18:51:13+0530

Overall Test Object Results (including Coverage)



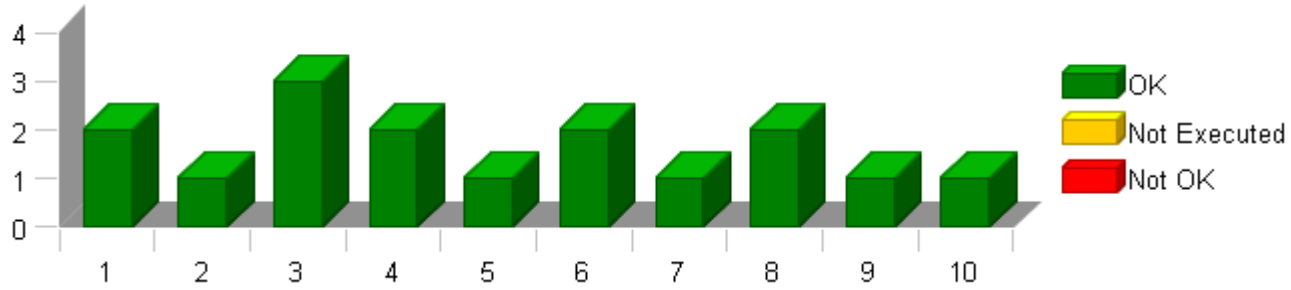
Selected Project Items

Test Collection "CBD_UnitTest"

Used Test Environments

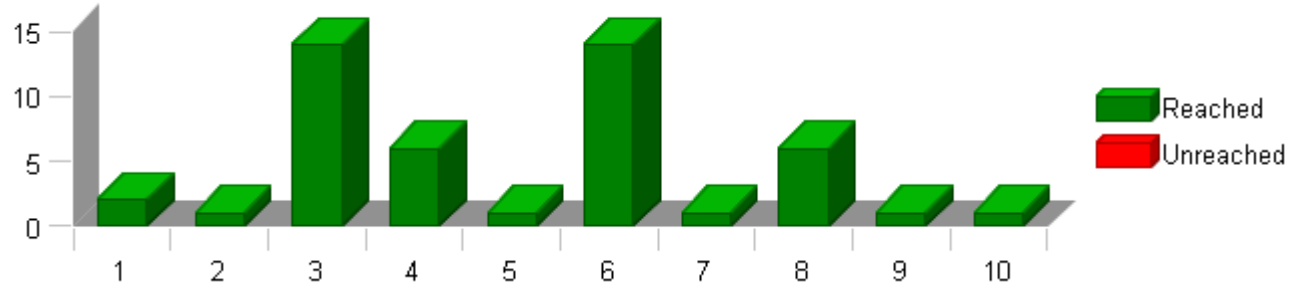
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



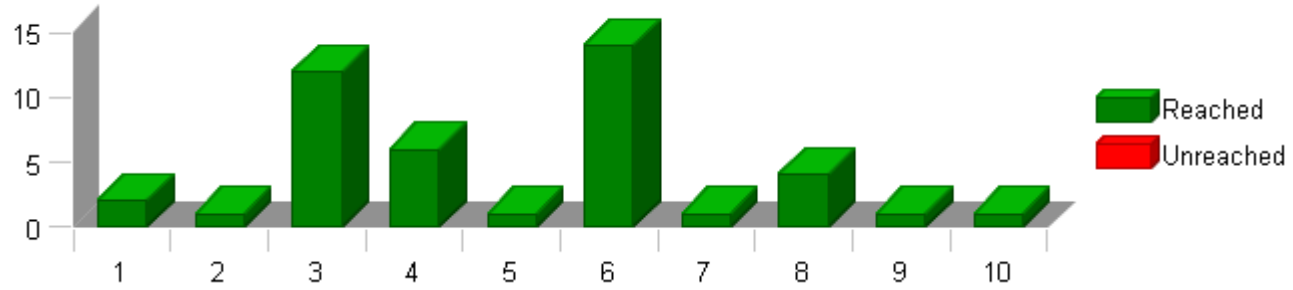
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



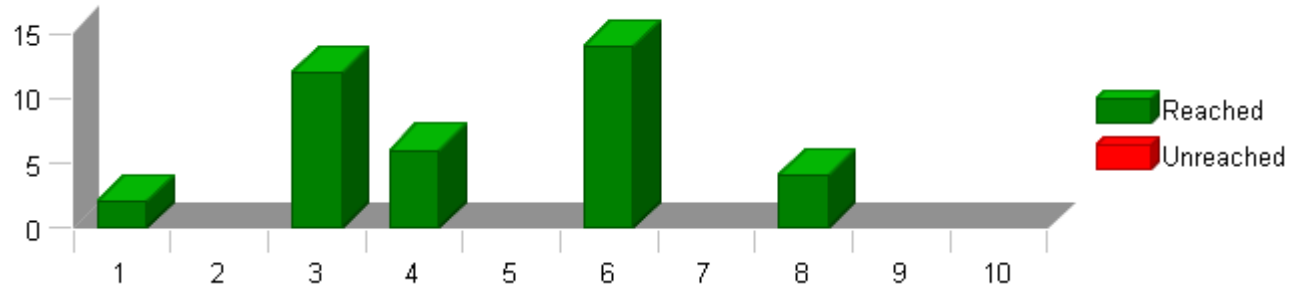
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

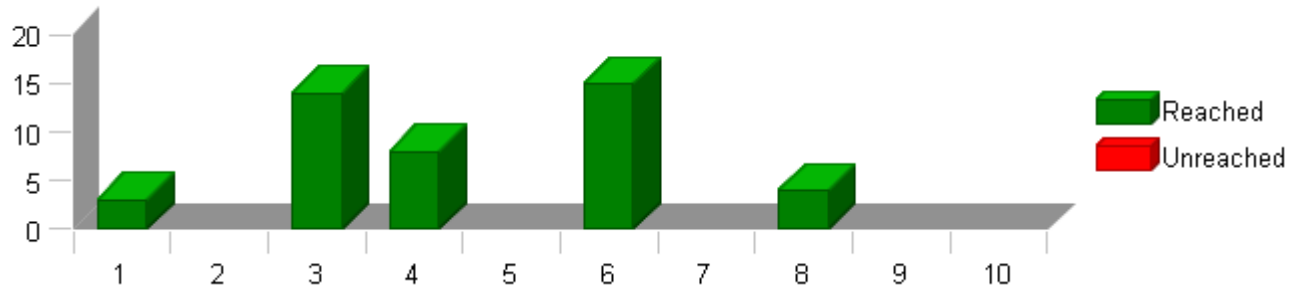
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	Test Cases	Result
	DemIf	100 %	100 %	100 %	100 %	16 of 16 passed	✔
	CBD_UnitTest	100 %	100 %	100 %	100 %	16 of 16 passed	✔
	DemIf	100 %	100 %	100 %	100 %	16 of 16 passed	✔
1	DemIf_CheckVoltageRange	100 %	100 %	100 %	100 %	2 of 2 passed	✔
2	DemIf_DemShutdown	100 %	100 %	-	-	1 of 1 passed	✔
3	DemIf_DTCStatusChanged	100 %	100 %	100 %	100 %	3 of 3 passed	✔
4	DemIf_EvaluateLogicalCondition	100 %	100 %	100 %	100 %	2 of 2 passed	✔
5	DemIf_Init	100 %	100 %	-	-	1 of 1 passed	✔
6	DemIf_Per	100 %	100 %	100 %	100 %	2 of 2 passed	✔
7	DemIf_RestartDem	100 %	100 %	-	-	1 of 1 passed	✔
8	DemIf_SetEventStatus	100 %	100 %	100 %	100 %	2 of 2 passed	✔
9	DemIf_SetOperationCycleState	100 %	100 %	-	-	1 of 1 passed	✔
10	DemIf_VehSpdControl	100 %	100 %	-	-	1 of 1 passed	✔

TEST DETAILS REPORT

DemIf_SetEventStatus

2018-04-10, 18:49:26+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_SetEventStatus

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Attributes

Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metric Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 564.00 Cycles
TS 1.2 553.00 Cycles
```

Description

Vector Description:

TS 1.1 Shortest Execution Path=>if (RTE_CONST_NTC_STATUS_FAILED == EventStatus)=>False
TS 1.2 Longest Execution Path=>if (RTE_CONST_NTC_STATUS_FAILED == EventStatus)=>True
if (0u == (CTCInhibitionMask_Cnt_M_u08[EventId] & CTCInhibitionState_Cnt_M_u08))=>True

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	0
Dem_SetEventStatus()	0
EventId	0
EventStatus	0

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	0
Dem_SetEventStatus()	0
EventId	0
EventStatus	1

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Case 2: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 579.00 Cycles
TS 2.2 550.00 Cycles
TS 2.3 567.00 Cycles
TS 2.4 536.00 Cycles
TS 2.5 518.00 Cycles
TS 2.6 536.00 Cycles
TS 2.7 536.00 Cycles
TS 2.8 518.00 Cycles
TS 2.9 536.00 Cycles
TS 2.10 536.00 Cycles
TS 2.11 518.00 Cycles
TS 2.12 536.00 Cycles
TS 2.13 536.00 Cycles
TS 2.14 31.00 Cycles
```

Description

Vector Description:

TS 2.1All Min
TS 2.2All Max
TS 2.3EventId=>Min
TS 2.4EventId=>Max
TS 2.5EventId=>Pos
TS 2.6EventStatus=>Min
TS 2.7EventStatus=>Max
TS 2.8EventStatus=>Pos
TS 2.9Dem_SetEventStatus=>Min
TS 2.10Dem_SetEventStatus=>Max
TS 2.11Dem_SetEventStatus=>Mid

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	0
Dem_SetEventStatus()	0
EventId	0
EventStatus	0

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	255
Dem_SetEventStatus()	255
EventId	255
EventStatus	3

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	255	255	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.3 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	0
Dem_SetEventStatus()	0
EventId	0
EventStatus	1

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	231
Dem_SetEventStatus()	13
EventId	255
EventStatus	2

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	13	13	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	12
Dem_SetEventStatus()	127
EventId	90
EventStatus	1

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	127	127	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	43
Dem_SetEventStatus()	45
EventId	34
EventStatus	0

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	45	45	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	224
Dem_SetEventStatus()	116
EventId	56
EventStatus	3

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	116	116	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.8 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	42
Dem_SetEventStatus()	31
EventId	67
EventStatus	1

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	31	31	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.9 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	123
Dem_SetEventStatus()	0
EventId	12
EventStatus	0

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.10 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	124
Dem_SetEventStatus()	255
EventId	45
EventStatus	3

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	255	255	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.11 (Repeat Count = 1)

Name	Input Value
CTCInhibitionState_Cnt_M_u08	31
Dem_SetEventStatus()	113
EventId	84
EventStatus	1

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	113	113	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	0
Dem_SetEventStatus()	0
EventId	0
EventStatus	0

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	255
Dem_SetEventStatus()	21
EventId	255
EventStatus	3

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	21	21	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
CTCInhibitionState_Cnt_M_u08	128
Dem_SetEventStatus()	2
EventId	1
EventStatus	1

Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

TEST DETAILS REPORT

DemIf_DemShutdown

2018-04-10, 18:41:25+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_DemShutdown

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 536.00 Cycles
```

Description

Vector Description:

TS1.1 Only Call trace is checked

Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_Shutdown	1	Dem_Shutdown	1	✔

TEST DETAILS REPORT

DemIf_Init

2018-04-10, 18:46:08+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_Init

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 558.00 Cycles
TS 1.2 558.00 Cycles
TS 1.3 558.00 Cycles
```

Description

Vector Description:

TS 1.1 Rte_Call_SystemTime_GetSystemTime_mS_u32=>Min
TS 1.2 Rte_Call_SystemTime_GetSystemTime_mS_u32=>Max
TS 1.3 Rte_Call_SystemTime_GetSystemTime_mS_u32=>Pos

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionBsi_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionCmm_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔

Test Step 1.3 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	200

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	200	200	✔
CTCInhibitionBsi_Cnt_M_u32	200	200	✔
CTCInhibitionCav_Cnt_M_u32	200	200	✔
CTCInhibitionCmm_Cnt_M_u32	200	200	✔
CTCInhibitionEsc_Cnt_M_u32	200	200	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔

TEST DETAILS REPORT

DemIf_Per

2018-04-10, 18:47:39+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_Per

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Attributes

Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 4166.00 Cycles
TS 1.2 4110.00 Cycles
```

Description

Vector Description:

TS 1.1 Shortest Execution Path=>if (ElapseTime_Cnt_T_u16 < k_EscActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_BsiActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_CavActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_AasActvTimeout_mS_u16)=>False
if (ElapseTime_Cnt_T_u16 < k_CmmActvTimeout_mS_u16)=>False
if ((TRUE == BusOff_Cnt_T_lgc)=>False||
(TRUE == VehSpdControl_Cnt_M_lgc)=>False)
if (TRUE == ElectronicIntegration_Cnt_T_lgc)=>False

TS 1.2 Longest Execution Path=> if (ElapseTime_Cnt_T_u16 < k_EscActvTimeout_mS_u16)=>True
if (ElapseTime_Cnt_T_u16 < k_BsiActvTimeout_mS_u16)=>True
if (ElapseTime_Cnt_T_u16 < k_CavActvTimeout_mS_u16)=>True
if (ElapseTime_Cnt_T_u16 < k_AasActvTimeout_mS_u16)=>True
if (ElapseTime_Cnt_T_u16 < k_CmmActvTimeout_mS_u16)=>True
if ((TRUE == BusOff_Cnt_T_lgc)=>True ||
(TRUE == VehSpdControl_Cnt_M_lgc))
if (TRUE == ElectronicIntegration_Cnt_T_lgc)=>True

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	0
k_AasActvVBattMax_Volt_f32	0
k_AasActvVBattMin_Volt_f32	0
k_BsiActvTimeout_mS_u16	0
k_BsiActvVBattMax_Volt_f32	0
k_BsiActvVBattMin_Volt_f32	0
k_CavActvTimeout_mS_u16	0
k_CavActvVBattMax_Volt_f32	0
k_CavActvVBattMin_Volt_f32	0
k_CmmActvTimeout_mS_u16	0
k_CmmActvVBattMax_Volt_f32	0
k_CmmActvVBattMin_Volt_f32	0
k_EscActvTimeout_mS_u16	0
k_EscActvVBattMax_Volt_f32	0
k_EscActvVBattMin_Volt_f32	0
target_DemIf_Per_BatteryVoltage_Volt_f32.value	0
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	0
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
VehSpdControl_Cnt_M_Igc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	19.9340992
target_DemIf_Per_BusOff_Cnt_Igc.value	1
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	0
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3633311787
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionBsi_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionCav_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionCmm_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionEsc_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionState_Cnt_M_u08	223	223	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Case 2: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 4063.00 Cycles
TS 2.2 4089.00 Cycles
TS 2.3 4067.00 Cycles
TS 2.4 4067.00 Cycles
TS 2.5 4067.00 Cycles
TS 2.6 4067.00 Cycles
TS 2.7 4067.00 Cycles
TS 2.8 4067.00 Cycles
TS 2.9 4067.00 Cycles
TS 2.10 4067.00 Cycles
TS 2.11 4067.00 Cycles
TS 2.12 4067.00 Cycles
TS 2.13 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.15 4067.00 Cycles
TS 2.16 4029.00 Cycles
TS 2.17 4051.00 Cycles
TS 2.18 4051.00 Cycles
TS 2.19 4051.00 Cycles
TS 2.20 4051.00 Cycles
TS 2.21 4029.00 Cycles
TS 2.22 4051.00 Cycles
TS 2.23 4029.00 Cycles
TS 2.24 4051.00 Cycles
TS 2.25 4029.00 Cycles
TS 2.26 4051.00 Cycles
TS 2.27 4029.00 Cycles
TS 2.28 4029.00 Cycles
TS 2.29 4051.00 Cycles
TS 2.30 4029.00 Cycles
TS 2.31 4029.00 Cycles
TS 2.32 4051.00 Cycles
```

Description

Vector Description:

TS 2.1 All Min
TS 2.2All Max
TS 2.3DemIf_Per_BatteryVoltage_Volt_f32=>Min
TS 2.4DemIf_Per_BatteryVoltage_Volt_f32=>Max
TS 2.5DemIf_Per_BatteryVoltage_Volt_f32=>Pos
TS 2.6DemIf_Per_ElectronicIntegration_Cnt_lgc=>Min
TS 2.7DemIf_Per_ElectronicIntegration_Cnt_lgc=>Max
TS 2.8DemIf_Per_BusOff_Cnt_lgc=>Min
TS 2.9DemIf_Per_BusOff_Cnt_lgc=>Max
TS 2.10Rte_Call_SystemTime_GetSystemTime_mS_u32=>Min
TS 2.11Rte_Call_SystemTime_GetSystemTime_mS_u32=>Max
TS 2.12Rte_Call_SystemTime_GetSystemTime_mS_u32=>Pos
TS 2.13Rte_Call_SystemTime_DtrmnElapsedTime_mS_u16=>Min
TS 2.14Rte_Call_SystemTime_DtrmnElapsedTime_mS_u16=>Max
TS 2.15Rte_Call_SystemTime_DtrmnElapsedTime_mS_u16=>Pos
TS 2.16VehSpdControl_Cnt_M_lgc=>Min
TS 2.17VehSpdControl_Cnt_M_lgc=>Max
TS 2.18k_EscActvTimeout_mS_u16=>Min
TS 2.19k_EscActvTimeout_mS_u16=>Max
TS 2.20k_EscActvTimeout_mS_u16=>Pos
TS 2.21k_BsiActvTimeout_mS_u16=>Min
TS 2.22k_BsiActvTimeout_mS_u16=>Max
TS 2.23k_BsiActvTimeout_mS_u16=>Pos
TS 2.24k_CavActvTimeout_mS_u16=>Min
TS 2.25k_CavActvTimeout_mS_u16=>Max
TS 2.26k_CavActvTimeout_mS_u16=>Pos
TS 2.27k_AasActvTimeout_mS_u16=>Min
TS 2.28k_AasActvTimeout_mS_u16=>Max
TS 2.29k_AasActvTimeout_mS_u16=>Pos
TS 2.30k_CmmActvTimeout_mS_u16=>Min
TS 2.31k_CmmActvTimeout_mS_u16=>Max
TS 2.32k_CmmActvTimeout_mS_u16=>Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	0
k_AasActvVBattMax_Volt_f32	0
k_AasActvVBattMin_Volt_f32	0
k_BsiActvTimeout_mS_u16	0
k_BsiActvVBattMax_Volt_f32	0
k_BsiActvVBattMin_Volt_f32	0
k_CavActvTimeout_mS_u16	0
k_CavActvVBattMax_Volt_f32	0
k_CavActvVBattMin_Volt_f32	0
k_CmmActvTimeout_mS_u16	0
k_CmmActvVBattMax_Volt_f32	0

TEST DETAILS REPORT

DemIf_Per

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Name	Input Value
k_CmmActvVBattMin_Volt_f32	0
k_EscActvTimeout_mS_u16	0
k_EscActvVBattMax_Volt_f32	0
k_EscActvVBattMin_Volt_f32	0
target_DemIf_Per_BatteryVoltage_Volt_f32.value	0
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	0
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_Igc	1
k_AasActvTimeout_mS_u16	65535
k_AasActvVBattMax_Volt_f32	31
k_AasActvVBattMin_Volt_f32	31
k_BsiActvTimeout_mS_u16	65535
k_BsiActvVBattMax_Volt_f32	31
k_BsiActvVBattMin_Volt_f32	31
k_CavActvTimeout_mS_u16	65535
k_CavActvVBattMax_Volt_f32	31
k_CavActvVBattMin_Volt_f32	31
k_CmmActvTimeout_mS_u16	65535
k_CmmActvVBattMax_Volt_f32	31
k_CmmActvVBattMin_Volt_f32	31
k_EscActvTimeout_mS_u16	65535
k_EscActvVBattMax_Volt_f32	31
k_EscActvVBattMin_Volt_f32	31
target_DemIf_Per_BatteryVoltage_Volt_f32.value	31
target_DemIf_Per_BusOff_Cnt_Igc.value	1
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	15
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	65535
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔
CTCInhibitionState_Cnt_M_u08	192	192	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.3 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_Igc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8

Name	Input Value
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	0
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	35422
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	616684576
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	616684576	616684576	✔
CTCInhibitionBsi_Cnt_M_u32	616684576	616684576	✔
CTCInhibitionCav_Cnt_M_u32	616684576	616684576	✔
CTCInhibitionCmm_Cnt_M_u32	616684576	616684576	✔
CTCInhibitionEsc_Cnt_M_u32	616684576	616684576	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	31
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	44450
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2274712120
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc

Name	Input Value
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2274712120	2274712120	✔
CTCInhibitionBsi_Cnt_M_u32	2274712120	2274712120	✔
CTCInhibitionCav_Cnt_M_u32	2274712120	2274712120	✔
CTCInhibitionCmm_Cnt_M_u32	2274712120	2274712120	✔
CTCInhibitionEsc_Cnt_M_u32	2274712120	2274712120	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	23.1233997
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	13073
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1199317560
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1199317560	1199317560	✔
CTCInhibitionBsi_Cnt_M_u32	1199317560	1199317560	✔
CTCInhibitionCav_Cnt_M_u32	1199317560	1199317560	✔
CTCInhibitionCmm_Cnt_M_u32	1199317560	1199317560	✔
CTCInhibitionEsc_Cnt_M_u32	1199317560	1199317560	✔
CTCInhibitionState_Cnt_M_u08	192	192	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_Igc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	19.0732002
target_DemIf_Per_BusOff_Cnt_Igc.value	1
target_DemIf_Per_CTerm_Cnt_Igc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	1
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	11127
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3539035437
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime

Name	Input Value
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	14.1280003
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	34139
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2825399010
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionState_Cnt_M_u08	128	128	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16

Name	Input Value
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	15.1973
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	10391
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1774937490
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	7.63290024
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	1
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	10133
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2290771965
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionBsi_Cnt_M_u32	2290771965	2290771965	✔

Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionCmm_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionEsc_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionState_Cnt_M_u08	192	192	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	15.5703001
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	1
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	37505
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionEsc_Cnt_M_u32	2290771965	2290771965	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.11 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	2.43390012
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	17221
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionBsi_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionCmm_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionState_Cnt_M_u08	192	192	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.12 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8

Name	Input Value
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	7.41270018
target_DemIf_Per_BusOff_Cnt_Igc.value	1
target_DemIf_Per_CTerm_Cnt_Igc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	14136
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1533825676
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1533825676	1533825676	✔
CTCInhibitionBsi_Cnt_M_u32	1533825676	1533825676	✔
CTCInhibitionCav_Cnt_M_u32	1533825676	1533825676	✔
CTCInhibitionCmm_Cnt_M_u32	1533825676	1533825676	✔
CTCInhibitionEsc_Cnt_M_u32	1533825676	1533825676	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
VehSpdControl_Cnt_M_Igc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	19.9340992
target_DemIf_Per_BusOff_Cnt_Igc.value	1
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	0
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3633311787
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc

Name	Input Value
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionBsi_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionCav_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionCmm_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionEsc_Cnt_M_u32	3633311787	3633311787	✔
CTCInhibitionState_Cnt_M_u08	223	223	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	7.89410019
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	65535
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2447925560
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionBsi_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionCav_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionCmm_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionEsc_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_Igc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	14.2438002
target_DemIf_Per_BusOff_Cnt_Igc.value	1
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	1241
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3091959789
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionBsi_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionCav_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionCmm_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionEsc_Cnt_M_u32	2447925560	2447925560	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	✔
DemIf_EvaluateLogicalCondition	1	DemIf_EvaluateLogicalCondition	1	✔
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔
DemIf_CheckVoltageRange	5	DemIf_CheckVoltageRange	5	✔
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime

Name	Input Value
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_Igc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	5.31850004
target_DemIf_Per_BusOff_Cnt_Igc.value	0
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	11
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	51058
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3923762454
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionBsi_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionCav_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionCmm_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionEsc_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_Igc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	5.31850004
target_DemIf_Per_BusOff_Cnt_Igc.value	0
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	11
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	51058
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3923762454
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32

Name	Input Value
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionBsi_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionCav_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionCmm_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionEsc_Cnt_M_u32	3923762454	3923762454	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	0
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	2.17689991
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	7
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	53021
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	785100198
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	785100198	785100198	✔
CTCInhibitionBsi_Cnt_M_u32	785100198	785100198	✔
CTCInhibitionCav_Cnt_M_u32	785100198	785100198	✔
CTCInhibitionCmm_Cnt_M_u32	785100198	785100198	✔
CTCInhibitionEsc_Cnt_M_u32	785100198	785100198	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600

Name	Input Value
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	65535
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	1.71889997
target_DemIf_Per_BusOff_Cnt_Igc.value	0
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	14
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	33512
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1652918279
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1652918279	1652918279	✔
CTCInhibitionBsi_Cnt_M_u32	1652918279	1652918279	✔
CTCInhibitionCav_Cnt_M_u32	1652918279	1652918279	✔
CTCInhibitionCmm_Cnt_M_u32	1652918279	1652918279	✔
CTCInhibitionEsc_Cnt_M_u32	1652918279	1652918279	✔
CTCInhibitionState_Cnt_M_u08	193	193	✔

Test Step 2.20 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_Igc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	7.58209991
target_DemIf_Per_BusOff_Cnt_Igc.value	0
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	8
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	42407
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1905186906
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1905186906	1905186906	✔
CTCInhibitionBsi_Cnt_M_u32	1905186906	1905186906	✔

Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	1905186906	1905186906	✔
CTCInhibitionCmm_Cnt_M_u32	1905186906	1905186906	✔
CTCInhibitionEsc_Cnt_M_u32	1905186906	1905186906	✔
CTCInhibitionState_Cnt_M_u08	192	192	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_Igc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	0
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	2.12019992
target_DemIf_Per_BusOff_Cnt_Igc.value	0
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	11
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	21862
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	921326253
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	921326253	921326253	✔
CTCInhibitionBsi_Cnt_M_u32	921326253	921326253	✔
CTCInhibitionCav_Cnt_M_u32	921326253	921326253	✔
CTCInhibitionCmm_Cnt_M_u32	921326253	921326253	✔
CTCInhibitionEsc_Cnt_M_u32	921326253	921326253	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_Igc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	65535
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16

Name	Input Value
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	2.67659998
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	7
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	58660
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3172092003
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3172092003	3172092003	✔
CTCInhibitionBsi_Cnt_M_u32	3172092003	3172092003	✔
CTCInhibitionCav_Cnt_M_u32	3172092003	3172092003	✔
CTCInhibitionCmm_Cnt_M_u32	3172092003	3172092003	✔
CTCInhibitionEsc_Cnt_M_u32	3172092003	3172092003	✔
CTCInhibitionState_Cnt_M_u08	66	66	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	5.91480017
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	12
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	4345
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2417842237
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2417842237	2417842237	✔
CTCInhibitionBsi_Cnt_M_u32	2417842237	2417842237	✔
CTCInhibitionCav_Cnt_M_u32	2417842237	2417842237	✔
CTCInhibitionCmm_Cnt_M_u32	2417842237	2417842237	✔
CTCInhibitionEsc_Cnt_M_u32	2417842237	2417842237	✔
CTCInhibitionState_Cnt_M_u08	0	0	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	0
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	0.0749000013
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	2
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	50842
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	544823061
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	544823061	544823061	✔
CTCInhibitionBsi_Cnt_M_u32	544823061	544823061	✔
CTCInhibitionCav_Cnt_M_u32	544823061	544823061	✔
CTCInhibitionCmm_Cnt_M_u32	544823061	544823061	✔
CTCInhibitionEsc_Cnt_M_u32	544823061	544823061	✔
CTCInhibitionState_Cnt_M_u08	192	192	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	65535
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	0.40959999
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1

Name	Input Value
target_DemIf_Per_EtatMt_Cnt_u08.value	15
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	8547
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1368639926
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1368639926	1368639926	✔
CTCInhibitionBsi_Cnt_M_u32	1368639926	1368639926	✔
CTCInhibitionCav_Cnt_M_u32	1368639926	1368639926	✔
CTCInhibitionCmm_Cnt_M_u32	1368639926	1368639926	✔
CTCInhibitionEsc_Cnt_M_u32	1368639926	1368639926	✔
CTCInhibitionState_Cnt_M_u08	132	132	✔

Test Step 2.26 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	4.39799976
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	5
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	4041
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1967358071
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionBsi_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionCav_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionCmm_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionEsc_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step 2.27 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3

Name	Input Value
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	0
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	15.6511002
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	3
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	22989
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4288551715
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionBsi_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionCav_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionCmm_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionEsc_Cnt_M_u32	1967358071	1967358071	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	65535
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	1.24150002
target_DemIf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	14
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	28869
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1311140043
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc

Name	Input Value
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1311140043	1311140043	✔
CTCInhibitionBsi_Cnt_M_u32	1311140043	1311140043	✔
CTCInhibitionCav_Cnt_M_u32	1311140043	1311140043	✔
CTCInhibitionCmm_Cnt_M_u32	1311140043	1311140043	✔
CTCInhibitionEsc_Cnt_M_u32	1311140043	1311140043	✔
CTCInhibitionState_Cnt_M_u08	8	8	✔

Test Step 2.29 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	24.6821003
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	12
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	1356
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2740672965
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2740672965	2740672965	✔
CTCInhibitionBsi_Cnt_M_u32	2740672965	2740672965	✔
CTCInhibitionCav_Cnt_M_u32	2740672965	2740672965	✔
CTCInhibitionCmm_Cnt_M_u32	2740672965	2740672965	✔
CTCInhibitionEsc_Cnt_M_u32	2740672965	2740672965	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step 2.30 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8

Name	Input Value
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	0
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	0.328999996
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	12
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	26304
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3599977200
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3599977200	3599977200	✔
CTCInhibitionBsi_Cnt_M_u32	3599977200	3599977200	✔
CTCInhibitionCav_Cnt_M_u32	3599977200	3599977200	✔
CTCInhibitionCmm_Cnt_M_u32	3599977200	3599977200	✔
CTCInhibitionEsc_Cnt_M_u32	3599977200	3599977200	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

Test Step 2.31 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	65535
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	1.57360005
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	1
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	62048
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3314516146
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3314516146	3314516146	✔
CTCInhibitionBsi_Cnt_M_u32	3314516146	3314516146	✔
CTCInhibitionCav_Cnt_M_u32	3314516146	3314516146	✔
CTCInhibitionCmm_Cnt_M_u32	3314516146	3314516146	✔

Name	Actual Value	Expected Value	Result
CTCInhibitionEsc_Cnt_M_u32	3314516146	3314516146	✔
CTCInhibitionState_Cnt_M_u08	208	208	✔

Test Step 2.32 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_DemIf_Per_BatteryVoltage_Volt_f32.value	8.26420021
target_DemIf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	5
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	54812
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1306746881
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1306746881	1306746881	✔
CTCInhibitionBsi_Cnt_M_u32	1306746881	1306746881	✔
CTCInhibitionCav_Cnt_M_u32	1306746881	1306746881	✔
CTCInhibitionCmm_Cnt_M_u32	1306746881	1306746881	✔
CTCInhibitionEsc_Cnt_M_u32	1306746881	1306746881	✔
CTCInhibitionState_Cnt_M_u08	64	64	✔

TEST DETAILS REPORT

DemIf_EvaluateLogicalCondition

2018-04-10, 18:45:44+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_EvaluateLogicalCondition

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$ (PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Attributes

Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

DemIf_EvaluateLogicalCondition

2018-04-10, 18:45:44+0530

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 1103.00 Cycles
TS 1.2 1038.00 Cycles
```

Description

Vector Description:

TS 1.1 Shortest Execution Path=>if (IoHwAb_BoolType_LowerLimit == Ignition_Cnt_T_enum)=>False
if (((uint8)kETAT_MT_Starting == EtatMt_Cnt_T_u08)=>False ||
((uint8)kETAT_MT_Autonomous_Starting == EtatMt_Cnt_T_u08)=>False)
TS 1.2 Longest Execution Path=> if (IoHwAb_BoolType_LowerLimit == Ignition_Cnt_T_enum)=>True
if ((FALSE == CTerm_Cnt_T_Igc)=>True &&
(RTE_MODE_StaMd_Mode_OPERATE != SystemState_Cnt_T_enum)=>True)

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
Time_ms_T_u32	4294967295
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	15
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
Time_ms_T_u32	0
target_DemIf_Per_CTerm_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Case 2: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 1032.00 Cycles
TS 2.2 1032.00 Cycles
TS 2.3 1032.00 Cycles
TS 2.4 1032.00 Cycles
TS 2.5 1032.00 Cycles
TS 2.6 1032.00 Cycles
TS 2.7 1032.00 Cycles
TS 2.8 1032.00 Cycles
TS 2.9 1032.00 Cycles
TS 2.10 1032.00 Cycles
TS 2.11 1032.00 Cycles
TS 2.12 1032.00 Cycles
TS 2.13 1032.00 Cycles
TS 2.14 1032.00 Cycles
TS 2.15 1032.00 Cycles
TS 2.16 1032.00 Cycles
TS 2.17 1032.00 Cycles
```

Description

Vector Description:

TS 1.1All Min
TS 1.2All Max
TS 1.3Time_ms_T_u32=>Min
TS 1.4Time_ms_T_u32=>Max
TS 1.5Time_ms_T_u32=>Pos
TS 1.6DemIf_Per_CTerm_Cnt_lgc=>Min
TS 1.7DemIf_Per_CTerm_Cnt_lgc=>Max
TS 1.8DemIf_Per_EtatMt_Cnt_u08=>Min
TS 1.9DemIf_Per_EtatMt_Cnt_u08=>Max
TS 1.10DemIf_Per_EtatMt_Cnt_u08=>Pos
TS 1.11Rte_Mode_SystemState_Mode=>RTE_MODE_StaMd_Mode_DISABLE
TS 1.12Rte_Mode_SystemState_Mode=>RTE_MODE_StaMd_Mode_OFF
TS 1.13Rte_Mode_SystemState_Mode=>RTE_MODE_StaMd_Mode_OPERATE
TS 1.14Rte_Mode_SystemState_Mode=>RTE_MODE_StaMd_Mode_WARMINIT
TS 1.15Rte_Mode_SystemState_Mode=>RTE_TRANSITION_StaMd_Mode
TS 1.16Rte_Call_Ignition_OP_GET=>Min
TS 1.17Rte_Call_Ignition_OP_GET=>Max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
Time_ms_T_u32	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
Time_ms_T_u32	4294967295
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	15
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔

Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
Time_ms_T_u32	0
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	1
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	0	0	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
Time_ms_T_u32	4294967295
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	2
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
Time_ms_T_u32	125351
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	3

Name	Input Value
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	125351	125351	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	125351	125351	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
Time_ms_T_u32	252315
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	4
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	125351	125351	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	125351	125351	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
Time_ms_T_u32	1352463
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	5
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.8 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
Time_ms_T_u32	324253
target_DemIf_Per_CTerm_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.9 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
Time_ms_T_u32	676575
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	15
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.10 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
Time_ms_T_u32	32426532
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	11
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionBsi_Cnt_M_u32	0	0	✔
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	✔
CTCInhibitionCmm_Cnt_M_u32	0	0	✔
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
Time_ms_T_u32	57742
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	6
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	57742	57742	✔
CTCInhibitionBsi_Cnt_M_u32	57742	57742	✔
CTCInhibitionCav_Cnt_M_u32	57742	57742	✔
CTCInhibitionCmm_Cnt_M_u32	57742	57742	✔
CTCInhibitionEsc_Cnt_M_u32	57742	57742	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
Time_ms_T_u32	45
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	7
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	45	45	✔
CTCInhibitionBsi_Cnt_M_u32	45	45	✔
CTCInhibitionCav_Cnt_M_u32	45	45	✔
CTCInhibitionCmm_Cnt_M_u32	45	45	✔
CTCInhibitionEsc_Cnt_M_u32	45	45	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.13 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
Time_ms_T_u32	7574621
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	8
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	45	45	✔
CTCInhibitionBsi_Cnt_M_u32	45	45	✔
CTCInhibitionCav_Cnt_M_u32	45	45	✔
CTCInhibitionCmm_Cnt_M_u32	45	45	✔
CTCInhibitionEsc_Cnt_M_u32	45	45	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.14 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
Time_ms_T_u32	5785
target_DemIf_Per_CTerm_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	9
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	5785	5785	✔
CTCInhibitionBsi_Cnt_M_u32	5785	5785	✔
CTCInhibitionCav_Cnt_M_u32	5785	5785	✔
CTCInhibitionCmm_Cnt_M_u32	5785	5785	✔
CTCInhibitionEsc_Cnt_M_u32	5785	5785	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.15 (Repeat Count = 1)

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
Time_ms_T_u32	14165
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	10
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	14165	14165	✔
CTCInhibitionBsi_Cnt_M_u32	5785	5785	✔
CTCInhibitionCav_Cnt_M_u32	14165	14165	✔
CTCInhibitionCmm_Cnt_M_u32	5785	5785	✔
CTCInhibitionEsc_Cnt_M_u32	14165	14165	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
Time_ms_T_u32	415241
target_DemIf_Per_CTerm_Cnt_Igc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	13
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	415241	415241	✔
CTCInhibitionBsi_Cnt_M_u32	5785	5785	✔
CTCInhibitionCav_Cnt_M_u32	415241	415241	✔
CTCInhibitionCmm_Cnt_M_u32	5785	5785	✔
CTCInhibitionEsc_Cnt_M_u32	14165	14165	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	2
Time_ms_T_u32	213526
target_DemIf_Per_CTerm_Cnt_Igc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	12
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_Igc
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08

Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	415241	415241	✔
CTCInhibitionBsi_Cnt_M_u32	5785	5785	✔
CTCInhibitionCav_Cnt_M_u32	415241	415241	✔
CTCInhibitionCmm_Cnt_M_u32	5785	5785	✔
CTCInhibitionEsc_Cnt_M_u32	14165	14165	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	✔
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_DTCStatusChanged

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$ (PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Attributes

Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test ✔

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 3296.00 Cycles
TS 1.2 2545.00 Cycles
```

Description

Vector Description:

TS1.1"Shortest Path:
((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16)==> TRUE &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08)==> FALSE)
(DTCFound_Cnt_T_lgc == TRUE)==> FALSE"
TS1.2"Longest Path:
((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16) &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08))==> TRUE
(DTCFound_Cnt_T_lgc == TRUE)==> TRUE
((DTCStatusNew & D_FAILBITMASK_CNT_U08) == D_FAILBITMASK_CNT_U08)==> FALSE
(CTCFailedBuf_Cnt_M_lgc[i] == TRUE)==> TRUE
"

Test Step 1.1 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	0
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	0
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_lgc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32]	0
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	0
CTCFailedBuf_Cnt_M_Igc[54]	0
CTCFailedBuf_Cnt_M_Igc[55]	0
CTCFailedBuf_Cnt_M_Igc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_Igc[58]	0
CTCFailedBuf_Cnt_M_Igc[59]	0
CTCFailedBuf_Cnt_M_Igc[60]	0
CTCFailedBuf_Cnt_M_Igc[61]	0
CTCFailedBuf_Cnt_M_Igc[62]	0
CTCFailedBuf_Cnt_M_Igc[63]	0
CTCFailedBuf_Cnt_M_Igc[64]	0
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0

Name	Input Value
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[11]	255
Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem_DTC_FTB_Table[14]	255
Dem_DTC_FTB_Table[15]	255
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
Dem_DTC_FTB_Table[30]	255
Dem_DTC_FTB_Table[31]	255
Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[33]	255
Dem_DTC_FTB_Table[34]	255
Dem_DTC_FTB_Table[35]	255
Dem_DTC_FTB_Table[36]	255
Dem_DTC_FTB_Table[37]	255
Dem_DTC_FTB_Table[38]	255

Name	Input Value
Dem_DTC_FTB_Table[39]	255
Dem_DTC_FTB_Table[40]	255
Dem_DTC_FTB_Table[41]	255
Dem_DTC_FTB_Table[42]	255
Dem_DTC_FTB_Table[43]	255
Dem_DTC_FTB_Table[44]	255
Dem_DTC_FTB_Table[45]	255
Dem_DTC_FTB_Table[46]	255
Dem_DTC_FTB_Table[47]	255
Dem_DTC_FTB_Table[48]	255
Dem_DTC_FTB_Table[49]	255
Dem_DTC_FTB_Table[50]	255
Dem_DTC_FTB_Table[51]	255
Dem_DTC_FTB_Table[52]	255
Dem_DTC_FTB_Table[53]	255
Dem_DTC_FTB_Table[54]	255
Dem_DTC_FTB_Table[55]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[57]	255
Dem_DTC_FTB_Table[58]	255
Dem_DTC_FTB_Table[59]	255
Dem_DTC_FTB_Table[60]	255
Dem_DTC_FTB_Table[61]	255
Dem_DTC_FTB_Table[62]	255
Dem_DTC_FTB_Table[63]	255
Dem_DTC_FTB_Table[64]	255
Dem_DTC_FTB_Table[65]	255
Dem_DTC_FTB_Table[66]	255
Dem_DTC_FTB_Table[67]	255
Dem_DTC_FTB_Table[68]	255
Dem_DTC_FTB_Table[69]	255
Dem_DTC_FTB_Table[70]	255
Dem_DTC_FTB_Table[71]	255
Dem_DTC_FTB_Table[72]	255
Dem_DTC_FTB_Table[73]	255
Dem_DTC_FTB_Table[74]	255
Dem_DTC_FTB_Table[75]	255
Dem_DTC_FTB_Table[76]	255

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[10]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[14]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[17]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[24]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[29]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[32]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[33]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[34]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[37]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[54]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[55]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[56]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[57]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[58]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[59]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[60]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[61]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[62]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[63]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[64]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	1
CTCFailedBuf_Cnt_M_Igc[21]	1
CTCFailedBuf_Cnt_M_Igc[22]	1
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	1
CTCFailedBuf_Cnt_M_Igc[35]	1
CTCFailedBuf_Cnt_M_Igc[36]	1
CTCFailedBuf_Cnt_M_Igc[37]	1
CTCFailedBuf_Cnt_M_Igc[38]	1
CTCFailedBuf_Cnt_M_Igc[39]	1
CTCFailedBuf_Cnt_M_Igc[40]	1
CTCFailedBuf_Cnt_M_Igc[41]	1
CTCFailedBuf_Cnt_M_Igc[42]	1
CTCFailedBuf_Cnt_M_Igc[43]	1
CTCFailedBuf_Cnt_M_Igc[44]	1
CTCFailedBuf_Cnt_M_Igc[45]	1
CTCFailedBuf_Cnt_M_Igc[46]	1
CTCFailedBuf_Cnt_M_Igc[47]	1
CTCFailedBuf_Cnt_M_Igc[48]	1
CTCFailedBuf_Cnt_M_Igc[49]	1
CTCFailedBuf_Cnt_M_Igc[50]	1
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_Igc[52]	1
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	1
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	1
CTCFailedBuf_Cnt_M_Igc[69]	1
CTCFailedBuf_Cnt_M_Igc[70]	1
CTCFailedBuf_Cnt_M_Igc[71]	1
CTCFailedBuf_Cnt_M_Igc[72]	1
CTCFailedBuf_Cnt_M_Igc[73]	1
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	1
CTCFailedBuf_Cnt_M_Igc[76]	1
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0

Name	Input Value
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0

Name	Input Value
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
Dem_DTC_FTB_Table[71]	0
Dem_DTC_FTB_Table[72]	0
Dem_DTC_FTB_Table[73]	0
Dem_DTC_FTB_Table[74]	0
Dem_DTC_FTB_Table[75]	0
Dem_DTC_FTB_Table[76]	0

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[21]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[22]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[35]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[36]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[37]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[38]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[39]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[40]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[41]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[42]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[43]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[44]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[45]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[46]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[47]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[48]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[49]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[50]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[51]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[52]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[66]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[67]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[68]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[69]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[70]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[71]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[72]	1	1	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[73]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[75]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[76]	1	1	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Case 2: Range Test ✔

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 2437.00 Cycles
TS 2.2 663.00 Cycles
TS 2.3 3222.00 Cycles
TS 2.4 3208.00 Cycles
TS 2.5 3208.00 Cycles
TS 2.6 3208.00 Cycles
TS 2.7 3208.00 Cycles
TS 2.8 3208.00 Cycles
TS 2.9 3208.00 Cycles
TS 2.10 3208.00 Cycles
TS 2.11 3208.00 Cycles
TS 2.12 3208.00 Cycles
TS 2.13 3208.00 Cycles
TS 2.14 3208.00 Cycles
TS 2.15 3208.00 Cycles
TS 2.16 3208.00 Cycles
TS 2.17 3208.00 Cycles
TS 2.18 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.20 3208.00 Cycles
TS 2.21 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
```

Description

Vector Description:

TS 2.1All Min
TS 2.2All Max
TS 2.3DTC==> Min
TS 2.4DTC==> Max
TS 2.5DTC==> Pos
TS 2.6DTCKind==> Min
TS 2.7DTCKind==> Max
TS 2.8DTCStatusOld==> Min
TS 2.9DTCStatusOld==> Max
TS 2.10DTCStatusOld==> Pos
TS 2.11DTCStatusNew==> Min
TS 2.12DTCStatusNew==> Max
TS 2.13DTCStatusNew==> Pos
TS 2.14CTCFailedBuf_Cnt_M_lgc[79]==> Min
TS 2.15CTCFailedBuf_Cnt_M_lgc[79]==> Max
TS 2.16CTCFailedBuf_Cnt_M_lgc[79]==> Pos
TS 2.17CTCFailed_Cnt_M_lgc==> Min
TS 2.18CTCFailed_Cnt_M_lgc==> Max
TS 2.19Dem_DTCNumberTable[79]==> Min
TS 2.20Dem_DTCNumberTable[79]==> Max
TS 2.21Dem_DTCNumberTable[79]==> Pos
TS 2.22Dem_DTC_FTB_Table[79]==> Min
TS 2.23Dem_DTC_FTB_Table[79]==> Max
TS 2.24Dem_DTC_FTB_Table[79]==> Pos

Test Step 2.1 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[12]	0
CTCFailedBuf_Cnt_M_Igc[13]	0
CTCFailedBuf_Cnt_M_Igc[14]	0
CTCFailedBuf_Cnt_M_Igc[15]	0
CTCFailedBuf_Cnt_M_Igc[16]	0
CTCFailedBuf_Cnt_M_Igc[17]	0
CTCFailedBuf_Cnt_M_Igc[18]	0
CTCFailedBuf_Cnt_M_Igc[19]	0
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	0
CTCFailedBuf_Cnt_M_Igc[24]	0
CTCFailedBuf_Cnt_M_Igc[25]	0
CTCFailedBuf_Cnt_M_Igc[26]	0
CTCFailedBuf_Cnt_M_Igc[27]	0
CTCFailedBuf_Cnt_M_Igc[28]	0
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_Igc[30]	0
CTCFailedBuf_Cnt_M_Igc[31]	0
CTCFailedBuf_Cnt_M_Igc[32]	0
CTCFailedBuf_Cnt_M_Igc[33]	0
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	0
CTCFailedBuf_Cnt_M_Igc[54]	0
CTCFailedBuf_Cnt_M_Igc[55]	0
CTCFailedBuf_Cnt_M_Igc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_Igc[58]	0
CTCFailedBuf_Cnt_M_Igc[59]	0
CTCFailedBuf_Cnt_M_Igc[60]	0
CTCFailedBuf_Cnt_M_Igc[61]	0
CTCFailedBuf_Cnt_M_Igc[62]	0
CTCFailedBuf_Cnt_M_Igc[63]	0
CTCFailedBuf_Cnt_M_Igc[64]	0
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0

Name	Input Value
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0

Name	Input Value
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
Dem_DTC_FTB_Table[71]	0

Name	Input Value
Dem_DTC_FTB_Table[72]	0
Dem_DTC_FTB_Table[73]	0
Dem_DTC_FTB_Table[74]	0
Dem_DTC_FTB_Table[75]	0
Dem_DTC_FTB_Table[76]	0

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[10]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[14]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[17]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[24]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[29]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[32]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[33]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[54]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[55]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[56]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[57]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[58]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[59]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[60]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[61]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[62]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[63]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[64]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	1
CTCFailedBuf_Cnt_M_Igc[1]	1
CTCFailedBuf_Cnt_M_Igc[2]	1
CTCFailedBuf_Cnt_M_Igc[3]	1
CTCFailedBuf_Cnt_M_Igc[4]	1
CTCFailedBuf_Cnt_M_Igc[5]	1
CTCFailedBuf_Cnt_M_Igc[6]	1
CTCFailedBuf_Cnt_M_Igc[7]	1
CTCFailedBuf_Cnt_M_Igc[8]	1
CTCFailedBuf_Cnt_M_Igc[9]	1
CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	1
CTCFailedBuf_Cnt_M_Igc[21]	1
CTCFailedBuf_Cnt_M_Igc[22]	1
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	1
CTCFailedBuf_Cnt_M_Igc[35]	1
CTCFailedBuf_Cnt_M_Igc[36]	1
CTCFailedBuf_Cnt_M_Igc[37]	1
CTCFailedBuf_Cnt_M_Igc[38]	1
CTCFailedBuf_Cnt_M_Igc[39]	1
CTCFailedBuf_Cnt_M_Igc[40]	1
CTCFailedBuf_Cnt_M_Igc[41]	1
CTCFailedBuf_Cnt_M_Igc[42]	1
CTCFailedBuf_Cnt_M_Igc[43]	1
CTCFailedBuf_Cnt_M_Igc[44]	1
CTCFailedBuf_Cnt_M_Igc[45]	1
CTCFailedBuf_Cnt_M_Igc[46]	1
CTCFailedBuf_Cnt_M_Igc[47]	1
CTCFailedBuf_Cnt_M_Igc[48]	1
CTCFailedBuf_Cnt_M_Igc[49]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[50]	1
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_Igc[52]	1
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	1
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	1
CTCFailedBuf_Cnt_M_Igc[69]	1
CTCFailedBuf_Cnt_M_Igc[70]	1
CTCFailedBuf_Cnt_M_Igc[71]	1
CTCFailedBuf_Cnt_M_Igc[72]	1
CTCFailedBuf_Cnt_M_Igc[73]	1
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	1
CTCFailedBuf_Cnt_M_Igc[76]	1
CTCFailed_Cnt_M_Igc	1
DTC	4294967295
DTCKind	2
DTCStatusNew	255
DTCStatusOld	255
Dem_DTCNumberTable[0]	65535
Dem_DTCNumberTable[1]	65535
Dem_DTCNumberTable[2]	65535
Dem_DTCNumberTable[3]	65535
Dem_DTCNumberTable[4]	65535
Dem_DTCNumberTable[5]	65535
Dem_DTCNumberTable[6]	65535
Dem_DTCNumberTable[7]	65535
Dem_DTCNumberTable[8]	65535
Dem_DTCNumberTable[9]	65535
Dem_DTCNumberTable[10]	65535
Dem_DTCNumberTable[11]	65535
Dem_DTCNumberTable[12]	65535
Dem_DTCNumberTable[13]	65535
Dem_DTCNumberTable[14]	65535
Dem_DTCNumberTable[15]	65535
Dem_DTCNumberTable[16]	65535
Dem_DTCNumberTable[17]	65535
Dem_DTCNumberTable[18]	65535
Dem_DTCNumberTable[19]	65535
Dem_DTCNumberTable[20]	65535
Dem_DTCNumberTable[21]	65535
Dem_DTCNumberTable[22]	65535
Dem_DTCNumberTable[23]	65535
Dem_DTCNumberTable[24]	65535
Dem_DTCNumberTable[25]	65535
Dem_DTCNumberTable[26]	65535
Dem_DTCNumberTable[27]	65535
Dem_DTCNumberTable[28]	65535
Dem_DTCNumberTable[29]	65535
Dem_DTCNumberTable[30]	65535
Dem_DTCNumberTable[31]	65535
Dem_DTCNumberTable[32]	65535
Dem_DTCNumberTable[33]	65535
Dem_DTCNumberTable[34]	65535
Dem_DTCNumberTable[35]	65535
Dem_DTCNumberTable[36]	65535
Dem_DTCNumberTable[37]	65535
Dem_DTCNumberTable[38]	65535
Dem_DTCNumberTable[39]	65535
Dem_DTCNumberTable[40]	65535

Name	Input Value
Dem_DTCNumberTable[41]	65535
Dem_DTCNumberTable[42]	65535
Dem_DTCNumberTable[43]	65535
Dem_DTCNumberTable[44]	65535
Dem_DTCNumberTable[45]	65535
Dem_DTCNumberTable[46]	65535
Dem_DTCNumberTable[47]	65535
Dem_DTCNumberTable[48]	65535
Dem_DTCNumberTable[49]	65535
Dem_DTCNumberTable[50]	65535
Dem_DTCNumberTable[51]	65535
Dem_DTCNumberTable[52]	65535
Dem_DTCNumberTable[53]	65535
Dem_DTCNumberTable[54]	65535
Dem_DTCNumberTable[55]	65535
Dem_DTCNumberTable[56]	65535
Dem_DTCNumberTable[57]	65535
Dem_DTCNumberTable[58]	65535
Dem_DTCNumberTable[59]	65535
Dem_DTCNumberTable[60]	65535
Dem_DTCNumberTable[61]	65535
Dem_DTCNumberTable[62]	65535
Dem_DTCNumberTable[63]	65535
Dem_DTCNumberTable[64]	65535
Dem_DTCNumberTable[65]	65535
Dem_DTCNumberTable[66]	65535
Dem_DTCNumberTable[67]	65535
Dem_DTCNumberTable[68]	65535
Dem_DTCNumberTable[69]	65535
Dem_DTCNumberTable[70]	65535
Dem_DTCNumberTable[71]	65535
Dem_DTCNumberTable[72]	65535
Dem_DTCNumberTable[73]	65535
Dem_DTCNumberTable[74]	65535
Dem_DTCNumberTable[75]	65535
Dem_DTCNumberTable[76]	65535
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[11]	255
Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem_DTC_FTB_Table[14]	255
Dem_DTC_FTB_Table[15]	255
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
Dem_DTC_FTB_Table[30]	255
Dem_DTC_FTB_Table[31]	255
Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[33]	255
Dem_DTC_FTB_Table[34]	255
Dem_DTC_FTB_Table[35]	255
Dem_DTC_FTB_Table[36]	255

Name	Input Value
Dem_DTC_FTB_Table[37]	255
Dem_DTC_FTB_Table[38]	255
Dem_DTC_FTB_Table[39]	255
Dem_DTC_FTB_Table[40]	255
Dem_DTC_FTB_Table[41]	255
Dem_DTC_FTB_Table[42]	255
Dem_DTC_FTB_Table[43]	255
Dem_DTC_FTB_Table[44]	255
Dem_DTC_FTB_Table[45]	255
Dem_DTC_FTB_Table[46]	255
Dem_DTC_FTB_Table[47]	255
Dem_DTC_FTB_Table[48]	255
Dem_DTC_FTB_Table[49]	255
Dem_DTC_FTB_Table[50]	255
Dem_DTC_FTB_Table[51]	255
Dem_DTC_FTB_Table[52]	255
Dem_DTC_FTB_Table[53]	255
Dem_DTC_FTB_Table[54]	255
Dem_DTC_FTB_Table[55]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[57]	255
Dem_DTC_FTB_Table[58]	255
Dem_DTC_FTB_Table[59]	255
Dem_DTC_FTB_Table[60]	255
Dem_DTC_FTB_Table[61]	255
Dem_DTC_FTB_Table[62]	255
Dem_DTC_FTB_Table[63]	255
Dem_DTC_FTB_Table[64]	255
Dem_DTC_FTB_Table[65]	255
Dem_DTC_FTB_Table[66]	255
Dem_DTC_FTB_Table[67]	255
Dem_DTC_FTB_Table[68]	255
Dem_DTC_FTB_Table[69]	255
Dem_DTC_FTB_Table[70]	255
Dem_DTC_FTB_Table[71]	255
Dem_DTC_FTB_Table[72]	255
Dem_DTC_FTB_Table[73]	255
Dem_DTC_FTB_Table[74]	255
Dem_DTC_FTB_Table[75]	255
Dem_DTC_FTB_Table[76]	255

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[21]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[22]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[35]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[36]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[37]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[38]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[39]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[40]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[41]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[42]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[43]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[44]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[45]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[46]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[47]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[48]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[49]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[50]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[51]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[52]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[66]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[67]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[68]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[69]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[70]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[71]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[72]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[73]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[75]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[76]	1	1	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	0
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	0
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	148
DTCStatusOld	39
Dem_DTCNumberTable[0]	181
Dem_DTCNumberTable[1]	1
Dem_DTCNumberTable[2]	41
Dem_DTCNumberTable[3]	22
Dem_DTCNumberTable[4]	24
Dem_DTCNumberTable[5]	254

Name	Input Value
Dem_DTCNumberTable[6]	209
Dem_DTCNumberTable[7]	209
Dem_DTCNumberTable[8]	181
Dem_DTCNumberTable[9]	1
Dem_DTCNumberTable[10]	209
Dem_DTCNumberTable[11]	128
Dem_DTCNumberTable[12]	1
Dem_DTCNumberTable[13]	209
Dem_DTCNumberTable[14]	181
Dem_DTCNumberTable[15]	1
Dem_DTCNumberTable[16]	1
Dem_DTCNumberTable[17]	209
Dem_DTCNumberTable[18]	33
Dem_DTCNumberTable[19]	181
Dem_DTCNumberTable[20]	1
Dem_DTCNumberTable[21]	209
Dem_DTCNumberTable[22]	181
Dem_DTCNumberTable[23]	41
Dem_DTCNumberTable[24]	22
Dem_DTCNumberTable[25]	24
Dem_DTCNumberTable[26]	254
Dem_DTCNumberTable[27]	1
Dem_DTCNumberTable[28]	181
Dem_DTCNumberTable[29]	1
Dem_DTCNumberTable[30]	181
Dem_DTCNumberTable[31]	181
Dem_DTCNumberTable[32]	1
Dem_DTCNumberTable[33]	1
Dem_DTCNumberTable[34]	181
Dem_DTCNumberTable[35]	1
Dem_DTCNumberTable[36]	181
Dem_DTCNumberTable[37]	181
Dem_DTCNumberTable[38]	181
Dem_DTCNumberTable[39]	1
Dem_DTCNumberTable[40]	1
Dem_DTCNumberTable[41]	41
Dem_DTCNumberTable[42]	22
Dem_DTCNumberTable[43]	24
Dem_DTCNumberTable[44]	254
Dem_DTCNumberTable[45]	209
Dem_DTCNumberTable[46]	181
Dem_DTCNumberTable[47]	1
Dem_DTCNumberTable[48]	22
Dem_DTCNumberTable[49]	181
Dem_DTCNumberTable[50]	1
Dem_DTCNumberTable[51]	181
Dem_DTCNumberTable[52]	181
Dem_DTCNumberTable[53]	1
Dem_DTCNumberTable[54]	22
Dem_DTCNumberTable[55]	209
Dem_DTCNumberTable[56]	181
Dem_DTCNumberTable[57]	1
Dem_DTCNumberTable[58]	181
Dem_DTCNumberTable[59]	209
Dem_DTCNumberTable[60]	181
Dem_DTCNumberTable[61]	1
Dem_DTCNumberTable[62]	22
Dem_DTCNumberTable[63]	41
Dem_DTCNumberTable[64]	22
Dem_DTCNumberTable[65]	24
Dem_DTCNumberTable[66]	254
Dem_DTCNumberTable[67]	181
Dem_DTCNumberTable[68]	181
Dem_DTCNumberTable[69]	1
Dem_DTCNumberTable[70]	22
Dem_DTCNumberTable[71]	209
Dem_DTCNumberTable[72]	22
Dem_DTCNumberTable[73]	41
Dem_DTCNumberTable[74]	22
Dem_DTCNumberTable[75]	24
Dem_DTCNumberTable[76]	254
Dem_DTC_FTB_Table[0]	245
Dem_DTC_FTB_Table[1]	151

Name	Input Value
Dem_DTC_FTB_Table[2]	199
Dem_DTC_FTB_Table[3]	160
Dem_DTC_FTB_Table[4]	30
Dem_DTC_FTB_Table[5]	136
Dem_DTC_FTB_Table[6]	178
Dem_DTC_FTB_Table[7]	178
Dem_DTC_FTB_Table[8]	245
Dem_DTC_FTB_Table[9]	151
Dem_DTC_FTB_Table[10]	178
Dem_DTC_FTB_Table[11]	31
Dem_DTC_FTB_Table[12]	151
Dem_DTC_FTB_Table[13]	178
Dem_DTC_FTB_Table[14]	245
Dem_DTC_FTB_Table[15]	151
Dem_DTC_FTB_Table[16]	151
Dem_DTC_FTB_Table[17]	178
Dem_DTC_FTB_Table[18]	234
Dem_DTC_FTB_Table[19]	245
Dem_DTC_FTB_Table[20]	151
Dem_DTC_FTB_Table[21]	178
Dem_DTC_FTB_Table[22]	245
Dem_DTC_FTB_Table[23]	199
Dem_DTC_FTB_Table[24]	160
Dem_DTC_FTB_Table[25]	30
Dem_DTC_FTB_Table[26]	136
Dem_DTC_FTB_Table[27]	151
Dem_DTC_FTB_Table[28]	245
Dem_DTC_FTB_Table[29]	151
Dem_DTC_FTB_Table[30]	245
Dem_DTC_FTB_Table[31]	245
Dem_DTC_FTB_Table[32]	151
Dem_DTC_FTB_Table[33]	151
Dem_DTC_FTB_Table[34]	245
Dem_DTC_FTB_Table[35]	151
Dem_DTC_FTB_Table[36]	245
Dem_DTC_FTB_Table[37]	245
Dem_DTC_FTB_Table[38]	245
Dem_DTC_FTB_Table[39]	151
Dem_DTC_FTB_Table[40]	151
Dem_DTC_FTB_Table[41]	199
Dem_DTC_FTB_Table[42]	160
Dem_DTC_FTB_Table[43]	30
Dem_DTC_FTB_Table[44]	136
Dem_DTC_FTB_Table[45]	178
Dem_DTC_FTB_Table[46]	245
Dem_DTC_FTB_Table[47]	151
Dem_DTC_FTB_Table[48]	160
Dem_DTC_FTB_Table[49]	245
Dem_DTC_FTB_Table[50]	151
Dem_DTC_FTB_Table[51]	245
Dem_DTC_FTB_Table[52]	245
Dem_DTC_FTB_Table[53]	151
Dem_DTC_FTB_Table[54]	160
Dem_DTC_FTB_Table[55]	178
Dem_DTC_FTB_Table[56]	245
Dem_DTC_FTB_Table[57]	151
Dem_DTC_FTB_Table[58]	245
Dem_DTC_FTB_Table[59]	178
Dem_DTC_FTB_Table[60]	245
Dem_DTC_FTB_Table[61]	151
Dem_DTC_FTB_Table[62]	160
Dem_DTC_FTB_Table[63]	199
Dem_DTC_FTB_Table[64]	160
Dem_DTC_FTB_Table[65]	30
Dem_DTC_FTB_Table[66]	136
Dem_DTC_FTB_Table[67]	245
Dem_DTC_FTB_Table[68]	245
Dem_DTC_FTB_Table[69]	151
Dem_DTC_FTB_Table[70]	160
Dem_DTC_FTB_Table[71]	178
Dem_DTC_FTB_Table[72]	160
Dem_DTC_FTB_Table[73]	199
Dem_DTC_FTB_Table[74]	160

Name	Input Value
Dem_DTC_FTB_Table[75]	30
Dem_DTC_FTB_Table[76]	136

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	1
CTCFailedBuf_Cnt_M_Igc[1]	1
CTCFailedBuf_Cnt_M_Igc[2]	1
CTCFailedBuf_Cnt_M_Igc[3]	1
CTCFailedBuf_Cnt_M_Igc[4]	1
CTCFailedBuf_Cnt_M_Igc[5]	1
CTCFailedBuf_Cnt_M_Igc[6]	1
CTCFailedBuf_Cnt_M_Igc[7]	1
CTCFailedBuf_Cnt_M_Igc[8]	1
CTCFailedBuf_Cnt_M_Igc[9]	1
CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	0
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	1
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	4294967295
DTCKind	2
DTCStatusNew	126
DTCStatusOld	203
Dem_DTCNumberTable[0]	182
Dem_DTCNumberTable[1]	221
Dem_DTCNumberTable[2]	159
Dem_DTCNumberTable[3]	164
Dem_DTCNumberTable[4]	34
Dem_DTCNumberTable[5]	166
Dem_DTCNumberTable[6]	237
Dem_DTCNumberTable[7]	237
Dem_DTCNumberTable[8]	182
Dem_DTCNumberTable[9]	221
Dem_DTCNumberTable[10]	237
Dem_DTCNumberTable[11]	123
Dem_DTCNumberTable[12]	221
Dem_DTCNumberTable[13]	237
Dem_DTCNumberTable[14]	182
Dem_DTCNumberTable[15]	221
Dem_DTCNumberTable[16]	221
Dem_DTCNumberTable[17]	237
Dem_DTCNumberTable[18]	239
Dem_DTCNumberTable[19]	182
Dem_DTCNumberTable[20]	221
Dem_DTCNumberTable[21]	237
Dem_DTCNumberTable[22]	182
Dem_DTCNumberTable[23]	159
Dem_DTCNumberTable[24]	164
Dem_DTCNumberTable[25]	34
Dem_DTCNumberTable[26]	166
Dem_DTCNumberTable[27]	221
Dem_DTCNumberTable[28]	182
Dem_DTCNumberTable[29]	221
Dem_DTCNumberTable[30]	182
Dem_DTCNumberTable[31]	182
Dem_DTCNumberTable[32]	221
Dem_DTCNumberTable[33]	221
Dem_DTCNumberTable[34]	182
Dem_DTCNumberTable[35]	221
Dem_DTCNumberTable[36]	182
Dem_DTCNumberTable[37]	182
Dem_DTCNumberTable[38]	182
Dem_DTCNumberTable[39]	221
Dem_DTCNumberTable[40]	221
Dem_DTCNumberTable[41]	159
Dem_DTCNumberTable[42]	164
Dem_DTCNumberTable[43]	34

Name	Input Value
Dem_DTCNumberTable[44]	166
Dem_DTCNumberTable[45]	237
Dem_DTCNumberTable[46]	182
Dem_DTCNumberTable[47]	221
Dem_DTCNumberTable[48]	164
Dem_DTCNumberTable[49]	182
Dem_DTCNumberTable[50]	221
Dem_DTCNumberTable[51]	182
Dem_DTCNumberTable[52]	182
Dem_DTCNumberTable[53]	221
Dem_DTCNumberTable[54]	164
Dem_DTCNumberTable[55]	237
Dem_DTCNumberTable[56]	182
Dem_DTCNumberTable[57]	221
Dem_DTCNumberTable[58]	182
Dem_DTCNumberTable[59]	237
Dem_DTCNumberTable[60]	182
Dem_DTCNumberTable[61]	221
Dem_DTCNumberTable[62]	164
Dem_DTCNumberTable[63]	159
Dem_DTCNumberTable[64]	164
Dem_DTCNumberTable[65]	34
Dem_DTCNumberTable[66]	166
Dem_DTCNumberTable[67]	182
Dem_DTCNumberTable[68]	182
Dem_DTCNumberTable[69]	221
Dem_DTCNumberTable[70]	164
Dem_DTCNumberTable[71]	237
Dem_DTCNumberTable[72]	164
Dem_DTCNumberTable[73]	159
Dem_DTCNumberTable[74]	164
Dem_DTCNumberTable[75]	34
Dem_DTCNumberTable[76]	166
Dem_DTC_FTB_Table[0]	100
Dem_DTC_FTB_Table[1]	77
Dem_DTC_FTB_Table[2]	185
Dem_DTC_FTB_Table[3]	93
Dem_DTC_FTB_Table[4]	72
Dem_DTC_FTB_Table[5]	20
Dem_DTC_FTB_Table[6]	13
Dem_DTC_FTB_Table[7]	13
Dem_DTC_FTB_Table[8]	100
Dem_DTC_FTB_Table[9]	77
Dem_DTC_FTB_Table[10]	13
Dem_DTC_FTB_Table[11]	191
Dem_DTC_FTB_Table[12]	77
Dem_DTC_FTB_Table[13]	13
Dem_DTC_FTB_Table[14]	100
Dem_DTC_FTB_Table[15]	77
Dem_DTC_FTB_Table[16]	77
Dem_DTC_FTB_Table[17]	13
Dem_DTC_FTB_Table[18]	69
Dem_DTC_FTB_Table[19]	100
Dem_DTC_FTB_Table[20]	77
Dem_DTC_FTB_Table[21]	13
Dem_DTC_FTB_Table[22]	100
Dem_DTC_FTB_Table[23]	185
Dem_DTC_FTB_Table[24]	93
Dem_DTC_FTB_Table[25]	72
Dem_DTC_FTB_Table[26]	20
Dem_DTC_FTB_Table[27]	77
Dem_DTC_FTB_Table[28]	100
Dem_DTC_FTB_Table[29]	77
Dem_DTC_FTB_Table[30]	100
Dem_DTC_FTB_Table[31]	100
Dem_DTC_FTB_Table[32]	77
Dem_DTC_FTB_Table[33]	77
Dem_DTC_FTB_Table[34]	100
Dem_DTC_FTB_Table[35]	77
Dem_DTC_FTB_Table[36]	100
Dem_DTC_FTB_Table[37]	100
Dem_DTC_FTB_Table[38]	100
Dem_DTC_FTB_Table[39]	77

Name	Input Value
Dem_DTC_FTB_Table[40]	77
Dem_DTC_FTB_Table[41]	185
Dem_DTC_FTB_Table[42]	93
Dem_DTC_FTB_Table[43]	72
Dem_DTC_FTB_Table[44]	20
Dem_DTC_FTB_Table[45]	13
Dem_DTC_FTB_Table[46]	100
Dem_DTC_FTB_Table[47]	77
Dem_DTC_FTB_Table[48]	93
Dem_DTC_FTB_Table[49]	100
Dem_DTC_FTB_Table[50]	77
Dem_DTC_FTB_Table[51]	100
Dem_DTC_FTB_Table[52]	100
Dem_DTC_FTB_Table[53]	77
Dem_DTC_FTB_Table[54]	93
Dem_DTC_FTB_Table[55]	13
Dem_DTC_FTB_Table[56]	100
Dem_DTC_FTB_Table[57]	77
Dem_DTC_FTB_Table[58]	100
Dem_DTC_FTB_Table[59]	13
Dem_DTC_FTB_Table[60]	100
Dem_DTC_FTB_Table[61]	77
Dem_DTC_FTB_Table[62]	93
Dem_DTC_FTB_Table[63]	185
Dem_DTC_FTB_Table[64]	93
Dem_DTC_FTB_Table[65]	72
Dem_DTC_FTB_Table[66]	20
Dem_DTC_FTB_Table[67]	100
Dem_DTC_FTB_Table[68]	100
Dem_DTC_FTB_Table[69]	77
Dem_DTC_FTB_Table[70]	93
Dem_DTC_FTB_Table[71]	13
Dem_DTC_FTB_Table[72]	93
Dem_DTC_FTB_Table[73]	185
Dem_DTC_FTB_Table[74]	93
Dem_DTC_FTB_Table[75]	72
Dem_DTC_FTB_Table[76]	20

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[37]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	1
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	256327693
DTCKind	1
DTCStatusNew	30
DTCStatusOld	178
Dem_DTCNumberTable[0]	99
Dem_DTCNumberTable[1]	143
Dem_DTCNumberTable[2]	36
Dem_DTCNumberTable[3]	85
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	62
Dem_DTCNumberTable[6]	217
Dem_DTCNumberTable[7]	217
Dem_DTCNumberTable[8]	99

Name	Input Value
Dem_DTCNumberTable[9]	143
Dem_DTCNumberTable[10]	217
Dem_DTCNumberTable[11]	101
Dem_DTCNumberTable[12]	143
Dem_DTCNumberTable[13]	217
Dem_DTCNumberTable[14]	99
Dem_DTCNumberTable[15]	143
Dem_DTCNumberTable[16]	143
Dem_DTCNumberTable[17]	217
Dem_DTCNumberTable[18]	236
Dem_DTCNumberTable[19]	99
Dem_DTCNumberTable[20]	143
Dem_DTCNumberTable[21]	217
Dem_DTCNumberTable[22]	99
Dem_DTCNumberTable[23]	36
Dem_DTCNumberTable[24]	85
Dem_DTCNumberTable[25]	238
Dem_DTCNumberTable[26]	62
Dem_DTCNumberTable[27]	143
Dem_DTCNumberTable[28]	99
Dem_DTCNumberTable[29]	143
Dem_DTCNumberTable[30]	99
Dem_DTCNumberTable[31]	99
Dem_DTCNumberTable[32]	143
Dem_DTCNumberTable[33]	143
Dem_DTCNumberTable[34]	99
Dem_DTCNumberTable[35]	143
Dem_DTCNumberTable[36]	99
Dem_DTCNumberTable[37]	99
Dem_DTCNumberTable[38]	99
Dem_DTCNumberTable[39]	143
Dem_DTCNumberTable[40]	143
Dem_DTCNumberTable[41]	36
Dem_DTCNumberTable[42]	85
Dem_DTCNumberTable[43]	238
Dem_DTCNumberTable[44]	62
Dem_DTCNumberTable[45]	217
Dem_DTCNumberTable[46]	99
Dem_DTCNumberTable[47]	143
Dem_DTCNumberTable[48]	85
Dem_DTCNumberTable[49]	99
Dem_DTCNumberTable[50]	143
Dem_DTCNumberTable[51]	99
Dem_DTCNumberTable[52]	99
Dem_DTCNumberTable[53]	143
Dem_DTCNumberTable[54]	85
Dem_DTCNumberTable[55]	217
Dem_DTCNumberTable[56]	99
Dem_DTCNumberTable[57]	143
Dem_DTCNumberTable[58]	99
Dem_DTCNumberTable[59]	217
Dem_DTCNumberTable[60]	99
Dem_DTCNumberTable[61]	143
Dem_DTCNumberTable[62]	85
Dem_DTCNumberTable[63]	36
Dem_DTCNumberTable[64]	85
Dem_DTCNumberTable[65]	238
Dem_DTCNumberTable[66]	62
Dem_DTCNumberTable[67]	99
Dem_DTCNumberTable[68]	99
Dem_DTCNumberTable[69]	143
Dem_DTCNumberTable[70]	85
Dem_DTCNumberTable[71]	217
Dem_DTCNumberTable[72]	85
Dem_DTCNumberTable[73]	36
Dem_DTCNumberTable[74]	85
Dem_DTCNumberTable[75]	238
Dem_DTCNumberTable[76]	62
Dem_DTC_FTB_Table[0]	161
Dem_DTC_FTB_Table[1]	211
Dem_DTC_FTB_Table[2]	7
Dem_DTC_FTB_Table[3]	239
Dem_DTC_FTB_Table[4]	206

Name	Input Value
Dem_DTC_FTB_Table[5]	70
Dem_DTC_FTB_Table[6]	84
Dem_DTC_FTB_Table[7]	84
Dem_DTC_FTB_Table[8]	161
Dem_DTC_FTB_Table[9]	211
Dem_DTC_FTB_Table[10]	84
Dem_DTC_FTB_Table[11]	193
Dem_DTC_FTB_Table[12]	211
Dem_DTC_FTB_Table[13]	84
Dem_DTC_FTB_Table[14]	161
Dem_DTC_FTB_Table[15]	211
Dem_DTC_FTB_Table[16]	211
Dem_DTC_FTB_Table[17]	84
Dem_DTC_FTB_Table[18]	108
Dem_DTC_FTB_Table[19]	161
Dem_DTC_FTB_Table[20]	211
Dem_DTC_FTB_Table[21]	84
Dem_DTC_FTB_Table[22]	161
Dem_DTC_FTB_Table[23]	7
Dem_DTC_FTB_Table[24]	239
Dem_DTC_FTB_Table[25]	206
Dem_DTC_FTB_Table[26]	70
Dem_DTC_FTB_Table[27]	211
Dem_DTC_FTB_Table[28]	161
Dem_DTC_FTB_Table[29]	211
Dem_DTC_FTB_Table[30]	161
Dem_DTC_FTB_Table[31]	161
Dem_DTC_FTB_Table[32]	211
Dem_DTC_FTB_Table[33]	211
Dem_DTC_FTB_Table[34]	161
Dem_DTC_FTB_Table[35]	211
Dem_DTC_FTB_Table[36]	161
Dem_DTC_FTB_Table[37]	161
Dem_DTC_FTB_Table[38]	161
Dem_DTC_FTB_Table[39]	211
Dem_DTC_FTB_Table[40]	211
Dem_DTC_FTB_Table[41]	7
Dem_DTC_FTB_Table[42]	239
Dem_DTC_FTB_Table[43]	206
Dem_DTC_FTB_Table[44]	70
Dem_DTC_FTB_Table[45]	84
Dem_DTC_FTB_Table[46]	161
Dem_DTC_FTB_Table[47]	211
Dem_DTC_FTB_Table[48]	239
Dem_DTC_FTB_Table[49]	161
Dem_DTC_FTB_Table[50]	211
Dem_DTC_FTB_Table[51]	161
Dem_DTC_FTB_Table[52]	161
Dem_DTC_FTB_Table[53]	211
Dem_DTC_FTB_Table[54]	239
Dem_DTC_FTB_Table[55]	84
Dem_DTC_FTB_Table[56]	161
Dem_DTC_FTB_Table[57]	211
Dem_DTC_FTB_Table[58]	161
Dem_DTC_FTB_Table[59]	84
Dem_DTC_FTB_Table[60]	161
Dem_DTC_FTB_Table[61]	211
Dem_DTC_FTB_Table[62]	239
Dem_DTC_FTB_Table[63]	7
Dem_DTC_FTB_Table[64]	239
Dem_DTC_FTB_Table[65]	206
Dem_DTC_FTB_Table[66]	70
Dem_DTC_FTB_Table[67]	161
Dem_DTC_FTB_Table[68]	161
Dem_DTC_FTB_Table[69]	211
Dem_DTC_FTB_Table[70]	239
Dem_DTC_FTB_Table[71]	84
Dem_DTC_FTB_Table[72]	239
Dem_DTC_FTB_Table[73]	7
Dem_DTC_FTB_Table[74]	239
Dem_DTC_FTB_Table[75]	206
Dem_DTC_FTB_Table[76]	70

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	3061213468
DTCKind	1
DTCStatusNew	72
DTCStatusOld	13
Dem_DTCNumberTable[0]	31
Dem_DTCNumberTable[1]	227
Dem_DTCNumberTable[2]	66
Dem_DTCNumberTable[3]	96
Dem_DTCNumberTable[4]	130
Dem_DTCNumberTable[5]	24
Dem_DTCNumberTable[6]	240
Dem_DTCNumberTable[7]	240
Dem_DTCNumberTable[8]	31
Dem_DTCNumberTable[9]	227
Dem_DTCNumberTable[10]	240
Dem_DTCNumberTable[11]	151
Dem_DTCNumberTable[12]	227
Dem_DTCNumberTable[13]	240
Dem_DTCNumberTable[14]	31
Dem_DTCNumberTable[15]	227
Dem_DTCNumberTable[16]	227
Dem_DTCNumberTable[17]	240
Dem_DTCNumberTable[18]	241
Dem_DTCNumberTable[19]	31
Dem_DTCNumberTable[20]	227
Dem_DTCNumberTable[21]	240
Dem_DTCNumberTable[22]	31
Dem_DTCNumberTable[23]	66
Dem_DTCNumberTable[24]	96
Dem_DTCNumberTable[25]	130
Dem_DTCNumberTable[26]	24
Dem_DTCNumberTable[27]	227
Dem_DTCNumberTable[28]	31
Dem_DTCNumberTable[29]	227
Dem_DTCNumberTable[30]	31
Dem_DTCNumberTable[31]	31
Dem_DTCNumberTable[32]	227
Dem_DTCNumberTable[33]	227
Dem_DTCNumberTable[34]	31
Dem_DTCNumberTable[35]	227
Dem_DTCNumberTable[36]	31
Dem_DTCNumberTable[37]	31
Dem_DTCNumberTable[38]	31
Dem_DTCNumberTable[39]	227
Dem_DTCNumberTable[40]	227
Dem_DTCNumberTable[41]	66
Dem_DTCNumberTable[42]	96
Dem_DTCNumberTable[43]	130
Dem_DTCNumberTable[44]	24
Dem_DTCNumberTable[45]	240
Dem_DTCNumberTable[46]	31

Name	Input Value
Dem_DTCNumberTable[47]	227
Dem_DTCNumberTable[48]	96
Dem_DTCNumberTable[49]	31
Dem_DTCNumberTable[50]	227
Dem_DTCNumberTable[51]	31
Dem_DTCNumberTable[52]	31
Dem_DTCNumberTable[53]	227
Dem_DTCNumberTable[54]	96
Dem_DTCNumberTable[55]	240
Dem_DTCNumberTable[56]	31
Dem_DTCNumberTable[57]	227
Dem_DTCNumberTable[58]	31
Dem_DTCNumberTable[59]	240
Dem_DTCNumberTable[60]	31
Dem_DTCNumberTable[61]	227
Dem_DTCNumberTable[62]	96
Dem_DTCNumberTable[63]	66
Dem_DTCNumberTable[64]	96
Dem_DTCNumberTable[65]	130
Dem_DTCNumberTable[66]	24
Dem_DTCNumberTable[67]	31
Dem_DTCNumberTable[68]	31
Dem_DTCNumberTable[69]	227
Dem_DTCNumberTable[70]	96
Dem_DTCNumberTable[71]	240
Dem_DTCNumberTable[72]	96
Dem_DTCNumberTable[73]	66
Dem_DTCNumberTable[74]	96
Dem_DTCNumberTable[75]	130
Dem_DTCNumberTable[76]	24
Dem_DTC_FTB_Table[0]	181
Dem_DTC_FTB_Table[1]	1
Dem_DTC_FTB_Table[2]	41
Dem_DTC_FTB_Table[3]	22
Dem_DTC_FTB_Table[4]	24
Dem_DTC_FTB_Table[5]	254
Dem_DTC_FTB_Table[6]	209
Dem_DTC_FTB_Table[7]	209
Dem_DTC_FTB_Table[8]	181
Dem_DTC_FTB_Table[9]	1
Dem_DTC_FTB_Table[10]	209
Dem_DTC_FTB_Table[11]	128
Dem_DTC_FTB_Table[12]	1
Dem_DTC_FTB_Table[13]	209
Dem_DTC_FTB_Table[14]	181
Dem_DTC_FTB_Table[15]	1
Dem_DTC_FTB_Table[16]	1
Dem_DTC_FTB_Table[17]	209
Dem_DTC_FTB_Table[18]	33
Dem_DTC_FTB_Table[19]	181
Dem_DTC_FTB_Table[20]	1
Dem_DTC_FTB_Table[21]	209
Dem_DTC_FTB_Table[22]	181
Dem_DTC_FTB_Table[23]	41
Dem_DTC_FTB_Table[24]	22
Dem_DTC_FTB_Table[25]	24
Dem_DTC_FTB_Table[26]	254
Dem_DTC_FTB_Table[27]	1
Dem_DTC_FTB_Table[28]	181
Dem_DTC_FTB_Table[29]	1
Dem_DTC_FTB_Table[30]	181
Dem_DTC_FTB_Table[31]	181
Dem_DTC_FTB_Table[32]	1
Dem_DTC_FTB_Table[33]	1
Dem_DTC_FTB_Table[34]	181
Dem_DTC_FTB_Table[35]	1
Dem_DTC_FTB_Table[36]	181
Dem_DTC_FTB_Table[37]	181
Dem_DTC_FTB_Table[38]	181
Dem_DTC_FTB_Table[39]	1
Dem_DTC_FTB_Table[40]	1
Dem_DTC_FTB_Table[41]	41
Dem_DTC_FTB_Table[42]	22

Name	Input Value
Dem_DTC_FTB_Table[43]	24
Dem_DTC_FTB_Table[44]	254
Dem_DTC_FTB_Table[45]	209
Dem_DTC_FTB_Table[46]	181
Dem_DTC_FTB_Table[47]	1
Dem_DTC_FTB_Table[48]	22
Dem_DTC_FTB_Table[49]	181
Dem_DTC_FTB_Table[50]	1
Dem_DTC_FTB_Table[51]	181
Dem_DTC_FTB_Table[52]	181
Dem_DTC_FTB_Table[53]	1
Dem_DTC_FTB_Table[54]	22
Dem_DTC_FTB_Table[55]	209
Dem_DTC_FTB_Table[56]	181
Dem_DTC_FTB_Table[57]	1
Dem_DTC_FTB_Table[58]	181
Dem_DTC_FTB_Table[59]	209
Dem_DTC_FTB_Table[60]	181
Dem_DTC_FTB_Table[61]	1
Dem_DTC_FTB_Table[62]	22
Dem_DTC_FTB_Table[63]	41
Dem_DTC_FTB_Table[64]	22
Dem_DTC_FTB_Table[65]	24
Dem_DTC_FTB_Table[66]	254
Dem_DTC_FTB_Table[67]	181
Dem_DTC_FTB_Table[68]	181
Dem_DTC_FTB_Table[69]	1
Dem_DTC_FTB_Table[70]	22
Dem_DTC_FTB_Table[71]	209
Dem_DTC_FTB_Table[72]	22
Dem_DTC_FTB_Table[73]	41
Dem_DTC_FTB_Table[74]	22
Dem_DTC_FTB_Table[75]	24
Dem_DTC_FTB_Table[76]	254

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	3405792142
DTCKind	2
DTCStatusNew	206
DTCStatusOld	84
Dem_DTCNumberTable[0]	83
Dem_DTCNumberTable[1]	99
Dem_DTCNumberTable[2]	240
Dem_DTCNumberTable[3]	233
Dem_DTCNumberTable[4]	31
Dem_DTCNumberTable[5]	75
Dem_DTCNumberTable[6]	164
Dem_DTCNumberTable[7]	164
Dem_DTCNumberTable[8]	83
Dem_DTCNumberTable[9]	99
Dem_DTCNumberTable[10]	164
Dem_DTCNumberTable[11]	40

Name	Input Value
Dem_DTCNumberTable[12]	99
Dem_DTCNumberTable[13]	164
Dem_DTCNumberTable[14]	83
Dem_DTCNumberTable[15]	99
Dem_DTCNumberTable[16]	99
Dem_DTCNumberTable[17]	164
Dem_DTCNumberTable[18]	74
Dem_DTCNumberTable[19]	83
Dem_DTCNumberTable[20]	99
Dem_DTCNumberTable[21]	164
Dem_DTCNumberTable[22]	83
Dem_DTCNumberTable[23]	240
Dem_DTCNumberTable[24]	233
Dem_DTCNumberTable[25]	31
Dem_DTCNumberTable[26]	75
Dem_DTCNumberTable[27]	99
Dem_DTCNumberTable[28]	83
Dem_DTCNumberTable[29]	99
Dem_DTCNumberTable[30]	83
Dem_DTCNumberTable[31]	83
Dem_DTCNumberTable[32]	99
Dem_DTCNumberTable[33]	99
Dem_DTCNumberTable[34]	83
Dem_DTCNumberTable[35]	99
Dem_DTCNumberTable[36]	83
Dem_DTCNumberTable[37]	83
Dem_DTCNumberTable[38]	83
Dem_DTCNumberTable[39]	99
Dem_DTCNumberTable[40]	99
Dem_DTCNumberTable[41]	240
Dem_DTCNumberTable[42]	233
Dem_DTCNumberTable[43]	31
Dem_DTCNumberTable[44]	75
Dem_DTCNumberTable[45]	164
Dem_DTCNumberTable[46]	83
Dem_DTCNumberTable[47]	99
Dem_DTCNumberTable[48]	233
Dem_DTCNumberTable[49]	83
Dem_DTCNumberTable[50]	99
Dem_DTCNumberTable[51]	83
Dem_DTCNumberTable[52]	83
Dem_DTCNumberTable[53]	99
Dem_DTCNumberTable[54]	233
Dem_DTCNumberTable[55]	164
Dem_DTCNumberTable[56]	83
Dem_DTCNumberTable[57]	99
Dem_DTCNumberTable[58]	83
Dem_DTCNumberTable[59]	164
Dem_DTCNumberTable[60]	83
Dem_DTCNumberTable[61]	99
Dem_DTCNumberTable[62]	233
Dem_DTCNumberTable[63]	240
Dem_DTCNumberTable[64]	233
Dem_DTCNumberTable[65]	31
Dem_DTCNumberTable[66]	75
Dem_DTCNumberTable[67]	83
Dem_DTCNumberTable[68]	83
Dem_DTCNumberTable[69]	99
Dem_DTCNumberTable[70]	233
Dem_DTCNumberTable[71]	164
Dem_DTCNumberTable[72]	233
Dem_DTCNumberTable[73]	240
Dem_DTCNumberTable[74]	233
Dem_DTCNumberTable[75]	31
Dem_DTCNumberTable[76]	75
Dem_DTC_FTB_Table[0]	182
Dem_DTC_FTB_Table[1]	221
Dem_DTC_FTB_Table[2]	159
Dem_DTC_FTB_Table[3]	164
Dem_DTC_FTB_Table[4]	34
Dem_DTC_FTB_Table[5]	166
Dem_DTC_FTB_Table[6]	237
Dem_DTC_FTB_Table[7]	237

Name	Input Value
Dem_DTC_FTB_Table[8]	182
Dem_DTC_FTB_Table[9]	221
Dem_DTC_FTB_Table[10]	237
Dem_DTC_FTB_Table[11]	123
Dem_DTC_FTB_Table[12]	221
Dem_DTC_FTB_Table[13]	237
Dem_DTC_FTB_Table[14]	182
Dem_DTC_FTB_Table[15]	221
Dem_DTC_FTB_Table[16]	221
Dem_DTC_FTB_Table[17]	237
Dem_DTC_FTB_Table[18]	239
Dem_DTC_FTB_Table[19]	182
Dem_DTC_FTB_Table[20]	221
Dem_DTC_FTB_Table[21]	237
Dem_DTC_FTB_Table[22]	182
Dem_DTC_FTB_Table[23]	159
Dem_DTC_FTB_Table[24]	164
Dem_DTC_FTB_Table[25]	34
Dem_DTC_FTB_Table[26]	166
Dem_DTC_FTB_Table[27]	221
Dem_DTC_FTB_Table[28]	182
Dem_DTC_FTB_Table[29]	221
Dem_DTC_FTB_Table[30]	182
Dem_DTC_FTB_Table[31]	182
Dem_DTC_FTB_Table[32]	221
Dem_DTC_FTB_Table[33]	221
Dem_DTC_FTB_Table[34]	182
Dem_DTC_FTB_Table[35]	221
Dem_DTC_FTB_Table[36]	182
Dem_DTC_FTB_Table[37]	182
Dem_DTC_FTB_Table[38]	182
Dem_DTC_FTB_Table[39]	221
Dem_DTC_FTB_Table[40]	221
Dem_DTC_FTB_Table[41]	159
Dem_DTC_FTB_Table[42]	164
Dem_DTC_FTB_Table[43]	34
Dem_DTC_FTB_Table[44]	166
Dem_DTC_FTB_Table[45]	237
Dem_DTC_FTB_Table[46]	182
Dem_DTC_FTB_Table[47]	221
Dem_DTC_FTB_Table[48]	164
Dem_DTC_FTB_Table[49]	182
Dem_DTC_FTB_Table[50]	221
Dem_DTC_FTB_Table[51]	182
Dem_DTC_FTB_Table[52]	182
Dem_DTC_FTB_Table[53]	221
Dem_DTC_FTB_Table[54]	164
Dem_DTC_FTB_Table[55]	237
Dem_DTC_FTB_Table[56]	182
Dem_DTC_FTB_Table[57]	221
Dem_DTC_FTB_Table[58]	182
Dem_DTC_FTB_Table[59]	237
Dem_DTC_FTB_Table[60]	182
Dem_DTC_FTB_Table[61]	221
Dem_DTC_FTB_Table[62]	164
Dem_DTC_FTB_Table[63]	159
Dem_DTC_FTB_Table[64]	164
Dem_DTC_FTB_Table[65]	34
Dem_DTC_FTB_Table[66]	166
Dem_DTC_FTB_Table[67]	182
Dem_DTC_FTB_Table[68]	182
Dem_DTC_FTB_Table[69]	221
Dem_DTC_FTB_Table[70]	164
Dem_DTC_FTB_Table[71]	237
Dem_DTC_FTB_Table[72]	164
Dem_DTC_FTB_Table[73]	159
Dem_DTC_FTB_Table[74]	164
Dem_DTC_FTB_Table[75]	34
Dem_DTC_FTB_Table[76]	166

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	20
DTCKind	1
DTCStatusNew	24
DTCStatusOld	0
Dem_DTCNumberTable[0]	67
Dem_DTCNumberTable[1]	177
Dem_DTCNumberTable[2]	247
Dem_DTCNumberTable[3]	156
Dem_DTCNumberTable[4]	178
Dem_DTCNumberTable[5]	171
Dem_DTCNumberTable[6]	176
Dem_DTCNumberTable[7]	176
Dem_DTCNumberTable[8]	67
Dem_DTCNumberTable[9]	177
Dem_DTCNumberTable[10]	176
Dem_DTCNumberTable[11]	116
Dem_DTCNumberTable[12]	177
Dem_DTCNumberTable[13]	176
Dem_DTCNumberTable[14]	67
Dem_DTCNumberTable[15]	177
Dem_DTCNumberTable[16]	177
Dem_DTCNumberTable[17]	176
Dem_DTCNumberTable[18]	171
Dem_DTCNumberTable[19]	67
Dem_DTCNumberTable[20]	177
Dem_DTCNumberTable[21]	176
Dem_DTCNumberTable[22]	67
Dem_DTCNumberTable[23]	247
Dem_DTCNumberTable[24]	156
Dem_DTCNumberTable[25]	178
Dem_DTCNumberTable[26]	171
Dem_DTCNumberTable[27]	177
Dem_DTCNumberTable[28]	67
Dem_DTCNumberTable[29]	177
Dem_DTCNumberTable[30]	67
Dem_DTCNumberTable[31]	67
Dem_DTCNumberTable[32]	177
Dem_DTCNumberTable[33]	177
Dem_DTCNumberTable[34]	67
Dem_DTCNumberTable[35]	177
Dem_DTCNumberTable[36]	67
Dem_DTCNumberTable[37]	67
Dem_DTCNumberTable[38]	67
Dem_DTCNumberTable[39]	177
Dem_DTCNumberTable[40]	177
Dem_DTCNumberTable[41]	247
Dem_DTCNumberTable[42]	156
Dem_DTCNumberTable[43]	178
Dem_DTCNumberTable[44]	171
Dem_DTCNumberTable[45]	176
Dem_DTCNumberTable[46]	67
Dem_DTCNumberTable[47]	177
Dem_DTCNumberTable[48]	156
Dem_DTCNumberTable[49]	67

Name	Input Value
Dem_DTCNumberTable[50]	177
Dem_DTCNumberTable[51]	67
Dem_DTCNumberTable[52]	67
Dem_DTCNumberTable[53]	177
Dem_DTCNumberTable[54]	156
Dem_DTCNumberTable[55]	176
Dem_DTCNumberTable[56]	67
Dem_DTCNumberTable[57]	177
Dem_DTCNumberTable[58]	67
Dem_DTCNumberTable[59]	176
Dem_DTCNumberTable[60]	67
Dem_DTCNumberTable[61]	177
Dem_DTCNumberTable[62]	156
Dem_DTCNumberTable[63]	247
Dem_DTCNumberTable[64]	156
Dem_DTCNumberTable[65]	178
Dem_DTCNumberTable[66]	171
Dem_DTCNumberTable[67]	67
Dem_DTCNumberTable[68]	67
Dem_DTCNumberTable[69]	177
Dem_DTCNumberTable[70]	156
Dem_DTCNumberTable[71]	176
Dem_DTCNumberTable[72]	156
Dem_DTCNumberTable[73]	247
Dem_DTCNumberTable[74]	156
Dem_DTCNumberTable[75]	178
Dem_DTCNumberTable[76]	171
Dem_DTC_FTB_Table[0]	99
Dem_DTC_FTB_Table[1]	143
Dem_DTC_FTB_Table[2]	36
Dem_DTC_FTB_Table[3]	85
Dem_DTC_FTB_Table[4]	238
Dem_DTC_FTB_Table[5]	62
Dem_DTC_FTB_Table[6]	217
Dem_DTC_FTB_Table[7]	217
Dem_DTC_FTB_Table[8]	99
Dem_DTC_FTB_Table[9]	143
Dem_DTC_FTB_Table[10]	217
Dem_DTC_FTB_Table[11]	101
Dem_DTC_FTB_Table[12]	143
Dem_DTC_FTB_Table[13]	217
Dem_DTC_FTB_Table[14]	99
Dem_DTC_FTB_Table[15]	143
Dem_DTC_FTB_Table[16]	143
Dem_DTC_FTB_Table[17]	217
Dem_DTC_FTB_Table[18]	236
Dem_DTC_FTB_Table[19]	99
Dem_DTC_FTB_Table[20]	143
Dem_DTC_FTB_Table[21]	217
Dem_DTC_FTB_Table[22]	99
Dem_DTC_FTB_Table[23]	36
Dem_DTC_FTB_Table[24]	85
Dem_DTC_FTB_Table[25]	238
Dem_DTC_FTB_Table[26]	62
Dem_DTC_FTB_Table[27]	143
Dem_DTC_FTB_Table[28]	99
Dem_DTC_FTB_Table[29]	143
Dem_DTC_FTB_Table[30]	99
Dem_DTC_FTB_Table[31]	99
Dem_DTC_FTB_Table[32]	143
Dem_DTC_FTB_Table[33]	143
Dem_DTC_FTB_Table[34]	99
Dem_DTC_FTB_Table[35]	143
Dem_DTC_FTB_Table[36]	99
Dem_DTC_FTB_Table[37]	99
Dem_DTC_FTB_Table[38]	99
Dem_DTC_FTB_Table[39]	143
Dem_DTC_FTB_Table[40]	143
Dem_DTC_FTB_Table[41]	36
Dem_DTC_FTB_Table[42]	85
Dem_DTC_FTB_Table[43]	238
Dem_DTC_FTB_Table[44]	62
Dem_DTC_FTB_Table[45]	217

Name	Input Value
Dem_DTC_FTB_Table[46]	99
Dem_DTC_FTB_Table[47]	143
Dem_DTC_FTB_Table[48]	85
Dem_DTC_FTB_Table[49]	99
Dem_DTC_FTB_Table[50]	143
Dem_DTC_FTB_Table[51]	99
Dem_DTC_FTB_Table[52]	99
Dem_DTC_FTB_Table[53]	143
Dem_DTC_FTB_Table[54]	85
Dem_DTC_FTB_Table[55]	217
Dem_DTC_FTB_Table[56]	99
Dem_DTC_FTB_Table[57]	143
Dem_DTC_FTB_Table[58]	99
Dem_DTC_FTB_Table[59]	217
Dem_DTC_FTB_Table[60]	99
Dem_DTC_FTB_Table[61]	143
Dem_DTC_FTB_Table[62]	85
Dem_DTC_FTB_Table[63]	36
Dem_DTC_FTB_Table[64]	85
Dem_DTC_FTB_Table[65]	238
Dem_DTC_FTB_Table[66]	62
Dem_DTC_FTB_Table[67]	99
Dem_DTC_FTB_Table[68]	99
Dem_DTC_FTB_Table[69]	143
Dem_DTC_FTB_Table[70]	85
Dem_DTC_FTB_Table[71]	217
Dem_DTC_FTB_Table[72]	85
Dem_DTC_FTB_Table[73]	36
Dem_DTC_FTB_Table[74]	85
Dem_DTC_FTB_Table[75]	238
Dem_DTC_FTB_Table[76]	62

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	1
CTCFailedBuf_Cnt_M_Igc[1]	1
CTCFailedBuf_Cnt_M_Igc[2]	1
CTCFailedBuf_Cnt_M_Igc[3]	1
CTCFailedBuf_Cnt_M_Igc[4]	1
CTCFailedBuf_Cnt_M_Igc[5]	1
CTCFailedBuf_Cnt_M_Igc[6]	1
CTCFailedBuf_Cnt_M_Igc[7]	1
CTCFailedBuf_Cnt_M_Igc[8]	1
CTCFailedBuf_Cnt_M_Igc[9]	1
CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	0
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	0
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	1692840925
DTCKind	1
DTCStatusNew	34
DTCStatusOld	255
Dem_DTCNumberTable[0]	89
Dem_DTCNumberTable[1]	78
Dem_DTCNumberTable[2]	204
Dem_DTCNumberTable[3]	103
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	77
Dem_DTCNumberTable[6]	228
Dem_DTCNumberTable[7]	228
Dem_DTCNumberTable[8]	89
Dem_DTCNumberTable[9]	78
Dem_DTCNumberTable[10]	228
Dem_DTCNumberTable[11]	90
Dem_DTCNumberTable[12]	78
Dem_DTCNumberTable[13]	228
Dem_DTCNumberTable[14]	89

Name	Input Value
Dem_DTCNumberTable[15]	78
Dem_DTCNumberTable[16]	78
Dem_DTCNumberTable[17]	228
Dem_DTCNumberTable[18]	228
Dem_DTCNumberTable[19]	89
Dem_DTCNumberTable[20]	78
Dem_DTCNumberTable[21]	228
Dem_DTCNumberTable[22]	89
Dem_DTCNumberTable[23]	204
Dem_DTCNumberTable[24]	103
Dem_DTCNumberTable[25]	238
Dem_DTCNumberTable[26]	77
Dem_DTCNumberTable[27]	78
Dem_DTCNumberTable[28]	89
Dem_DTCNumberTable[29]	78
Dem_DTCNumberTable[30]	89
Dem_DTCNumberTable[31]	89
Dem_DTCNumberTable[32]	78
Dem_DTCNumberTable[33]	78
Dem_DTCNumberTable[34]	89
Dem_DTCNumberTable[35]	78
Dem_DTCNumberTable[36]	89
Dem_DTCNumberTable[37]	89
Dem_DTCNumberTable[38]	89
Dem_DTCNumberTable[39]	78
Dem_DTCNumberTable[40]	78
Dem_DTCNumberTable[41]	204
Dem_DTCNumberTable[42]	103
Dem_DTCNumberTable[43]	238
Dem_DTCNumberTable[44]	77
Dem_DTCNumberTable[45]	228
Dem_DTCNumberTable[46]	89
Dem_DTCNumberTable[47]	78
Dem_DTCNumberTable[48]	103
Dem_DTCNumberTable[49]	89
Dem_DTCNumberTable[50]	78
Dem_DTCNumberTable[51]	89
Dem_DTCNumberTable[52]	89
Dem_DTCNumberTable[53]	78
Dem_DTCNumberTable[54]	103
Dem_DTCNumberTable[55]	228
Dem_DTCNumberTable[56]	89
Dem_DTCNumberTable[57]	78
Dem_DTCNumberTable[58]	89
Dem_DTCNumberTable[59]	228
Dem_DTCNumberTable[60]	89
Dem_DTCNumberTable[61]	78
Dem_DTCNumberTable[62]	103
Dem_DTCNumberTable[63]	204
Dem_DTCNumberTable[64]	103
Dem_DTCNumberTable[65]	238
Dem_DTCNumberTable[66]	77
Dem_DTCNumberTable[67]	89
Dem_DTCNumberTable[68]	89
Dem_DTCNumberTable[69]	78
Dem_DTCNumberTable[70]	103
Dem_DTCNumberTable[71]	228
Dem_DTCNumberTable[72]	103
Dem_DTCNumberTable[73]	204
Dem_DTCNumberTable[74]	103
Dem_DTCNumberTable[75]	238
Dem_DTCNumberTable[76]	77
Dem_DTC_FTB_Table[0]	31
Dem_DTC_FTB_Table[1]	227
Dem_DTC_FTB_Table[2]	66
Dem_DTC_FTB_Table[3]	96
Dem_DTC_FTB_Table[4]	130
Dem_DTC_FTB_Table[5]	24
Dem_DTC_FTB_Table[6]	240
Dem_DTC_FTB_Table[7]	240
Dem_DTC_FTB_Table[8]	31
Dem_DTC_FTB_Table[9]	227
Dem_DTC_FTB_Table[10]	240

Name	Input Value
Dem_DTC_FTB_Table[11]	151
Dem_DTC_FTB_Table[12]	227
Dem_DTC_FTB_Table[13]	240
Dem_DTC_FTB_Table[14]	31
Dem_DTC_FTB_Table[15]	227
Dem_DTC_FTB_Table[16]	227
Dem_DTC_FTB_Table[17]	240
Dem_DTC_FTB_Table[18]	241
Dem_DTC_FTB_Table[19]	31
Dem_DTC_FTB_Table[20]	227
Dem_DTC_FTB_Table[21]	240
Dem_DTC_FTB_Table[22]	31
Dem_DTC_FTB_Table[23]	66
Dem_DTC_FTB_Table[24]	96
Dem_DTC_FTB_Table[25]	130
Dem_DTC_FTB_Table[26]	24
Dem_DTC_FTB_Table[27]	227
Dem_DTC_FTB_Table[28]	31
Dem_DTC_FTB_Table[29]	227
Dem_DTC_FTB_Table[30]	31
Dem_DTC_FTB_Table[31]	31
Dem_DTC_FTB_Table[32]	227
Dem_DTC_FTB_Table[33]	227
Dem_DTC_FTB_Table[34]	31
Dem_DTC_FTB_Table[35]	227
Dem_DTC_FTB_Table[36]	31
Dem_DTC_FTB_Table[37]	31
Dem_DTC_FTB_Table[38]	31
Dem_DTC_FTB_Table[39]	227
Dem_DTC_FTB_Table[40]	227
Dem_DTC_FTB_Table[41]	66
Dem_DTC_FTB_Table[42]	96
Dem_DTC_FTB_Table[43]	130
Dem_DTC_FTB_Table[44]	24
Dem_DTC_FTB_Table[45]	240
Dem_DTC_FTB_Table[46]	31
Dem_DTC_FTB_Table[47]	227
Dem_DTC_FTB_Table[48]	96
Dem_DTC_FTB_Table[49]	31
Dem_DTC_FTB_Table[50]	227
Dem_DTC_FTB_Table[51]	31
Dem_DTC_FTB_Table[52]	31
Dem_DTC_FTB_Table[53]	227
Dem_DTC_FTB_Table[54]	96
Dem_DTC_FTB_Table[55]	240
Dem_DTC_FTB_Table[56]	31
Dem_DTC_FTB_Table[57]	227
Dem_DTC_FTB_Table[58]	31
Dem_DTC_FTB_Table[59]	240
Dem_DTC_FTB_Table[60]	31
Dem_DTC_FTB_Table[61]	227
Dem_DTC_FTB_Table[62]	96
Dem_DTC_FTB_Table[63]	66
Dem_DTC_FTB_Table[64]	96
Dem_DTC_FTB_Table[65]	130
Dem_DTC_FTB_Table[66]	24
Dem_DTC_FTB_Table[67]	31
Dem_DTC_FTB_Table[68]	31
Dem_DTC_FTB_Table[69]	227
Dem_DTC_FTB_Table[70]	96
Dem_DTC_FTB_Table[71]	240
Dem_DTC_FTB_Table[72]	96
Dem_DTC_FTB_Table[73]	66
Dem_DTC_FTB_Table[74]	96
Dem_DTC_FTB_Table[75]	130
Dem_DTC_FTB_Table[76]	24

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[6]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[7]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[8]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[9]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[10]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[11]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[12]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[13]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[14]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[15]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[16]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[17]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[18]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[19]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[20]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[21]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[22]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[23]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[24]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[25]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[26]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[27]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[28]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[29]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[30]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[37]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔

Name	Actual Value	Expected Value	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[62]	0
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	1392997139
DTCKind	2
DTCStatusNew	238
DTCStatusOld	217
Dem_DTCNumberTable[0]	170
Dem_DTCNumberTable[1]	194
Dem_DTCNumberTable[2]	13
Dem_DTCNumberTable[3]	32
Dem_DTCNumberTable[4]	172
Dem_DTCNumberTable[5]	241
Dem_DTCNumberTable[6]	91
Dem_DTCNumberTable[7]	91
Dem_DTCNumberTable[8]	170
Dem_DTCNumberTable[9]	194
Dem_DTCNumberTable[10]	91
Dem_DTCNumberTable[11]	82
Dem_DTCNumberTable[12]	194
Dem_DTCNumberTable[13]	91
Dem_DTCNumberTable[14]	170
Dem_DTCNumberTable[15]	194
Dem_DTCNumberTable[16]	194
Dem_DTCNumberTable[17]	91
Dem_DTCNumberTable[18]	55
Dem_DTCNumberTable[19]	170
Dem_DTCNumberTable[20]	194
Dem_DTCNumberTable[21]	91
Dem_DTCNumberTable[22]	170
Dem_DTCNumberTable[23]	13
Dem_DTCNumberTable[24]	32
Dem_DTCNumberTable[25]	172
Dem_DTCNumberTable[26]	241
Dem_DTCNumberTable[27]	194
Dem_DTCNumberTable[28]	170
Dem_DTCNumberTable[29]	194
Dem_DTCNumberTable[30]	170
Dem_DTCNumberTable[31]	170
Dem_DTCNumberTable[32]	194
Dem_DTCNumberTable[33]	194
Dem_DTCNumberTable[34]	170
Dem_DTCNumberTable[35]	194
Dem_DTCNumberTable[36]	170
Dem_DTCNumberTable[37]	170
Dem_DTCNumberTable[38]	170
Dem_DTCNumberTable[39]	194
Dem_DTCNumberTable[40]	194
Dem_DTCNumberTable[41]	13
Dem_DTCNumberTable[42]	32
Dem_DTCNumberTable[43]	172
Dem_DTCNumberTable[44]	241
Dem_DTCNumberTable[45]	91
Dem_DTCNumberTable[46]	170
Dem_DTCNumberTable[47]	194
Dem_DTCNumberTable[48]	32
Dem_DTCNumberTable[49]	170
Dem_DTCNumberTable[50]	194
Dem_DTCNumberTable[51]	170
Dem_DTCNumberTable[52]	170

Name	Input Value
Dem_DTCNumberTable[53]	194
Dem_DTCNumberTable[54]	32
Dem_DTCNumberTable[55]	91
Dem_DTCNumberTable[56]	170
Dem_DTCNumberTable[57]	194
Dem_DTCNumberTable[58]	170
Dem_DTCNumberTable[59]	91
Dem_DTCNumberTable[60]	170
Dem_DTCNumberTable[61]	194
Dem_DTCNumberTable[62]	32
Dem_DTCNumberTable[63]	13
Dem_DTCNumberTable[64]	32
Dem_DTCNumberTable[65]	172
Dem_DTCNumberTable[66]	241
Dem_DTCNumberTable[67]	170
Dem_DTCNumberTable[68]	170
Dem_DTCNumberTable[69]	194
Dem_DTCNumberTable[70]	32
Dem_DTCNumberTable[71]	91
Dem_DTCNumberTable[72]	32
Dem_DTCNumberTable[73]	13
Dem_DTCNumberTable[74]	32
Dem_DTCNumberTable[75]	172
Dem_DTCNumberTable[76]	241
Dem_DTC_FTB_Table[0]	83
Dem_DTC_FTB_Table[1]	99
Dem_DTC_FTB_Table[2]	240
Dem_DTC_FTB_Table[3]	233
Dem_DTC_FTB_Table[4]	31
Dem_DTC_FTB_Table[5]	75
Dem_DTC_FTB_Table[6]	164
Dem_DTC_FTB_Table[7]	164
Dem_DTC_FTB_Table[8]	83
Dem_DTC_FTB_Table[9]	99
Dem_DTC_FTB_Table[10]	164
Dem_DTC_FTB_Table[11]	40
Dem_DTC_FTB_Table[12]	99
Dem_DTC_FTB_Table[13]	164
Dem_DTC_FTB_Table[14]	83
Dem_DTC_FTB_Table[15]	99
Dem_DTC_FTB_Table[16]	99
Dem_DTC_FTB_Table[17]	164
Dem_DTC_FTB_Table[18]	74
Dem_DTC_FTB_Table[19]	83
Dem_DTC_FTB_Table[20]	99
Dem_DTC_FTB_Table[21]	164
Dem_DTC_FTB_Table[22]	83
Dem_DTC_FTB_Table[23]	240
Dem_DTC_FTB_Table[24]	233
Dem_DTC_FTB_Table[25]	31
Dem_DTC_FTB_Table[26]	75
Dem_DTC_FTB_Table[27]	99
Dem_DTC_FTB_Table[28]	83
Dem_DTC_FTB_Table[29]	99
Dem_DTC_FTB_Table[30]	83
Dem_DTC_FTB_Table[31]	83
Dem_DTC_FTB_Table[32]	99
Dem_DTC_FTB_Table[33]	99
Dem_DTC_FTB_Table[34]	83
Dem_DTC_FTB_Table[35]	99
Dem_DTC_FTB_Table[36]	83
Dem_DTC_FTB_Table[37]	83
Dem_DTC_FTB_Table[38]	83
Dem_DTC_FTB_Table[39]	99
Dem_DTC_FTB_Table[40]	99
Dem_DTC_FTB_Table[41]	240
Dem_DTC_FTB_Table[42]	233
Dem_DTC_FTB_Table[43]	31
Dem_DTC_FTB_Table[44]	75
Dem_DTC_FTB_Table[45]	164
Dem_DTC_FTB_Table[46]	83
Dem_DTC_FTB_Table[47]	99
Dem_DTC_FTB_Table[48]	233

Name	Input Value
Dem_DTC_FTB_Table[49]	83
Dem_DTC_FTB_Table[50]	99
Dem_DTC_FTB_Table[51]	83
Dem_DTC_FTB_Table[52]	83
Dem_DTC_FTB_Table[53]	99
Dem_DTC_FTB_Table[54]	233
Dem_DTC_FTB_Table[55]	164
Dem_DTC_FTB_Table[56]	83
Dem_DTC_FTB_Table[57]	99
Dem_DTC_FTB_Table[58]	83
Dem_DTC_FTB_Table[59]	164
Dem_DTC_FTB_Table[60]	83
Dem_DTC_FTB_Table[61]	99
Dem_DTC_FTB_Table[62]	233
Dem_DTC_FTB_Table[63]	240
Dem_DTC_FTB_Table[64]	233
Dem_DTC_FTB_Table[65]	31
Dem_DTC_FTB_Table[66]	75
Dem_DTC_FTB_Table[67]	83
Dem_DTC_FTB_Table[68]	83
Dem_DTC_FTB_Table[69]	99
Dem_DTC_FTB_Table[70]	233
Dem_DTC_FTB_Table[71]	164
Dem_DTC_FTB_Table[72]	233
Dem_DTC_FTB_Table[73]	240
Dem_DTC_FTB_Table[74]	233
Dem_DTC_FTB_Table[75]	31
Dem_DTC_FTB_Table[76]	75

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	1
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	983749041
DTCKind	2
DTCStatusNew	0
DTCStatusOld	240
Dem_DTCNumberTable[0]	161
Dem_DTCNumberTable[1]	211
Dem_DTCNumberTable[2]	7
Dem_DTCNumberTable[3]	239
Dem_DTCNumberTable[4]	206
Dem_DTCNumberTable[5]	70
Dem_DTCNumberTable[6]	84
Dem_DTCNumberTable[7]	84
Dem_DTCNumberTable[8]	161
Dem_DTCNumberTable[9]	211
Dem_DTCNumberTable[10]	84
Dem_DTCNumberTable[11]	193
Dem_DTCNumberTable[12]	211
Dem_DTCNumberTable[13]	84
Dem_DTCNumberTable[14]	161
Dem_DTCNumberTable[15]	211
Dem_DTCNumberTable[16]	211
Dem_DTCNumberTable[17]	84

Name	Input Value
Dem_DTCNumberTable[18]	108
Dem_DTCNumberTable[19]	161
Dem_DTCNumberTable[20]	211
Dem_DTCNumberTable[21]	84
Dem_DTCNumberTable[22]	161
Dem_DTCNumberTable[23]	7
Dem_DTCNumberTable[24]	239
Dem_DTCNumberTable[25]	206
Dem_DTCNumberTable[26]	70
Dem_DTCNumberTable[27]	211
Dem_DTCNumberTable[28]	161
Dem_DTCNumberTable[29]	211
Dem_DTCNumberTable[30]	161
Dem_DTCNumberTable[31]	161
Dem_DTCNumberTable[32]	211
Dem_DTCNumberTable[33]	211
Dem_DTCNumberTable[34]	161
Dem_DTCNumberTable[35]	211
Dem_DTCNumberTable[36]	161
Dem_DTCNumberTable[37]	161
Dem_DTCNumberTable[38]	161
Dem_DTCNumberTable[39]	211
Dem_DTCNumberTable[40]	211
Dem_DTCNumberTable[41]	7
Dem_DTCNumberTable[42]	239
Dem_DTCNumberTable[43]	206
Dem_DTCNumberTable[44]	70
Dem_DTCNumberTable[45]	84
Dem_DTCNumberTable[46]	161
Dem_DTCNumberTable[47]	211
Dem_DTCNumberTable[48]	239
Dem_DTCNumberTable[49]	161
Dem_DTCNumberTable[50]	211
Dem_DTCNumberTable[51]	161
Dem_DTCNumberTable[52]	161
Dem_DTCNumberTable[53]	211
Dem_DTCNumberTable[54]	239
Dem_DTCNumberTable[55]	84
Dem_DTCNumberTable[56]	161
Dem_DTCNumberTable[57]	211
Dem_DTCNumberTable[58]	161
Dem_DTCNumberTable[59]	84
Dem_DTCNumberTable[60]	161
Dem_DTCNumberTable[61]	211
Dem_DTCNumberTable[62]	239
Dem_DTCNumberTable[63]	7
Dem_DTCNumberTable[64]	239
Dem_DTCNumberTable[65]	206
Dem_DTCNumberTable[66]	70
Dem_DTCNumberTable[67]	161
Dem_DTCNumberTable[68]	161
Dem_DTCNumberTable[69]	211
Dem_DTCNumberTable[70]	239
Dem_DTCNumberTable[71]	84
Dem_DTCNumberTable[72]	239
Dem_DTCNumberTable[73]	7
Dem_DTCNumberTable[74]	239
Dem_DTCNumberTable[75]	206
Dem_DTCNumberTable[76]	70
Dem_DTC_FTB_Table[0]	46
Dem_DTC_FTB_Table[1]	245
Dem_DTC_FTB_Table[2]	24
Dem_DTC_FTB_Table[3]	143
Dem_DTC_FTB_Table[4]	13
Dem_DTC_FTB_Table[5]	12
Dem_DTC_FTB_Table[6]	209
Dem_DTC_FTB_Table[7]	209
Dem_DTC_FTB_Table[8]	46
Dem_DTC_FTB_Table[9]	245
Dem_DTC_FTB_Table[10]	209
Dem_DTC_FTB_Table[11]	145
Dem_DTC_FTB_Table[12]	245
Dem_DTC_FTB_Table[13]	209

Name	Input Value
Dem_DTC_FTB_Table[14]	46
Dem_DTC_FTB_Table[15]	245
Dem_DTC_FTB_Table[16]	245
Dem_DTC_FTB_Table[17]	209
Dem_DTC_FTB_Table[18]	239
Dem_DTC_FTB_Table[19]	46
Dem_DTC_FTB_Table[20]	245
Dem_DTC_FTB_Table[21]	209
Dem_DTC_FTB_Table[22]	46
Dem_DTC_FTB_Table[23]	24
Dem_DTC_FTB_Table[24]	143
Dem_DTC_FTB_Table[25]	13
Dem_DTC_FTB_Table[26]	12
Dem_DTC_FTB_Table[27]	245
Dem_DTC_FTB_Table[28]	46
Dem_DTC_FTB_Table[29]	245
Dem_DTC_FTB_Table[30]	46
Dem_DTC_FTB_Table[31]	46
Dem_DTC_FTB_Table[32]	245
Dem_DTC_FTB_Table[33]	245
Dem_DTC_FTB_Table[34]	46
Dem_DTC_FTB_Table[35]	245
Dem_DTC_FTB_Table[36]	46
Dem_DTC_FTB_Table[37]	46
Dem_DTC_FTB_Table[38]	46
Dem_DTC_FTB_Table[39]	245
Dem_DTC_FTB_Table[40]	245
Dem_DTC_FTB_Table[41]	24
Dem_DTC_FTB_Table[42]	143
Dem_DTC_FTB_Table[43]	13
Dem_DTC_FTB_Table[44]	12
Dem_DTC_FTB_Table[45]	209
Dem_DTC_FTB_Table[46]	46
Dem_DTC_FTB_Table[47]	245
Dem_DTC_FTB_Table[48]	143
Dem_DTC_FTB_Table[49]	46
Dem_DTC_FTB_Table[50]	245
Dem_DTC_FTB_Table[51]	46
Dem_DTC_FTB_Table[52]	46
Dem_DTC_FTB_Table[53]	245
Dem_DTC_FTB_Table[54]	143
Dem_DTC_FTB_Table[55]	209
Dem_DTC_FTB_Table[56]	46
Dem_DTC_FTB_Table[57]	245
Dem_DTC_FTB_Table[58]	46
Dem_DTC_FTB_Table[59]	209
Dem_DTC_FTB_Table[60]	46
Dem_DTC_FTB_Table[61]	245
Dem_DTC_FTB_Table[62]	143
Dem_DTC_FTB_Table[63]	24
Dem_DTC_FTB_Table[64]	143
Dem_DTC_FTB_Table[65]	13
Dem_DTC_FTB_Table[66]	12
Dem_DTC_FTB_Table[67]	46
Dem_DTC_FTB_Table[68]	46
Dem_DTC_FTB_Table[69]	245
Dem_DTC_FTB_Table[70]	143
Dem_DTC_FTB_Table[71]	209
Dem_DTC_FTB_Table[72]	143
Dem_DTC_FTB_Table[73]	24
Dem_DTC_FTB_Table[74]	143
Dem_DTC_FTB_Table[75]	13
Dem_DTC_FTB_Table[76]	12

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[9]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[10]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[11]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[12]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[13]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[14]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[15]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[16]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[17]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[18]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[19]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[20]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[21]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[22]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[23]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[24]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[25]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[26]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[27]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[28]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[29]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[30]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[37]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	1
CTCFailedBuf_Cnt_M_Igc[1]	1
CTCFailedBuf_Cnt_M_Igc[2]	1
CTCFailedBuf_Cnt_M_Igc[3]	1
CTCFailedBuf_Cnt_M_Igc[4]	1
CTCFailedBuf_Cnt_M_Igc[5]	1
CTCFailedBuf_Cnt_M_Igc[6]	1
CTCFailedBuf_Cnt_M_Igc[7]	1
CTCFailedBuf_Cnt_M_Igc[8]	0
CTCFailedBuf_Cnt_M_Igc[9]	1
CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	0
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	56
DTCKind	1
DTCStatusNew	255
DTCStatusOld	164
Dem_DTCNumberTable[0]	181
Dem_DTCNumberTable[1]	1
Dem_DTCNumberTable[2]	41
Dem_DTCNumberTable[3]	22
Dem_DTCNumberTable[4]	24
Dem_DTCNumberTable[5]	254
Dem_DTCNumberTable[6]	209
Dem_DTCNumberTable[7]	209
Dem_DTCNumberTable[8]	181
Dem_DTCNumberTable[9]	1
Dem_DTCNumberTable[10]	209
Dem_DTCNumberTable[11]	128
Dem_DTCNumberTable[12]	1
Dem_DTCNumberTable[13]	209
Dem_DTCNumberTable[14]	181
Dem_DTCNumberTable[15]	1
Dem_DTCNumberTable[16]	1
Dem_DTCNumberTable[17]	209
Dem_DTCNumberTable[18]	33
Dem_DTCNumberTable[19]	181
Dem_DTCNumberTable[20]	1
Dem_DTCNumberTable[21]	209
Dem_DTCNumberTable[22]	181
Dem_DTCNumberTable[23]	41
Dem_DTCNumberTable[24]	22
Dem_DTCNumberTable[25]	24
Dem_DTCNumberTable[26]	254
Dem_DTCNumberTable[27]	1
Dem_DTCNumberTable[28]	181
Dem_DTCNumberTable[29]	1
Dem_DTCNumberTable[30]	181
Dem_DTCNumberTable[31]	181
Dem_DTCNumberTable[32]	1
Dem_DTCNumberTable[33]	1
Dem_DTCNumberTable[34]	181
Dem_DTCNumberTable[35]	1
Dem_DTCNumberTable[36]	181
Dem_DTCNumberTable[37]	181
Dem_DTCNumberTable[38]	181
Dem_DTCNumberTable[39]	1
Dem_DTCNumberTable[40]	1
Dem_DTCNumberTable[41]	41
Dem_DTCNumberTable[42]	22
Dem_DTCNumberTable[43]	24
Dem_DTCNumberTable[44]	254
Dem_DTCNumberTable[45]	209
Dem_DTCNumberTable[46]	181
Dem_DTCNumberTable[47]	1
Dem_DTCNumberTable[48]	22
Dem_DTCNumberTable[49]	181
Dem_DTCNumberTable[50]	1
Dem_DTCNumberTable[51]	181
Dem_DTCNumberTable[52]	181
Dem_DTCNumberTable[53]	1
Dem_DTCNumberTable[54]	22

Name	Input Value
Dem_DTCNumberTable[55]	209
Dem_DTCNumberTable[56]	181
Dem_DTCNumberTable[57]	1
Dem_DTCNumberTable[58]	181
Dem_DTCNumberTable[59]	209
Dem_DTCNumberTable[60]	181
Dem_DTCNumberTable[61]	1
Dem_DTCNumberTable[62]	22
Dem_DTCNumberTable[63]	41
Dem_DTCNumberTable[64]	22
Dem_DTCNumberTable[65]	24
Dem_DTCNumberTable[66]	254
Dem_DTCNumberTable[67]	181
Dem_DTCNumberTable[68]	181
Dem_DTCNumberTable[69]	1
Dem_DTCNumberTable[70]	22
Dem_DTCNumberTable[71]	209
Dem_DTCNumberTable[72]	22
Dem_DTCNumberTable[73]	41
Dem_DTCNumberTable[74]	22
Dem_DTCNumberTable[75]	24
Dem_DTCNumberTable[76]	254
Dem_DTC_FTB_Table[0]	112
Dem_DTC_FTB_Table[1]	227
Dem_DTC_FTB_Table[2]	76
Dem_DTC_FTB_Table[3]	252
Dem_DTC_FTB_Table[4]	240
Dem_DTC_FTB_Table[5]	206
Dem_DTC_FTB_Table[6]	62
Dem_DTC_FTB_Table[7]	62
Dem_DTC_FTB_Table[8]	112
Dem_DTC_FTB_Table[9]	227
Dem_DTC_FTB_Table[10]	62
Dem_DTC_FTB_Table[11]	80
Dem_DTC_FTB_Table[12]	227
Dem_DTC_FTB_Table[13]	62
Dem_DTC_FTB_Table[14]	112
Dem_DTC_FTB_Table[15]	227
Dem_DTC_FTB_Table[16]	227
Dem_DTC_FTB_Table[17]	62
Dem_DTC_FTB_Table[18]	57
Dem_DTC_FTB_Table[19]	112
Dem_DTC_FTB_Table[20]	227
Dem_DTC_FTB_Table[21]	62
Dem_DTC_FTB_Table[22]	112
Dem_DTC_FTB_Table[23]	76
Dem_DTC_FTB_Table[24]	252
Dem_DTC_FTB_Table[25]	240
Dem_DTC_FTB_Table[26]	206
Dem_DTC_FTB_Table[27]	227
Dem_DTC_FTB_Table[28]	112
Dem_DTC_FTB_Table[29]	227
Dem_DTC_FTB_Table[30]	112
Dem_DTC_FTB_Table[31]	112
Dem_DTC_FTB_Table[32]	227
Dem_DTC_FTB_Table[33]	227
Dem_DTC_FTB_Table[34]	112
Dem_DTC_FTB_Table[35]	227
Dem_DTC_FTB_Table[36]	112
Dem_DTC_FTB_Table[37]	112
Dem_DTC_FTB_Table[38]	112
Dem_DTC_FTB_Table[39]	227
Dem_DTC_FTB_Table[40]	227
Dem_DTC_FTB_Table[41]	76
Dem_DTC_FTB_Table[42]	252
Dem_DTC_FTB_Table[43]	240
Dem_DTC_FTB_Table[44]	206
Dem_DTC_FTB_Table[45]	62
Dem_DTC_FTB_Table[46]	112
Dem_DTC_FTB_Table[47]	227
Dem_DTC_FTB_Table[48]	252
Dem_DTC_FTB_Table[49]	112
Dem_DTC_FTB_Table[50]	227

Name	Input Value
Dem_DTC_FTB_Table[51]	112
Dem_DTC_FTB_Table[52]	112
Dem_DTC_FTB_Table[53]	227
Dem_DTC_FTB_Table[54]	252
Dem_DTC_FTB_Table[55]	62
Dem_DTC_FTB_Table[56]	112
Dem_DTC_FTB_Table[57]	227
Dem_DTC_FTB_Table[58]	112
Dem_DTC_FTB_Table[59]	62
Dem_DTC_FTB_Table[60]	112
Dem_DTC_FTB_Table[61]	227
Dem_DTC_FTB_Table[62]	252
Dem_DTC_FTB_Table[63]	76
Dem_DTC_FTB_Table[64]	252
Dem_DTC_FTB_Table[65]	240
Dem_DTC_FTB_Table[66]	206
Dem_DTC_FTB_Table[67]	112
Dem_DTC_FTB_Table[68]	112
Dem_DTC_FTB_Table[69]	227
Dem_DTC_FTB_Table[70]	252
Dem_DTC_FTB_Table[71]	62
Dem_DTC_FTB_Table[72]	252
Dem_DTC_FTB_Table[73]	76
Dem_DTC_FTB_Table[74]	252
Dem_DTC_FTB_Table[75]	240
Dem_DTC_FTB_Table[76]	206

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	1
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	0
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	1
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	180560374
DTCKind	1
DTCStatusNew	13
DTCStatusOld	209
Dem_DTCNumberTable[0]	182
Dem_DTCNumberTable[1]	221
Dem_DTCNumberTable[2]	159
Dem_DTCNumberTable[3]	164
Dem_DTCNumberTable[4]	34
Dem_DTCNumberTable[5]	166
Dem_DTCNumberTable[6]	237
Dem_DTCNumberTable[7]	237
Dem_DTCNumberTable[8]	182
Dem_DTCNumberTable[9]	221
Dem_DTCNumberTable[10]	237
Dem_DTCNumberTable[11]	123
Dem_DTCNumberTable[12]	221
Dem_DTCNumberTable[13]	237
Dem_DTCNumberTable[14]	182
Dem_DTCNumberTable[15]	221
Dem_DTCNumberTable[16]	221
Dem_DTCNumberTable[17]	237
Dem_DTCNumberTable[18]	239
Dem_DTCNumberTable[19]	182

Name	Input Value
Dem_DTCNumberTable[20]	221
Dem_DTCNumberTable[21]	237
Dem_DTCNumberTable[22]	182
Dem_DTCNumberTable[23]	159
Dem_DTCNumberTable[24]	164
Dem_DTCNumberTable[25]	34
Dem_DTCNumberTable[26]	166
Dem_DTCNumberTable[27]	221
Dem_DTCNumberTable[28]	182
Dem_DTCNumberTable[29]	221
Dem_DTCNumberTable[30]	182
Dem_DTCNumberTable[31]	182
Dem_DTCNumberTable[32]	221
Dem_DTCNumberTable[33]	221
Dem_DTCNumberTable[34]	182
Dem_DTCNumberTable[35]	221
Dem_DTCNumberTable[36]	182
Dem_DTCNumberTable[37]	182
Dem_DTCNumberTable[38]	182
Dem_DTCNumberTable[39]	221
Dem_DTCNumberTable[40]	221
Dem_DTCNumberTable[41]	159
Dem_DTCNumberTable[42]	164
Dem_DTCNumberTable[43]	34
Dem_DTCNumberTable[44]	166
Dem_DTCNumberTable[45]	237
Dem_DTCNumberTable[46]	182
Dem_DTCNumberTable[47]	221
Dem_DTCNumberTable[48]	164
Dem_DTCNumberTable[49]	182
Dem_DTCNumberTable[50]	221
Dem_DTCNumberTable[51]	182
Dem_DTCNumberTable[52]	182
Dem_DTCNumberTable[53]	221
Dem_DTCNumberTable[54]	164
Dem_DTCNumberTable[55]	237
Dem_DTCNumberTable[56]	182
Dem_DTCNumberTable[57]	221
Dem_DTCNumberTable[58]	182
Dem_DTCNumberTable[59]	237
Dem_DTCNumberTable[60]	182
Dem_DTCNumberTable[61]	221
Dem_DTCNumberTable[62]	164
Dem_DTCNumberTable[63]	159
Dem_DTCNumberTable[64]	164
Dem_DTCNumberTable[65]	34
Dem_DTCNumberTable[66]	166
Dem_DTCNumberTable[67]	182
Dem_DTCNumberTable[68]	182
Dem_DTCNumberTable[69]	221
Dem_DTCNumberTable[70]	164
Dem_DTCNumberTable[71]	237
Dem_DTCNumberTable[72]	164
Dem_DTCNumberTable[73]	159
Dem_DTCNumberTable[74]	164
Dem_DTCNumberTable[75]	34
Dem_DTCNumberTable[76]	166
Dem_DTC_FTB_Table[0]	252
Dem_DTC_FTB_Table[1]	122
Dem_DTC_FTB_Table[2]	173
Dem_DTC_FTB_Table[3]	253
Dem_DTC_FTB_Table[4]	78
Dem_DTC_FTB_Table[5]	251
Dem_DTC_FTB_Table[6]	172
Dem_DTC_FTB_Table[7]	172
Dem_DTC_FTB_Table[8]	252
Dem_DTC_FTB_Table[9]	122
Dem_DTC_FTB_Table[10]	172
Dem_DTC_FTB_Table[11]	225
Dem_DTC_FTB_Table[12]	122
Dem_DTC_FTB_Table[13]	172
Dem_DTC_FTB_Table[14]	252
Dem_DTC_FTB_Table[15]	122

Name	Input Value
Dem_DTC_FTB_Table[16]	122
Dem_DTC_FTB_Table[17]	172
Dem_DTC_FTB_Table[18]	117
Dem_DTC_FTB_Table[19]	252
Dem_DTC_FTB_Table[20]	122
Dem_DTC_FTB_Table[21]	172
Dem_DTC_FTB_Table[22]	252
Dem_DTC_FTB_Table[23]	173
Dem_DTC_FTB_Table[24]	253
Dem_DTC_FTB_Table[25]	78
Dem_DTC_FTB_Table[26]	251
Dem_DTC_FTB_Table[27]	122
Dem_DTC_FTB_Table[28]	252
Dem_DTC_FTB_Table[29]	122
Dem_DTC_FTB_Table[30]	252
Dem_DTC_FTB_Table[31]	252
Dem_DTC_FTB_Table[32]	122
Dem_DTC_FTB_Table[33]	122
Dem_DTC_FTB_Table[34]	252
Dem_DTC_FTB_Table[35]	122
Dem_DTC_FTB_Table[36]	252
Dem_DTC_FTB_Table[37]	252
Dem_DTC_FTB_Table[38]	252
Dem_DTC_FTB_Table[39]	122
Dem_DTC_FTB_Table[40]	122
Dem_DTC_FTB_Table[41]	173
Dem_DTC_FTB_Table[42]	253
Dem_DTC_FTB_Table[43]	78
Dem_DTC_FTB_Table[44]	251
Dem_DTC_FTB_Table[45]	172
Dem_DTC_FTB_Table[46]	252
Dem_DTC_FTB_Table[47]	122
Dem_DTC_FTB_Table[48]	253
Dem_DTC_FTB_Table[49]	252
Dem_DTC_FTB_Table[50]	122
Dem_DTC_FTB_Table[51]	252
Dem_DTC_FTB_Table[52]	252
Dem_DTC_FTB_Table[53]	122
Dem_DTC_FTB_Table[54]	253
Dem_DTC_FTB_Table[55]	172
Dem_DTC_FTB_Table[56]	252
Dem_DTC_FTB_Table[57]	122
Dem_DTC_FTB_Table[58]	252
Dem_DTC_FTB_Table[59]	172
Dem_DTC_FTB_Table[60]	252
Dem_DTC_FTB_Table[61]	122
Dem_DTC_FTB_Table[62]	253
Dem_DTC_FTB_Table[63]	173
Dem_DTC_FTB_Table[64]	253
Dem_DTC_FTB_Table[65]	78
Dem_DTC_FTB_Table[66]	251
Dem_DTC_FTB_Table[67]	252
Dem_DTC_FTB_Table[68]	252
Dem_DTC_FTB_Table[69]	122
Dem_DTC_FTB_Table[70]	253
Dem_DTC_FTB_Table[71]	172
Dem_DTC_FTB_Table[72]	253
Dem_DTC_FTB_Table[73]	173
Dem_DTC_FTB_Table[74]	253
Dem_DTC_FTB_Table[75]	78
Dem_DTC_FTB_Table[76]	251

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	0
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	0
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_lgc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32]	0
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61]	0
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	0
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	2534667367
DTCKind	2
DTCStatusNew	240
DTCStatusOld	62
Dem_DTCNumberTable[0]	99
Dem_DTCNumberTable[1]	143
Dem_DTCNumberTable[2]	36
Dem_DTCNumberTable[3]	85
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	62
Dem_DTCNumberTable[6]	217
Dem_DTCNumberTable[7]	217
Dem_DTCNumberTable[8]	99
Dem_DTCNumberTable[9]	143
Dem_DTCNumberTable[10]	217
Dem_DTCNumberTable[11]	101
Dem_DTCNumberTable[12]	143
Dem_DTCNumberTable[13]	217
Dem_DTCNumberTable[14]	99
Dem_DTCNumberTable[15]	143
Dem_DTCNumberTable[16]	143
Dem_DTCNumberTable[17]	217
Dem_DTCNumberTable[18]	236
Dem_DTCNumberTable[19]	99
Dem_DTCNumberTable[20]	143
Dem_DTCNumberTable[21]	217
Dem_DTCNumberTable[22]	99
Dem_DTCNumberTable[23]	36
Dem_DTCNumberTable[24]	85
Dem_DTCNumberTable[25]	238
Dem_DTCNumberTable[26]	62
Dem_DTCNumberTable[27]	143
Dem_DTCNumberTable[28]	99
Dem_DTCNumberTable[29]	143
Dem_DTCNumberTable[30]	99
Dem_DTCNumberTable[31]	99
Dem_DTCNumberTable[32]	143
Dem_DTCNumberTable[33]	143
Dem_DTCNumberTable[34]	99
Dem_DTCNumberTable[35]	143
Dem_DTCNumberTable[36]	99
Dem_DTCNumberTable[37]	99
Dem_DTCNumberTable[38]	99
Dem_DTCNumberTable[39]	143
Dem_DTCNumberTable[40]	143
Dem_DTCNumberTable[41]	36
Dem_DTCNumberTable[42]	85
Dem_DTCNumberTable[43]	238
Dem_DTCNumberTable[44]	62
Dem_DTCNumberTable[45]	217
Dem_DTCNumberTable[46]	99
Dem_DTCNumberTable[47]	143
Dem_DTCNumberTable[48]	85
Dem_DTCNumberTable[49]	99
Dem_DTCNumberTable[50]	143
Dem_DTCNumberTable[51]	99
Dem_DTCNumberTable[52]	99
Dem_DTCNumberTable[53]	143
Dem_DTCNumberTable[54]	85

Name	Input Value
Dem_DTCNumberTable[55]	217
Dem_DTCNumberTable[56]	99
Dem_DTCNumberTable[57]	143
Dem_DTCNumberTable[58]	99
Dem_DTCNumberTable[59]	217
Dem_DTCNumberTable[60]	99
Dem_DTCNumberTable[61]	143
Dem_DTCNumberTable[62]	85
Dem_DTCNumberTable[63]	36
Dem_DTCNumberTable[64]	85
Dem_DTCNumberTable[65]	238
Dem_DTCNumberTable[66]	62
Dem_DTCNumberTable[67]	99
Dem_DTCNumberTable[68]	99
Dem_DTCNumberTable[69]	143
Dem_DTCNumberTable[70]	85
Dem_DTCNumberTable[71]	217
Dem_DTCNumberTable[72]	85
Dem_DTCNumberTable[73]	36
Dem_DTCNumberTable[74]	85
Dem_DTCNumberTable[75]	238
Dem_DTCNumberTable[76]	62
Dem_DTC_FTB_Table[0]	67
Dem_DTC_FTB_Table[1]	177
Dem_DTC_FTB_Table[2]	247
Dem_DTC_FTB_Table[3]	156
Dem_DTC_FTB_Table[4]	178
Dem_DTC_FTB_Table[5]	171
Dem_DTC_FTB_Table[6]	176
Dem_DTC_FTB_Table[7]	176
Dem_DTC_FTB_Table[8]	67
Dem_DTC_FTB_Table[9]	177
Dem_DTC_FTB_Table[10]	176
Dem_DTC_FTB_Table[11]	116
Dem_DTC_FTB_Table[12]	177
Dem_DTC_FTB_Table[13]	176
Dem_DTC_FTB_Table[14]	67
Dem_DTC_FTB_Table[15]	177
Dem_DTC_FTB_Table[16]	177
Dem_DTC_FTB_Table[17]	176
Dem_DTC_FTB_Table[18]	171
Dem_DTC_FTB_Table[19]	67
Dem_DTC_FTB_Table[20]	177
Dem_DTC_FTB_Table[21]	176
Dem_DTC_FTB_Table[22]	67
Dem_DTC_FTB_Table[23]	247
Dem_DTC_FTB_Table[24]	156
Dem_DTC_FTB_Table[25]	178
Dem_DTC_FTB_Table[26]	171
Dem_DTC_FTB_Table[27]	177
Dem_DTC_FTB_Table[28]	67
Dem_DTC_FTB_Table[29]	177
Dem_DTC_FTB_Table[30]	67
Dem_DTC_FTB_Table[31]	67
Dem_DTC_FTB_Table[32]	177
Dem_DTC_FTB_Table[33]	177
Dem_DTC_FTB_Table[34]	67
Dem_DTC_FTB_Table[35]	177
Dem_DTC_FTB_Table[36]	67
Dem_DTC_FTB_Table[37]	67
Dem_DTC_FTB_Table[38]	67
Dem_DTC_FTB_Table[39]	177
Dem_DTC_FTB_Table[40]	177
Dem_DTC_FTB_Table[41]	247
Dem_DTC_FTB_Table[42]	156
Dem_DTC_FTB_Table[43]	178
Dem_DTC_FTB_Table[44]	171
Dem_DTC_FTB_Table[45]	176
Dem_DTC_FTB_Table[46]	67
Dem_DTC_FTB_Table[47]	177
Dem_DTC_FTB_Table[48]	156
Dem_DTC_FTB_Table[49]	67
Dem_DTC_FTB_Table[50]	177

Name	Input Value
Dem_DTC_FTB_Table[51]	67
Dem_DTC_FTB_Table[52]	67
Dem_DTC_FTB_Table[53]	177
Dem_DTC_FTB_Table[54]	156
Dem_DTC_FTB_Table[55]	176
Dem_DTC_FTB_Table[56]	67
Dem_DTC_FTB_Table[57]	177
Dem_DTC_FTB_Table[58]	67
Dem_DTC_FTB_Table[59]	176
Dem_DTC_FTB_Table[60]	67
Dem_DTC_FTB_Table[61]	177
Dem_DTC_FTB_Table[62]	156
Dem_DTC_FTB_Table[63]	247
Dem_DTC_FTB_Table[64]	156
Dem_DTC_FTB_Table[65]	178
Dem_DTC_FTB_Table[66]	171
Dem_DTC_FTB_Table[67]	67
Dem_DTC_FTB_Table[68]	67
Dem_DTC_FTB_Table[69]	177
Dem_DTC_FTB_Table[70]	156
Dem_DTC_FTB_Table[71]	176
Dem_DTC_FTB_Table[72]	156
Dem_DTC_FTB_Table[73]	247
Dem_DTC_FTB_Table[74]	156
Dem_DTC_FTB_Table[75]	178
Dem_DTC_FTB_Table[76]	171

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[10]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[14]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[17]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[24]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[29]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[32]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[33]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[54]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[55]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[56]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[57]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[58]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[59]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[60]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[61]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[62]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[63]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[64]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	1
CTCFailedBuf_Cnt_M_Igc[1]	1
CTCFailedBuf_Cnt_M_Igc[2]	1
CTCFailedBuf_Cnt_M_Igc[3]	1
CTCFailedBuf_Cnt_M_Igc[4]	1
CTCFailedBuf_Cnt_M_Igc[5]	1
CTCFailedBuf_Cnt_M_Igc[6]	1
CTCFailedBuf_Cnt_M_Igc[7]	1
CTCFailedBuf_Cnt_M_Igc[8]	1
CTCFailedBuf_Cnt_M_Igc[9]	1
CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	1
CTCFailedBuf_Cnt_M_Igc[21]	1
CTCFailedBuf_Cnt_M_Igc[22]	1
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	1
CTCFailedBuf_Cnt_M_Igc[35]	1
CTCFailedBuf_Cnt_M_Igc[36]	1
CTCFailedBuf_Cnt_M_Igc[37]	1
CTCFailedBuf_Cnt_M_Igc[38]	1
CTCFailedBuf_Cnt_M_Igc[39]	1
CTCFailedBuf_Cnt_M_Igc[40]	1
CTCFailedBuf_Cnt_M_Igc[41]	1
CTCFailedBuf_Cnt_M_Igc[42]	1
CTCFailedBuf_Cnt_M_Igc[43]	1
CTCFailedBuf_Cnt_M_Igc[44]	1
CTCFailedBuf_Cnt_M_Igc[45]	1
CTCFailedBuf_Cnt_M_Igc[46]	1
CTCFailedBuf_Cnt_M_Igc[47]	1
CTCFailedBuf_Cnt_M_Igc[48]	1
CTCFailedBuf_Cnt_M_Igc[49]	1
CTCFailedBuf_Cnt_M_Igc[50]	1
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_Igc[52]	1
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	1
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	1
CTCFailedBuf_Cnt_M_Igc[69]	1
CTCFailedBuf_Cnt_M_Igc[70]	1
CTCFailedBuf_Cnt_M_Igc[71]	1
CTCFailedBuf_Cnt_M_Igc[72]	1
CTCFailedBuf_Cnt_M_Igc[73]	1
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	1
CTCFailedBuf_Cnt_M_Igc[76]	1
CTCFailed_Cnt_M_Igc	0
DTC	3261627242
DTCKind	1
DTCStatusNew	78
DTCStatusOld	172
Dem_DTCNumberTable[0]	31
Dem_DTCNumberTable[1]	227
Dem_DTCNumberTable[2]	66
Dem_DTCNumberTable[3]	96
Dem_DTCNumberTable[4]	130
Dem_DTCNumberTable[5]	24
Dem_DTCNumberTable[6]	240
Dem_DTCNumberTable[7]	240
Dem_DTCNumberTable[8]	31
Dem_DTCNumberTable[9]	227
Dem_DTCNumberTable[10]	240
Dem_DTCNumberTable[11]	151
Dem_DTCNumberTable[12]	227
Dem_DTCNumberTable[13]	240
Dem_DTCNumberTable[14]	31
Dem_DTCNumberTable[15]	227
Dem_DTCNumberTable[16]	227
Dem_DTCNumberTable[17]	240
Dem_DTCNumberTable[18]	241
Dem_DTCNumberTable[19]	31

Name	Input Value
Dem_DTCNumberTable[20]	227
Dem_DTCNumberTable[21]	240
Dem_DTCNumberTable[22]	31
Dem_DTCNumberTable[23]	66
Dem_DTCNumberTable[24]	96
Dem_DTCNumberTable[25]	130
Dem_DTCNumberTable[26]	24
Dem_DTCNumberTable[27]	227
Dem_DTCNumberTable[28]	31
Dem_DTCNumberTable[29]	227
Dem_DTCNumberTable[30]	31
Dem_DTCNumberTable[31]	31
Dem_DTCNumberTable[32]	227
Dem_DTCNumberTable[33]	227
Dem_DTCNumberTable[34]	31
Dem_DTCNumberTable[35]	227
Dem_DTCNumberTable[36]	31
Dem_DTCNumberTable[37]	31
Dem_DTCNumberTable[38]	31
Dem_DTCNumberTable[39]	227
Dem_DTCNumberTable[40]	227
Dem_DTCNumberTable[41]	66
Dem_DTCNumberTable[42]	96
Dem_DTCNumberTable[43]	130
Dem_DTCNumberTable[44]	24
Dem_DTCNumberTable[45]	240
Dem_DTCNumberTable[46]	31
Dem_DTCNumberTable[47]	227
Dem_DTCNumberTable[48]	96
Dem_DTCNumberTable[49]	31
Dem_DTCNumberTable[50]	227
Dem_DTCNumberTable[51]	31
Dem_DTCNumberTable[52]	31
Dem_DTCNumberTable[53]	227
Dem_DTCNumberTable[54]	96
Dem_DTCNumberTable[55]	240
Dem_DTCNumberTable[56]	31
Dem_DTCNumberTable[57]	227
Dem_DTCNumberTable[58]	31
Dem_DTCNumberTable[59]	240
Dem_DTCNumberTable[60]	31
Dem_DTCNumberTable[61]	227
Dem_DTCNumberTable[62]	96
Dem_DTCNumberTable[63]	66
Dem_DTCNumberTable[64]	96
Dem_DTCNumberTable[65]	130
Dem_DTCNumberTable[66]	24
Dem_DTCNumberTable[67]	31
Dem_DTCNumberTable[68]	31
Dem_DTCNumberTable[69]	227
Dem_DTCNumberTable[70]	96
Dem_DTCNumberTable[71]	240
Dem_DTCNumberTable[72]	96
Dem_DTCNumberTable[73]	66
Dem_DTCNumberTable[74]	96
Dem_DTCNumberTable[75]	130
Dem_DTCNumberTable[76]	24
Dem_DTC_FTB_Table[0]	89
Dem_DTC_FTB_Table[1]	78
Dem_DTC_FTB_Table[2]	204
Dem_DTC_FTB_Table[3]	103
Dem_DTC_FTB_Table[4]	238
Dem_DTC_FTB_Table[5]	77
Dem_DTC_FTB_Table[6]	228
Dem_DTC_FTB_Table[7]	228
Dem_DTC_FTB_Table[8]	89
Dem_DTC_FTB_Table[9]	78
Dem_DTC_FTB_Table[10]	228
Dem_DTC_FTB_Table[11]	90
Dem_DTC_FTB_Table[12]	78
Dem_DTC_FTB_Table[13]	228
Dem_DTC_FTB_Table[14]	89
Dem_DTC_FTB_Table[15]	78

Name	Input Value
Dem_DTC_FTB_Table[16]	78
Dem_DTC_FTB_Table[17]	228
Dem_DTC_FTB_Table[18]	228
Dem_DTC_FTB_Table[19]	89
Dem_DTC_FTB_Table[20]	78
Dem_DTC_FTB_Table[21]	228
Dem_DTC_FTB_Table[22]	89
Dem_DTC_FTB_Table[23]	204
Dem_DTC_FTB_Table[24]	103
Dem_DTC_FTB_Table[25]	238
Dem_DTC_FTB_Table[26]	77
Dem_DTC_FTB_Table[27]	78
Dem_DTC_FTB_Table[28]	89
Dem_DTC_FTB_Table[29]	78
Dem_DTC_FTB_Table[30]	89
Dem_DTC_FTB_Table[31]	89
Dem_DTC_FTB_Table[32]	78
Dem_DTC_FTB_Table[33]	78
Dem_DTC_FTB_Table[34]	89
Dem_DTC_FTB_Table[35]	78
Dem_DTC_FTB_Table[36]	89
Dem_DTC_FTB_Table[37]	89
Dem_DTC_FTB_Table[38]	89
Dem_DTC_FTB_Table[39]	78
Dem_DTC_FTB_Table[40]	78
Dem_DTC_FTB_Table[41]	204
Dem_DTC_FTB_Table[42]	103
Dem_DTC_FTB_Table[43]	238
Dem_DTC_FTB_Table[44]	77
Dem_DTC_FTB_Table[45]	228
Dem_DTC_FTB_Table[46]	89
Dem_DTC_FTB_Table[47]	78
Dem_DTC_FTB_Table[48]	103
Dem_DTC_FTB_Table[49]	89
Dem_DTC_FTB_Table[50]	78
Dem_DTC_FTB_Table[51]	89
Dem_DTC_FTB_Table[52]	89
Dem_DTC_FTB_Table[53]	78
Dem_DTC_FTB_Table[54]	103
Dem_DTC_FTB_Table[55]	228
Dem_DTC_FTB_Table[56]	89
Dem_DTC_FTB_Table[57]	78
Dem_DTC_FTB_Table[58]	89
Dem_DTC_FTB_Table[59]	228
Dem_DTC_FTB_Table[60]	89
Dem_DTC_FTB_Table[61]	78
Dem_DTC_FTB_Table[62]	103
Dem_DTC_FTB_Table[63]	204
Dem_DTC_FTB_Table[64]	103
Dem_DTC_FTB_Table[65]	238
Dem_DTC_FTB_Table[66]	77
Dem_DTC_FTB_Table[67]	89
Dem_DTC_FTB_Table[68]	89
Dem_DTC_FTB_Table[69]	78
Dem_DTC_FTB_Table[70]	103
Dem_DTC_FTB_Table[71]	228
Dem_DTC_FTB_Table[72]	103
Dem_DTC_FTB_Table[73]	204
Dem_DTC_FTB_Table[74]	103
Dem_DTC_FTB_Table[75]	238
Dem_DTC_FTB_Table[76]	77

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[12]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[13]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[14]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[15]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[16]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[17]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[18]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[19]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[20]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[21]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[22]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[23]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[24]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[25]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[26]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[27]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[28]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[29]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[30]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[35]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[36]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[37]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[38]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[39]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[40]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[41]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[42]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[43]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[44]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[45]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[46]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[47]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[48]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[49]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[50]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[51]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[52]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[66]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[67]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[68]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[69]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[70]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[71]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[72]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[73]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[75]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[76]	1	1	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	4231674622
DTCKind	2
DTCStatusNew	178
DTCStatusOld	176
Dem_DTCNumberTable[0]	83
Dem_DTCNumberTable[1]	99
Dem_DTCNumberTable[2]	240
Dem_DTCNumberTable[3]	233
Dem_DTCNumberTable[4]	31
Dem_DTCNumberTable[5]	75
Dem_DTCNumberTable[6]	164
Dem_DTCNumberTable[7]	164
Dem_DTCNumberTable[8]	83
Dem_DTCNumberTable[9]	99
Dem_DTCNumberTable[10]	164
Dem_DTCNumberTable[11]	40
Dem_DTCNumberTable[12]	99
Dem_DTCNumberTable[13]	164
Dem_DTCNumberTable[14]	83
Dem_DTCNumberTable[15]	99
Dem_DTCNumberTable[16]	99
Dem_DTCNumberTable[17]	164
Dem_DTCNumberTable[18]	74
Dem_DTCNumberTable[19]	83
Dem_DTCNumberTable[20]	99
Dem_DTCNumberTable[21]	164
Dem_DTCNumberTable[22]	83
Dem_DTCNumberTable[23]	240
Dem_DTCNumberTable[24]	233
Dem_DTCNumberTable[25]	31
Dem_DTCNumberTable[26]	75
Dem_DTCNumberTable[27]	99
Dem_DTCNumberTable[28]	83
Dem_DTCNumberTable[29]	99
Dem_DTCNumberTable[30]	83
Dem_DTCNumberTable[31]	83
Dem_DTCNumberTable[32]	99
Dem_DTCNumberTable[33]	99
Dem_DTCNumberTable[34]	83
Dem_DTCNumberTable[35]	99
Dem_DTCNumberTable[36]	83
Dem_DTCNumberTable[37]	83
Dem_DTCNumberTable[38]	83
Dem_DTCNumberTable[39]	99
Dem_DTCNumberTable[40]	99
Dem_DTCNumberTable[41]	240
Dem_DTCNumberTable[42]	233
Dem_DTCNumberTable[43]	31
Dem_DTCNumberTable[44]	75
Dem_DTCNumberTable[45]	164
Dem_DTCNumberTable[46]	83
Dem_DTCNumberTable[47]	99
Dem_DTCNumberTable[48]	233
Dem_DTCNumberTable[49]	83
Dem_DTCNumberTable[50]	99
Dem_DTCNumberTable[51]	83
Dem_DTCNumberTable[52]	83
Dem_DTCNumberTable[53]	99
Dem_DTCNumberTable[54]	233

Name	Input Value
Dem_DTCNumberTable[55]	164
Dem_DTCNumberTable[56]	83
Dem_DTCNumberTable[57]	99
Dem_DTCNumberTable[58]	83
Dem_DTCNumberTable[59]	164
Dem_DTCNumberTable[60]	83
Dem_DTCNumberTable[61]	99
Dem_DTCNumberTable[62]	233
Dem_DTCNumberTable[63]	240
Dem_DTCNumberTable[64]	233
Dem_DTCNumberTable[65]	31
Dem_DTCNumberTable[66]	75
Dem_DTCNumberTable[67]	83
Dem_DTCNumberTable[68]	83
Dem_DTCNumberTable[69]	99
Dem_DTCNumberTable[70]	233
Dem_DTCNumberTable[71]	164
Dem_DTCNumberTable[72]	233
Dem_DTCNumberTable[73]	240
Dem_DTCNumberTable[74]	233
Dem_DTCNumberTable[75]	31
Dem_DTCNumberTable[76]	75
Dem_DTC_FTB_Table[0]	170
Dem_DTC_FTB_Table[1]	194
Dem_DTC_FTB_Table[2]	13
Dem_DTC_FTB_Table[3]	32
Dem_DTC_FTB_Table[4]	172
Dem_DTC_FTB_Table[5]	241
Dem_DTC_FTB_Table[6]	91
Dem_DTC_FTB_Table[7]	91
Dem_DTC_FTB_Table[8]	170
Dem_DTC_FTB_Table[9]	194
Dem_DTC_FTB_Table[10]	91
Dem_DTC_FTB_Table[11]	82
Dem_DTC_FTB_Table[12]	194
Dem_DTC_FTB_Table[13]	91
Dem_DTC_FTB_Table[14]	170
Dem_DTC_FTB_Table[15]	194
Dem_DTC_FTB_Table[16]	194
Dem_DTC_FTB_Table[17]	91
Dem_DTC_FTB_Table[18]	55
Dem_DTC_FTB_Table[19]	170
Dem_DTC_FTB_Table[20]	194
Dem_DTC_FTB_Table[21]	91
Dem_DTC_FTB_Table[22]	170
Dem_DTC_FTB_Table[23]	13
Dem_DTC_FTB_Table[24]	32
Dem_DTC_FTB_Table[25]	172
Dem_DTC_FTB_Table[26]	241
Dem_DTC_FTB_Table[27]	194
Dem_DTC_FTB_Table[28]	170
Dem_DTC_FTB_Table[29]	194
Dem_DTC_FTB_Table[30]	170
Dem_DTC_FTB_Table[31]	170
Dem_DTC_FTB_Table[32]	194
Dem_DTC_FTB_Table[33]	194
Dem_DTC_FTB_Table[34]	170
Dem_DTC_FTB_Table[35]	194
Dem_DTC_FTB_Table[36]	170
Dem_DTC_FTB_Table[37]	170
Dem_DTC_FTB_Table[38]	170
Dem_DTC_FTB_Table[39]	194
Dem_DTC_FTB_Table[40]	194
Dem_DTC_FTB_Table[41]	13
Dem_DTC_FTB_Table[42]	32
Dem_DTC_FTB_Table[43]	172
Dem_DTC_FTB_Table[44]	241
Dem_DTC_FTB_Table[45]	91
Dem_DTC_FTB_Table[46]	170
Dem_DTC_FTB_Table[47]	194
Dem_DTC_FTB_Table[48]	32
Dem_DTC_FTB_Table[49]	170
Dem_DTC_FTB_Table[50]	194

Name	Input Value
Dem_DTC_FTB_Table[51]	170
Dem_DTC_FTB_Table[52]	170
Dem_DTC_FTB_Table[53]	194
Dem_DTC_FTB_Table[54]	32
Dem_DTC_FTB_Table[55]	91
Dem_DTC_FTB_Table[56]	170
Dem_DTC_FTB_Table[57]	194
Dem_DTC_FTB_Table[58]	170
Dem_DTC_FTB_Table[59]	91
Dem_DTC_FTB_Table[60]	170
Dem_DTC_FTB_Table[61]	194
Dem_DTC_FTB_Table[62]	32
Dem_DTC_FTB_Table[63]	13
Dem_DTC_FTB_Table[64]	32
Dem_DTC_FTB_Table[65]	172
Dem_DTC_FTB_Table[66]	241
Dem_DTC_FTB_Table[67]	170
Dem_DTC_FTB_Table[68]	170
Dem_DTC_FTB_Table[69]	194
Dem_DTC_FTB_Table[70]	32
Dem_DTC_FTB_Table[71]	91
Dem_DTC_FTB_Table[72]	32
Dem_DTC_FTB_Table[73]	13
Dem_DTC_FTB_Table[74]	32
Dem_DTC_FTB_Table[75]	172
Dem_DTC_FTB_Table[76]	241

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	1673189688
DTCKind	1
DTCStatusNew	238
DTCStatusOld	228
Dem_DTCNumberTable[0]	46
Dem_DTCNumberTable[1]	245
Dem_DTCNumberTable[2]	24
Dem_DTCNumberTable[3]	143
Dem_DTCNumberTable[4]	13
Dem_DTCNumberTable[5]	12
Dem_DTCNumberTable[6]	209
Dem_DTCNumberTable[7]	209
Dem_DTCNumberTable[8]	46
Dem_DTCNumberTable[9]	245
Dem_DTCNumberTable[10]	209
Dem_DTCNumberTable[11]	145
Dem_DTCNumberTable[12]	245
Dem_DTCNumberTable[13]	209
Dem_DTCNumberTable[14]	46
Dem_DTCNumberTable[15]	245
Dem_DTCNumberTable[16]	245
Dem_DTCNumberTable[17]	209
Dem_DTCNumberTable[18]	239
Dem_DTCNumberTable[19]	46

Name	Input Value
Dem_DTCNumberTable[20]	245
Dem_DTCNumberTable[21]	209
Dem_DTCNumberTable[22]	46
Dem_DTCNumberTable[23]	24
Dem_DTCNumberTable[24]	143
Dem_DTCNumberTable[25]	13
Dem_DTCNumberTable[26]	12
Dem_DTCNumberTable[27]	245
Dem_DTCNumberTable[28]	46
Dem_DTCNumberTable[29]	245
Dem_DTCNumberTable[30]	46
Dem_DTCNumberTable[31]	46
Dem_DTCNumberTable[32]	245
Dem_DTCNumberTable[33]	245
Dem_DTCNumberTable[34]	46
Dem_DTCNumberTable[35]	245
Dem_DTCNumberTable[36]	46
Dem_DTCNumberTable[37]	46
Dem_DTCNumberTable[38]	46
Dem_DTCNumberTable[39]	245
Dem_DTCNumberTable[40]	245
Dem_DTCNumberTable[41]	24
Dem_DTCNumberTable[42]	143
Dem_DTCNumberTable[43]	13
Dem_DTCNumberTable[44]	12
Dem_DTCNumberTable[45]	209
Dem_DTCNumberTable[46]	46
Dem_DTCNumberTable[47]	245
Dem_DTCNumberTable[48]	143
Dem_DTCNumberTable[49]	46
Dem_DTCNumberTable[50]	245
Dem_DTCNumberTable[51]	46
Dem_DTCNumberTable[52]	46
Dem_DTCNumberTable[53]	245
Dem_DTCNumberTable[54]	143
Dem_DTCNumberTable[55]	209
Dem_DTCNumberTable[56]	46
Dem_DTCNumberTable[57]	245
Dem_DTCNumberTable[58]	46
Dem_DTCNumberTable[59]	209
Dem_DTCNumberTable[60]	46
Dem_DTCNumberTable[61]	245
Dem_DTCNumberTable[62]	143
Dem_DTCNumberTable[63]	24
Dem_DTCNumberTable[64]	143
Dem_DTCNumberTable[65]	13
Dem_DTCNumberTable[66]	12
Dem_DTCNumberTable[67]	46
Dem_DTCNumberTable[68]	46
Dem_DTCNumberTable[69]	245
Dem_DTCNumberTable[70]	143
Dem_DTCNumberTable[71]	209
Dem_DTCNumberTable[72]	143
Dem_DTCNumberTable[73]	24
Dem_DTCNumberTable[74]	143
Dem_DTCNumberTable[75]	13
Dem_DTCNumberTable[76]	12
Dem_DTC_FTB_Table[0]	107
Dem_DTC_FTB_Table[1]	156
Dem_DTC_FTB_Table[2]	5
Dem_DTC_FTB_Table[3]	166
Dem_DTC_FTB_Table[4]	182
Dem_DTC_FTB_Table[5]	118
Dem_DTC_FTB_Table[6]	237
Dem_DTC_FTB_Table[7]	237
Dem_DTC_FTB_Table[8]	107
Dem_DTC_FTB_Table[9]	156
Dem_DTC_FTB_Table[10]	237
Dem_DTC_FTB_Table[11]	66
Dem_DTC_FTB_Table[12]	156
Dem_DTC_FTB_Table[13]	237
Dem_DTC_FTB_Table[14]	107
Dem_DTC_FTB_Table[15]	156

Name	Input Value
Dem_DTC_FTB_Table[16]	156
Dem_DTC_FTB_Table[17]	237
Dem_DTC_FTB_Table[18]	106
Dem_DTC_FTB_Table[19]	107
Dem_DTC_FTB_Table[20]	156
Dem_DTC_FTB_Table[21]	237
Dem_DTC_FTB_Table[22]	107
Dem_DTC_FTB_Table[23]	5
Dem_DTC_FTB_Table[24]	166
Dem_DTC_FTB_Table[25]	182
Dem_DTC_FTB_Table[26]	118
Dem_DTC_FTB_Table[27]	156
Dem_DTC_FTB_Table[28]	107
Dem_DTC_FTB_Table[29]	156
Dem_DTC_FTB_Table[30]	107
Dem_DTC_FTB_Table[31]	107
Dem_DTC_FTB_Table[32]	156
Dem_DTC_FTB_Table[33]	156
Dem_DTC_FTB_Table[34]	107
Dem_DTC_FTB_Table[35]	156
Dem_DTC_FTB_Table[36]	107
Dem_DTC_FTB_Table[37]	107
Dem_DTC_FTB_Table[38]	107
Dem_DTC_FTB_Table[39]	156
Dem_DTC_FTB_Table[40]	156
Dem_DTC_FTB_Table[41]	5
Dem_DTC_FTB_Table[42]	166
Dem_DTC_FTB_Table[43]	182
Dem_DTC_FTB_Table[44]	118
Dem_DTC_FTB_Table[45]	237
Dem_DTC_FTB_Table[46]	107
Dem_DTC_FTB_Table[47]	156
Dem_DTC_FTB_Table[48]	166
Dem_DTC_FTB_Table[49]	107
Dem_DTC_FTB_Table[50]	156
Dem_DTC_FTB_Table[51]	107
Dem_DTC_FTB_Table[52]	107
Dem_DTC_FTB_Table[53]	156
Dem_DTC_FTB_Table[54]	166
Dem_DTC_FTB_Table[55]	237
Dem_DTC_FTB_Table[56]	107
Dem_DTC_FTB_Table[57]	156
Dem_DTC_FTB_Table[58]	107
Dem_DTC_FTB_Table[59]	237
Dem_DTC_FTB_Table[60]	107
Dem_DTC_FTB_Table[61]	156
Dem_DTC_FTB_Table[62]	166
Dem_DTC_FTB_Table[63]	5
Dem_DTC_FTB_Table[64]	166
Dem_DTC_FTB_Table[65]	182
Dem_DTC_FTB_Table[66]	118
Dem_DTC_FTB_Table[67]	107
Dem_DTC_FTB_Table[68]	107
Dem_DTC_FTB_Table[69]	156
Dem_DTC_FTB_Table[70]	166
Dem_DTC_FTB_Table[71]	237
Dem_DTC_FTB_Table[72]	166
Dem_DTC_FTB_Table[73]	5
Dem_DTC_FTB_Table[74]	166
Dem_DTC_FTB_Table[75]	182
Dem_DTC_FTB_Table[76]	118

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[12]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[13]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[14]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[15]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[16]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[17]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[18]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[19]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[20]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[21]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[22]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[23]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[24]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[25]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[26]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[27]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[28]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[29]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[30]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[37]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[43]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[44]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	3302797192
DTCKind	1
DTCStatusNew	172
DTCStatusOld	91
Dem_DTCNumberTable[0]	112
Dem_DTCNumberTable[1]	227
Dem_DTCNumberTable[2]	76
Dem_DTCNumberTable[3]	252
Dem_DTCNumberTable[4]	240
Dem_DTCNumberTable[5]	206
Dem_DTCNumberTable[6]	62
Dem_DTCNumberTable[7]	62
Dem_DTCNumberTable[8]	112
Dem_DTCNumberTable[9]	227
Dem_DTCNumberTable[10]	62
Dem_DTCNumberTable[11]	80
Dem_DTCNumberTable[12]	227
Dem_DTCNumberTable[13]	62
Dem_DTCNumberTable[14]	112
Dem_DTCNumberTable[15]	227
Dem_DTCNumberTable[16]	227
Dem_DTCNumberTable[17]	62
Dem_DTCNumberTable[18]	57
Dem_DTCNumberTable[19]	112
Dem_DTCNumberTable[20]	227
Dem_DTCNumberTable[21]	62
Dem_DTCNumberTable[22]	112
Dem_DTCNumberTable[23]	76
Dem_DTCNumberTable[24]	252
Dem_DTCNumberTable[25]	240
Dem_DTCNumberTable[26]	206
Dem_DTCNumberTable[27]	227
Dem_DTCNumberTable[28]	112
Dem_DTCNumberTable[29]	227
Dem_DTCNumberTable[30]	112
Dem_DTCNumberTable[31]	112
Dem_DTCNumberTable[32]	227
Dem_DTCNumberTable[33]	227
Dem_DTCNumberTable[34]	112
Dem_DTCNumberTable[35]	227
Dem_DTCNumberTable[36]	112
Dem_DTCNumberTable[37]	112
Dem_DTCNumberTable[38]	112
Dem_DTCNumberTable[39]	227
Dem_DTCNumberTable[40]	227
Dem_DTCNumberTable[41]	76
Dem_DTCNumberTable[42]	252
Dem_DTCNumberTable[43]	240
Dem_DTCNumberTable[44]	206
Dem_DTCNumberTable[45]	62
Dem_DTCNumberTable[46]	112
Dem_DTCNumberTable[47]	227
Dem_DTCNumberTable[48]	252
Dem_DTCNumberTable[49]	112
Dem_DTCNumberTable[50]	227
Dem_DTCNumberTable[51]	112
Dem_DTCNumberTable[52]	112
Dem_DTCNumberTable[53]	227
Dem_DTCNumberTable[54]	252

Name	Input Value
Dem_DTCNumberTable[55]	62
Dem_DTCNumberTable[56]	112
Dem_DTCNumberTable[57]	227
Dem_DTCNumberTable[58]	112
Dem_DTCNumberTable[59]	62
Dem_DTCNumberTable[60]	112
Dem_DTCNumberTable[61]	227
Dem_DTCNumberTable[62]	252
Dem_DTCNumberTable[63]	76
Dem_DTCNumberTable[64]	252
Dem_DTCNumberTable[65]	240
Dem_DTCNumberTable[66]	206
Dem_DTCNumberTable[67]	112
Dem_DTCNumberTable[68]	112
Dem_DTCNumberTable[69]	227
Dem_DTCNumberTable[70]	252
Dem_DTCNumberTable[71]	62
Dem_DTCNumberTable[72]	252
Dem_DTCNumberTable[73]	76
Dem_DTCNumberTable[74]	252
Dem_DTCNumberTable[75]	240
Dem_DTCNumberTable[76]	206
Dem_DTC_FTB_Table[0]	219
Dem_DTC_FTB_Table[1]	237
Dem_DTC_FTB_Table[2]	46
Dem_DTC_FTB_Table[3]	187
Dem_DTC_FTB_Table[4]	250
Dem_DTC_FTB_Table[5]	36
Dem_DTC_FTB_Table[6]	202
Dem_DTC_FTB_Table[7]	202
Dem_DTC_FTB_Table[8]	219
Dem_DTC_FTB_Table[9]	237
Dem_DTC_FTB_Table[10]	202
Dem_DTC_FTB_Table[11]	126
Dem_DTC_FTB_Table[12]	237
Dem_DTC_FTB_Table[13]	202
Dem_DTC_FTB_Table[14]	219
Dem_DTC_FTB_Table[15]	237
Dem_DTC_FTB_Table[16]	237
Dem_DTC_FTB_Table[17]	202
Dem_DTC_FTB_Table[18]	86
Dem_DTC_FTB_Table[19]	219
Dem_DTC_FTB_Table[20]	237
Dem_DTC_FTB_Table[21]	202
Dem_DTC_FTB_Table[22]	219
Dem_DTC_FTB_Table[23]	46
Dem_DTC_FTB_Table[24]	187
Dem_DTC_FTB_Table[25]	250
Dem_DTC_FTB_Table[26]	36
Dem_DTC_FTB_Table[27]	237
Dem_DTC_FTB_Table[28]	219
Dem_DTC_FTB_Table[29]	237
Dem_DTC_FTB_Table[30]	219
Dem_DTC_FTB_Table[31]	219
Dem_DTC_FTB_Table[32]	237
Dem_DTC_FTB_Table[33]	237
Dem_DTC_FTB_Table[34]	219
Dem_DTC_FTB_Table[35]	237
Dem_DTC_FTB_Table[36]	219
Dem_DTC_FTB_Table[37]	219
Dem_DTC_FTB_Table[38]	219
Dem_DTC_FTB_Table[39]	237
Dem_DTC_FTB_Table[40]	237
Dem_DTC_FTB_Table[41]	46
Dem_DTC_FTB_Table[42]	187
Dem_DTC_FTB_Table[43]	250
Dem_DTC_FTB_Table[44]	36
Dem_DTC_FTB_Table[45]	202
Dem_DTC_FTB_Table[46]	219
Dem_DTC_FTB_Table[47]	237
Dem_DTC_FTB_Table[48]	187
Dem_DTC_FTB_Table[49]	219
Dem_DTC_FTB_Table[50]	237

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Input Value
Dem_DTC_FTB_Table[51]	219
Dem_DTC_FTB_Table[52]	219
Dem_DTC_FTB_Table[53]	237
Dem_DTC_FTB_Table[54]	187
Dem_DTC_FTB_Table[55]	202
Dem_DTC_FTB_Table[56]	219
Dem_DTC_FTB_Table[57]	237
Dem_DTC_FTB_Table[58]	219
Dem_DTC_FTB_Table[59]	202
Dem_DTC_FTB_Table[60]	219
Dem_DTC_FTB_Table[61]	237
Dem_DTC_FTB_Table[62]	187
Dem_DTC_FTB_Table[63]	46
Dem_DTC_FTB_Table[64]	187
Dem_DTC_FTB_Table[65]	250
Dem_DTC_FTB_Table[66]	36
Dem_DTC_FTB_Table[67]	219
Dem_DTC_FTB_Table[68]	219
Dem_DTC_FTB_Table[69]	237
Dem_DTC_FTB_Table[70]	187
Dem_DTC_FTB_Table[71]	202
Dem_DTC_FTB_Table[72]	187
Dem_DTC_FTB_Table[73]	46
Dem_DTC_FTB_Table[74]	187
Dem_DTC_FTB_Table[75]	250
Dem_DTC_FTB_Table[76]	36

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	0
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	3645660753
DTCKind	1
DTCStatusNew	182
DTCStatusOld	237
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0

Name	Input Value
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	69
Dem_DTC_FTB_Table[1]	30
Dem_DTC_FTB_Table[2]	148
Dem_DTC_FTB_Table[3]	120
Dem_DTC_FTB_Table[4]	135
Dem_DTC_FTB_Table[5]	193
Dem_DTC_FTB_Table[6]	53
Dem_DTC_FTB_Table[7]	53
Dem_DTC_FTB_Table[8]	69
Dem_DTC_FTB_Table[9]	30
Dem_DTC_FTB_Table[10]	53
Dem_DTC_FTB_Table[11]	189
Dem_DTC_FTB_Table[12]	30
Dem_DTC_FTB_Table[13]	53
Dem_DTC_FTB_Table[14]	69
Dem_DTC_FTB_Table[15]	30

Name	Input Value
Dem_DTC_FTB_Table[16]	30
Dem_DTC_FTB_Table[17]	53
Dem_DTC_FTB_Table[18]	127
Dem_DTC_FTB_Table[19]	69
Dem_DTC_FTB_Table[20]	30
Dem_DTC_FTB_Table[21]	53
Dem_DTC_FTB_Table[22]	69
Dem_DTC_FTB_Table[23]	148
Dem_DTC_FTB_Table[24]	120
Dem_DTC_FTB_Table[25]	135
Dem_DTC_FTB_Table[26]	193
Dem_DTC_FTB_Table[27]	30
Dem_DTC_FTB_Table[28]	69
Dem_DTC_FTB_Table[29]	30
Dem_DTC_FTB_Table[30]	69
Dem_DTC_FTB_Table[31]	69
Dem_DTC_FTB_Table[32]	30
Dem_DTC_FTB_Table[33]	30
Dem_DTC_FTB_Table[34]	69
Dem_DTC_FTB_Table[35]	30
Dem_DTC_FTB_Table[36]	69
Dem_DTC_FTB_Table[37]	69
Dem_DTC_FTB_Table[38]	69
Dem_DTC_FTB_Table[39]	30
Dem_DTC_FTB_Table[40]	30
Dem_DTC_FTB_Table[41]	148
Dem_DTC_FTB_Table[42]	120
Dem_DTC_FTB_Table[43]	135
Dem_DTC_FTB_Table[44]	193
Dem_DTC_FTB_Table[45]	53
Dem_DTC_FTB_Table[46]	69
Dem_DTC_FTB_Table[47]	30
Dem_DTC_FTB_Table[48]	120
Dem_DTC_FTB_Table[49]	69
Dem_DTC_FTB_Table[50]	30
Dem_DTC_FTB_Table[51]	69
Dem_DTC_FTB_Table[52]	69
Dem_DTC_FTB_Table[53]	30
Dem_DTC_FTB_Table[54]	120
Dem_DTC_FTB_Table[55]	53
Dem_DTC_FTB_Table[56]	69
Dem_DTC_FTB_Table[57]	30
Dem_DTC_FTB_Table[58]	69
Dem_DTC_FTB_Table[59]	53
Dem_DTC_FTB_Table[60]	69
Dem_DTC_FTB_Table[61]	30
Dem_DTC_FTB_Table[62]	120
Dem_DTC_FTB_Table[63]	148
Dem_DTC_FTB_Table[64]	120
Dem_DTC_FTB_Table[65]	135
Dem_DTC_FTB_Table[66]	193
Dem_DTC_FTB_Table[67]	69
Dem_DTC_FTB_Table[68]	69
Dem_DTC_FTB_Table[69]	30
Dem_DTC_FTB_Table[70]	120
Dem_DTC_FTB_Table[71]	53
Dem_DTC_FTB_Table[72]	120
Dem_DTC_FTB_Table[73]	148
Dem_DTC_FTB_Table[74]	120
Dem_DTC_FTB_Table[75]	135
Dem_DTC_FTB_Table[76]	193

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Step 2.20 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	1
CTCFailedBuf_Cnt_M_Igc[1]	1
CTCFailedBuf_Cnt_M_Igc[2]	1
CTCFailedBuf_Cnt_M_Igc[3]	1
CTCFailedBuf_Cnt_M_Igc[4]	1
CTCFailedBuf_Cnt_M_Igc[5]	1
CTCFailedBuf_Cnt_M_Igc[6]	1
CTCFailedBuf_Cnt_M_Igc[7]	1
CTCFailedBuf_Cnt_M_Igc[8]	1
CTCFailedBuf_Cnt_M_Igc[9]	1
CTCFailedBuf_Cnt_M_Igc[10]	1
CTCFailedBuf_Cnt_M_Igc[11]	1
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	0
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	4137755052
DTCKind	2
DTCStatusNew	250
DTCStatusOld	202
Dem_DTCNumberTable[0]	65535
Dem_DTCNumberTable[1]	65535
Dem_DTCNumberTable[2]	65535
Dem_DTCNumberTable[3]	65535
Dem_DTCNumberTable[4]	65535
Dem_DTCNumberTable[5]	65535
Dem_DTCNumberTable[6]	65535
Dem_DTCNumberTable[7]	65535
Dem_DTCNumberTable[8]	65535
Dem_DTCNumberTable[9]	65535
Dem_DTCNumberTable[10]	65535
Dem_DTCNumberTable[11]	65535
Dem_DTCNumberTable[12]	65535
Dem_DTCNumberTable[13]	65535
Dem_DTCNumberTable[14]	65535
Dem_DTCNumberTable[15]	65535
Dem_DTCNumberTable[16]	65535
Dem_DTCNumberTable[17]	65535
Dem_DTCNumberTable[18]	65535
Dem_DTCNumberTable[19]	65535
Dem_DTCNumberTable[20]	65535
Dem_DTCNumberTable[21]	65535
Dem_DTCNumberTable[22]	65535
Dem_DTCNumberTable[23]	65535
Dem_DTCNumberTable[24]	65535
Dem_DTCNumberTable[25]	65535
Dem_DTCNumberTable[26]	65535
Dem_DTCNumberTable[27]	65535
Dem_DTCNumberTable[28]	65535
Dem_DTCNumberTable[29]	65535
Dem_DTCNumberTable[30]	65535
Dem_DTCNumberTable[31]	65535
Dem_DTCNumberTable[32]	65535
Dem_DTCNumberTable[33]	65535
Dem_DTCNumberTable[34]	65535
Dem_DTCNumberTable[35]	65535
Dem_DTCNumberTable[36]	65535
Dem_DTCNumberTable[37]	65535
Dem_DTCNumberTable[38]	65535
Dem_DTCNumberTable[39]	65535
Dem_DTCNumberTable[40]	65535
Dem_DTCNumberTable[41]	65535
Dem_DTCNumberTable[42]	65535
Dem_DTCNumberTable[43]	65535
Dem_DTCNumberTable[44]	65535
Dem_DTCNumberTable[45]	65535
Dem_DTCNumberTable[46]	65535
Dem_DTCNumberTable[47]	65535
Dem_DTCNumberTable[48]	65535
Dem_DTCNumberTable[49]	65535
Dem_DTCNumberTable[50]	65535
Dem_DTCNumberTable[51]	65535
Dem_DTCNumberTable[52]	65535
Dem_DTCNumberTable[53]	65535
Dem_DTCNumberTable[54]	65535

Name	Input Value
Dem_DTCNumberTable[55]	65535
Dem_DTCNumberTable[56]	65535
Dem_DTCNumberTable[57]	65535
Dem_DTCNumberTable[58]	65535
Dem_DTCNumberTable[59]	65535
Dem_DTCNumberTable[60]	65535
Dem_DTCNumberTable[61]	65535
Dem_DTCNumberTable[62]	65535
Dem_DTCNumberTable[63]	65535
Dem_DTCNumberTable[64]	65535
Dem_DTCNumberTable[65]	65535
Dem_DTCNumberTable[66]	65535
Dem_DTCNumberTable[67]	65535
Dem_DTCNumberTable[68]	65535
Dem_DTCNumberTable[69]	65535
Dem_DTCNumberTable[70]	65535
Dem_DTCNumberTable[71]	65535
Dem_DTCNumberTable[72]	65535
Dem_DTCNumberTable[73]	65535
Dem_DTCNumberTable[74]	65535
Dem_DTCNumberTable[75]	65535
Dem_DTCNumberTable[76]	65535
Dem_DTC_FTB_Table[0]	254
Dem_DTC_FTB_Table[1]	153
Dem_DTC_FTB_Table[2]	91
Dem_DTC_FTB_Table[3]	138
Dem_DTC_FTB_Table[4]	54
Dem_DTC_FTB_Table[5]	108
Dem_DTC_FTB_Table[6]	239
Dem_DTC_FTB_Table[7]	239
Dem_DTC_FTB_Table[8]	254
Dem_DTC_FTB_Table[9]	153
Dem_DTC_FTB_Table[10]	239
Dem_DTC_FTB_Table[11]	200
Dem_DTC_FTB_Table[12]	153
Dem_DTC_FTB_Table[13]	239
Dem_DTC_FTB_Table[14]	254
Dem_DTC_FTB_Table[15]	153
Dem_DTC_FTB_Table[16]	153
Dem_DTC_FTB_Table[17]	239
Dem_DTC_FTB_Table[18]	33
Dem_DTC_FTB_Table[19]	254
Dem_DTC_FTB_Table[20]	153
Dem_DTC_FTB_Table[21]	239
Dem_DTC_FTB_Table[22]	254
Dem_DTC_FTB_Table[23]	91
Dem_DTC_FTB_Table[24]	138
Dem_DTC_FTB_Table[25]	54
Dem_DTC_FTB_Table[26]	108
Dem_DTC_FTB_Table[27]	153
Dem_DTC_FTB_Table[28]	254
Dem_DTC_FTB_Table[29]	153
Dem_DTC_FTB_Table[30]	254
Dem_DTC_FTB_Table[31]	254
Dem_DTC_FTB_Table[32]	153
Dem_DTC_FTB_Table[33]	153
Dem_DTC_FTB_Table[34]	254
Dem_DTC_FTB_Table[35]	153
Dem_DTC_FTB_Table[36]	254
Dem_DTC_FTB_Table[37]	254
Dem_DTC_FTB_Table[38]	254
Dem_DTC_FTB_Table[39]	153
Dem_DTC_FTB_Table[40]	153
Dem_DTC_FTB_Table[41]	91
Dem_DTC_FTB_Table[42]	138
Dem_DTC_FTB_Table[43]	54
Dem_DTC_FTB_Table[44]	108
Dem_DTC_FTB_Table[45]	239
Dem_DTC_FTB_Table[46]	254
Dem_DTC_FTB_Table[47]	153
Dem_DTC_FTB_Table[48]	138
Dem_DTC_FTB_Table[49]	254
Dem_DTC_FTB_Table[50]	153

TEST DETAILS REPORT

DemIf_DTCStatusChanged

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Name	Input Value
Dem_DTC_FTB_Table[51]	254
Dem_DTC_FTB_Table[52]	254
Dem_DTC_FTB_Table[53]	153
Dem_DTC_FTB_Table[54]	138
Dem_DTC_FTB_Table[55]	239
Dem_DTC_FTB_Table[56]	254
Dem_DTC_FTB_Table[57]	153
Dem_DTC_FTB_Table[58]	254
Dem_DTC_FTB_Table[59]	239
Dem_DTC_FTB_Table[60]	254
Dem_DTC_FTB_Table[61]	153
Dem_DTC_FTB_Table[62]	138
Dem_DTC_FTB_Table[63]	91
Dem_DTC_FTB_Table[64]	138
Dem_DTC_FTB_Table[65]	54
Dem_DTC_FTB_Table[66]	108
Dem_DTC_FTB_Table[67]	254
Dem_DTC_FTB_Table[68]	254
Dem_DTC_FTB_Table[69]	153
Dem_DTC_FTB_Table[70]	138
Dem_DTC_FTB_Table[71]	239
Dem_DTC_FTB_Table[72]	138
Dem_DTC_FTB_Table[73]	91
Dem_DTC_FTB_Table[74]	138
Dem_DTC_FTB_Table[75]	54
Dem_DTC_FTB_Table[76]	108

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	0
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	1
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	1
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	0
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	2969842604
DTCKind	1
DTCStatusNew	135
DTCStatusOld	53
Dem_DTCNumberTable[0]	219
Dem_DTCNumberTable[1]	237
Dem_DTCNumberTable[2]	46
Dem_DTCNumberTable[3]	187
Dem_DTCNumberTable[4]	250
Dem_DTCNumberTable[5]	36
Dem_DTCNumberTable[6]	202
Dem_DTCNumberTable[7]	202
Dem_DTCNumberTable[8]	219
Dem_DTCNumberTable[9]	237
Dem_DTCNumberTable[10]	202
Dem_DTCNumberTable[11]	126
Dem_DTCNumberTable[12]	237
Dem_DTCNumberTable[13]	202
Dem_DTCNumberTable[14]	219
Dem_DTCNumberTable[15]	237
Dem_DTCNumberTable[16]	237
Dem_DTCNumberTable[17]	202
Dem_DTCNumberTable[18]	86
Dem_DTCNumberTable[19]	219

Name	Input Value
Dem_DTCNumberTable[20]	237
Dem_DTCNumberTable[21]	202
Dem_DTCNumberTable[22]	219
Dem_DTCNumberTable[23]	46
Dem_DTCNumberTable[24]	187
Dem_DTCNumberTable[25]	250
Dem_DTCNumberTable[26]	36
Dem_DTCNumberTable[27]	237
Dem_DTCNumberTable[28]	219
Dem_DTCNumberTable[29]	237
Dem_DTCNumberTable[30]	219
Dem_DTCNumberTable[31]	219
Dem_DTCNumberTable[32]	237
Dem_DTCNumberTable[33]	237
Dem_DTCNumberTable[34]	219
Dem_DTCNumberTable[35]	237
Dem_DTCNumberTable[36]	219
Dem_DTCNumberTable[37]	219
Dem_DTCNumberTable[38]	219
Dem_DTCNumberTable[39]	237
Dem_DTCNumberTable[40]	237
Dem_DTCNumberTable[41]	46
Dem_DTCNumberTable[42]	187
Dem_DTCNumberTable[43]	250
Dem_DTCNumberTable[44]	36
Dem_DTCNumberTable[45]	202
Dem_DTCNumberTable[46]	219
Dem_DTCNumberTable[47]	237
Dem_DTCNumberTable[48]	187
Dem_DTCNumberTable[49]	219
Dem_DTCNumberTable[50]	237
Dem_DTCNumberTable[51]	219
Dem_DTCNumberTable[52]	219
Dem_DTCNumberTable[53]	237
Dem_DTCNumberTable[54]	187
Dem_DTCNumberTable[55]	202
Dem_DTCNumberTable[56]	219
Dem_DTCNumberTable[57]	237
Dem_DTCNumberTable[58]	219
Dem_DTCNumberTable[59]	202
Dem_DTCNumberTable[60]	219
Dem_DTCNumberTable[61]	237
Dem_DTCNumberTable[62]	187
Dem_DTCNumberTable[63]	46
Dem_DTCNumberTable[64]	187
Dem_DTCNumberTable[65]	250
Dem_DTCNumberTable[66]	36
Dem_DTCNumberTable[67]	219
Dem_DTCNumberTable[68]	219
Dem_DTCNumberTable[69]	237
Dem_DTCNumberTable[70]	187
Dem_DTCNumberTable[71]	202
Dem_DTCNumberTable[72]	187
Dem_DTCNumberTable[73]	46
Dem_DTCNumberTable[74]	187
Dem_DTCNumberTable[75]	250
Dem_DTCNumberTable[76]	36
Dem_DTC_FTB_Table[0]	157
Dem_DTC_FTB_Table[1]	1
Dem_DTC_FTB_Table[2]	112
Dem_DTC_FTB_Table[3]	195
Dem_DTC_FTB_Table[4]	200
Dem_DTC_FTB_Table[5]	99
Dem_DTC_FTB_Table[6]	203
Dem_DTC_FTB_Table[7]	203
Dem_DTC_FTB_Table[8]	157
Dem_DTC_FTB_Table[9]	1
Dem_DTC_FTB_Table[10]	203
Dem_DTC_FTB_Table[11]	201
Dem_DTC_FTB_Table[12]	1
Dem_DTC_FTB_Table[13]	203
Dem_DTC_FTB_Table[14]	157
Dem_DTC_FTB_Table[15]	1

Name	Input Value
Dem_DTC_FTB_Table[16]	1
Dem_DTC_FTB_Table[17]	203
Dem_DTC_FTB_Table[18]	101
Dem_DTC_FTB_Table[19]	157
Dem_DTC_FTB_Table[20]	1
Dem_DTC_FTB_Table[21]	203
Dem_DTC_FTB_Table[22]	157
Dem_DTC_FTB_Table[23]	112
Dem_DTC_FTB_Table[24]	195
Dem_DTC_FTB_Table[25]	200
Dem_DTC_FTB_Table[26]	99
Dem_DTC_FTB_Table[27]	1
Dem_DTC_FTB_Table[28]	157
Dem_DTC_FTB_Table[29]	1
Dem_DTC_FTB_Table[30]	157
Dem_DTC_FTB_Table[31]	157
Dem_DTC_FTB_Table[32]	1
Dem_DTC_FTB_Table[33]	1
Dem_DTC_FTB_Table[34]	157
Dem_DTC_FTB_Table[35]	1
Dem_DTC_FTB_Table[36]	157
Dem_DTC_FTB_Table[37]	157
Dem_DTC_FTB_Table[38]	157
Dem_DTC_FTB_Table[39]	1
Dem_DTC_FTB_Table[40]	1
Dem_DTC_FTB_Table[41]	112
Dem_DTC_FTB_Table[42]	195
Dem_DTC_FTB_Table[43]	200
Dem_DTC_FTB_Table[44]	99
Dem_DTC_FTB_Table[45]	203
Dem_DTC_FTB_Table[46]	157
Dem_DTC_FTB_Table[47]	1
Dem_DTC_FTB_Table[48]	195
Dem_DTC_FTB_Table[49]	157
Dem_DTC_FTB_Table[50]	1
Dem_DTC_FTB_Table[51]	157
Dem_DTC_FTB_Table[52]	157
Dem_DTC_FTB_Table[53]	1
Dem_DTC_FTB_Table[54]	195
Dem_DTC_FTB_Table[55]	203
Dem_DTC_FTB_Table[56]	157
Dem_DTC_FTB_Table[57]	1
Dem_DTC_FTB_Table[58]	157
Dem_DTC_FTB_Table[59]	203
Dem_DTC_FTB_Table[60]	157
Dem_DTC_FTB_Table[61]	1
Dem_DTC_FTB_Table[62]	195
Dem_DTC_FTB_Table[63]	112
Dem_DTC_FTB_Table[64]	195
Dem_DTC_FTB_Table[65]	200
Dem_DTC_FTB_Table[66]	99
Dem_DTC_FTB_Table[67]	157
Dem_DTC_FTB_Table[68]	157
Dem_DTC_FTB_Table[69]	1
Dem_DTC_FTB_Table[70]	195
Dem_DTC_FTB_Table[71]	203
Dem_DTC_FTB_Table[72]	195
Dem_DTC_FTB_Table[73]	112
Dem_DTC_FTB_Table[74]	195
Dem_DTC_FTB_Table[75]	200
Dem_DTC_FTB_Table[76]	99

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	1
DTC	598152539
DTCKind	1
DTCStatusNew	54
DTCStatusOld	239
Dem_DTCNumberTable[0]	69
Dem_DTCNumberTable[1]	30
Dem_DTCNumberTable[2]	148
Dem_DTCNumberTable[3]	120
Dem_DTCNumberTable[4]	135
Dem_DTCNumberTable[5]	193
Dem_DTCNumberTable[6]	53
Dem_DTCNumberTable[7]	53
Dem_DTCNumberTable[8]	69
Dem_DTCNumberTable[9]	30
Dem_DTCNumberTable[10]	53
Dem_DTCNumberTable[11]	189
Dem_DTCNumberTable[12]	30
Dem_DTCNumberTable[13]	53
Dem_DTCNumberTable[14]	69
Dem_DTCNumberTable[15]	30
Dem_DTCNumberTable[16]	30
Dem_DTCNumberTable[17]	53
Dem_DTCNumberTable[18]	127
Dem_DTCNumberTable[19]	69
Dem_DTCNumberTable[20]	30
Dem_DTCNumberTable[21]	53
Dem_DTCNumberTable[22]	69
Dem_DTCNumberTable[23]	148
Dem_DTCNumberTable[24]	120
Dem_DTCNumberTable[25]	135
Dem_DTCNumberTable[26]	193
Dem_DTCNumberTable[27]	30
Dem_DTCNumberTable[28]	69
Dem_DTCNumberTable[29]	30
Dem_DTCNumberTable[30]	69
Dem_DTCNumberTable[31]	69
Dem_DTCNumberTable[32]	30
Dem_DTCNumberTable[33]	30
Dem_DTCNumberTable[34]	69
Dem_DTCNumberTable[35]	30
Dem_DTCNumberTable[36]	69
Dem_DTCNumberTable[37]	69
Dem_DTCNumberTable[38]	69
Dem_DTCNumberTable[39]	30
Dem_DTCNumberTable[40]	30
Dem_DTCNumberTable[41]	148
Dem_DTCNumberTable[42]	120
Dem_DTCNumberTable[43]	135
Dem_DTCNumberTable[44]	193
Dem_DTCNumberTable[45]	53
Dem_DTCNumberTable[46]	69
Dem_DTCNumberTable[47]	30
Dem_DTCNumberTable[48]	120
Dem_DTCNumberTable[49]	69
Dem_DTCNumberTable[50]	30
Dem_DTCNumberTable[51]	69
Dem_DTCNumberTable[52]	69
Dem_DTCNumberTable[53]	30
Dem_DTCNumberTable[54]	120

Name	Input Value
Dem_DTCNumberTable[55]	53
Dem_DTCNumberTable[56]	69
Dem_DTCNumberTable[57]	30
Dem_DTCNumberTable[58]	69
Dem_DTCNumberTable[59]	53
Dem_DTCNumberTable[60]	69
Dem_DTCNumberTable[61]	30
Dem_DTCNumberTable[62]	120
Dem_DTCNumberTable[63]	148
Dem_DTCNumberTable[64]	120
Dem_DTCNumberTable[65]	135
Dem_DTCNumberTable[66]	193
Dem_DTCNumberTable[67]	69
Dem_DTCNumberTable[68]	69
Dem_DTCNumberTable[69]	30
Dem_DTCNumberTable[70]	120
Dem_DTCNumberTable[71]	53
Dem_DTCNumberTable[72]	120
Dem_DTCNumberTable[73]	148
Dem_DTCNumberTable[74]	120
Dem_DTCNumberTable[75]	135
Dem_DTCNumberTable[76]	193
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0

Name	Input Value
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
Dem_DTC_FTB_Table[71]	0
Dem_DTC_FTB_Table[72]	0
Dem_DTC_FTB_Table[73]	0
Dem_DTC_FTB_Table[74]	0
Dem_DTC_FTB_Table[75]	0
Dem_DTC_FTB_Table[76]	0

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[50]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	4118147944
DTCKind	2
DTCStatusNew	200
DTCStatusOld	203
Dem_DTCNumberTable[0]	254
Dem_DTCNumberTable[1]	153
Dem_DTCNumberTable[2]	91
Dem_DTCNumberTable[3]	138
Dem_DTCNumberTable[4]	54
Dem_DTCNumberTable[5]	108
Dem_DTCNumberTable[6]	239
Dem_DTCNumberTable[7]	239
Dem_DTCNumberTable[8]	254
Dem_DTCNumberTable[9]	153
Dem_DTCNumberTable[10]	239
Dem_DTCNumberTable[11]	200
Dem_DTCNumberTable[12]	153
Dem_DTCNumberTable[13]	239
Dem_DTCNumberTable[14]	254
Dem_DTCNumberTable[15]	153
Dem_DTCNumberTable[16]	153
Dem_DTCNumberTable[17]	239
Dem_DTCNumberTable[18]	33
Dem_DTCNumberTable[19]	254

Name	Input Value
Dem_DTCNumberTable[20]	153
Dem_DTCNumberTable[21]	239
Dem_DTCNumberTable[22]	254
Dem_DTCNumberTable[23]	91
Dem_DTCNumberTable[24]	138
Dem_DTCNumberTable[25]	54
Dem_DTCNumberTable[26]	108
Dem_DTCNumberTable[27]	153
Dem_DTCNumberTable[28]	254
Dem_DTCNumberTable[29]	153
Dem_DTCNumberTable[30]	254
Dem_DTCNumberTable[31]	254
Dem_DTCNumberTable[32]	153
Dem_DTCNumberTable[33]	153
Dem_DTCNumberTable[34]	254
Dem_DTCNumberTable[35]	153
Dem_DTCNumberTable[36]	254
Dem_DTCNumberTable[37]	254
Dem_DTCNumberTable[38]	254
Dem_DTCNumberTable[39]	153
Dem_DTCNumberTable[40]	153
Dem_DTCNumberTable[41]	91
Dem_DTCNumberTable[42]	138
Dem_DTCNumberTable[43]	54
Dem_DTCNumberTable[44]	108
Dem_DTCNumberTable[45]	239
Dem_DTCNumberTable[46]	254
Dem_DTCNumberTable[47]	153
Dem_DTCNumberTable[48]	138
Dem_DTCNumberTable[49]	254
Dem_DTCNumberTable[50]	153
Dem_DTCNumberTable[51]	254
Dem_DTCNumberTable[52]	254
Dem_DTCNumberTable[53]	153
Dem_DTCNumberTable[54]	138
Dem_DTCNumberTable[55]	239
Dem_DTCNumberTable[56]	254
Dem_DTCNumberTable[57]	153
Dem_DTCNumberTable[58]	254
Dem_DTCNumberTable[59]	239
Dem_DTCNumberTable[60]	254
Dem_DTCNumberTable[61]	153
Dem_DTCNumberTable[62]	138
Dem_DTCNumberTable[63]	91
Dem_DTCNumberTable[64]	138
Dem_DTCNumberTable[65]	54
Dem_DTCNumberTable[66]	108
Dem_DTCNumberTable[67]	254
Dem_DTCNumberTable[68]	254
Dem_DTCNumberTable[69]	153
Dem_DTCNumberTable[70]	138
Dem_DTCNumberTable[71]	239
Dem_DTCNumberTable[72]	138
Dem_DTCNumberTable[73]	91
Dem_DTCNumberTable[74]	138
Dem_DTCNumberTable[75]	54
Dem_DTCNumberTable[76]	108
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[11]	255
Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem_DTC_FTB_Table[14]	255
Dem_DTC_FTB_Table[15]	255

Name	Input Value
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
Dem_DTC_FTB_Table[30]	255
Dem_DTC_FTB_Table[31]	255
Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[33]	255
Dem_DTC_FTB_Table[34]	255
Dem_DTC_FTB_Table[35]	255
Dem_DTC_FTB_Table[36]	255
Dem_DTC_FTB_Table[37]	255
Dem_DTC_FTB_Table[38]	255
Dem_DTC_FTB_Table[39]	255
Dem_DTC_FTB_Table[40]	255
Dem_DTC_FTB_Table[41]	255
Dem_DTC_FTB_Table[42]	255
Dem_DTC_FTB_Table[43]	255
Dem_DTC_FTB_Table[44]	255
Dem_DTC_FTB_Table[45]	255
Dem_DTC_FTB_Table[46]	255
Dem_DTC_FTB_Table[47]	255
Dem_DTC_FTB_Table[48]	255
Dem_DTC_FTB_Table[49]	255
Dem_DTC_FTB_Table[50]	255
Dem_DTC_FTB_Table[51]	255
Dem_DTC_FTB_Table[52]	255
Dem_DTC_FTB_Table[53]	255
Dem_DTC_FTB_Table[54]	255
Dem_DTC_FTB_Table[55]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[57]	255
Dem_DTC_FTB_Table[58]	255
Dem_DTC_FTB_Table[59]	255
Dem_DTC_FTB_Table[60]	255
Dem_DTC_FTB_Table[61]	255
Dem_DTC_FTB_Table[62]	255
Dem_DTC_FTB_Table[63]	255
Dem_DTC_FTB_Table[64]	255
Dem_DTC_FTB_Table[65]	255
Dem_DTC_FTB_Table[66]	255
Dem_DTC_FTB_Table[67]	255
Dem_DTC_FTB_Table[68]	255
Dem_DTC_FTB_Table[69]	255
Dem_DTC_FTB_Table[70]	255
Dem_DTC_FTB_Table[71]	255
Dem_DTC_FTB_Table[72]	255
Dem_DTC_FTB_Table[73]	255
Dem_DTC_FTB_Table[74]	255
Dem_DTC_FTB_Table[75]	255
Dem_DTC_FTB_Table[76]	255

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	2120792415
DTCKind	2
DTCStatusNew	226
DTCStatusOld	69
Dem_DTCNumberTable[0]	157
Dem_DTCNumberTable[1]	1
Dem_DTCNumberTable[2]	112
Dem_DTCNumberTable[3]	195
Dem_DTCNumberTable[4]	200
Dem_DTCNumberTable[5]	99
Dem_DTCNumberTable[6]	203
Dem_DTCNumberTable[7]	203
Dem_DTCNumberTable[8]	157
Dem_DTCNumberTable[9]	1
Dem_DTCNumberTable[10]	203
Dem_DTCNumberTable[11]	201
Dem_DTCNumberTable[12]	1
Dem_DTCNumberTable[13]	203
Dem_DTCNumberTable[14]	157
Dem_DTCNumberTable[15]	1
Dem_DTCNumberTable[16]	1
Dem_DTCNumberTable[17]	203
Dem_DTCNumberTable[18]	101
Dem_DTCNumberTable[19]	157
Dem_DTCNumberTable[20]	1
Dem_DTCNumberTable[21]	203
Dem_DTCNumberTable[22]	157
Dem_DTCNumberTable[23]	112
Dem_DTCNumberTable[24]	195
Dem_DTCNumberTable[25]	200
Dem_DTCNumberTable[26]	99
Dem_DTCNumberTable[27]	1
Dem_DTCNumberTable[28]	157
Dem_DTCNumberTable[29]	1
Dem_DTCNumberTable[30]	157
Dem_DTCNumberTable[31]	157
Dem_DTCNumberTable[32]	1
Dem_DTCNumberTable[33]	1
Dem_DTCNumberTable[34]	157
Dem_DTCNumberTable[35]	1
Dem_DTCNumberTable[36]	157
Dem_DTCNumberTable[37]	157
Dem_DTCNumberTable[38]	157
Dem_DTCNumberTable[39]	1
Dem_DTCNumberTable[40]	1
Dem_DTCNumberTable[41]	112
Dem_DTCNumberTable[42]	195
Dem_DTCNumberTable[43]	200
Dem_DTCNumberTable[44]	99
Dem_DTCNumberTable[45]	203
Dem_DTCNumberTable[46]	157
Dem_DTCNumberTable[47]	1
Dem_DTCNumberTable[48]	195
Dem_DTCNumberTable[49]	157
Dem_DTCNumberTable[50]	1
Dem_DTCNumberTable[51]	157
Dem_DTCNumberTable[52]	157
Dem_DTCNumberTable[53]	1
Dem_DTCNumberTable[54]	195

Name	Input Value
Dem_DTCNumberTable[55]	203
Dem_DTCNumberTable[56]	157
Dem_DTCNumberTable[57]	1
Dem_DTCNumberTable[58]	157
Dem_DTCNumberTable[59]	203
Dem_DTCNumberTable[60]	157
Dem_DTCNumberTable[61]	1
Dem_DTCNumberTable[62]	195
Dem_DTCNumberTable[63]	112
Dem_DTCNumberTable[64]	195
Dem_DTCNumberTable[65]	200
Dem_DTCNumberTable[66]	99
Dem_DTCNumberTable[67]	157
Dem_DTCNumberTable[68]	157
Dem_DTCNumberTable[69]	1
Dem_DTCNumberTable[70]	195
Dem_DTCNumberTable[71]	203
Dem_DTCNumberTable[72]	195
Dem_DTCNumberTable[73]	112
Dem_DTCNumberTable[74]	195
Dem_DTCNumberTable[75]	200
Dem_DTCNumberTable[76]	99
Dem_DTC_FTB_Table[0]	31
Dem_DTC_FTB_Table[1]	227
Dem_DTC_FTB_Table[2]	66
Dem_DTC_FTB_Table[3]	96
Dem_DTC_FTB_Table[4]	130
Dem_DTC_FTB_Table[5]	24
Dem_DTC_FTB_Table[6]	240
Dem_DTC_FTB_Table[7]	240
Dem_DTC_FTB_Table[8]	31
Dem_DTC_FTB_Table[9]	227
Dem_DTC_FTB_Table[10]	240
Dem_DTC_FTB_Table[11]	151
Dem_DTC_FTB_Table[12]	227
Dem_DTC_FTB_Table[13]	240
Dem_DTC_FTB_Table[14]	31
Dem_DTC_FTB_Table[15]	227
Dem_DTC_FTB_Table[16]	227
Dem_DTC_FTB_Table[17]	240
Dem_DTC_FTB_Table[18]	241
Dem_DTC_FTB_Table[19]	31
Dem_DTC_FTB_Table[20]	227
Dem_DTC_FTB_Table[21]	240
Dem_DTC_FTB_Table[22]	31
Dem_DTC_FTB_Table[23]	66
Dem_DTC_FTB_Table[24]	96
Dem_DTC_FTB_Table[25]	130
Dem_DTC_FTB_Table[26]	24
Dem_DTC_FTB_Table[27]	227
Dem_DTC_FTB_Table[28]	31
Dem_DTC_FTB_Table[29]	227
Dem_DTC_FTB_Table[30]	31
Dem_DTC_FTB_Table[31]	31
Dem_DTC_FTB_Table[32]	227
Dem_DTC_FTB_Table[33]	227
Dem_DTC_FTB_Table[34]	31
Dem_DTC_FTB_Table[35]	227
Dem_DTC_FTB_Table[36]	31
Dem_DTC_FTB_Table[37]	31
Dem_DTC_FTB_Table[38]	31
Dem_DTC_FTB_Table[39]	227
Dem_DTC_FTB_Table[40]	227
Dem_DTC_FTB_Table[41]	66
Dem_DTC_FTB_Table[42]	96
Dem_DTC_FTB_Table[43]	130
Dem_DTC_FTB_Table[44]	24
Dem_DTC_FTB_Table[45]	240
Dem_DTC_FTB_Table[46]	31
Dem_DTC_FTB_Table[47]	227
Dem_DTC_FTB_Table[48]	96
Dem_DTC_FTB_Table[49]	31
Dem_DTC_FTB_Table[50]	227

Name	Input Value
Dem_DTC_FTB_Table[51]	31
Dem_DTC_FTB_Table[52]	31
Dem_DTC_FTB_Table[53]	227
Dem_DTC_FTB_Table[54]	96
Dem_DTC_FTB_Table[55]	240
Dem_DTC_FTB_Table[56]	31
Dem_DTC_FTB_Table[57]	227
Dem_DTC_FTB_Table[58]	31
Dem_DTC_FTB_Table[59]	240
Dem_DTC_FTB_Table[60]	31
Dem_DTC_FTB_Table[61]	227
Dem_DTC_FTB_Table[62]	96
Dem_DTC_FTB_Table[63]	66
Dem_DTC_FTB_Table[64]	96
Dem_DTC_FTB_Table[65]	130
Dem_DTC_FTB_Table[66]	24
Dem_DTC_FTB_Table[67]	31
Dem_DTC_FTB_Table[68]	31
Dem_DTC_FTB_Table[69]	227
Dem_DTC_FTB_Table[70]	96
Dem_DTC_FTB_Table[71]	240
Dem_DTC_FTB_Table[72]	96
Dem_DTC_FTB_Table[73]	66
Dem_DTC_FTB_Table[74]	96
Dem_DTC_FTB_Table[75]	130
Dem_DTC_FTB_Table[76]	24

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

Test Case 3: Path Test ✔

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 3.1 3237.00 Cycles
TS 3.2 2512.00 Cycles
TS 3.3 2424.00 Cycles
TS 3.4 680.00 Cycles
TS 3.5 3208.00 Cycles
```

Description

Vector Description:

TS3.1"((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16)==> TRUE &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08)==> FALSE)"
TS3.2(CTCFailedBuf_Cnt_M_Igc[i] == TRUE)==> TRUE
TS3.3"((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16)==> TRUE &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08)==> TRUE)
(DTCFound_Cnt_T_Igc == TRUE)==> TRUE
((DTCStatusNew & D_FAILBITMASK_CNT_U08) == D_FAILBITMASK_CNT_U08)==> FALSE
(CTCFailedBuf_Cnt_M_Igc[i] == TRUE)==> FALSE"
TS3.4"((DTCStatusNew & D_FAILBITMASK_CNT_U08) == D_FAILBITMASK_CNT_U08)==> TRUE
"
TS3.5"((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16)==> FALSE &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08))
(DTCFound_Cnt_T_Igc == TRUE)==> FALSE"

Test Step 3.1 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[0]	0
CTCFailedBuf_Cnt_M_Igc[1]	0
CTCFailedBuf_Cnt_M_Igc[2]	0
CTCFailedBuf_Cnt_M_Igc[3]	0
CTCFailedBuf_Cnt_M_Igc[4]	0
CTCFailedBuf_Cnt_M_Igc[5]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[6]	0
CTCFailedBuf_Cnt_M_Igc[7]	0
CTCFailedBuf_Cnt_M_Igc[8]	0
CTCFailedBuf_Cnt_M_Igc[9]	0
CTCFailedBuf_Cnt_M_Igc[10]	0
CTCFailedBuf_Cnt_M_Igc[11]	0
CTCFailedBuf_Cnt_M_Igc[12]	0
CTCFailedBuf_Cnt_M_Igc[13]	0
CTCFailedBuf_Cnt_M_Igc[14]	0
CTCFailedBuf_Cnt_M_Igc[15]	0
CTCFailedBuf_Cnt_M_Igc[16]	0
CTCFailedBuf_Cnt_M_Igc[17]	0
CTCFailedBuf_Cnt_M_Igc[18]	0
CTCFailedBuf_Cnt_M_Igc[19]	0
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	0
CTCFailedBuf_Cnt_M_Igc[24]	0
CTCFailedBuf_Cnt_M_Igc[25]	0
CTCFailedBuf_Cnt_M_Igc[26]	0
CTCFailedBuf_Cnt_M_Igc[27]	0
CTCFailedBuf_Cnt_M_Igc[28]	0
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_Igc[30]	0
CTCFailedBuf_Cnt_M_Igc[31]	0
CTCFailedBuf_Cnt_M_Igc[32]	0
CTCFailedBuf_Cnt_M_Igc[33]	0
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	0
CTCFailedBuf_Cnt_M_Igc[54]	0
CTCFailedBuf_Cnt_M_Igc[55]	0
CTCFailedBuf_Cnt_M_Igc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_Igc[58]	0
CTCFailedBuf_Cnt_M_Igc[59]	0
CTCFailedBuf_Cnt_M_Igc[60]	0
CTCFailedBuf_Cnt_M_Igc[61]	0
CTCFailedBuf_Cnt_M_Igc[62]	0
CTCFailedBuf_Cnt_M_Igc[63]	0
CTCFailedBuf_Cnt_M_Igc[64]	0
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	0

Name	Input Value
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0

Name	Input Value
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[11]	255
Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem_DTC_FTB_Table[14]	255
Dem_DTC_FTB_Table[15]	255
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
Dem_DTC_FTB_Table[30]	255
Dem_DTC_FTB_Table[31]	255
Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[33]	255
Dem_DTC_FTB_Table[34]	255
Dem_DTC_FTB_Table[35]	255
Dem_DTC_FTB_Table[36]	255
Dem_DTC_FTB_Table[37]	255
Dem_DTC_FTB_Table[38]	255
Dem_DTC_FTB_Table[39]	255
Dem_DTC_FTB_Table[40]	255
Dem_DTC_FTB_Table[41]	255
Dem_DTC_FTB_Table[42]	255
Dem_DTC_FTB_Table[43]	255
Dem_DTC_FTB_Table[44]	255
Dem_DTC_FTB_Table[45]	255
Dem_DTC_FTB_Table[46]	255
Dem_DTC_FTB_Table[47]	255
Dem_DTC_FTB_Table[48]	255
Dem_DTC_FTB_Table[49]	255
Dem_DTC_FTB_Table[50]	255
Dem_DTC_FTB_Table[51]	255
Dem_DTC_FTB_Table[52]	255
Dem_DTC_FTB_Table[53]	255
Dem_DTC_FTB_Table[54]	255
Dem_DTC_FTB_Table[55]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[57]	255
Dem_DTC_FTB_Table[58]	255
Dem_DTC_FTB_Table[59]	255
Dem_DTC_FTB_Table[60]	255
Dem_DTC_FTB_Table[61]	255
Dem_DTC_FTB_Table[62]	255
Dem_DTC_FTB_Table[63]	255
Dem_DTC_FTB_Table[64]	255
Dem_DTC_FTB_Table[65]	255

Name	Input Value
Dem_DTC_FTB_Table[66]	255
Dem_DTC_FTB_Table[67]	255
Dem_DTC_FTB_Table[68]	255
Dem_DTC_FTB_Table[69]	255
Dem_DTC_FTB_Table[70]	255
Dem_DTC_FTB_Table[71]	255
Dem_DTC_FTB_Table[72]	255
Dem_DTC_FTB_Table[73]	255
Dem_DTC_FTB_Table[74]	255
Dem_DTC_FTB_Table[75]	255
Dem_DTC_FTB_Table[76]	255

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[10]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[14]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[17]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[24]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[29]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[32]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[33]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[54]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[55]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[56]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[57]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[58]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[59]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[60]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[61]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[62]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[63]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[64]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	1
CTCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[44]	1
CTCFailedBuf_Cnt_M_Igc[45]	1
CTCFailedBuf_Cnt_M_Igc[46]	1
CTCFailedBuf_Cnt_M_Igc[47]	1
CTCFailedBuf_Cnt_M_Igc[48]	1
CTCFailedBuf_Cnt_M_Igc[49]	1
CTCFailedBuf_Cnt_M_Igc[50]	1
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_Igc[52]	1
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	1
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	1
CTCFailedBuf_Cnt_M_Igc[69]	1
CTCFailedBuf_Cnt_M_Igc[70]	1
CTCFailedBuf_Cnt_M_Igc[71]	1
CTCFailedBuf_Cnt_M_Igc[72]	1
CTCFailedBuf_Cnt_M_Igc[73]	1
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	1
CTCFailedBuf_Cnt_M_Igc[76]	1
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0

Name	Input Value
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0

Name	Input Value
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
Dem_DTC_FTB_Table[71]	0
Dem_DTC_FTB_Table[72]	0
Dem_DTC_FTB_Table[73]	0
Dem_DTC_FTB_Table[74]	0
Dem_DTC_FTB_Table[75]	0
Dem_DTC_FTB_Table[76]	0

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[21]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[22]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[26]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[27]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[28]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[29]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[30]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[35]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[36]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[37]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[38]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[39]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[40]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[41]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[42]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[43]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[44]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[45]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[46]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[47]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[48]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[49]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[50]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[51]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[52]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[66]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[67]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[68]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[69]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[70]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[71]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[72]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[73]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[75]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[76]	1	1	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 3.3 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[9]	0
CTCFailedBuf_Cnt_M_Igc[10]	0
CTCFailedBuf_Cnt_M_Igc[11]	0
CTCFailedBuf_Cnt_M_Igc[12]	0
CTCFailedBuf_Cnt_M_Igc[13]	0
CTCFailedBuf_Cnt_M_Igc[14]	0
CTCFailedBuf_Cnt_M_Igc[15]	0
CTCFailedBuf_Cnt_M_Igc[16]	0
CTCFailedBuf_Cnt_M_Igc[17]	0
CTCFailedBuf_Cnt_M_Igc[18]	0
CTCFailedBuf_Cnt_M_Igc[19]	0
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	0
CTCFailedBuf_Cnt_M_Igc[24]	0
CTCFailedBuf_Cnt_M_Igc[25]	0
CTCFailedBuf_Cnt_M_Igc[26]	0
CTCFailedBuf_Cnt_M_Igc[27]	0
CTCFailedBuf_Cnt_M_Igc[28]	0
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_Igc[30]	0
CTCFailedBuf_Cnt_M_Igc[31]	0
CTCFailedBuf_Cnt_M_Igc[32]	0
CTCFailedBuf_Cnt_M_Igc[33]	0
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	0
CTCFailedBuf_Cnt_M_Igc[54]	0
CTCFailedBuf_Cnt_M_Igc[55]	0
CTCFailedBuf_Cnt_M_Igc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_Igc[58]	0
CTCFailedBuf_Cnt_M_Igc[59]	0
CTCFailedBuf_Cnt_M_Igc[60]	0
CTCFailedBuf_Cnt_M_Igc[61]	0
CTCFailedBuf_Cnt_M_Igc[62]	0
CTCFailedBuf_Cnt_M_Igc[63]	0
CTCFailedBuf_Cnt_M_Igc[64]	0
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0

Name	Input Value
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0

Name	Input Value
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
Dem_DTC_FTB_Table[14]	0
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0

Name	Input Value
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
Dem_DTC_FTB_Table[71]	0
Dem_DTC_FTB_Table[72]	0
Dem_DTC_FTB_Table[73]	0
Dem_DTC_FTB_Table[74]	0
Dem_DTC_FTB_Table[75]	0
Dem_DTC_FTB_Table[76]	0

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[1]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[2]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[3]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[4]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[7]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[8]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[9]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[10]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[11]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[12]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[13]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[14]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[15]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[16]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[17]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[18]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[19]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[24]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[27]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[28]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[29]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[30]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[31]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[32]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[33]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[54]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[55]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[56]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[57]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[58]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[59]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[60]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[61]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[62]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[63]	0	0	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[64]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✔
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✔
CTCFailed_Cnt_M_lgc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 3.4 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	1
CTCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	1
CTCFailedBuf_Cnt_M_lgc[44]	1
CTCFailedBuf_Cnt_M_lgc[45]	1
CTCFailedBuf_Cnt_M_lgc[46]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[47]	1
CTCFailedBuf_Cnt_M_Igc[48]	1
CTCFailedBuf_Cnt_M_Igc[49]	1
CTCFailedBuf_Cnt_M_Igc[50]	1
CTCFailedBuf_Cnt_M_Igc[51]	1
CTCFailedBuf_Cnt_M_Igc[52]	1
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	1
CTCFailedBuf_Cnt_M_Igc[66]	1
CTCFailedBuf_Cnt_M_Igc[67]	1
CTCFailedBuf_Cnt_M_Igc[68]	1
CTCFailedBuf_Cnt_M_Igc[69]	1
CTCFailedBuf_Cnt_M_Igc[70]	1
CTCFailedBuf_Cnt_M_Igc[71]	1
CTCFailedBuf_Cnt_M_Igc[72]	1
CTCFailedBuf_Cnt_M_Igc[73]	1
CTCFailedBuf_Cnt_M_Igc[74]	1
CTCFailedBuf_Cnt_M_Igc[75]	1
CTCFailedBuf_Cnt_M_Igc[76]	1
CTCFailed_Cnt_M_Igc	1
DTC	4294967295
DTCKind	2
DTCStatusNew	255
DTCStatusOld	255
Dem_DTCNumberTable[0]	65535
Dem_DTCNumberTable[1]	65535
Dem_DTCNumberTable[2]	65535
Dem_DTCNumberTable[3]	65535
Dem_DTCNumberTable[4]	65535
Dem_DTCNumberTable[5]	65535
Dem_DTCNumberTable[6]	65535
Dem_DTCNumberTable[7]	65535
Dem_DTCNumberTable[8]	65535
Dem_DTCNumberTable[9]	65535
Dem_DTCNumberTable[10]	65535
Dem_DTCNumberTable[11]	65535
Dem_DTCNumberTable[12]	65535
Dem_DTCNumberTable[13]	65535
Dem_DTCNumberTable[14]	65535
Dem_DTCNumberTable[15]	65535
Dem_DTCNumberTable[16]	65535
Dem_DTCNumberTable[17]	65535
Dem_DTCNumberTable[18]	65535
Dem_DTCNumberTable[19]	65535
Dem_DTCNumberTable[20]	65535
Dem_DTCNumberTable[21]	65535
Dem_DTCNumberTable[22]	65535
Dem_DTCNumberTable[23]	65535
Dem_DTCNumberTable[24]	65535
Dem_DTCNumberTable[25]	65535
Dem_DTCNumberTable[26]	65535
Dem_DTCNumberTable[27]	65535
Dem_DTCNumberTable[28]	65535
Dem_DTCNumberTable[29]	65535
Dem_DTCNumberTable[30]	65535
Dem_DTCNumberTable[31]	65535
Dem_DTCNumberTable[32]	65535
Dem_DTCNumberTable[33]	65535
Dem_DTCNumberTable[34]	65535
Dem_DTCNumberTable[35]	65535
Dem_DTCNumberTable[36]	65535
Dem_DTCNumberTable[37]	65535

Name	Input Value
Dem_DTCNumberTable[38]	65535
Dem_DTCNumberTable[39]	65535
Dem_DTCNumberTable[40]	65535
Dem_DTCNumberTable[41]	65535
Dem_DTCNumberTable[42]	65535
Dem_DTCNumberTable[43]	65535
Dem_DTCNumberTable[44]	65535
Dem_DTCNumberTable[45]	65535
Dem_DTCNumberTable[46]	65535
Dem_DTCNumberTable[47]	65535
Dem_DTCNumberTable[48]	65535
Dem_DTCNumberTable[49]	65535
Dem_DTCNumberTable[50]	65535
Dem_DTCNumberTable[51]	65535
Dem_DTCNumberTable[52]	65535
Dem_DTCNumberTable[53]	65535
Dem_DTCNumberTable[54]	65535
Dem_DTCNumberTable[55]	65535
Dem_DTCNumberTable[56]	65535
Dem_DTCNumberTable[57]	65535
Dem_DTCNumberTable[58]	65535
Dem_DTCNumberTable[59]	65535
Dem_DTCNumberTable[60]	65535
Dem_DTCNumberTable[61]	65535
Dem_DTCNumberTable[62]	65535
Dem_DTCNumberTable[63]	65535
Dem_DTCNumberTable[64]	65535
Dem_DTCNumberTable[65]	65535
Dem_DTCNumberTable[66]	65535
Dem_DTCNumberTable[67]	65535
Dem_DTCNumberTable[68]	65535
Dem_DTCNumberTable[69]	65535
Dem_DTCNumberTable[70]	65535
Dem_DTCNumberTable[71]	65535
Dem_DTCNumberTable[72]	65535
Dem_DTCNumberTable[73]	65535
Dem_DTCNumberTable[74]	65535
Dem_DTCNumberTable[75]	65535
Dem_DTCNumberTable[76]	65535
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[11]	255
Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem_DTC_FTB_Table[14]	255
Dem_DTC_FTB_Table[15]	255
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
Dem_DTC_FTB_Table[30]	255
Dem_DTC_FTB_Table[31]	255
Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[33]	255

Name	Input Value
Dem_DTC_FTB_Table[34]	255
Dem_DTC_FTB_Table[35]	255
Dem_DTC_FTB_Table[36]	255
Dem_DTC_FTB_Table[37]	255
Dem_DTC_FTB_Table[38]	255
Dem_DTC_FTB_Table[39]	255
Dem_DTC_FTB_Table[40]	255
Dem_DTC_FTB_Table[41]	255
Dem_DTC_FTB_Table[42]	255
Dem_DTC_FTB_Table[43]	255
Dem_DTC_FTB_Table[44]	255
Dem_DTC_FTB_Table[45]	255
Dem_DTC_FTB_Table[46]	255
Dem_DTC_FTB_Table[47]	255
Dem_DTC_FTB_Table[48]	255
Dem_DTC_FTB_Table[49]	255
Dem_DTC_FTB_Table[50]	255
Dem_DTC_FTB_Table[51]	255
Dem_DTC_FTB_Table[52]	255
Dem_DTC_FTB_Table[53]	255
Dem_DTC_FTB_Table[54]	255
Dem_DTC_FTB_Table[55]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[57]	255
Dem_DTC_FTB_Table[58]	255
Dem_DTC_FTB_Table[59]	255
Dem_DTC_FTB_Table[60]	255
Dem_DTC_FTB_Table[61]	255
Dem_DTC_FTB_Table[62]	255
Dem_DTC_FTB_Table[63]	255
Dem_DTC_FTB_Table[64]	255
Dem_DTC_FTB_Table[65]	255
Dem_DTC_FTB_Table[66]	255
Dem_DTC_FTB_Table[67]	255
Dem_DTC_FTB_Table[68]	255
Dem_DTC_FTB_Table[69]	255
Dem_DTC_FTB_Table[70]	255
Dem_DTC_FTB_Table[71]	255
Dem_DTC_FTB_Table[72]	255
Dem_DTC_FTB_Table[73]	255
Dem_DTC_FTB_Table[74]	255
Dem_DTC_FTB_Table[75]	255
Dem_DTC_FTB_Table[76]	255

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[21]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[22]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[29]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[30]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[32]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[34]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[35]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[36]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[37]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[38]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[39]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[40]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[41]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[42]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[43]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[44]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[45]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[46]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[47]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[48]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[49]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[50]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[51]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[52]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[65]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[66]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[67]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[68]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[69]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[70]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[71]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[72]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[73]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[75]	1	1	✔
CTCFailedBuf_Cnt_M_lgc[76]	1	1	✔
CTCFailed_Cnt_M_lgc	1	1	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1

Name	Input Value
CTCFailedBuf_Cnt_M_Igc[12]	1
CTCFailedBuf_Cnt_M_Igc[13]	1
CTCFailedBuf_Cnt_M_Igc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_Igc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_Igc[18]	1
CTCFailedBuf_Cnt_M_Igc[19]	1
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	0
CTCFailedBuf_Cnt_M_Igc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_Igc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_Igc[30]	1
CTCFailedBuf_Cnt_M_Igc[31]	1
CTCFailedBuf_Cnt_M_Igc[32]	1
CTCFailedBuf_Cnt_M_Igc[33]	1
CTCFailedBuf_Cnt_M_Igc[34]	0
CTCFailedBuf_Cnt_M_Igc[35]	0
CTCFailedBuf_Cnt_M_Igc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_Igc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_Igc[40]	0
CTCFailedBuf_Cnt_M_Igc[41]	0
CTCFailedBuf_Cnt_M_Igc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_Igc[44]	0
CTCFailedBuf_Cnt_M_Igc[45]	0
CTCFailedBuf_Cnt_M_Igc[46]	0
CTCFailedBuf_Cnt_M_Igc[47]	0
CTCFailedBuf_Cnt_M_Igc[48]	0
CTCFailedBuf_Cnt_M_Igc[49]	0
CTCFailedBuf_Cnt_M_Igc[50]	0
CTCFailedBuf_Cnt_M_Igc[51]	0
CTCFailedBuf_Cnt_M_Igc[52]	0
CTCFailedBuf_Cnt_M_Igc[53]	1
CTCFailedBuf_Cnt_M_Igc[54]	1
CTCFailedBuf_Cnt_M_Igc[55]	1
CTCFailedBuf_Cnt_M_Igc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_Igc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_Igc[60]	1
CTCFailedBuf_Cnt_M_Igc[61]	1
CTCFailedBuf_Cnt_M_Igc[62]	1
CTCFailedBuf_Cnt_M_Igc[63]	0
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_Igc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_Igc[68]	0
CTCFailedBuf_Cnt_M_Igc[69]	0
CTCFailedBuf_Cnt_M_Igc[70]	0
CTCFailedBuf_Cnt_M_Igc[71]	0
CTCFailedBuf_Cnt_M_Igc[72]	0
CTCFailedBuf_Cnt_M_Igc[73]	0
CTCFailedBuf_Cnt_M_Igc[74]	0
CTCFailedBuf_Cnt_M_Igc[75]	0
CTCFailedBuf_Cnt_M_Igc[76]	0
CTCFailed_Cnt_M_Igc	0
DTC	0
DTCKind	1
DTCStatusNew	148
DTCStatusOld	39
Dem_DTCNumberTable[0]	181
Dem_DTCNumberTable[1]	1
Dem_DTCNumberTable[2]	41

Name	Input Value
Dem_DTCNumberTable[3]	22
Dem_DTCNumberTable[4]	24
Dem_DTCNumberTable[5]	254
Dem_DTCNumberTable[6]	209
Dem_DTCNumberTable[7]	209
Dem_DTCNumberTable[8]	181
Dem_DTCNumberTable[9]	1
Dem_DTCNumberTable[10]	209
Dem_DTCNumberTable[11]	128
Dem_DTCNumberTable[12]	1
Dem_DTCNumberTable[13]	209
Dem_DTCNumberTable[14]	181
Dem_DTCNumberTable[15]	1
Dem_DTCNumberTable[16]	1
Dem_DTCNumberTable[17]	209
Dem_DTCNumberTable[18]	33
Dem_DTCNumberTable[19]	181
Dem_DTCNumberTable[20]	1
Dem_DTCNumberTable[21]	209
Dem_DTCNumberTable[22]	181
Dem_DTCNumberTable[23]	41
Dem_DTCNumberTable[24]	22
Dem_DTCNumberTable[25]	24
Dem_DTCNumberTable[26]	254
Dem_DTCNumberTable[27]	1
Dem_DTCNumberTable[28]	181
Dem_DTCNumberTable[29]	1
Dem_DTCNumberTable[30]	181
Dem_DTCNumberTable[31]	181
Dem_DTCNumberTable[32]	1
Dem_DTCNumberTable[33]	1
Dem_DTCNumberTable[34]	181
Dem_DTCNumberTable[35]	1
Dem_DTCNumberTable[36]	181
Dem_DTCNumberTable[37]	181
Dem_DTCNumberTable[38]	181
Dem_DTCNumberTable[39]	1
Dem_DTCNumberTable[40]	1
Dem_DTCNumberTable[41]	41
Dem_DTCNumberTable[42]	22
Dem_DTCNumberTable[43]	24
Dem_DTCNumberTable[44]	254
Dem_DTCNumberTable[45]	209
Dem_DTCNumberTable[46]	181
Dem_DTCNumberTable[47]	1
Dem_DTCNumberTable[48]	22
Dem_DTCNumberTable[49]	181
Dem_DTCNumberTable[50]	1
Dem_DTCNumberTable[51]	181
Dem_DTCNumberTable[52]	181
Dem_DTCNumberTable[53]	1
Dem_DTCNumberTable[54]	22
Dem_DTCNumberTable[55]	209
Dem_DTCNumberTable[56]	181
Dem_DTCNumberTable[57]	1
Dem_DTCNumberTable[58]	181
Dem_DTCNumberTable[59]	209
Dem_DTCNumberTable[60]	181
Dem_DTCNumberTable[61]	1
Dem_DTCNumberTable[62]	22
Dem_DTCNumberTable[63]	41
Dem_DTCNumberTable[64]	22
Dem_DTCNumberTable[65]	24
Dem_DTCNumberTable[66]	254
Dem_DTCNumberTable[67]	181
Dem_DTCNumberTable[68]	181
Dem_DTCNumberTable[69]	1
Dem_DTCNumberTable[70]	22
Dem_DTCNumberTable[71]	209
Dem_DTCNumberTable[72]	22
Dem_DTCNumberTable[73]	41
Dem_DTCNumberTable[74]	22
Dem_DTCNumberTable[75]	24

Name	Input Value
Dem_DTCNumberTable[76]	254
Dem_DTC_FTB_Table[0]	245
Dem_DTC_FTB_Table[1]	151
Dem_DTC_FTB_Table[2]	199
Dem_DTC_FTB_Table[3]	160
Dem_DTC_FTB_Table[4]	30
Dem_DTC_FTB_Table[5]	136
Dem_DTC_FTB_Table[6]	178
Dem_DTC_FTB_Table[7]	178
Dem_DTC_FTB_Table[8]	245
Dem_DTC_FTB_Table[9]	151
Dem_DTC_FTB_Table[10]	178
Dem_DTC_FTB_Table[11]	31
Dem_DTC_FTB_Table[12]	151
Dem_DTC_FTB_Table[13]	178
Dem_DTC_FTB_Table[14]	245
Dem_DTC_FTB_Table[15]	151
Dem_DTC_FTB_Table[16]	151
Dem_DTC_FTB_Table[17]	178
Dem_DTC_FTB_Table[18]	234
Dem_DTC_FTB_Table[19]	245
Dem_DTC_FTB_Table[20]	151
Dem_DTC_FTB_Table[21]	178
Dem_DTC_FTB_Table[22]	245
Dem_DTC_FTB_Table[23]	199
Dem_DTC_FTB_Table[24]	160
Dem_DTC_FTB_Table[25]	30
Dem_DTC_FTB_Table[26]	136
Dem_DTC_FTB_Table[27]	151
Dem_DTC_FTB_Table[28]	245
Dem_DTC_FTB_Table[29]	151
Dem_DTC_FTB_Table[30]	245
Dem_DTC_FTB_Table[31]	245
Dem_DTC_FTB_Table[32]	151
Dem_DTC_FTB_Table[33]	151
Dem_DTC_FTB_Table[34]	245
Dem_DTC_FTB_Table[35]	151
Dem_DTC_FTB_Table[36]	245
Dem_DTC_FTB_Table[37]	245
Dem_DTC_FTB_Table[38]	245
Dem_DTC_FTB_Table[39]	151
Dem_DTC_FTB_Table[40]	151
Dem_DTC_FTB_Table[41]	199
Dem_DTC_FTB_Table[42]	160
Dem_DTC_FTB_Table[43]	30
Dem_DTC_FTB_Table[44]	136
Dem_DTC_FTB_Table[45]	178
Dem_DTC_FTB_Table[46]	245
Dem_DTC_FTB_Table[47]	151
Dem_DTC_FTB_Table[48]	160
Dem_DTC_FTB_Table[49]	245
Dem_DTC_FTB_Table[50]	151
Dem_DTC_FTB_Table[51]	245
Dem_DTC_FTB_Table[52]	245
Dem_DTC_FTB_Table[53]	151
Dem_DTC_FTB_Table[54]	160
Dem_DTC_FTB_Table[55]	178
Dem_DTC_FTB_Table[56]	245
Dem_DTC_FTB_Table[57]	151
Dem_DTC_FTB_Table[58]	245
Dem_DTC_FTB_Table[59]	178
Dem_DTC_FTB_Table[60]	245
Dem_DTC_FTB_Table[61]	151
Dem_DTC_FTB_Table[62]	160
Dem_DTC_FTB_Table[63]	199
Dem_DTC_FTB_Table[64]	160
Dem_DTC_FTB_Table[65]	30
Dem_DTC_FTB_Table[66]	136
Dem_DTC_FTB_Table[67]	245
Dem_DTC_FTB_Table[68]	245
Dem_DTC_FTB_Table[69]	151
Dem_DTC_FTB_Table[70]	160
Dem_DTC_FTB_Table[71]	178

Name	Input Value
Dem_DTC_FTB_Table[72]	160
Dem_DTC_FTB_Table[73]	199
Dem_DTC_FTB_Table[74]	160
Dem_DTC_FTB_Table[75]	30
Dem_DTC_FTB_Table[76]	136

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[0]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[1]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[2]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[3]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[4]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[5]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[6]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[7]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[8]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[9]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[10]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[11]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[12]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[13]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[14]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[15]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[16]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[17]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[18]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[19]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[20]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[21]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[22]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[23]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[24]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[25]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[26]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[27]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[28]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[29]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[30]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[31]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[32]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[33]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[34]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[35]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[36]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[37]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[38]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[39]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[40]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[41]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[42]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[43]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[44]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[45]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[46]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[48]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[49]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[50]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[51]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[52]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[53]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[54]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[56]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[58]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[59]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[60]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[61]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[62]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[63]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[64]	1	1	✔
CTCFailedBuf_Cnt_M_Igc[65]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[66]	0	0	✔

TEST DETAILS REPORT

DemIf_DTCStatusChanged

2018-04-10, 18:44:44+0530

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_Igc[67]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[68]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[69]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[70]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[71]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[72]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[73]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[74]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[75]	0	0	✔
CTCFailedBuf_Cnt_M_Igc[76]	0	0	✔
CTCFailed_Cnt_M_Igc	0	0	✔
DemIf_DTCStatusChanged()	0	0	✔
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc(data)	0	0	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_Igc	1	✔

TEST DETAILS REPORT

DemIf_VehSpdControl

2018-04-10, 18:50:29+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_VehSpdControl

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 12.00 Cycles
TS 1.2 12.00 Cycles
```

Description

Vector Description:

TS 1.1 Enable_Cnt_T_lgc=>Min
TS 1.2 Enable_Cnt_T_lgc=>Max

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
Enable_Cnt_T_lgc	0

Name	Actual Value	Expected Value	Result
VehSpdControl_Cnt_M_lgc	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
Enable_Cnt_T_lgc	1

Name	Actual Value	Expected Value	Result
VehSpdControl_Cnt_M_lgc	1	1	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

TEST DETAILS REPORT

DemIf_SetOperationCycleState

2018-04-10, 18:49:59+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_SetOperationCycleState

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

Comments/Description/Specification

Name	Text
Module 'DemIf'	**********Unit Test Description********** Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_DemIf.c Code File(s) Version:3 Module Design Document:DemIf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 502.00 Cycles
```

Description Vector Description:

TS 1.1 Check for Call Trace

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
NxtrCycleState	*none*
NxtrOperationCycleId	*none*

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
Dem_SetOperationCycleState	1	Dem_SetOperationCycleState	1	✔

TEST DETAILS REPORT

DemIf_RestartDem

2018-04-10, 18:48:23+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_RestartDem

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

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Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Range Test ✔

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 500.00 Cycles
```

Description Vector Description:

TS1.1 Only Call trace is checked

Test Step 1.1 (Repeat Count = 1) ✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
Dem_Init	1	Dem_Init	1	✔

TEST DETAILS REPORT

DemIf_CheckVoltageRange

2018-04-10, 18:40:20+0530

Project	DemIf
Module	DemIf
Test Object	DemIf_CheckVoltageRange

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	2
Successful	2
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DemIf\src\Ap_DemIf.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DemIf\utp\contract -I$(PROJECTROOT)\DemIf\utp\contract\Ap_DemIf -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include

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Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Attributes

Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 76.00 Cycles
TS 1.2 97.00 Cycles
```

Description

Vector Description:

TS 1.1 Shortest Execution Path=>if ((voltage_Volt_T_f32 < min_Volt_T_f32)=>False || (max_Volt_T_f32 < voltage_Volt_T_f32)=>False)
TS 1.2 Longest Execution Path=>if ((voltage_Volt_T_f32 < min_Volt_T_f32)=>True || (max_Volt_T_f32 < voltage_Volt_T_f32))

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	0
min_Volt_T_f32	0
time_cnt_T_u32	0
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	0

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	0.426099986
min_Volt_T_f32	12.3562002
time_cnt_T_u32	1452352
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	0

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1452352	1452352	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 2: Range Test

Specification

```
Performance Metrics (With "None"
Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 76.00 Cycles
TS 2.2 76.00 Cycles
TS 2.3 97.00 Cycles
TS 2.4 101.00 Cycles
TS 2.5 78.00 Cycles
TS 2.6 78.00 Cycles
TS 2.7 99.00 Cycles
TS 2.8 99.00 Cycles
TS 2.9 78.00 Cycles
TS 2.10 96.00 Cycles
TS 2.11 76.00 Cycles
TS 2.12 97.00 Cycles
TS 2.13 101.00 Cycles
TS 2.14 99.00 Cycles
```

Description

Vector Description:

TS 1.1All Min
TS 1.2All Max
TS 1.3voltage_Volt_T_f32=>Min
TS 1.4voltage_Volt_T_f32=Max
TS 1.5voltage_Volt_T_f32=>Pos
TS 1.6min_Volt_T_f32=>Min
TS 1.7min_Volt_T_f32=>Max
TS 1.8min_Volt_T_f32=>Pos
TS 1.9max_Volt_T_f32=>Min
TS 1.10max_Volt_T_f32=>Max
TS 1.11max_Volt_T_f32=>Pos
TS 1.12time_cnt_T_u32=>Min
TS 1.13time_cnt_T_u32=>Max
TS 1.14time_cnt_T_u32=>Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	0
min_Volt_T_f32	0
time_cnt_T_u32	0
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	0

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	31
min_Volt_T_f32	31
time_cnt_T_u32	4294967295
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	31

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.3 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	0.426099986
min_Volt_T_f32	12.3562002
time_cnt_T_u32	1452352
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	0

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1452352	1452352	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.4 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	0.125400007
min_Volt_T_f32	8.41409969
time_cnt_T_u32	2151351
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	31

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	2151351	2151351	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.5 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	9.11979961
min_Volt_T_f32	5.12400007
time_cnt_T_u32	1241
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	12.1353998

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1241	1241	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.6 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	5.07380009
min_Volt_T_f32	0
time_cnt_T_u32	1151336
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	19.5648003

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1151336	1151336	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.7 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	1.73090005
min_Volt_T_f32	31
time_cnt_T_u32	52
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	12.3786001

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	52	52	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
max_Volt_T_f32	2.5236001
min_Volt_T_f32	8.14509964
time_cnt_T_u32	78073
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	0.0706999972

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	78073	78073	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
max_Volt_T_f32	0
min_Volt_T_f32	0.262400001
time_cnt_T_u32	3424
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	1.22490001

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
max_Volt_T_f32	31
min_Volt_T_f32	9.23530006
time_cnt_T_u32	857634
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	12.9097004

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
max_Volt_T_f32	14.2140999
min_Volt_T_f32	1.46340001
time_cnt_T_u32	352624
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	10.7594995

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.12 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	16.8927994
min_Volt_T_f32	26.1240997
time_cnt_T_u32	0
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	0

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.13 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	12.0332003
min_Volt_T_f32	12.1252003
time_cnt_T_u32	4294967295
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	21.4778004

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	4294967295	4294967295	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.14 (Repeat Count = 1)

Name	Input Value
max_Volt_T_f32	0.977800012
min_Volt_T_f32	3.65319991
time_cnt_T_u32	1524114
timer_cnt_T_u32	target_timer_cnt_T_u32
voltage_Volt_T_f32	1.12510002

Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1524114	1524114	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔