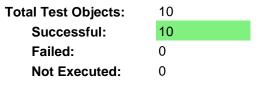
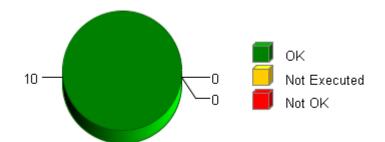


#### **Summary**

## **Overall Test Object Results (including Coverage)**



**Date:** 2018-04-10 **Time:** 18:51:13+0530



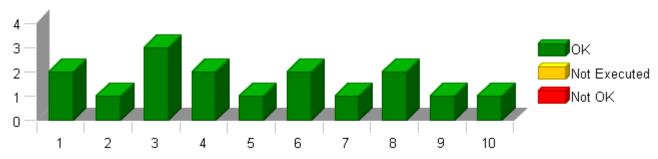
## **Selected Project Items**

Test Collection "CBD\_UnitTest"

#### **Used Test Environments**

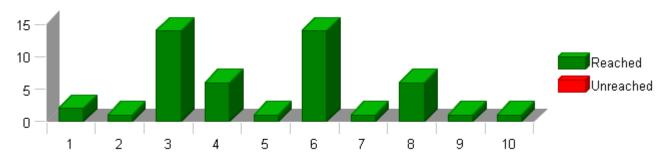
TI TMS 570 PLS UDE (Default)

## **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

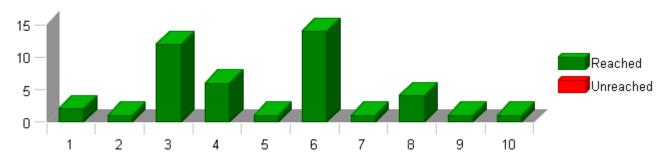
## Statement (C0) Coverage: Total Statements for Each Test Object



The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

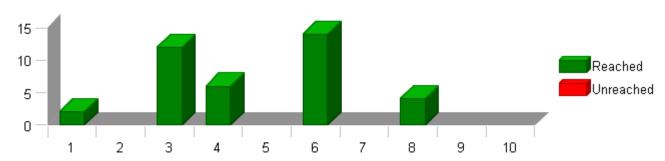


## Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

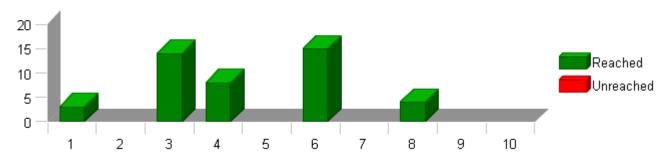
## **Decision Coverage: Total Decision Outcomes for Each Test Object**



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

## MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

## **TEST OVERVIEW REPORT**

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## **Test Object List**

Project Demlf

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	Test Cases Result
	Demlf	100 %	100 %	100 %	100 %	16 of 16 passed
	CBD_UnitTest	100 %	100 %	100 %	100 %	16 of 16 passed
	Demlf	100 %	100 %	100 %	100 %	16 of 16 passed
1	Demlf_CheckVoltageRange	100 %	100 %	100 %	100 %	2 of 2 passed
2	Demlf_DemShutdown	100 %	100 %	-	-	1 of 1 passed
3	Demlf_DTCStatusChanged	100 %	100 %	100 %	100 %	3 of 3 passed
4	Demlf EvaluateLogicalCondition	100 %	100 %	100 %	100 %	2 of 2 passed
5	Demlf Init	100 %	100 %	-	-	1 of 1 passed
6	Demlf Per	100 %	100 %	100 %	100 %	2 of 2 passed
7	Demlf_RestartDem	100 %	100 %	-	-	1 of 1 passed
8	<u>Demlf_SetEventStatus</u>	100 %	100 %	100 %	100 %	2 of 2 passed
9	Demlf SetOperationCycleState	100 %	100 %	-	-	1 of 1 passed
10	Demlf_VehSpdControl	100 %	100 %	-	-	1 of 1 passed

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 Project
 Demlf

 Module
 Demlf

 Test Object
 Demlf\_SetEventStatus

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	2	
Successful	2	~
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlflutp\contract -I\$(PROJECTROOT)\Demlflutp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes					
Name	Value				
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5				
Float Precision	9				
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj				
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src				
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd				
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl				
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4				
Time Unit	cycles				
Timer Enabled	false				
Timer Prescale	0				
Timer Resolution	1				
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg				

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Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### Test Case 1: Metric Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 564.00 Cycles TS 1.2 553.00 Cycles

Description Vector Description:

TS 1.1 Shortest Execution Path=>if (RTE\_CONST\_NTC\_STATUS\_FAILED == EventStatus)=>False TS 1.2 Longest Execution Path=>if (RTE\_CONST\_NTC\_STATUS\_FAILED == EventStatus)=>True if (0u == (CTClnhibitionMask\_Cnt\_M\_u08[EventId] & CTClnhibitionState\_Cnt\_M\_u08))=>True

Test Step 1.1 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	

Test Step 1.2 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~	



#### Test Case 2: Range Test

#### Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 579.00 Cycles
TS 2.2 550.00 Cycles
TS 2.3 567.00 Cycles
TS 2.4 536.00 Cycles
TS 2.5 518.00 Cycles
TS 2.6 536.00 Cycles
TS 2.7 536.00 Cycles
TS 2.7 536.00 Cycles
TS 2.9 536.00 Cycles
TS 2.9 536.00 Cycles
TS 2.10 536.00 Cycles
TS 2.11 518.00 Cycles
TS 2.12 536.00 Cycles
TS 2.12 536.00 Cycles
TS 2.13 536.00 Cycles
TS 2.14 31.00 Cycles
TS 2.14 31.00 Cycles

#### **Description** Vector Description:

TS 2.1All Min
TS 2.2All Max
TS 2.3EventId=>Min
TS 2.4EventId=>Max
TS 2.5EventId=>Pos
TS 2.5EventStatus=>Min
TS 2.7EventStatus=>Max
TS 2.8EventStatus=>Pos
TS 2.0EventStatus=>Pos

TS 2.7EventStatus=>Max
TS 2.7EventStatus=>Max
TS 2.8EventStatus=>Pos
TS 2.9Dem\_SetEventStatus=>Min
TS 2.10Dem\_SetEventStatus=>Max
TS 2.11Dem\_SetEventStatus=>Mid

Test Step 2.1 (Repeat Count = 1)			
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	0		
Name	Actual Value	Expected Value	Result
Demlf SetEventStatus()	0	0	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem SetEventStatus	1	Dem SetEventStatus	1	~

Test Step 2.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	255		
Dem_SetEventStatus()	255		
EventId	255		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	255	255	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.3 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	0		
Dem_SetEventStatus()	0		
EventId	0		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~



Test Step 2.4 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	231		
Dem_SetEventStatus()	13		
EventId	255		
EventStatus	2		
Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	13	13	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.5 (Repeat Count = 1)			V
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	12		
Dem_SetEventStatus()	127		
EventId	90		
EventStatus	1		
Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	127	127	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

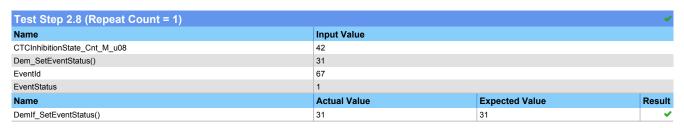
Test Step 2.6 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	43		
Dem_SetEventStatus()	45		
EventId	34		
EventStatus	0		
Name	Actual Value	Expected Value	Result
DemIf_SetEventStatus()	45	45	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.7 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	224		
Dem_SetEventStatus()	116		
EventId	56		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	116	116	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~





Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.9 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	123		
Dem_SetEventStatus()	0		
EventId	12		
EventStatus	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	•

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Resu	t
Dem_SetEventStatus	1	Dem_SetEventStatus	1		

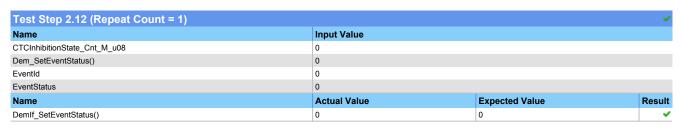
Test Step 2.10 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	124		
Dem_SetEventStatus()	255		
EventId	45		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	255	255	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.11 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	31		
Dem_SetEventStatus()	113		
EventId	84		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	113	113	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~





Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Dem SetEventStatus	1	Dem SetEventStatus	1	~

Test Step 2.13 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	255		
Dem_SetEventStatus()	21		
EventId	255		
EventStatus	3		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	21	21	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.14 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
CTCInhibitionState_Cnt_M_u08	128		
Dem_SetEventStatus()	2		
EventId	1		
EventStatus	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

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 Project
 Demlf

 Module
 Demlf

 Test Object
 Demlf\_DemShutdown

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note 1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

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Demlf\_DemShutdown

## Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 536.00 Cycles

Description Vector Description:

TS1.1 Only Call trace is checked

## Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_Shutdown	1	Dem_Shutdown	1	~

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DemIf\_Init

Project	Demlf
Module	Demlf
Test Object	Demlf_Init

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	✓
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demlf'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 558.00 Cycles TS 1.2 558.00 Cycles TS 1.3 558.00 Cycles

Description Vector Description:

TS 1.1 Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Min TS 1.2 Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Max TS 1.3 Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Pos

Test Step 1.1 (Repeat Count = 1)			~
Name	Input Value		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_Ge	etSystemTime_mS_u32_CurrentTime	
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	0		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	•
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	•
CTCInhibitionEsc_Cnt_M_u32	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~

Test Step 1.2 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_Ge	etSystemTime_mS_u32_CurrentTime	
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionBsi_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	•
CTCInhibitionCmm_Cnt_M_u32	4294967295	4294967295	<b>✓</b>
CTCInhibitionEsc Cnt M u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~

Test Sten 4.2 (Beneat Count = 4)			-0
Test Step 1.3 (Repeat Count = 1)			×
Name	Input Value		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_Ge	etSystemTime_mS_u32_CurrentTime	
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	200		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	200	200	~
CTCInhibitionBsi_Cnt_M_u32	200	200	~
CTCInhibitionCav_Cnt_M_u32	200	200	~
CTCInhibitionCmm_Cnt_M_u32	200	200	~
CTCInhibitionEsc Cnt M u32	200	200	-

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Call Ap Demlf SystemTime GetSystemTime mS u32	1	Rte Call Ap Demlf SystemTime GetSystemTime mS u32	1	~

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Project	Demlf
Module	Demlf
Test Object	Demlf_Per

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	2	
Successful	2	~
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlflutp\contract -I\$(PROJECTROOT)\Demlflutp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
/lodule 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision	9	
InitObjDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj</pre>	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl	
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4	
Time Unit	cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution	1	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	

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Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Test Step 1.1 (Repeat Count = 1) Name	Input Value		
	•	OD 057 : 1	
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_		- JT:
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	· · · - ·	Time_DtrmnElapsedTime_mS_u16_Elapse	
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)		Time_GetSystemTime_mS_u32_CurrentTi	ime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	0		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16			
k_AasActvVBattMax_Volt_f32	0		
k_AasActvVBattMin_Volt_f32	0		
k_BsiActvTimeout_mS_u16	0		
k_BsiActvVBattMax_Volt_f32	0		
k_BsiActvVBattMin_Volt_f32	0		
k_CavActvTimeout_mS_u16	0		
k_CavActvVBattMax_Volt_f32	0		
k_CavActvVBattMin_Volt_f32	0		
k_CmmActvTimeout_mS_u16	0		
k_CmmActvVBattMax_Volt_f32	0		
k_CmmActvVBattMin_Volt_f32		0	
k_EscActvTimeout_mS_u16	0		
k_EscActvVBattMax_Volt_f32		0	
k_EscActvVBattMin_Volt_f32		0	
target_Demlf_Per_BatteryVoltage_Volt_f32.value		0	
target_Demlf_Per_BusOff_Cnt_lgc.value		0	
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapsed			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime_ms_u32_CurrentTime_m			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_V	olt_f32	
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegra	tion_Cnt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas_Cnt_M_u32	0	0	
CTCInhibitionBsi_Cnt_M_u32	0	0	•
CTCInhibitionCav_Cnt_M_u32	0	0	
CTCInhibitionCmm_Cnt_M_u32	0	0	
CTCInhibitionEsc_Cnt_M_u32	0	0	
CTCInhibitionState Cnt M u08	0	0	



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	•
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	•
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>

Test Step 1.2 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GE	T_signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_Dt	rmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_G	etSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	19.9340992		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	0		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3633311787		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cn	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	3633311787	3633311787	~
CTCInhibitionBsi Cnt M u32	3633311787	3633311787	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	3633311787	3633311787	~
CTCInhibitionCmm_Cnt_M_u32	3633311787	3633311787	<b>✓</b>
	3633311787	3633311787	~
CTCInhibitionState_Cnt_M_u08	223	223	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>



#### **Test Case 2: Range Test**

#### Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

CPU Cycles:

TS 2.1 4063.00 Cycles
TS 2.2 4089.00 Cycles
TS 2.3 4067.00 Cycles
TS 2.3 4067.00 Cycles
TS 2.5 4067.00 Cycles
TS 2.5 4067.00 Cycles
TS 2.6 4067.00 Cycles
TS 2.7 4067.00 Cycles
TS 2.8 4067.00 Cycles
TS 2.10 4067.00 Cycles
TS 2.11 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.15 4067.00 Cycles
TS 2.14 4067.00 Cycles
TS 2.14 4051.00 Cycles
TS 2.15 4067.00 Cycles
TS 2.16 4029.00 Cycles
TS 2.17 4051.00 Cycles
TS 2.18 4051.00 Cycles
TS 2.21 4059.00 Cycles
TS 2.22 4051.00 Cycles
TS 2.23 4029.00 Cycles
TS 2.24 4051.00 Cycles
TS 2.25 4029.00 Cycles
TS 2.26 4051.00 Cycles
TS 2.27 4029.00 Cycles
TS 2.28 4029.00 Cycles
TS 2.29 4051.00 Cycles
TS 2.28 4029.00 Cycles
TS 2.29 4051.00 Cycles
TS 2.30 4029.00 Cycles
TS 2.31 4029.00 Cycles
TS 2.31 4029.00 Cycles
TS 2.32 4051.00 Cycles
TS 2.32 4051.00 Cycles

#### Description

#### Vector Description:

TS 2.1 All Min TS 2.2All Max

TS 2.2All Max
TS 2.3Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Min
TS 2.4Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Max
TS 2.5Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Pos
TS 2.6Demlf\_Per\_BatteryVoltage\_Volt\_f32=>Pos
TS 2.6Demlf\_Per\_ElectronicIntegration\_Cnt\_Igc=>Min
TS 2.7Demlf\_Per\_ElectronicIntegration\_Cnt\_Igc=>Max
TS 2.8Demlf\_Per\_BusOff\_Cnt\_Igc=>Min
TS 2.9Demlf\_Per\_BusOff\_Cnt\_Igc=>Max
TS 2.10Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Min
TS 2.11Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Max
TS 2.12Rte\_Call\_SystemTime\_GetSystemTime\_mS\_u32=>Pos
TS 2.13Rte\_Call\_SystemTime\_DtrmnElapsedTime\_mS\_u16=>Min
TS 2.14Rte\_Call\_SystemTime\_DtrmnElapsedTime\_mS\_u16=>Max
TS 2.15Rte\_Call\_SystemTime\_DtrmnElapsedTime\_mS\_u16=>Pos
TS 2.16VehSpdControl\_Cnt\_M\_Igc=>Min

TS 2.16VehSpdControl\_Cnt\_M\_lgc=>Min TS 2.17VehSpdControl\_Cnt\_M\_lgc=>Max TS 2.18k\_EscActvTimeout\_mS\_u16=>Min

TS 2.19k\_EscActvTimeout\_mS\_u16=>Max TS 2.20k\_EscActvTimeout\_mS\_u16=>Pos TS 2.21k\_BsiActvTimeout\_mS\_u16=>Min

TS 2.22k\_BsiActvTimeout\_mS\_u16=>Max TS 2.23k\_BsiActvTimeout\_mS\_u16=>Pos TS 2.24k\_CavActvTimeout\_mS\_u16=>Min

TS 2.25k\_CavActvTimeout\_mS\_u16=>Max

TS 2.26k\_CavActvTimeout\_mS\_u16=>Pos TS 2.27k\_AasActvTimeout\_mS\_u16=>Min

TS 2.28k\_AasActvTimeout\_mS\_u16=>Max

TS 2.29k\_AasActvTimeout\_mS\_u16=>Pos TS 2.30k\_CmmActvTimeout\_mS\_u16=>Min

TS 2.31k\_CmmActvTimeout\_mS\_u16=>Max TS 2.32k\_CmmActvTimeout\_mS\_u16=>Pos

Test Step 2.1 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	0
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	0
k_AasActvVBattMax_Volt_f32	0
k_AasActvVBattMin_Volt_f32	0
k_BsiActvTimeout_mS_u16	0
k_BsiActvVBattMax_Volt_f32	0
k_BsiActvVBattMin_Volt_f32	0
k_CavActvTimeout_mS_u16	0
k_CavActvVBattMax_Volt_f32	0
k_CavActvVBattMin_Volt_f32	0
k_CmmActvTimeout_mS_u16	0
k_CmmActvVBattMax_Volt_f32	0

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Name	Input Value		
k_CmmActvVBattMin_Volt_f32	0		
k_EscActvTimeout_mS_u16	0		
k_EscActvVBattMax_Volt_f32	0		
k_EscActvVBattMin_Volt_f32	0		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_DemIf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	m 0		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt	t_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	~
CTCInhibitionEsc_Cnt_M_u32	0	0	~
CTCInhibitionState_Cnt_M_u08	0	0	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>
DemIf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~



Test Step 2.2 (Repeat Count = 1)	In and Males		
Name	Input Value	- OD OFT signal	
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition		a alTimo
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)		mTime_DtrmnElapsedTime_mS_u16_Elaps	
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)		mTime_GetSystemTime_mS_u32_CurrentT	ime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4		
VehSpdControl_Cnt_M_lgc	1		
k_AasActvTimeout_mS_u16	65535		
k_AasActvVBattMax_Volt_f32	31		
k_AasActvVBattMin_Volt_f32	31		
k_BsiActvTimeout_mS_u16	65535		
k_BsiActvVBattMax_Volt_f32	31		
k_BsiActvVBattMin_Volt_f32	31		
k_CavActvTimeout_mS_u16	65535		
k_CavActvVBattMax_Volt_f32	31		
k_CavActvVBattMin_Volt_f32	31		
k_CmmActvTimeout_mS_u16	65535		
k_CmmActvVBattMax_Volt_f32	31		
k_CmmActvVBattMin_Volt_f32	31	31	
k_EscActvTimeout_mS_u16	65535		
k_EscActvVBattMax_Volt_f32	31	31	
k_EscActvVBattMin_Volt_f32	31	31	
target_Demlf_Per_BatteryVoltage_Volt_f32.value	31	31	
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_DemIf_Per_EtatMt_Cnt_u08.value	15		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	dTim 65535		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u33\_CurrentTime$	4294967295		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_	_Volt_f32	
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc	:	
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc	:	
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegr	ration_Cnt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08	3	
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas Cnt M u32	0	0	
CTCInhibitionBsi_Cnt_M_u32	0	0	
CTCInhibitionCav Cnt M u32	0	0	
CTCInhibitionCmm Cnt M u32	0	0	
CTCInhibitionEsc Cnt M u32	0	0	
CTCInhibitionState Cnt M u08	192	192	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Test Step 2.3 (Repeat Count = 1)	🗸
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8



Name	Immut Value		
	Input Value		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSuperscript{0}{1}{1}{1}{1}{1}{1}{1}{1}{1}{1}{1}{1}{1}$	35422		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	616684576		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	616684576	616684576	~
CTCInhibitionBsi_Cnt_M_u32	616684576	616684576	~
CTCInhibitionCav_Cnt_M_u32	616684576	616684576	~
CTCInhibitionCmm_Cnt_M_u32	616684576	616684576	~
CTCInhibitionEsc_Cnt_M_u32	616684576	616684576	~
CTCInhibitionState_Cnt_M_u08	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	•
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Test Step 2.4 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	31
target_Demlf_Per_BusOff_Cnt_lgc.value	1
target_Demlf_Per_CTerm_Cnt_lgc.value	1
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_Demlf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	44450
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2274712120
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc

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Name	Input Value		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_Electronic	cIntegration_Cnt_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_C	nt_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	2274712120	2274712120	~
CTCInhibitionBsi_Cnt_M_u32	2274712120	2274712120	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	2274712120	2274712120	~
CTCInhibitionCmm_Cnt_M_u32	2274712120	2274712120	✓
CTCInhibitionEsc_Cnt_M_u32	2274712120	2274712120	<b>✓</b>
CTCInhibitionState_Cnt_M_u08	64	64	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	<b>✓</b>
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	<b>~</b>
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>~</b>

Test Step 2.5 (Repeat Count = 1)			
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_	_GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	23.1233997		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	13073		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1199317560		
target_Rte_Inst_Ap_DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f3	32	
target_Rte_Inst_Ap_DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf_DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf_DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_0	Cnt_lgc	
target_Rte_Inst_Ap_DemIf_DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resul
CTCInhibitionAas Cnt M u32	1199317560	1199317560	
CTCInhibitionBsi_Cnt_M_u32	1199317560	1199317560	
CTCInhibitionCav Cnt M u32	1199317560	1199317560	
CTCInhibitionCmm_Cnt_M_u32	1199317560	1199317560	
CTCInhibitionEsc Cnt M u32	1199317560	1199317560	
CTCInhibitionState Cnt M u08	192	192	



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	•
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	•

Test Step 2.6 (Repeat Count = 1)			<b>√</b>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target Rte Call Ap Demlf Ignition	OP GET signal		
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf System	Time DtrmnElapsedTime mS u16 Elaps	edTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target Rte Call Ap Demlf System	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Inst Ap Demlf	target Rte Inst Ap Demlf			
Rte Mode Ap Demlf SystemState Mode()	3			
VehSpdControl Cnt M Igc	1			
k AasActvTimeout mS u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k CavActvTimeout mS u16	800			
k CavActvVBattMax Volt f32	16			
k_CavActvVBattMin_Volt_f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k_EscActvTimeout_mS_u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	19.0732002			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target Demlf Per EtatMt Cnt u08.value	1			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0			
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapse	dTim 11127			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTir	ne 3539035437			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_	Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc	<del>-</del>		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc			
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegra			
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas Cnt M u32	3539035437	3539035437	-	
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	•	
CTCInhibitionCav Cnt M u32	3539035437	3539035437	-	
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	•	
CTCInhibitionEsc Cnt M u32	3539035437	3539035437	•	
CTCInhibitionState Cnt M u08	64	64	•	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	<b>V</b>

Test Step 2.7 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime

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Name	Input Value		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	3		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	14.1280003		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	34139		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	2825399010		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	•
CTCInhibitionState_Cnt_M_u08	128	128	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>

Test Step 2.8 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	4
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16





Name	Input Value		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	15.1973		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	n 10391		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	1774937490		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cn	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionBsi_Cnt_M_u32	3539035437	3539035437	•
CTCInhibitionCav_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionCmm_Cnt_M_u32	3539035437	3539035437	<b>~</b>
CTCInhibitionEsc_Cnt_M_u32	3539035437	3539035437	~
CTCInhibitionState_Cnt_M_u08	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Name	Input Value		
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GE	T signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime Dt		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_Ge	etSystemTime mS u32 CurrentTime	
Rte Inst Ap Demlf	target Rte Inst Ap Demlf		
Rte Mode Ap Demlf SystemState Mode()	3		
VehSpdControl Cnt M lgc	1		
k AasActvTimeout mS u16	800		
k AasActvVBattMax Volt f32	16		
k AasActvVBattMin Volt f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.63290024		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	1		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	10133		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2290771965		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas_Cnt_M_u32	2290771965	2290771965	
CTCInhibitionBsi Cnt M u32	2290771965	2290771965	

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Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	2290771965	2290771965	~
CTCInhibitionCmm_Cnt_M_u32	2290771965	2290771965	~
CTCInhibitionEsc_Cnt_M_u32	2290771965	2290771965	~
CTCInhibitionState_Cnt_M_u08	192	192	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>~</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	•

Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Igni	tion OP GET signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime		temTime_DtrmnElapsedTime_mS_u16_Elapse	edTime
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)		temTime GetSystemTime mS u32 CurrentTi	
Rte Inst Ap Demif	target Rte Inst Ap Demlf	terrime_GetGysterrime_m3_u32_Gurrentm	iiiie
Rte Mode Ap Demlf SystemState Mode()	3		
VehSpdControl Cnt M Igc	0		
k AasActvTimeout mS u16	800		
k_AasActvVBattMax_Volt_f32	16		
k AasActvVBattMin Volt f32	8		
k BsiActvTimeout mS u16	600		
k BsiActvVBattMax Volt f32	16		
k BsiActvVBattMin Volt f32	8		
k CavActvTimeout mS u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	600		
k CmmActvVBattMax Volt f32	16		
k CmmActvVBattMin Volt f32	8		
k EscActvTimeout mS u16	1000		
k EscActvVBattMax Volt f32	16		
k EscActvVBattMin Volt f32	8		
target Demlf Per BatteryVoltage Volt f32.value	15.5703001		
target Demlf Per BusOff Cnt Igc.value	0		
target Demlf Per CTerm Cnt Igc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	1		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_Elaps	·		
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentT			
target Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage	ne Volt f32	
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_	· <del>-</del> -	
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target Demlf Per CTerm Cnt		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicInte	-	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_i		
Name	Actual Value	Expected Value	Resu
	O Actual value	0	Resu
CTCInhibitionAas_Cnt_M_u32		2290771965	
CTCInhibitionBsi_Cnt_M_u32	2290771965	0	
CTCInhibitionCav_Cnt_M_u32	0	-	
CTCInhibitionCmm_Cnt_M_u32	2290771965	2290771965	
CTCInhibitionEsc_Cnt_M_u32 CTCInhibitionState Cnt M u08	2290771965	2290771965 0	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~



Test Step 2.11 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GE	ET signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_D		
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target Rte Call Ap Demlf SystemTime G		
Rte Inst Ap Demlf	target Rte Inst Ap Demlf		
Rte_Mode_Ap_Demif_SystemState_Mode()	0		
VehSpdControl Cnt M lgc	1		
k AasActvTimeout mS u16	800		
k AasActvVBattMax Volt f32	16		
k_AasActvVBattMin_Volt_f32	8		
k BsiActvTimeout mS u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	600		
k CmmActvVBattMax Volt f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k EscActvVBattMin Volt f32	8		
target Demlf Per BatteryVoltage Volt f32.value	2.43390012		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTin	17221		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	4294967295		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegration Cn	t lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionBsi_Cnt_M_u32	4294967295	4294967295	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionCmm_Cnt_M_u32	4294967295	4294967295	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionState_Cnt_M_u08	192	192	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	<b>~</b>
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	<b>~</b>
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>~</b>
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	<b>~</b>
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~

Test Step 2.12 (Repeat Count = 1)	✓
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8





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Name	Input Value		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.41270018		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_DemIf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSuperscript{Main_control_co$	14136		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1533825676		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionBsi_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionCav_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionCmm_Cnt_M_u32	1533825676	1533825676	~
CTCInhibitionEsc_Cnt_M_u32	1533825676	1533825676	-
CTCInhibitionState_Cnt_M_u08	64	64	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	-
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>

Test Step 2.13 (Repeat Count = 1)	
Name	Input Value
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTime
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	19.9340992
target_Demlf_Per_BusOff_Cnt_lgc.value	1
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1
target_DemIf_Per_EtatMt_Cnt_u08.value	0
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	n 0
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	3633311787
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc

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Name Input Value target\_Rte\_Inst\_Ap\_DemIf.DemIf\_Per\_ElectronicIntegration\_Cnt\_Igc target\_Demlf\_Per\_ElectronicIntegration\_Cnt\_lgc target\_Rte\_Inst\_Ap\_DemIf.DemIf\_Per\_EtatMt\_Cnt\_u08 target\_DemIf\_Per\_EtatMt\_Cnt\_u08 Actual Value **Expected Value** Result CTCInhibitionAas\_Cnt\_M\_u32 3633311787 3633311787 CTCInhibitionBsi\_Cnt\_M\_u32 3633311787 3633311787 CTCInhibitionCav\_Cnt\_M\_u32 3633311787 3633311787 CTCInhibitionCmm\_Cnt\_M\_u32 3633311787 3633311787 CTCInhibitionEsc\_Cnt\_M\_u32 3633311787 3633311787 223 CTCInhibitionState\_Cnt\_M\_u08 223

Test Step Call Trace	Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	~	
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~	
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•	
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	~	

Test Step 2.14 (Repeat Count = 1)				
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal			
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime			
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_G	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	1			
VehSpdControl_Cnt_M_lgc	0			
k_AasActvTimeout_mS_u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16			
k_CavActvVBattMin_Volt_f32	8			
k_CmmActvTimeout_mS_u16	600			
k_CmmActvVBattMax_Volt_f32	16			
k_CmmActvVBattMin_Volt_f32	8			
k_EscActvTimeout_mS_u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.89410019			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	0			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0			
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSuperscript{Main_control_co$	65535			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2447925560			
target_Rte_Inst_Ap_DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32			
target_Rte_Inst_Ap_DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc			
target_Rte_Inst_Ap_DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_DemIf_DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cn	t_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Resu	
CTCInhibitionAas Cnt M u32	2447925560	2447925560		
CTCInhibitionBsi Cnt M u32	2447925560	2447925560		
CTCInhibitionCav Cnt M u32	2447925560	2447925560	٠,	
CTCInhibitionCmm Cnt M u32	2447925560	2447925560	,	
CTCInhibitionEsc Cnt M u32	2447925560	2447925560	٠,	
CTCInhibitionState Cnt M u08	64	64		



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
DemIf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	•
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	•
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	•
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16	5	<b>✓</b>

Test Step 2.15 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_G	ET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_D	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime		
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_G	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	4			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k CavActvVBattMax Volt f32	16			
k CavActvVBattMin Volt f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k EscActvTimeout mS u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	14.2438002			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target Demlf Per EtatMt Cnt u08.value	0			
target Rte Call Ap Demlf Ignition OP GET signal	1			
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTi	m 1241			
target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime	3091959789			
target Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage Volt f32			
target Rte Inst Ap Demlf.Demlf Per BusOff Cnt Igc	target Demlf Per BusOff Cnt Igc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc			
target Rte Inst Ap Demlf.Demlf Per ElectronicIntegration Cnt Igc	target Demlf Per ElectronicIntegration Cr	nt lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas Cnt M u32	2447925560	2447925560	_	
CTCInhibitionBsi Cnt M u32	2447925560	2447925560	-	
CTCInhibitionCav Cnt M u32	2447925560	2447925560		
CTCInhibitionCmm Cnt M u32	2447925560	2447925560		
CTCInhibitionEsc Cnt M u32	2447925560	2447925560	_	
CTCInhibitionState Cnt M u08	64	64		

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32	1	Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32	1	~
Demlf_EvaluateLogicalCondition	1	Demlf_EvaluateLogicalCondition	1	~
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~
Demlf_CheckVoltageRange	5	Demlf_CheckVoltageRange	5	~
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16	5	<b>V</b>

Test Step 2.16 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime

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Name	Input Value		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	3		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	5.31850004		
target_Demlf_Per_BusOff_Cnt_lgc.value	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	11		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	51058		
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3923762454		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cn	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	3923762454	3923762454	
CTCInhibitionBsi Cnt M u32	3923762454	3923762454	•
CTCInhibitionCav Cnt M u32	3923762454	3923762454	-
CTCInhibitionCmm Cnt M u32	3923762454	3923762454	•
CTCInhibitionEsc_Cnt_M_u32	3923762454	3923762454	-
CTCInhibitionState Cnt M u08	0	0	-

Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	5.31850004
target_Demlf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	1
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_Demlf_Per_EtatMt_Cnt_u08.value	11
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_Elapsed	Tim 51058
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTim	e 3923762454
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32



Name	Input Value		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_C	nt_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionBsi_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionCav_Cnt_M_u32	3923762454	3923762454	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	3923762454	3923762454	•
CTCInhibitionEsc_Cnt_M_u32	3923762454	3923762454	~
CTCInhibitionState_Cnt_M_u08	64	64	~

Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition	OP GET signal		
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)		_or _ot r_signal Time_DtrmnElapsedTime_mS_u16_Elapse	edTime	
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)		target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Inst Ap Demlf		target Rte Inst Ap Demlf		
Rte Mode Ap Demlf SystemState Mode()	4			
VehSpdControl Cnt M lgc	1			
k AasActvTimeout mS u16	800			
k AasActvVBattMax Volt f32	16			
k AasActvVBattMin Volt f32	8			
k BsiActvTimeout mS u16	600			
k BsiActvVBattMax Volt f32	16			
k BsiActvVBattMin Volt f32	8			
k CavActvTimeout mS u16	800			
k CavActvVBattMax Volt f32	16			
k CavActvVBattMin Volt f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k EscActvTimeout mS u16	0			
k EscActvVBattMax Volt f32	16			
k EscActvVBattMin Volt f32	8			
target Demlf Per BatteryVoltage Volt f32.value	2.17689991			
target_Demlf_Per_BusOff_Cnt_lgc.value	0			
target Demlf Per CTerm Cnt lgc.value	1			
target Demlf Per ElectronicIntegration Cnt Igc.value	0			
target Demlf Per EtatMt Cnt u08.value	7			
target Rte Call Ap Demlf Ignition OP GET signal	0			
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 Elapsed	Tim 53021			
target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTim				
target_Rte_Inst_Ap_Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_\	/olt f32		
target Rte Inst Ap Demlf.Demlf Per BusOff Cnt Igc	target Demlf Per BusOff Cnt Igc			
target Rte Inst Ap Demlf.Demlf Per CTerm Cnt Igc	target Demlf Per CTerm Cnt Igc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegra	tion Cnt Igc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08	0		
Name	Actual Value	Expected Value	Resu	
CTCInhibitionAas Cnt M u32	785100198	785100198		
CTCInhibitionBsi Cnt M u32	785100198	785100198		
CTCInhibitionCav Cnt M u32	785100198	785100198		
CTCInhibitionCmm_Cnt_M_u32	785100198	785100198		
CTCInhibitionEsc Cnt M u32	785100198	785100198		
CTCInhibitionState Cnt M u08	64	64		

Test Step 2.19 (Repeat Count = 1)	· ·
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	2
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600



Name	Input Value		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	65535		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	1.71889997		
target_DemIf_Per_BusOff_Cnt_lgc.value	0		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	14		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTim$	33512		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	1652918279		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_Igc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionBsi_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionCav_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionCmm_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionEsc_Cnt_M_u32	1652918279	1652918279	~
CTCInhibitionState_Cnt_M_u08	193	193	~

Name	Input Value			
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal			
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTime			
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime			
Rte Inst Ap Demlf	target Rte Inst Ap Demif			
Rte_Mode_Ap_Demlf_SystemState_Mode()	4			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800			
k AasActvVBattMax Volt f32	16			
k AasActvVBattMin Volt f32	8			
k BsiActvTimeout mS u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16	111		
k_CavActvVBattMin_Volt_f32	8			
k_CmmActvTimeout_mS_u16	600			
k_CmmActvVBattMax_Volt_f32	16			
k_CmmActvVBattMin_Volt_f32	8			
k_EscActvTimeout_mS_u16	1000			
k_EscActvVBattMax_Volt_f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	7.58209991			
target_Demlf_Per_BusOff_Cnt_lgc.value	0			
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	1			
target_Demlf_Per_EtatMt_Cnt_u08.value	8			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0			
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedT	im 42407			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1905186906			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demif_Per_BatteryVoltage_Volt_f32			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_Igc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	1905186906	1905186906	•	
CTCInhibitionBsi Cnt M u32	1905186906	1905186906		

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Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	1905186906	1905186906	~
CTCInhibitionCmm_Cnt_M_u32	1905186906	1905186906	•
CTCInhibitionEsc_Cnt_M_u32	1905186906	1905186906	~
CTCInhibitionState_Cnt_M_u08	192	192	•

Test Step 2.21 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTime		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte Inst Ap Demif	target_Rte_Inst_Ap_Demlf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	0		
VehSpdControl Cnt M lgc	0		
k AasActvTimeout mS u16	800		
k AasActvVBattMax Volt f32	16		
k AasActvVBattMin Volt f32	8		
k_BsiActvTimeout_mS_u16	0		
k BsiActvVBattMax Volt f32	16		
k BsiActvVBattMin Volt f32	8		
k CavActvTimeout mS u16	800		
k_CavActvVBattMax_Volt_f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	600		
k CmmActvVBattMax Volt f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k EscActvVBattMin Volt f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	2.12019992		
target_DemIf_Per_BusOff_Cnt_lgc.value	0		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_DemIf_Per_EtatMt_Cnt_u08.value	11		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedT	m 21862		
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	921326253		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_Igc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cn	ıt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	921326253	921326253	~
CTCInhibitionBsi Cnt M u32	921326253	921326253	~
CTCInhibitionCav Cnt M u32	921326253	921326253	
CTCInhibitionCmm Cnt M u32	921326253	921326253	~
CTCInhibitionEsc Cnt M u32	921326253	921326253	~
CTCInhibitionState Cnt M u08	0	0	~

Test Step 2.22 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	1
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	65535
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16

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Name	Input Value			
k CmmActvVBattMin Volt f32	8			
k EscActvTimeout mS u16	1000			
k EscActvVBattMax Volt f32	16			
k EscActvVBattMin Volt f32	8			
target Demlf Per BatteryVoltage Volt f32.value	2.67659998			
target Demlf Per BusOff Cnt Igc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_DemIf_Per_EtatMt_Cnt_u08.value	7			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1			
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	58660			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	3172092003			
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32			
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cnt_	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	3172092003	3172092003	~	
CTCInhibitionBsi_Cnt_M_u32	3172092003	3172092003	~	
CTCInhibitionCav_Cnt_M_u32	3172092003	3172092003	~	
CTCInhibitionCmm_Cnt_M_u32	3172092003	3172092003	~	
CTCInhibitionEsc_Cnt_M_u32	3172092003	3172092003	~	
CTCInhibitionState_Cnt_M_u08	66	66	<b>✓</b>	

Name	Input Value			
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GET signal			
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTime			
Rte Call Ap Demlf SystemTime GetSystemTime mS u32(CurrentTime)	target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime			
Rte Inst Ap Demlf	target Rte Inst Ap Demlf			
Rte Mode Ap Demlf SystemState Mode()	4			
VehSpdControl Cnt M Igc	0			
k AasActvTimeout mS u16	800			
k AasActvVBattMax Volt f32	16			
k AasActvVBattMin Volt f32	8			
k BsiActvTimeout mS u16	600			
k BsiActvVBattMax Volt f32	16			
k BsiActvVBattMin Volt f32	8			
k CavActvTimeout mS u16	800			
k CavActvVBattMax Volt f32	16			
k CavActvVBattMin Volt f32	8			
k CmmActvTimeout mS u16	600			
k CmmActvVBattMax Volt f32	16			
k CmmActvVBattMin Volt f32	8			
k EscActvTimeout mS u16	1000			
k EscActvVBattMax Volt f32	16			
k_EscActvVBattMin_Volt_f32	8			
target_Demlf_Per_BatteryVoltage_Volt_f32.value	5.91480017			
target_Demlf_Per_BusOff_Cnt_lgc.value	0			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	12			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedT	m 4345			
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2417842237			
target_Rte_Inst_Ap_Demlf_Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Vo	olt_f32		
target_Rte_Inst_Ap_Demlf_Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc			
target_Rte_Inst_Ap_Demlf_Demlf_Per_ElectronicIntegration_Cnt_lgc	target_Demlf_Per_ElectronicIntegration_Cnt_lgc			
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08			
Name	Actual Value	Expected Value	Resul	
CTCInhibitionAas Cnt M u32	2417842237	2417842237		
CTCInhibitionBsi Cnt M u32	2417842237	2417842237		
CTCInhibitionCav_Cnt_M_u32	2417842237	2417842237		
<del></del>		2417842237		
CTCInhibitionCmm Cnt M u32	2417842237	2417042237		
CTCInhibitionCmm_Cnt_M_u32 CTCInhibitionEsc Cnt M u32	2417842237	2417842237		



Test Step 2.24 (Repeat Count = 1)			~
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GE	T signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime Dt		
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_Ge	etSystemTime mS u32 CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte Mode Ap Demlf SystemState Mode()	0		
VehSpdControl Cnt M lgc	1		
k AasActvTimeout mS u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	0		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0.0749000013		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_DemIf_Per_ElectronicIntegration_Cnt_Igc.value	1		
target_DemIf_Per_EtatMt_Cnt_u08.value	2		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_ms_u16\_ElapsedT$	50842		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	544823061		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	544823061	544823061	~
CTCInhibitionBsi_Cnt_M_u32	544823061	544823061	~
CTCInhibitionCav_Cnt_M_u32	544823061	544823061	~
CTCInhibitionCmm_Cnt_M_u32	544823061	544823061	•
CTCInhibitionEsc_Cnt_M_u32	544823061	544823061	~
CTCInhibitionState_Cnt_M_u08	192	192	•

Test Step 2.25 (Repeat Count = 1)	
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_Demlf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	65535
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0.40959999
target_Demlf_Per_BusOff_Cnt_lgc.value	0
target_Demlf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	1



Name	Input Value		
target_Demlf_Per_EtatMt_Cnt_u08.value	15		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	8547		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1368639926		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration_Cnt_	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionBsi_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionCav_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionCmm_Cnt_M_u32	1368639926	1368639926	~
CTCInhibitionEsc_Cnt_M_u32	1368639926	1368639926	<b>~</b>
CTCInhibitionState_Cnt_M_u08	132	132	~

Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_O	P GET signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)		ne_DtrmnElapsedTime_mS_u16_Elapse	edTime
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)		ne_GetSystemTime_mS_u32_CurrentTi	
Rte Inst Ap Demlf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	1		
VehSpdControl Cnt M lgc	1		
k AasActvTimeout mS u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k BsiActvVBattMax Volt f32	16		
k BsiActvVBattMin Volt f32	8		
k CavActvTimeout mS u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	4.39799976		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	5		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedT	Tim 4041		
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1967358071		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Voltage	t_f32	
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_DemIf_Per_ElectronicIntegration	n_Cnt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionBsi_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionCav_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionCmm_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionEsc_Cnt_M_u32	1967358071	1967358071	
CTCInhibitionState Cnt M u08	64	64	

Test Step 2.27 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	
Rte_Mode_Ap_DemIf_SystemState_Mode()	3	

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Name	Input Value		
VehSpdControl_Cnt_M_lgc	0		
k_AasActvTimeout_mS_u16	0		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	15.6511002		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	3		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mS_u16\_ElapsedT$	edTim 22989		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u33\_CurrentTime$	ime 4288551715		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_	Volt_f32	
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegra	ation_Cnt_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08	3	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionBsi_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionCav_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionCmm_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionEsc_Cnt_M_u32	1967358071	1967358071	~
CTCInhibitionState_Cnt_M_u08	64	64	~

Test Step 2.28 (Repeat Count = 1)	<b>√</b>
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	3
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	65535
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8
k_CavActvTimeout_mS_u16	800
k_CavActvVBattMax_Volt_f32	16
k_CavActvVBattMin_Volt_f32	8
k_CmmActvTimeout_mS_u16	600
k_CmmActvVBattMax_Volt_f32	16
k_CmmActvVBattMin_Volt_f32	8
k_EscActvTimeout_mS_u16	1000
k_EscActvVBattMax_Volt_f32	16
k_EscActvVBattMin_Volt_f32	8
target_Demlf_Per_BatteryVoltage_Volt_f32.value	1.24150002
target_Demlf_Per_BusOff_Cnt_lgc.value	0
target_DemIf_Per_CTerm_Cnt_lgc.value	0
target_DemIf_Per_ElectronicIntegration_Cnt_lgc.value	0
target_DemIf_Per_EtatMt_Cnt_u08.value	14
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime\_mSu16\_Elap$	28869
target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime	1311140043
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lgc
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lgc

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Demlf\_Per



Name	Input Value		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_Electronic	Integration_Cnt_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cr	nt_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1311140043	1311140043	~
CTCInhibitionBsi_Cnt_M_u32	1311140043	1311140043	✓
CTCInhibitionCav_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	1311140043	1311140043	<b>✓</b>
CTCInhibitionState_Cnt_M_u08	8	8	<b>✓</b>

Test Step 2.29 (Repeat Count = 1)			~
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GE	ET_signal	
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_D	trmnElapsedTime_mS_u16_ElapsedTime	
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_G	etSystemTime_mS_u32_CurrentTime	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	2		
VehSpdControl_Cnt_M_lgc	1		
k_AasActvTimeout_mS_u16	800		
k_AasActvVBattMax_Volt_f32	16		
k_AasActvVBattMin_Volt_f32	8		
k_BsiActvTimeout_mS_u16	600		
k_BsiActvVBattMax_Volt_f32	16		
k_BsiActvVBattMin_Volt_f32	8		
k_CavActvTimeout_mS_u16	800		
k_CavActvVBattMax_Volt_f32	16		
k_CavActvVBattMin_Volt_f32	8		
k_CmmActvTimeout_mS_u16	600		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	24.6821003		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	12		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime_ms_u16_ElapsedTim	m 1356		
target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime	2740672965		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_Demlf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cn	t_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas Cnt M u32	2740672965	2740672965	<b>~</b>
CTCInhibitionBsi Cnt M u32	2740672965	2740672965	•
CTCInhibitionCav Cnt M u32	2740672965	2740672965	
CTCInhibitionCmm Cnt M u32	2740672965	2740672965	_
CTCInhibitionEsc Cnt M u32	2740672965	2740672965	-
CTCInhibitionState Cnt M u08	64	64	<b>V</b>

Test Step 2.30 (Repeat Count = 1)	✓
Name	Input Value
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal
Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTime
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32_CurrentTime
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf
Rte_Mode_Ap_DemIf_SystemState_Mode()	1
VehSpdControl_Cnt_M_lgc	0
k_AasActvTimeout_mS_u16	800
k_AasActvVBattMax_Volt_f32	16
k_AasActvVBattMin_Volt_f32	8
k_BsiActvTimeout_mS_u16	600
k_BsiActvVBattMax_Volt_f32	16
k_BsiActvVBattMin_Volt_f32	8





Name	Input Value		
k CavActvTimeout mS u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k_CmmActvTimeout_mS_u16	0		
k_CmmActvVBattMax_Volt_f32	16		
k_CmmActvVBattMin_Volt_f32	8		
k_EscActvTimeout_mS_u16	1000		
k_EscActvVBattMax_Volt_f32	16		
k_EscActvVBattMin_Volt_f32	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	0.328999996		
target_Demlf_Per_BusOff_Cnt_lgc.value	1		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	12		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 ElapsedTim	26304		
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime$	3599977200		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BatteryVoltage_Volt_f32	target_DemIf_Per_BatteryVoltage_Volt_f32		
target_Rte_Inst_Ap_Demlf.Demlf_Per_BusOff_Cnt_lgc	target_DemIf_Per_BusOff_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_ElectronicIntegration_Cnt_lgc	target_DemIf_Per_ElectronicIntegration_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionBsi_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionCav_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionCmm_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionEsc_Cnt_M_u32	3599977200	3599977200	~
CTCInhibitionState_Cnt_M_u08	64	64	~

Name	Input Value		
Rte Call Ap Demlf Ignition OP GET(signal)	target Rte Call Ap Demlf Ignition OP GE	T signal	
Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16(ElapsedTime)	target Rte Call Ap Demlf SystemTime D	_ ·	
Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_SystemTime_G		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	ctoyotemrime_mo_uoz_ouncmrime	
Rte Mode Ap Demlf SystemState Mode()	2		
VehSpdControl Cnt M Igc	0		
k AasActvTimeout mS u16	800		
k AasActvVBattMax Volt f32	16		
k AasActvVBattMin Volt f32	8		
k BsiActvTimeout mS u16	600		
k BsiActvVBattMax Volt f32	16		
k BsiActvVBattMin Volt f32	8		
k CavActvTimeout mS u16	800		
k CavActvVBattMax Volt f32	16		
k CavActvVBattMin Volt f32	8		
k CmmActvTimeout mS u16	65535		
k CmmActvVBattMax Volt f32	16		
k CmmActvVBattMin Volt f32	8		
k EscActvTimeout mS u16	1000		
k EscActvVBattMax Volt f32	16		
k EscActvVBattMin Volt f32	8		
target Demlf Per BatteryVoltage Volt f32.value	1.57360005		
target Demlf Per BusOff Cnt Igc.value	1		
target Demlf Per CTerm Cnt Igc.value	0		
target Demlf Per ElectronicIntegration Cnt Igc.value	1		
target Demlf Per EtatMt Cnt u08.value	1		
target Rte Call Ap Demlf Ignition OP GET signal	0		
target_Rte_Call_Ap_DemIf_SystemTime_DtrmnElapsedTime_mS_u16_ElapsedTim	62048		
target Rte Call Ap Demlf SystemTime GetSystemTime mS u32 CurrentTime	3314516146		
target Rte Inst Ap Demlf.Demlf Per BatteryVoltage Volt f32	target Demlf Per BatteryVoltage Volt f32		
target Rte Inst Ap Demlf.Demlf Per BusOff Cnt Igc	target Demlf Per BusOff Cnt Igc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicIntegration_Cn	t_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resu
CTCInhibitionAas Cnt M u32	3314516146	3314516146	
CTCInhibitionBsi Cnt M u32	3314516146	3314516146	
CTCInhibitionCav Cnt M u32	3314516146	3314516146	
CTCInhibitionCmm Cnt M u32	3314516146	3314516146	

Demlf\_Per

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Name	Actual Value	Expected Value	Result
CTCInhibitionEsc_Cnt_M_u32	3314516146	3314516146	✓
CTCInhibitionState Cnt M u08	208	208	<b>✓</b>

Test Step 2.32 (Repeat Count = 1)			•	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignitio	n_OP_GET_signal		
Rte_Call_Ap_Demlf_SystemTime_DtrmnElapsedTime_mS_u16(ElapsedTime)	target_Rte_Call_Ap_DemIf_System	mTime_DtrmnElapsedTime_mS_u16_Elaps	edTime	
Rte_Call_Ap_DemIf_SystemTime_GetSystemTime_mS_u32(CurrentTime)	target_Rte_Call_Ap_DemIf_Syste	target_Rte_Call_Ap_Demlf_SystemTime_GetSystemTime_mS_u32_CurrentTime		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_Demlf_SystemState_Mode()	3			
VehSpdControl_Cnt_M_lgc	1			
k_AasActvTimeout_mS_u16	800			
k_AasActvVBattMax_Volt_f32	16			
k_AasActvVBattMin_Volt_f32	8			
k_BsiActvTimeout_mS_u16	600			
k_BsiActvVBattMax_Volt_f32	16			
k_BsiActvVBattMin_Volt_f32	8			
k_CavActvTimeout_mS_u16	800			
k_CavActvVBattMax_Volt_f32	16			
k_CavActvVBattMin_Volt_f32	8			
k_CmmActvTimeout_mS_u16	600			
k_CmmActvVBattMax_Volt_f32	16			
k_CmmActvVBattMin_Volt_f32	8			
k_EscActvTimeout_mS_u16	1000	1000		
k_EscActvVBattMax_Volt_f32	16	16		
k_EscActvVBattMin_Volt_f32	8	8		
target_Demlf_Per_BatteryVoltage_Volt_f32.value	8.26420021			
target_Demlf_Per_BusOff_Cnt_lgc.value	1			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_ElectronicIntegration_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	5			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0			
target Rte Call Ap Demlf SystemTime DtrmnElapsedTime mS u16 Elapse	edTim 54812			
$target\_Rte\_Call\_Ap\_Demlf\_SystemTime\_GetSystemTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u32\_CurrentTime\_mS\_u33\_CurrentTime$	me 1306746881			
target_Rte_Inst_Ap_DemIf.DemIf_Per_BatteryVoltage_Volt_f32	target_Demlf_Per_BatteryVoltage	_Volt_f32		
target_Rte_Inst_Ap_DemIf.DemIf_Per_BusOff_Cnt_Igc	target_Demlf_Per_BusOff_Cnt_lge	С		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt_lge	С		
target_Rte_Inst_Ap_DemIf.DemIf_Per_ElectronicIntegration_Cnt_Igc	target_Demlf_Per_ElectronicInteg	ration_Cnt_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_u0	target_Demlf_Per_EtatMt_Cnt_u08		
Name	Actual Value	Expected Value	Resul	
CTCInhibitionAas_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionBsi_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionCav_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionCmm_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionEsc_Cnt_M_u32	1306746881	1306746881	•	
CTCInhibitionState_Cnt_M_u08	64	64		

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Demlf\_EvaluateLogicalCondition

Project	Demlf
Module	Demlf
Test Object	Demlf_EvaluateLogicalCondition

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	2	
Successful	2	✓
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes			
Name	Value		
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5		
Float Precision	9		
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj		
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src		
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd		
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl		
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4		
Time Unit	cycles		
Timer Enabled	false		
Timer Prescale	0		
Timer Resolution	1		
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		

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Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### **Test Case 1: Metrics Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 1103.00 Cycles TS 1.2 1038.00 Cycles

Description Vector Description:

TS 1.1 Shortest Execution Path=>if (IoHwAb\_BoolType\_LowerLimit == Ignition\_Cnt\_T\_enum)=>False if (((uint8)kETAT\_MT\_Starting == EtatMt\_Cnt\_T\_u08)=>False || ((uint8)kETAT\_MT\_Autonomous\_Starting == EtatMt\_Cnt\_T\_u08)=>False)
TS 1.2 Longest Execution Path=> if (IoHwAb\_BoolType\_LowerLimit == Ignition\_Cnt\_T\_enum)=>True if ((FALSE == CTerm\_Cnt\_T\_lgc)=>True && (RTE\_MODE\_StaMd\_Mode\_OPERATE != SystemState\_Cnt\_T\_enum)=>True)

Test Step 1.1 (Repeat Count = 1)			✓	
Name	Input Value			
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igi	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	4			
Time_ms_T_u32	4294967295			
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_EtatMt_Cnt_u08.value	15	15		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	:_lgc		
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	0	0	~	
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionCav_Cnt_M_u32	0	0	~	
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	0	0	~	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~

Test Step 1.2 (Repeat Count = 1)			✓	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	0			
Time_ms_T_u32	0			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	0			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	0	0	~	
CTCInhibitionBsi_Cnt_M_u32	0	0	~	
CTCInhibitionCav_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>	
CTCInhibitionEsc Cnt M u32	0	0	<b>✓</b>	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>



#### Test Case 2: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 1032.00 Cycles
TS 2.2 1032.00 Cycles
TS 2.2 1032.00 Cycles
TS 2.3 1032.00 Cycles
TS 2.4 1032.00 Cycles
TS 2.4 1032.00 Cycles
TS 2.5 1032.00 Cycles
TS 2.6 1032.00 Cycles
TS 2.7 1032.00 Cycles
TS 2.9 1032.00 Cycles
TS 2.9 1032.00 Cycles
TS 2.10 1032.00 Cycles
TS 2.11 1032.00 Cycles
TS 2.12 1032.00 Cycles
TS 2.12 1032.00 Cycles
TS 2.13 1032.00 Cycles
TS 2.14 1032.00 Cycles
TS 2.15 1032.00 Cycles
TS 2.15 1032.00 Cycles
TS 2.16 1032.00 Cycles
TS 2.17 1032.00 Cycles
TS 2.17 1032.00 Cycles
TS 2.17 1032.00 Cycles

#### Description

#### Vector Description:

TS 1.1All Min

TS 1.2All Max

IS 1.2All Max

S 1.3Time\_ms\_T\_u32=>Min

TS 1.4Time\_ms\_T\_u32=>Max

TS 1.5Time\_ms\_T\_u32=>Pos

TS 1.6Demlf\_Per\_CTerm\_Cnt\_lgc=>Min

TS 1.7Demlf\_Per\_CTerm\_Cnt\_lgc=>Max

TS 1.8Demlf\_Per\_EtatMt\_Cnt\_u08=>Min

TS 1.9Demlf\_Per\_EtatMt\_Cnt\_u08=>Max

TS 1.9Demlf\_Per\_EtatMt\_Cnt\_u08=>Max

TS 1.9Demlf\_Per\_EtatMt\_Cnt\_u08=>Max
TS 1.10Demlf\_Per\_EtatMt\_Cnt\_u08=>Pos
TS 1.10Demlf\_Per\_EtatMt\_Cnt\_u08=>Pos
TS 1.11Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_DISABLE
TS 1.12Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_OFF
TS 1.13Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_OPERATE
TS 1.14Rte\_Mode\_SystemState\_Mode=>RTE\_MODE\_StaMd\_Mode\_WARMINIT
TS 1.15Rte\_Mode\_SystemState\_Mode=>RTE\_TRANSITION\_StaMd\_Mode
TS 1.16Rte\_Call\_Ignition\_OP\_GET=>Min
TS 1.17Rte\_Call\_Ignition\_OP\_GET=>Max

Test Step 2.1 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ign	ition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	0		
Time_ms_T_u32	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	~
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	0	0	✓
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode Ap Demlf SystemState Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Ign	ition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf			
Rte_Mode_Ap_DemIf_SystemState_Mode()	4			
Time_ms_T_u32	4294967295			
target_Demlf_Per_CTerm_Cnt_lgc.value	1	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	15			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08		
Name	Actual Value	Expected Value	Resul	
CTCInhibitionAas_Cnt_M_u32	0	0	•	
CTCInhibitionBsi Cnt M u32	0	0		

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Name	Actual Value	Expected Value	Result
CTCInhibitionCav_Cnt_M_u32	0	0	~
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc Cnt M u32	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Test Step 2.3 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	0		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	1		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode Ap Demlf SystemState Mode	1	Rte Mode Ap Demlf SystemState Mode	1	<b>✓</b>

Test Step 2.4 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2		
Time_ms_T_u32	4294967295		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	2		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	4294967295	4294967295	~
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•

Test Step 2.5 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	
Rte_Mode_Ap_DemIf_SystemState_Mode()	2	
Time_ms_T_u32	125351	
target_Demlf_Per_CTerm_Cnt_lgc.value	0	
target_Demlf_Per_EtatMt_Cnt_u08.value	3	

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Name	Input Value		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cn	nt_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cn	t_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	125351	125351	✓
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	125351	125351	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace					
Actual Function	Expected Function	Count	Result		
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	•	

Test Step 2.6 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	4		
Time_ms_T_u32	252315		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	4		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1	1	
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	:_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	125351	125351	~
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	125351	125351	~
CTCInhibitionCmm_Cnt_M_u32	0	0	~
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				V
Actual Function	Expected Function	Count	Result	
Rte_Call_Ap_DemIf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	~

Test Step 2.7 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4		
Time_ms_T_u32	1352463		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	5		
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	0	0	~
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	~
CTCInhibitionCmm_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				V
Actual Function Count Expected Function				Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>



Test Step 2.8 (Repeat Count = 1)			✓
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ign	ition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	324253		
target_DemIf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	0		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt_	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	~
CTCInhibitionBsi_Cnt_M_u32	0	0	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	0	0	~
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•

Test Step 2.9 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ign	ition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	0		
Time_ms_T_u32	676575		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_EtatMt_Cnt_u08.value	15		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	~
CTCInhibitionBsi_Cnt_M_u32	0	0	✓
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	~
CTCInhibitionCmm_Cnt_M_u32	0	0	✓
CTCInhibitionEsc_Cnt_M_u32	4294967295	4294967295	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>

Test Step 2.10 (Repeat Count = 1)			
Name	Input Value		
Rte_Call_Ap_DemIf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	32426532		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_EtatMt_Cnt_u08.value	11		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1		
target_Rte_Inst_Ap_DemIf.DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	1352463	1352463	•
CTCInhibitionBsi_Cnt_M_u32	0	0	•
CTCInhibitionCav_Cnt_M_u32	1352463	1352463	•
CTCInhibitionCmm_Cnt_M_u32	0	0	•
CTCInhibitionEsc Cnt M u32	4294967295	4294967295	•



Test Step Call Trace					
	Actual Function	Count	Expected Function	Count	Result
	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
	Rte Mode An Demlf SystemState Mode	1	Rte Mode An Demif SystemState Mode	1	<b>V</b>

Test Step 2.11 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	0		
Time_ms_T_u32	57742		
target_Demlf_Per_CTerm_Cnt_lgc.value	0		
target_Demlf_Per_EtatMt_Cnt_u08.value	6		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	57742	57742	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	57742	57742	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	57742	57742	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	57742	57742	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	57742	57742	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>

Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Igr	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1	1		
Time_ms_T_u32	45			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	7	7		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt_	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	45	45	~	
CTCInhibitionBsi_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionCav_Cnt_M_u32	45	45	~	
CTCInhibitionCmm_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionEsc Cnt M u32	45	45	<b>✓</b>	

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>	



Test Step 2.13 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2	2		
Time_ms_T_u32	7574621	7574621		
target_Demlf_Per_CTerm_Cnt_lgc.value	1			
target_Demlf_Per_EtatMt_Cnt_u08.value	8			
target_Rte_Call_Ap_DemIf_Ignition_OP_GET_signal	1			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	:_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	45	45	~	
CTCInhibitionBsi_Cnt_M_u32	45	45	~	
CTCInhibitionCav_Cnt_M_u32	45	45	~	
CTCInhibitionCmm_Cnt_M_u32	45	45	<b>✓</b>	
CTCInhibitionEsc_Cnt_M_u32	45	45	~	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_Demlf_SystemState_Mode	1	Rte_Mode_Ap_Demlf_SystemState_Mode	1	•

Test Step 2.14 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_Demlf_SystemState_Mode()	3			
Time_ms_T_u32	5785			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	9			
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0			
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	5785	5785	~	
CTCInhibitionBsi_Cnt_M_u32	5785	5785	✓	
CTCInhibitionCav_Cnt_M_u32	5785	5785	~	
CTCInhibitionCmm_Cnt_M_u32	5785	5785	~	
CTCInhibitionEsc_Cnt_M_u32	5785	5785	<b>✓</b>	

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~	
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>	

Test Step 2.15 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	4		
Time_ms_T_u32	14165		
target_Demlf_Per_CTerm_Cnt_lgc.value	1		
target_Demlf_Per_EtatMt_Cnt_u08.value	10		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_Demlf_Per_CTerm_Cnt	:_lgc	
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_Demlf_Per_EtatMt_Cnt	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	14165	14165	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	14165	14165	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionEsc_Cnt_M_u32	14165	14165	<b>✓</b>



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte Mode An Demlf SystemState Mode	1	Rte Mode An Demif SystemState Mode	1	<b>V</b>

Test Step 2.16 (Repeat Count = 1)			•
Name	Input Value		
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_DemIf_Igr	nition_OP_GET_signal	
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	1		
Time_ms_T_u32	415241		
target_DemIf_Per_CTerm_Cnt_lgc.value	1		
target_DemIf_Per_EtatMt_Cnt_u08.value	13		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	0		
target_Rte_Inst_Ap_DemIf_DemIf_Per_CTerm_Cnt_Igc	target_Demlf_Per_CTerm_Cnt	_lgc	
target_Rte_Inst_Ap_DemIf.DemIf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08	
Name	Actual Value	Expected Value	Result
CTCInhibitionAas_Cnt_M_u32	415241	415241	<b>✓</b>
CTCInhibitionBsi_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionCav_Cnt_M_u32	415241	415241	<b>✓</b>
CTCInhibitionCmm_Cnt_M_u32	5785	5785	<b>✓</b>
CTCInhibitionEsc Cnt M u32	14165	14165	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_DemIf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>

Name	Input Value			
Rte_Call_Ap_Demlf_Ignition_OP_GET(signal)	target_Rte_Call_Ap_Demlf_Ign	target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal		
Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf	target_Rte_Inst_Ap_DemIf		
Rte_Mode_Ap_DemIf_SystemState_Mode()	2			
Time_ms_T_u32	213526			
target_Demlf_Per_CTerm_Cnt_lgc.value	0			
target_Demlf_Per_EtatMt_Cnt_u08.value	12	12		
target_Rte_Call_Ap_Demlf_Ignition_OP_GET_signal	1	1		
target_Rte_Inst_Ap_Demlf.Demlf_Per_CTerm_Cnt_lgc	target_DemIf_Per_CTerm_Cnt	_lgc		
target_Rte_Inst_Ap_Demlf.Demlf_Per_EtatMt_Cnt_u08	target_DemIf_Per_EtatMt_Cnt_	_u08		
Name	Actual Value	Expected Value	Result	
CTCInhibitionAas_Cnt_M_u32	415241	415241	~	
CTCInhibitionBsi_Cnt_M_u32	5785	5785	~	
CTCInhibitionCav_Cnt_M_u32	415241	415241	~	
CTCInhibitionCmm_Cnt_M_u32	5785	5785	<b>✓</b>	
CTCInhibitionEsc Cnt M u32	14165	14165	<b>✓</b>	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_Ap_Demlf_Ignition_OP_GET	1	Rte_Call_Ap_Demlf_Ignition_OP_GET	1	~
Rte_Mode_Ap_DemIf_SystemState_Mode	1	Rte_Mode_Ap_DemIf_SystemState_Mode	1	<b>✓</b>

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Demlf\_DTCStatusChanged

Project	Demlf
Module	Demlf
Test Object	Demlf DTCStatusChanged

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlflutp\contract -I\$(PROJECTROOT)\Demlflutp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	<pre>\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5</pre>
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	<pre>\$(ProgramFiles)\pls\UDE 4.4</pre>
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

Demlf\_DTCStatusChanged

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Attributes

Name

Value

Workspace File

D:\Synergy\_Work\_Area\PSA\_CMP\_05.01.01\_DemIf\UnitTestEnv\config\UDE\_TMS570\_DEBUG.WSP



```
Test Case 1: Metrics Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 1.1 3296.00 Cycles
TS 1.2 2545.00 Cycles
TS 1.2 2545.00 Cycles

TS1.1"Shortest Path:
((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16) ==> TRUE &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08) ==> FALSE)
(DTCFound_Cnt_T_lgc == TRUE ) ==> FALSE"

TS1.2"Longest Path:
((Dem_DTCNumberTable[i] == DTCNumber_Cnt_T_u16) &&
(Dem_DTC_FTB_Table[i] == DTCFTB_Cnt_T_u08) ) ==> TRUE
(DTCFound_Cnt_T_lgc == TRUE ) ==> TRUE
(DTCFound_Cnt_T_lgc == TRUE ) ==> TRUE
(CTCFailedBuf_Cnt_M_lgc[i] == DTCHB_CNT_U08) == D_FAILBITMASK_CNT_U08 ) ==> FALSE
```

Test Step 1.1 (Repeat Count = 1)	Innut Value	
Name	Input Value	
TCFailedBuf_Cnt_M_lgc[0]	0	
TCFailedBuf_Cnt_M_lgc[1]	0	
TCFailedBuf_Cnt_M_lgc[2]	0	
TCFailedBuf_Cnt_M_lgc[3]	0	
TCFailedBuf_Cnt_M_lgc[4]	0	
TCFailedBuf_Cnt_M_lgc[5]	0	
TCFailedBuf_Cnt_M_lgc[6]	0	
TCFailedBuf_Cnt_M_lgc[7]	0	
TCFailedBuf_Cnt_M_lgc[8]	0	
TCFailedBuf_Cnt_M_lgc[9]	0	
TCFailedBuf_Cnt_M_lgc[10]	0	
TCFailedBuf_Cnt_M_lgc[11]	0	
ΓCFailedBuf_Cnt_M_lgc[12]	0	
TCFailedBuf_Cnt_M_lgc[13]	0	
TCFailedBuf_Cnt_M_lgc[14]	0	
TCFailedBuf_Cnt_M_lgc[15]	0	
TCFailedBuf_Cnt_M_lgc[16]	0	
FCFailedBuf_Cnt_M_lgc[17]	0	
TCFailedBuf_Cnt_M_lgc[18]	0	
FCFailedBuf_Cnt_M_lgc[19]	0	
TCFailedBuf_Cnt_M_lgc[20]	0	
CFailedBuf_Cnt_M_lgc[21]	0	
CFailedBuf_Cnt_M_lgc[22]	0	
TCFailedBuf_Cnt_M_lgc[23]	0	
TCFailedBuf_Cnt_M_lgc[24]	0	
TCFailedBuf_Cnt_M_lgc[25]	0	
TCFailedBuf_Cnt_M_lgc[26]	0	
TCFailedBuf_Cnt_M_lgc[27]	0	
CFailedBuf_Cnt_M_lgc[28]	0	
CFailedBuf_Cnt_M_lgc[29]	0	
ΓCFailedBuf_Cnt_M_lgc[30]	0	
FCFailedBuf_Cnt_M_lgc[31]	0	
TCFailedBuf_Cnt_M_lgc[32]	0	
TCFailedBuf_Cnt_M_lgc[33]	0	
TCFailedBuf_Cnt_M_Igc[34]	0	
TCFailedBuf_Cnt_M_lgc[35]	0	
TCFailedBuf_Cnt_M_lgc[36]	0	
TCFailedBuf_Cnt_M_lgc[37]	0	
FCFailedBuf_Cnt_M_lgc[38]	0	
FCFailedBuf_Cnt_M_lgc[39]	0	
	0	
CFailedBuf_Cnt_M_lgc[40]	0	
FCFailedBuf_Cnt_M_lgc[41]	0	
FCFailedBuf_Cnt_M_lgc[42]		
CFailedBuf_Cnt_M_lgc[43]	0	
CFailedBuf_Cnt_M_lgc[44]	0	
TCFailedBuf_Cnt_M_lgc[45]	0	
TCFailedBuf_Cnt_M_lgc[46]	0	
TCFailedBuf_Cnt_M_lgc[47]	0	
TCFailedBuf_Cnt_M_lgc[48]	0	
CFailedBuf_Cnt_M_lgc[49]	0	
TCFailedBuf_Cnt_M_lgc[50]	0	
TCFailedBuf_Cnt_M_lgc[51]	0	

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0 0
CTCFailedBuf_Cnt_M_lgc[61] CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_gc[63]	0
CTCFailedBuf Cnt M Igc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0 0
CTCFailedBuf_Cnt_M_lgc[74] CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3] Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14]	0 0
Dem_DTCNumberTable[14]	0
Dem DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0 0
Dem_DTCNumberTable[25] Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0 0
Dem_DTCNumberTable[37] Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0

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Demlf_DTCStatusChanged	MACI	COL
Name	Input Value	
Dem_DTCNumberTable[43]	0	
Dem_DTCNumberTable[44]	0	
Dem_DTCNumberTable[45]	0	
Dem_DTCNumberTable[46]	0	
Dem_DTCNumberTable[47]	0	
Dem_DTCNumberTable[48]	0	
Dem_DTCNumberTable[49]	0	
Dem_DTCNumberTable[50]	0	
Dem_DTCNumberTable[51]	0	
Dem_DTCNumberTable[52]	0	
Dem_DTCNumberTable[53]	0	
Dem_DTCNumberTable[54]	0	
Dem_DTCNumberTable[55]	0	
Dem_DTCNumberTable[56]	0 0	
Dem_DTCNumberTable[57] Dem_DTCNumberTable[58]	0	
Dem_DTCNumberTable[56]	0	
Dem_DTCNumberTable[60]	0	
Dem_DTCNumberTable[61]	0	
Dem_DTCNumberTable[62]	0	
Dem DTCNumberTable[63]	0	
Dem_DTCNumberTable[64]	0	
Dem_DTCNumberTable[65]	0	
Dem_DTCNumberTable[66]	0	
Dem_DTCNumberTable[67]	0	
Dem_DTCNumberTable[68]	0	
Dem_DTCNumberTable[69]	0	
Dem_DTCNumberTable[70]	0	
Dem_DTCNumberTable[71]	0	
Dem_DTCNumberTable[72]	0	
Dem_DTCNumberTable[73]	0	
Dem_DTCNumberTable[74]	0	
Dem_DTCNumberTable[75]	0	
Dem_DTCNumberTable[76]	0	
Dem_DTC_FTB_Table[0]	255	
Dem_DTC_FTB_Table[1]	255	
Dem_DTC_FTB_Table[2] Dem_DTC_FTB_Table[3]	255 255	
Dem_DTC_FTB_Table[3]	255	
Dem DTC FTB Table[5]	255	
Dem_DTC_FTB_Table[6]	255	
Dem_DTC_FTB_Table[7]	255	
Dem_DTC_FTB_Table[8]	255	
Dem_DTC_FTB_Table[9]	255	
Dem_DTC_FTB_Table[10]	255	
Dem_DTC_FTB_Table[11]	255	
Dem_DTC_FTB_Table[12]	255	
Dem_DTC_FTB_Table[13]	255	
Dem_DTC_FTB_Table[14]	255	
Dem_DTC_FTB_Table[15]	255	
Dem_DTC_FTB_Table[16]	255	
Dem_DTC_FTB_Table[17]	255	
Dem_DTC_FTB_Table[18]	255	
Dem_DTC_FTB_Table[19]	255	
Dem_DTC_FTB_Table[20]	255	
Dem_DTC_FTB_Table[21]	255	
Dem_DTC_FTB_Table[22]	255	
Dem_DTC_FTB_Table[23]	255	
Dem_DTC_FTB_Table[24]	255	
Dem_DTC_FTB_Table[25]	255 255	
Dem_DTC_FTB_Table[26] Dem_DTC_FTB_Table[27]	255	
Dem_DTC_FTB_Table[27]	255	
Dem_DTC_FTB_Table[29]	255	
Dem_DTC_FTB_Table[30]	255	
Dem_DTC_FTB_Table[30]	255	
Dem_DTC_FTB_Table[31]	255	
Dem_DTC_FTB_Table[33]	255	
Dem_DTC_FTB_Table[34]	255	
	255	
Delli DTC FTB Table[35]		
	255	
Dem_DTC_FTB_Table[35] Dem_DTC_FTB_Table[36] Dem_DTC_FTB_Table[37]		

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Name	Input Value		
Dem_DTC_FTB_Table[39]	255		
Dem_DTC_FTB_Table[40]	255		
Dem_DTC_FTB_Table[41]	255		
Dem_DTC_FTB_Table[42]	255		
Dem_DTC_FTB_Table[43] Dem_DTC_FTB_Table[44]	255 255		
Dem_DTC_FTB_Table[45]	255		
Dem_DTC_FTB_Table[46]	255		
Dem_DTC_FTB_Table[47]	255		
Dem_DTC_FTB_Table[48]	255		
Dem_DTC_FTB_Table[49]	255 255		
Dem_DTC_FTB_Table[50] Dem_DTC_FTB_Table[51]	255		
Dem_DTC_FTB_Table[52]	255		
Dem_DTC_FTB_Table[53]	255		
Dem_DTC_FTB_Table[54]	255		
Dem_DTC_FTB_Table[55]	255		
Dem_DTC_FTB_Table[56]	255 255		
Dem_DTC_FTB_Table[57] Dem_DTC_FTB_Table[58]	255		
Dem_DTC_FTB_Table[59]	255		
Dem_DTC_FTB_Table[60]	255		
Dem_DTC_FTB_Table[61]	255		
Dem_DTC_FTB_Table[62]	255		
Dem_DTC_FTB_Table[63]	255		
Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65]	255 255		
Dem_DTC_FTB_Table[66]	255		
Dem_DTC_FTB_Table[67]	255		
Dem_DTC_FTB_Table[68]	255		
Dem_DTC_FTB_Table[69]	255		
Dem_DTC_FTB_Table[70]	255		
Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	255 255		
Dem_DTC_FTB_Table[73]	255		
Dem_DTC_FTB_Table[74]	255		
Dem_DTC_FTB_Table[75]	255		
Dem_DTC_FTB_Table[76]	255		l=
Dem_DTC_FTB_Table[76]  Name	255 Actual Value	Expected Value	Result
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	Actual Value	0	Result
Dem_DTC_FTB_Table[76]  Name	255 Actual Value	•	~
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]	Actual Value 0 0	0	· ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]	Actual Value 0 0 0 0 0	0 0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]	255 Actual Value 0 0 0 0 0 0 0	0 0 0 0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]	255 Actual Value 0 0 0 0 0 0 0 0	0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]	255 Actual Value 0 0 0 0 0 0 0	0 0 0 0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]	255 Actual Value 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]	255 Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]	255 Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]	255 Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[17]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]	255  Actual Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[36]	0	0	✓
CTCFailedBuf_Cnt_M_Igc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[39]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[40]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[41]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[42]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_Igc[47]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[48]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[52]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[53]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[54]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[55]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[56]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[57]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[58]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[59]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[60]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[61]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[62]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[63]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[64]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	✓
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	_

Test Step 1.2 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
	1
CTCFailedBuf_Cnt_M_lgc[25]	
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	
CTCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	1
	1
CTCFailedBuf_Cnt_M_lgc[44]	
CTCFailedBuf_Cnt_M_lgc[45]	1
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	1
CTCFailedBuf_Cnt_M_lgc[49]	1
CTCFailedBuf_Cnt_M_lgc[50]	1
CTCFailedBuf_Cnt_M_lgc[51]	1
CTCFailedBuf_Cnt_M_lgc[52]	1
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
	1
CTCFailedBuf_Cnt_M_lgc[63]	
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	1
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	1
CTCFailedBuf_Cnt_M_lgc[69]	1
CTCFailedBuf_Cnt_M_lgc[70]	1
CTCFailedBuf_Cnt_M_lgc[71]	1
CTCFailedBuf Cnt M lgc[72]	1
CTCFailedBuf_Cnt_M_lgc[73]	1
CTCFailedBuf_Cnt_M_lgc[74]	1
CTCFailedBuf_Cnt_M_lgc[75]	1
CTCFailedBuf_Cnt_M_lgc[76]	1
CTCFailed_Cnt_M_lgc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
	0
Dem_DTCNumberTable[0]	
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[4] Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[5]	0

Dem\_DTCNumberTable[30]

Dem\_DTCNumberTable[31]

Dem\_DTCNumberTable[32]

Dem\_DTCNumberTable[33]

Dem\_DTCNumberTable[34]

Dem\_DTCNumberTable[35]

Dem DTCNumberTable[36]

Dem\_DTCNumberTable[37]

Dem DTCNumberTable[38]

Dem\_DTCNumberTable[39]

Dem DTCNumberTable[40]

Dem\_DTCNumberTable[41]

Dem\_DTCNumberTable[42]

Dem\_DTCNumberTable[43]

Dem\_DTCNumberTable[44]

Dem\_DTCNumberTable[45]
Dem\_DTCNumberTable[46]

Dem\_DTCNumberTable[47]

Dem\_DTCNumberTable[48]

Dem\_DTCNumberTable[49]
Dem\_DTCNumberTable[50]

Dem\_DTCNumberTable[51]

Dem\_DTCNumberTable[52]

Dem\_DTCNumberTable[53]

Dem DTCNumberTable[54]

Dem\_DTCNumberTable[55]

Dem DTCNumberTable[56]

Dem\_DTCNumberTable[57]

Dem\_DTCNumberTable[58]

Dem\_DTCNumberTable[59]

Dem\_DTCNumberTable[60]

Dem\_DTCNumberTable[61]

Dem\_DTCNumberTable[62]

Dem\_DTCNumberTable[63]

Dem\_DTCNumberTable[64]

Dem\_DTCNumberTable[65]

Dem\_DTCNumberTable[66]

Dem\_DTCNumberTable[67]
Dem\_DTCNumberTable[68]

Dem\_DTCNumberTable[69]
Dem\_DTCNumberTable[70]

Dem\_DTCNumberTable[71]

Dem\_DTCNumberTable[72]

Dem\_DTCNumberTable[73]

Dem\_DTCNumberTable[74]

Dem\_DTCNumberTable[75]

Dem\_DTCNumberTable[76]

Dem\_DTC\_FTB\_Table[0]

Dem\_DTC\_FTB\_Table[1]

Dem\_DTC\_FTB\_Table[2]

Dem\_DTC\_FTB\_Table[3]

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[8] 0 Dem\_DTCNumberTable[9] 0 Dem DTCNumberTable[10] 0 Dem\_DTCNumberTable[11] 0 Dem DTCNumberTable[12] 0 Dem\_DTCNumberTable[13] 0 Dem\_DTCNumberTable[14] 0 Dem\_DTCNumberTable[15] 0 Dem\_DTCNumberTable[16] 0 Dem\_DTCNumberTable[17] 0 Dem\_DTCNumberTable[18] 0 Dem\_DTCNumberTable[19] 0 Dem\_DTCNumberTable[20] 0 Dem\_DTCNumberTable[21] 0 Dem\_DTCNumberTable[22] 0 Dem\_DTCNumberTable[23] 0 Dem\_DTCNumberTable[24] 0 Dem\_DTCNumberTable[25] 0 Dem\_DTCNumberTable[26] 0 Dem\_DTCNumberTable[27] 0 Dem\_DTCNumberTable[28] 0 Dem\_DTCNumberTable[29] 0

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Demlf\_DTCStatusChanged

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Input Value Dem\_DTC\_FTB\_Table[4] 0 Dem\_DTC\_FTB\_Table[5] 0 Dem\_DTC\_FTB\_Table[6] 0 Dem\_DTC\_FTB\_Table[7] 0 Dem\_DTC\_FTB\_Table[8] 0 Dem\_DTC\_FTB\_Table[9] 0 Dem\_DTC\_FTB\_Table[10] 0 Dem\_DTC\_FTB\_Table[11] 0 Dem\_DTC\_FTB\_Table[12] 0 Dem\_DTC\_FTB\_Table[13] n Dem\_DTC\_FTB\_Table[14] 0 Dem\_DTC\_FTB\_Table[15] n Dem\_DTC\_FTB\_Table[16] 0 Dem DTC FTB Table[17] n Dem\_DTC\_FTB\_Table[18] 0 Dem\_DTC\_FTB\_Table[19] 0 Dem\_DTC\_FTB\_Table[20] 0 Dem\_DTC\_FTB\_Table[21] 0 Dem\_DTC\_FTB\_Table[22] 0 Dem\_DTC\_FTB\_Table[23] 0 Dem\_DTC\_FTB\_Table[24] 0 Dem\_DTC\_FTB\_Table[25] 0 Dem\_DTC\_FTB\_Table[26] 0 Dem\_DTC\_FTB\_Table[27] 0 Dem\_DTC\_FTB\_Table[28] 0 Dem\_DTC\_FTB\_Table[29] 0 Dem\_DTC\_FTB\_Table[30] 0 Dem\_DTC\_FTB\_Table[31] 0 Dem DTC FTB Table[32] 0 Dem\_DTC\_FTB\_Table[33] 0 Dem DTC FTB Table[34] 0 Dem\_DTC\_FTB\_Table[35] 0 Dem DTC FTB Table[36] 0 Dem\_DTC\_FTB\_Table[37] 0 Dem\_DTC\_FTB\_Table[38] 0 Dem\_DTC\_FTB\_Table[39] 0 Dem\_DTC\_FTB\_Table[40] 0 Dem\_DTC\_FTB\_Table[41] 0 Dem\_DTC\_FTB\_Table[42] 0 Dem DTC\_FTB\_Table[43] 0 Dem\_DTC\_FTB\_Table[44] 0 Dem DTC FTB Table[45] 0 Dem\_DTC\_FTB\_Table[46] 0 Dem\_DTC\_FTB\_Table[47] 0 Dem\_DTC\_FTB\_Table[48] 0 Dem\_DTC\_FTB\_Table[49] 0 Dem\_DTC\_FTB\_Table[50] 0 Dem\_DTC\_FTB\_Table[51] 0 Dem\_DTC\_FTB\_Table[52] 0 Dem\_DTC\_FTB\_Table[53] 0 Dem\_DTC\_FTB\_Table[54] 0 Dem\_DTC\_FTB\_Table[55] 0 Dem\_DTC\_FTB\_Table[56] 0 Dem\_DTC\_FTB\_Table[57] 0 Dem\_DTC\_FTB\_Table[58] 0 Dem\_DTC\_FTB\_Table[59] 0 0 Dem\_DTC\_FTB\_Table[60] Dem\_DTC\_FTB\_Table[61] 0 Dem\_DTC\_FTB\_Table[62] 0 Dem\_DTC\_FTB\_Table[63] 0 Dem\_DTC\_FTB\_Table[64] 0 Dem\_DTC\_FTB\_Table[65] 0 Dem\_DTC\_FTB\_Table[66] 0 Dem\_DTC\_FTB\_Table[67] 0 Dem\_DTC\_FTB\_Table[68] 0 Dem DTC FTB Table[69] 0 Dem\_DTC\_FTB\_Table[70] 0 Dem DTC FTB Table[71] 0 Dem\_DTC\_FTB\_Table[72] 0 Dem\_DTC\_FTB\_Table[73] 0 Dem\_DTC\_FTB\_Table[74] 0 Dem\_DTC\_FTB\_Table[75] 0 Dem\_DTC\_FTB\_Table[76] 0

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Name				
COTON-MONE, COLUN, Mag 20 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			•	
CD-SinceApt_Cor_M_yeq    CD-SinceApt_Cor_M_y				-
CICCHARDAL COM, Mysell 1		0	0	~
COT-Selection, Cott, Majord  COT-Selection, C	CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CICCHARGE OF M, 1969  CICCHARGE OF M, 1969  CICCHARGE OF M, 1967	CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CICTRIAMED CM M 1970 CICTRIAMED CM M 1971 CICTRIAMED CM M 1972 CICTRIAMED CM M 1973 CICTRIAMED CM M 1974 CICTRIAME	CTCFailedBuf_Cnt_M_lgc[4]	1	1	-
COT-Basedu, Cott, M., 1981  COT-Basedu, Cott, M., 1982  COT-Basedu, Cott, M., 1983  COT-Basedu, Cott, M., 1984  CO	CTCFailedBuf_Cnt_M_lgc[5]	1	1	~
CICCHICAGE CHE M 1989 1	CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CITCHARDIST CAN 19,591  1	CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CICS-alesting Core, Mag 1981   1	CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFaieblid CH, M, Mgd11  CTCFaieblid CH, M, M, Mgd21  CTCFaieblid CH, M, M, Mgd31  CTCFaieblid CH, M,	CTCFailedBuf_Cnt_M_lgc[9]	1	1	<b>✓</b>
CTCPaintall Cett M, Mg-913   1	CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CICCR-SIGNUD, CM, Mg-1913 1	CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCPainaGed_Cort_M_M_GETS		1	1	~
CTCS-instellar Core   M. 19210   1	CTCFailedBuf_Cnt_M_lgc[13]	1	1	•
CTCFaseBull Crit M, pdf16   1   1   1   V   V   V   V   V   V   V		1	1	~
CTCFaseSed_Cot_M_get[0]	CTCFailedBuf Cnt M lgc[15]	1	1	<b>✓</b>
CTCFaieddd Crit M, pdf19		1	1	~
CTCFaineSetU.CTM, Mgc190		1	1	<b>✓</b>
CICFaeodust_Cit, M. jet20		1	1	~
CFCFaieAbd Cmt M p6210				<b>~</b>
CTCFaiedful, Cott, M, Sept21				_
CITCPaceMart Cott M. 19620 1 1 1 1				-
CICFaindbuf, Cit, M., 19629				
CTCFalesburd_CTM_bigst31				-
CTCFaledBuf_CTM_blgq27				
CTCFaledbut_Cnm_M_gd28				-
CTCFaledbuf, CM, M, 19d28				
CTCFaledbut_CN_M_9ct29				
CTCFaledBuf Cnt M   pqc28    1				
CTCFaledBut_Cnt_M_lgd31				
CTCFaledBut_Cnt_M_logt31				
CTCFaledBuf_Cnt_M_lgc(32)  CTCFaledBuf_Cnt_M_lgc(33)  CTCFaledBuf_Cnt_M_lgc(43)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(44)  CTCFaledBuf_Cnt_M_lgc(45)  CTCFaledBuf_Cnt_M_lgc(46)  CTCFaledBuf_Cnt_M_lgc				-
CTCFaledBuf_Cnt_Migct33				
CTCFaledBuf_Cnt_M_lgq53   1				-
CTCFaledBuf_Cnt_M_lgq35    1				
CTCFaledBuf_Cnt_M_lgq38  1 1 1 1				
CTCFailedBuf_Cnt_M_lgc(37)   1				
CTCFaiedBuf_Cnt_M_lgc(38)				
CTCFailedBuf_Cnt_M_lgc[39]   1				~
CTCFaledBuf_Cnt_M_lgcf40] 1 1 1 1				-
CTCFailedBuf_Cnt_M_lgc[41]				~
CTCFailedBuf_Cnt_Migc[42]				~
CTCFailedBuf_Cnt_M_lgcl43				~
CTCFailedBuf_Cnt_M_lgc(44)  1				
CTCFailedBuf_Cnt_M_lgc(45)				~
CTCFailedBuf_Cnt_M_lgc[46]       1       1         CTCFailedBuf_Cnt_M_lgc[48]       1       1         CTCFailedBuf_Cnt_M_lgc[49]       1       1         CTCFailedBuf_Cnt_M_lgc[50]       1       1         CTCFailedBuf_Cnt_M_lgc[51]       1       1         CTCFailedBuf_Cnt_M_lgc[52]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_l				~
CTCFailedBuf_Cnt_M_lgc[47]       1       1         CTCFailedBuf_Cnt_M_lgc[48]       1       1         CTCFailedBuf_Cnt_M_lgc[50]       1       1         CTCFailedBuf_Cnt_M_lgc[50]       1       1         CTCFailedBuf_Cnt_M_lgc[51]       1       1         CTCFailedBuf_Cnt_M_lgc[52]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[45]			~
CTCFailedBuf_Cnt_M_lgc[48]       1       1       1         CTCFailedBuf_Cnt_M_lgc[49]       1       1       1         CTCFailedBuf_Cnt_M_lgc[50]       1       1       1         CTCFailedBuf_Cnt_M_lgc[51]       1       1       1         CTCFailedBuf_Cnt_M_lgc[52]       1       1       1         CTCFailedBuf_Cnt_M_lgc[53]       1       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       2         CTCFailedBuf_Cnt_M_lgc[66]       1       1       1 <td< td=""><td></td><td></td><td></td><td>~</td></td<>				~
CTCFailedBuf_Cnt_M_lgc[49]       1       1          CTCFailedBuf_Cnt_M_lgc[50]       1       1           CTCFailedBuf_Cnt_M_lgc[51]       1       1  .				
CTCFailedBuf_Cnt_M_lgc[50]       1       1          CTCFailedBuf_Cnt_M_lgc[51]       1       1          CTCFailedBuf_Cnt_M_lgc[52]       1       1          CTCFailedBuf_Cnt_M_lgc[53]       1       1          CTCFailedBuf_Cnt_M_lgc[54]       1       1          CTCFailedBuf_Cnt_M_lgc[55]       1       1          CTCFailedBuf_Cnt_M_lgc[56]       1       1          CTCFailedBuf_Cnt_M_lgc[57]       1       1          CTCFailedBuf_Cnt_M_lgc[58]       1       1          CTCFailedBuf_Cnt_M_lgc[60]       1       1          CTCFailedBuf_Cnt_M_lgc[60]       1       1          CTCFailedBuf_Cnt_M_lgc[61]       1       1          CTCFailedBuf_Cnt_M_lgc[62]       1       1          CTCFailedBuf_Cnt_M_lgc[63]       1       1          CTCFailedBuf_Cnt_M_lgc[63]       1       1          CTCFailedBuf_Cnt_M_lgc[66]       1       1          CTCFailedBuf_Cnt_M_lgc[66]       1       1          CTCFailedBuf_Cnt_M_lgc[68]       1       1       .	CTCFailedBuf_Cnt_M_lgc[48]			
CTCFailedBuf_Cnt_M_lgc[51]       1       1          CTCFailedBuf_Cnt_M_lgc[52]       1       1           CTCFailedBuf_Cnt_M_lgc[53]       1       1  .	CTCFailedBuf_Cnt_M_lgc[49]	1	1	~
CTCFailedBuf_Cnt_M_lgc[52]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[53]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[54]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[55]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[56]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[57]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[58]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[59]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[60]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[61]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[62]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[63]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[64]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[65]       1       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[66]       1       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[68]       1       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[68]       1       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[69]       1	CTCFailedBuf_Cnt_M_lgc[50]		1	
CTCFailedBuf_Cnt_M_lgc[53]       1       1         CTCFailedBuf_Cnt_M_lgc[54]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_l	CTCFailedBuf_Cnt_M_lgc[51]	1	1	~
CTCFailedBuf_Cnt_M_lgc[54]       1       1          CTCFailedBuf_Cnt_M_lgc[55]       1       1           CTCFailedBuf_Cnt_M_lgc[56]       1       1  .	CTCFailedBuf_Cnt_M_lgc[52]		1	~
CTCFailedBuf_Cnt_M_lgc[55]       1       1         CTCFailedBuf_Cnt_M_lgc[56]       1       1         CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1	CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]       1       1          CTCFailedBuf_Cnt_M_lgc[57]       1       1          CTCFailedBuf_Cnt_M_lgc[58]       1       1          CTCFailedBuf_Cnt_M_lgc[59]       1       1           CTCFailedBuf_Cnt_M_lgc[60]       1       1       1           CTCFailedBuf_Cnt_M_lgc[61]       1       1       1 </td <td>CTCFailedBuf_Cnt_M_lgc[54]</td> <td>1</td> <td>1</td> <td>~</td>	CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]       1       1          CTCFailedBuf_Cnt_M_lgc[57]       1       1          CTCFailedBuf_Cnt_M_lgc[58]       1       1          CTCFailedBuf_Cnt_M_lgc[69]       1       1           CTCFailedBuf_Cnt_M_lgc[61]       1       1  .	CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1	1	~
CTCFailedBuf_Cnt_M_lgc[58]       1       1         CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[59]       1       1         CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1	1	~
CTCFailedBuf_Cnt_M_lgc[60]       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[61]       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1			1	~
CTCFailedBuf_Cnt_M_lgc[62]       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1		1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[63]       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[64]       1       1         CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				<b>~</b>
CTCFailedBuf_Cnt_M_lgc[65]       1       1         CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				~
CTCFailedBuf_Cnt_M_lgc[66]       1       1         CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				<b>V</b>
CTCFailedBuf_Cnt_M_lgc[67]       1       1         CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				
CTCFailedBuf_Cnt_M_lgc[68]       1       1         CTCFailedBuf_Cnt_M_lgc[69]       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       1       1				
CTCFailedBuf_Cnt_M_lgc[69]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[70]       1       1       ✓         CTCFailedBuf_Cnt_M_lgc[71]       1       1       ✓				
CTCFailedBuf_Cnt_M_lgc[70]         1         1         ✓           CTCFailedBuf_Cnt_M_lgc[71]         1         1         ✓				
CTCFailedBuf_Cnt_M_lgc[71]         1         1         ✓				
	O.O. G.CUDUL_OIL_IN_IGG[12]	ı ·	l ·	

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Demlf DTCStatusChanged	1
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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[73]	1	1	~
CTCFailedBuf_Cnt_M_lgc[74]	1	1	~
CTCFailedBuf_Cnt_M_lgc[75]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	1	1	~
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	✓

Test Step Call Trace				<b>✓</b>	
	Actual Function	Count	Expected Function	Count	Result
	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

#### **Test Case 2: Range Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

CPU Cycles:

TS 2.1 2437.00 Cycles
TS 2.2 663.00 Cycles
TS 2.3 3222.00 Cycles
TS 2.4 3208.00 Cycles
TS 2.4 3208.00 Cycles
TS 2.5 3208.00 Cycles
TS 2.6 3208.00 Cycles
TS 2.7 3208.00 Cycles
TS 2.8 3208.00 Cycles
TS 2.9 3208.00 Cycles
TS 2.10 3208.00 Cycles
TS 2.11 3208.00 Cycles
TS 2.11 3208.00 Cycles
TS 2.12 3208.00 Cycles
TS 2.13 3208.00 Cycles
TS 2.14 3208.00 Cycles
TS 2.15 3208.00 Cycles
TS 2.16 3208.00 Cycles
TS 2.17 3208.00 Cycles
TS 2.18 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.19 3208.00 Cycles
TS 2.21 3208.00 Cycles
TS 2.21 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
TS 2.22 3208.00 Cycles
TS 2.23 3208.00 Cycles
TS 2.24 3208.00 Cycles
TS 2.24 3208.00 Cycles

#### Vector Description: Description

TS 2.1All Min TS 2.2All Max TS 2.3DTC==> Min TS 2.4DTC==> Max TS 2.5DTC==> Pos TS 2.6DTCKind==> Min TS 2.7DTCKind==> Max TS 2.8DTCStatusOld==> Min TS 2.9DTCStatusOld==> Max
TS 2.10DTCStatusOld==> Pos TS 2.11DTCStatusNew==> Min TS 2.12DTCStatusNew==> Max TS 2.13DTCStatusNew==> Pos TS 2.14CTCFailedBuf\_Cnt\_M\_lgc[79]==> Min
TS 2.15CTCFailedBuf\_Cnt\_M\_lgc[79]==> Max
TS 2.16CTCFailedBuf\_Cnt\_M\_lgc[79]==> Pos
TS 2.17CTCFailed\_Cnt\_M\_lgc==> Min IS 2.1/CTCFalled\_Cnt\_M\_lgc==> Min
S 2.18CTCFalled\_Cnt\_M\_lgc=> Max
TS 2.19Dem\_DTCNumberTable[79]==> Min
TS 2.20Dem\_DTCNumberTable[79]==> Max
S 2.21Dem\_DTCNumberTable[79]==> Pos
TS 2.22Dem\_DTC\_FTB\_Table[79]==> Min
TS 2.23Dem\_DTC\_FTB\_Table[79]==> Max
TS 2.24Dem\_DTC\_FTB\_Table[79]==> Pos

Test Step 2.1 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0

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	( = = 10=10
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
	0
CTCFailedBuf_Cnt_M_lgc[14]	
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	0
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32]	0
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
	0
CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[39]	0
	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61]	0
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	0
CTCFailedBuf_Cnt_M_lgc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	0
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
	0
Dem_DTCNumberTable[0]	
Dem_DTCNumberTable[0] Dem_DTCNumberTable[1]	0
	0 0

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Name	Input Value
Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[12]	0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19] Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21]	0
Dem_DTCNumberTable[21]	0
Dem DTCNumberTable[23]	0
Dem DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30]	0
Dem_DTCNumberTable[31]	0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39]	0
Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42] Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0
Dem_DTCNumberTable[48]	0
Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57]	0
Dem_DTCNumberTable[58]	0
Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[60]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67] Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[68] Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[70] Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[71] Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0

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Name	Input Value
	•
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem_DTC_FTB_Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
	0
Dem_DTC_FTB_Table[9]	
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
Dem_DTC_FTB_Table[13]	0
	0
Dem_DTC_FTB_Table[14]	
Dem_DTC_FTB_Table[15]	0
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
	0
Dem_DTC_FTB_Table[31]	
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
	0
Dem_DTC_FTB_Table[37]	
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[42]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[44]	0
Dem_DTC_FTB_Table[45]	0
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[49]	0
Dem_DTC_FTB_Table[50]	0
Dem_DTC_FTB_Table[51]	0
Dem_DTC_FTB_Table[52]	0
Dem_DTC_FTB_Table[53]	0
Dem_DTC_FTB_Table[54]	0
Dem_DTC_FTB_Table[55]	0
Dem_DTC_FTB_Table[56]	0
Dem_DTC_FTB_Table[57]	0
Dem_DTC_FTB_Table[58]	0
Dem_DTC_FTB_Table[59]	0
Dem_DTC_FTB_Table[60]	0
Dem_DTC_FTB_Table[61]	0
Dem_DTC_FTB_Table[62]	0
Dem_DTC_FTB_Table[63]	0
Dem_DTC_FTB_Table[64]	0
Dem_DTC_FTB_Table[65]	0
Dem_DTC_FTB_Table[66]	0
Dem_DTC_FTB_Table[67]	0
Dem_DTC_FTB_Table[68]	0
Dem_DTC_FTB_Table[69]	0
Dem_DTC_FTB_Table[70]	0
	0
Dem_DTC_FTB_Table[71]	V

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		(	
Name	Input Value		
Dem_DTC_FTB_Table[72]	0		
Dem_DTC_FTB_Table[73]	0		
Dem_DTC_FTB_Table[74]	0		
Dem_DTC_FTB_Table[75]	0		
Dem_DTC_FTB_Table[76]	0		
Name	Actual Value	Expected Value	Result
		•	Result
CTCFailedBuf_Cnt_M_lgc[0]	0	0	-
CTCFailedBuf_Cnt_M_lgc[1]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[2]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[3]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[4]	0	0	~
CTCFailedBuf_Cnt_M_lgc[5]	0	0	~
CTCFailedBuf_Cnt_M_lgc[6]	0	0	~
CTCFailedBuf_Cnt_M_lgc[7]	0	0	~
CTCFailedBuf_Cnt_M_lgc[8]	0	0	~
CTCFailedBuf_Cnt_M_lgc[9]	0	0	~
CTCFailedBuf_Cnt_M_lgc[10]	0	0	~
CTCFailedBuf_Cnt_M_Igc[11]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[12]	0	0	~
CTCFailedBuf_Cnt_M_lgc[13]	0	0	~
CTCFailedBuf_Cnt_M_lgc[14]	0	0	~
CTCFailedBuf_Cnt_M_lgc[15]	0	0	~
CTCFailedBuf_Cnt_M_lgc[16]	0	0	~
CTCFailedBuf_Cnt_M_lgc[17]	0	0	~
CTCFailedBuf_Cnt_M_lgc[18]	0	0	~
CTCFailedBuf_Cnt_M_lgc[19]	0	0	V
CTCFailedBuf Cnt M Igc[20]	0	0	-
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	-
CTCFailedBuf_Cnt_M_lgc[23]	0	0	· ·
	0	0	
CTCFailedBuf_Cnt_M_lgc[24]			~
CTCFailedBuf_Cnt_M_lgc[25]	0	0	
CTCFailedBuf_Cnt_M_lgc[26]	0	0	
CTCFailedBuf_Cnt_M_lgc[27]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[28]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[29]	0	0	
CTCFailedBuf_Cnt_M_lgc[30]	0	0	~
CTCFailedBuf_Cnt_M_lgc[31]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[32]	0	0	~
CTCFailedBuf_Cnt_M_lgc[33]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_Igc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_Igc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_Igc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	~
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	~
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	0	0	~
CTCFailedBuf_Cnt_M_lgc[54]	0	0	-
CTCFailedBuf_Cnt_M_lgc[55]	0	0	~
CTCFailedBuf_Cnt_M_Igc[56]	0	0	~
CTCFailedBuf_Cnt_M_lgc[57]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[58]	0	0	-
CTCFailedBuf_Cnt_M_lgc[59]	0	0	
CTCFailedBuf_Cnt_M_lgc[60]	0	0	_
	0	0	•
CTCFailedBuf_Cnt_M_lgc[61]	0	0	J
CTCFailedBuf_Cnt_M_lgc[62]	0	0	- 4
CTCFailedBuf_Cnt_M_lgc[63]	0	0	-
CTCFailedBuf_Cnt_M_lgc[64]	0	0	-
CTCFailedBuf_Cnt_M_lgc[65] CTCFailedBuf_Cnt_M_lgc[66]	0	0	
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Demlf\_DTCStatusChanged

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	✓
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt Igc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	•

CTCPainceStur Crit. M. jpc71   1   1   1   1   1   1   1   1   1		
CTCPainedful, Cru, M, 1941    1	Test Step 2.2 (Repeat Count = 1)	
CTCFaledBuff_CTM_Mgd2  1	Name	
CTCFaledBuf_CR_M_IngS]	CTCFailedBuf_Cnt_M_lgc[0]	
CICPalestiful Cott, M. 1945  CICPalestiful Cott, M. 1941  CICPalestiful Cott, M. 1942  CICPalestiful Cott, M. 1943  CICPalestiful Cott, M. 1944  CICPalestiful Co	CTCFailedBuf_Cnt_M_lgc[1]	
CICFaiedbuf_Cn_M_lgclg) 1 CICFaiedbuf_Cn_M_l		
CTCFaiedBuf_Cnt_M_lgc[8]	CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFaiedBuf_Cnt_M_19d7	CTCFailedBuf_Cnt_M_lgc[4]	
CICFailedBuf_Crt_M_lgct0 CICFailedBuf_Crt_M_lgct0 CICFailedBuf_Crt_M_lgct0 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct11 1 CICFailedBuf_Crt_M_lgct11 1 CICFailedBuf_Crt_M_lgct12 CICFailedBuf_Crt_M_lgct13 1 CICFailedBuf_Crt_M_lgct13 1 CICFailedBuf_Crt_M_lgct16 CICFailedBuf_Crt_M_lgct16 CICFailedBuf_Crt_M_lgct17 CICFailedBuf_Crt_M_lgct18 CICFailedBuf_Crt_M_lgct18 CICFailedBuf_Crt_M_lgct18 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct10 CICFailedBuf_Crt_M_lgct20 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct30 1 CICFailedBuf_Crt_M_lgct40 1 CICFailed	CTCFailedBuf_Cnt_M_lgc[5]	1
CICFaiedBuf, Cnt, M, lgd?]  CI	CTCFailedBuf_Cnt_M_lgc[6]	1
CICFalesbur, Crit, M. Jog-10 CICFalesbur, Crit, M. Jog-20 CICFalesbur, Cri	CTCFailedBuf_Cnt_M_lgc[7]	1
CICFailedBuf_Cnt_M_lgc[10] 1 CICFailedBuf_Cnt_M_lgc[11] 1 CICFailedBuf_Cnt_M_lgc[13] 1 CICFailedBuf_Cnt_M_lgc[13] 1 CICFailedBuf_Cnt_M_lgc[14] 1 CICFailedBuf_Cnt_M_lgc[15] 1 CICFailedBuf_Cnt_M_lgc[15] 1 CICFailedBuf_Cnt_M_lgc[15] 1 CICFailedBuf_Cnt_M_lgc[16] 1 CICFailedBuf_Cnt_M_lgc[17] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[18] 1 CICFailedBuf_Cnt_M_lgc[20] 1 CICFailedBuf_Cnt_M_lgc[40] 1 CICFailedBuf_Cnt	CTCFailedBuf_Cnt_M_lgc[8]	1
CICFaiedBuf, Crit, M. Jog(19) CITCFaiedBuf, Crit, M. Jog(18) CITCFaiedBuf, Crit, M. Jog(18) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(19) CICFaiedBuf, Crit, M. Jog(20) CICFaiedBuf, Crit, M. Jog(40) CICF	CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc 12  1 CTCFailedBuf_Cnt_M_lgc 13  1 CTCFailedBuf_Cnt_M_lgc 14  1 CTCFailedBuf_Cnt_M_lgc 15  1 CTCFailedBuf_Cnt_M_lgc 16  1 CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 19  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 22  1 CTCFailedBuf_Cnt_M_lgc 23  1 CTCFailedBuf_Cnt_M_lgc 23  1 CTCFailedBuf_Cnt_M_lgc 25  1 CTCFailedBuf_Cnt_M_lgc 25  1 CTCFailedBuf_Cnt_M_lgc 26  1 CTCFailedBuf_Cnt_M_lgc 27  1 CTCFailedBuf_Cnt_M_lgc 28  1 CTCFailedBuf_Cnt_M_lgc 38  1 CTCFailedBuf_Cnt_M_lgc 48  1	CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFaiedBuf_Cnt_M_lgc[13] 1 CTCFaiedBuf_Cnt_M_lgc[15] 1 CTCFaiedBuf_Cnt_M_lgc[16] 1 CTCFaiedBuf_Cnt_M_lgc[16] 1 CTCFaiedBuf_Cnt_M_lgc[16] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[18] 1 CTCFaiedBuf_Cnt_M_lgc[20] 1 CTCFaiedBuf_Cnt_M_lgc[21] 1 CTCFaiedBuf_Cnt_M_lgc[21] 1 CTCFaiedBuf_Cnt_M_lgc[21] 1 CTCFaiedBuf_Cnt_M_lgc[23] 1 CTCFaiedBuf_Cnt_M_lgc[23] 1 CTCFaiedBuf_Cnt_M_lgc[24] 1 CTCFaiedBuf_Cnt_M_lgc[26] 1 CTCFaiedBuf_Cnt_M_lgc[26] 1 CTCFaiedBuf_Cnt_M_lgc[26] 1 CTCFaiedBuf_Cnt_M_lgc[28] 1 CTCFaiedBuf_Cnt_M_lgc[48] 1	CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc 14  1 CTCFailedBuf_Cnt_M_lgc 15  1 CTCFailedBuf_Cnt_M_lgc 16  1 CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 19  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 21  1 CTCFailedBuf_Cnt_M_lgc 22  1 CTCFailedBuf_Cnt_M_lgc 23  1 CTCFailedBuf_Cnt_M_lgc 24  1 CTCFailedBuf_Cnt_M_lgc 26  1 CTCFailedBuf_Cnt_M_lgc 28  1 CTCFailedBuf_Cnt_M_lgc 30  1 CTCFailedBuf_Cnt_M_lgc 30  1 CTCFailedBuf_Cnt_M_lgc 30  1 CTCFailedBuf_Cnt_M_lgc 35  1 CTCFailedBuf_Cnt_M_lgc 36  1 CTCFailedBuf_Cnt_M_lgc 38  1 CTCFailedBuf_Cnt_M_lgc 40  1	CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[15] 1 CTCFailedBuf_Cnt_M_lgc[16] 1 CTCFailedBuf_Cnt_M_lgc[17] 1 CTCFailedBuf_Cnt_M_lgc[18] 1 CTCFailedBuf_Cnt_M_lgc[18] 1 CTCFailedBuf_Cnt_M_lgc[18] 1 CTCFailedBuf_Cnt_M_lgc[20] 1 CTCFailedBuf_Cnt_M_lgc[21] 1 CTCFailedBuf_Cnt_M_lgc[22] 1 CTCFailedBuf_Cnt_M_lgc[23] 1 CTCFailedBuf_Cnt_M_lgc[23] 1 CTCFailedBuf_Cnt_M_lgc[24] 1 CTCFailedBuf_Cnt_M_lgc[25] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[26] 1 CTCFailedBuf_Cnt_M_lgc[27] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[28] 1 CTCFailedBuf_Cnt_M_lgc[30] 1 CTCFailedBuf_Cnt_M_lgc[40] 1 CTCFailedBuf_Cnt	CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFaledBuf_Cnt_M_lgc[16] 1 CTCFaledBuf_Cnt_M_lgc[18] 1 CTCFaledBuf_Cnt_M_lgc[18] 1 CTCFaledBuf_Cnt_M_lgc[19] 1 CTCFaledBuf_Cnt_M_lgc[20] 1 CTCFaledBuf_Cnt_M_lgc[20] 1 CTCFaledBuf_Cnt_M_lgc[21] 1 CTCFaledBuf_Cnt_M_lgc[22] 1 CTCFaledBuf_Cnt_M_lgc[23] 1 CTCFaledBuf_Cnt_M_lgc[23] 1 CTCFaledBuf_Cnt_M_lgc[23] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[26] 1 CTCFaledBuf_Cnt_M_lgc[28] 1 CTCFaledBuf_Cnt_M_lgc[48] 1	CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc 17  1 CTCFailedBuf_Cnt_M_lgc 18  1 CTCFailedBuf_Cnt_M_lgc 19  1 CTCFailedBuf_Cnt_M_lgc 20  1 CTCFailedBuf_Cnt_M_lgc 40  1	CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFaiedBuf_Cnt_M_lgct17] 1 CTCFaiedBuf_Cnt_M_lgct18] 1 CTCFaiedBuf_Cnt_M_lgct19] 1 CTCFaiedBuf_Cnt_M_lgct20] 1 CTCFaiedBuf_Cnt_M_lgct20] 1 CTCFaiedBuf_Cnt_M_lgct21] 1 CTCFaiedBuf_Cnt_M_lgct22] 1 CTCFaiedBuf_Cnt_M_lgct22] 1 CTCFaiedBuf_Cnt_M_lgct23] 1 CTCFaiedBuf_Cnt_M_lgct24] 1 CTCFaiedBuf_Cnt_M_lgct24] 1 CTCFaiedBuf_Cnt_M_lgct26] 1 CTCFaiedBuf_Cnt_M_lgct27] 1 CTCFaiedBuf_Cnt_M_lgct27] 1 CTCFaiedBuf_Cnt_M_lgct27] 1 CTCFaiedBuf_Cnt_M_lgct27] 1 CTCFaiedBuf_Cnt_M_lgct28] 1 CTCFaiedBuf_Cnt_M_lgct30] 1 CTCFaiedBuf_Cnt_M_lgct30] 1 CTCFaiedBuf_Cnt_M_lgct31] 1 CTCFaiedBuf_Cnt_M_lgct41] 1 CT	CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFaledBuf_Cnt_M_lgc[18]         1           CTCFaledBuf_Cnt_M_lgc[20]         1           CTCFaledBuf_Cnt_M_lgc[21]         1           CTCFaledBuf_Cnt_M_lgc[21]         1           CTCFaledBuf_Cnt_M_lgc[23]         1           CTCFaledBuf_Cnt_M_lgc[23]         1           CTCFaledBuf_Cnt_M_lgc[24]         1           CTCFaledBuf_Cnt_M_lgc[26]         1           CTCFaledBuf_Cnt_M_lgc[27]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[28]         1           CTCFaledBuf_Cnt_M_lgc[30]         1           CTCFaledBuf_Cnt_M_lgc[32]         1           CTCFaledBuf_Cnt_M_lgc[33]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[38]         1           CTCFaledBuf_Cnt_M_lgc[48]         1           CTCFaledBuf_Cnt_M_lgc[48]         1           CTCFaledBuf_Cnt_M_lgc[48]         1 <t< td=""><td></td><td>1</td></t<>		1
CTCFailedBuf_Cnt_M_lgd;21         1           CTCFailedBuf_Cnt_M_lgd;21         1           CTCFailedBuf_Cnt_M_lgd;23         1           CTCFailedBuf_Cnt_M_lgd;23         1           CTCFailedBuf_Cnt_M_lgd;24         1           CTCFailedBuf_Cnt_M_lgd;25         1           CTCFailedBuf_Cnt_M_lgd;26         1           CTCFailedBuf_Cnt_M_lgd;28         1           CTCFailedBuf_Cnt_M_lgd;28         1           CTCFailedBuf_Cnt_M_lgd;29         1           CTCFailedBuf_Cnt_M_lgd;31         1           CTCFailedBuf_Cnt_M_lgd;31         1           CTCFailedBuf_Cnt_M_lgd;32         1           CTCFailedBuf_Cnt_M_lgd;33         1           CTCFailedBuf_Cnt_M_lgd;34         1           CTCFailedBuf_Cnt_M_lgd;35         1           CTCFailedBuf_Cnt_M_lgd;37         1           CTCFailedBuf_Cnt_M_lgd;39         1           CTCFailedBuf_Cnt_M_lgd;39         1           CTCFailedBuf_Cnt_M_lgd;40         1           CTCFailedBuf_Cnt_M_lgd;41         1           CTCFailedBuf_Cnt_M_lgd;41         1           CTCFailedBuf_Cnt_M_lgd;41         1           CTCFailedBuf_Cnt_M_lgd;43         1           CTCFailedBuf_Cnt_M_lgd;43         1 <t< td=""><td></td><td>1</td></t<>		1
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CTCFailedBuf_Cnt_M_lgc[37]       1         CTCFailedBuf_Cnt_M_lgc[38]       1         CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[38]       1         CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[39]       1         CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[40]       1         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[42]       1         CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[43]       1         CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[44]       1         CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[45]       1         CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[46]       1         CTCFailedBuf_Cnt_M_lgc[47]       1         CTCFailedBuf_Cnt_M_lgc[48]       1		
CTCFailedBuf_Cnt_M_lgc[47]         1           CTCFailedBuf_Cnt_M_lgc[48]         1		
CTCFailedBuf_Cnt_M_lgc[48] 1		
OTOF-II-ID-II O-L M IIAO		
CTCFailedBuf_Cnt_M_lgc[49] 1	CTCFalledBut_Cnt_M_igc[49]	

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	104 12 1010
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[50]	1
CTCFailedBuf_Cnt_M_lgc[51]	1
CTCFailedBuf_Cnt_M_lgc[52]	1
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
	1
CTCFailedBuf_Cnt_M_lgc[59] CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	1
CTCFailedBuf_Cnt_M_lgc[69]	1
CTCFailedBuf_Cnt_M_lgc[70]	1
CTCFailedBuf_Cnt_M_lgc[71]	1
CTCFailedBuf_Cnt_M_lgc[72]	1
CTCFailedBuf_Cnt_M_lgc[73]	1
CTCFailedBuf_Cnt_M_lgc[74]	1
CTCFailedBuf_Cnt_M_lgc[75]	1
CTCFailedBuf_Cnt_M_lgc[76]	1
CTCFailed_Cnt_M_lgc	1
DTC	4294967295
DTCKind	2
DTCStatusNew	255
DTCStatusOld	255
Dem_DTCNumberTable[0]	65535
Dem_DTCNumberTable[1]	65535
Dem_DTCNumberTable[2]	65535
Dem_DTCNumberTable[3]	65535
Dem_DTCNumberTable[4]	65535
Dem_DTCNumberTable[5]	65535
Dem_DTCNumberTable[6]	65535
Dem_DTCNumberTable[7]	65535
Dem_DTCNumberTable[8]	65535
Dem_DTCNumberTable[9]	65535
Dem_DTCNumberTable[10]	65535
Dem_DTCNumberTable[11]	65535
Dem_DTCNumberTable[12]	65535
Dem_DTCNumberTable[13]	65535
Dem_DTCNumberTable[14]	65535
Dem_DTCNumberTable[15]	65535
Dem DTCNumberTable[16]	65535
Dem DTCNumberTable[17]	65535
Dem_DTCNumberTable[18]	65535
Dem_DTCNumberTable[18] Dem_DTCNumberTable[19]	65535
Dem_DTCNumberTable[20]	65535
Dem_DTCNumberTable[21]	65535
Dem_DTCNumberTable[22]	65535
Dem_DTCNumberTable[23]	65535
Dem_DTCNumberTable[24]	65535
Dem_DTCNumberTable[25]	65535
Dem_DTCNumberTable[26]	65535
Dem_DTCNumberTable[27]	65535
Dem_DTCNumberTable[28]	65535
Dem_DTCNumberTable[29]	65535
Dem_DTCNumberTable[30]	65535
Dem_DTCNumberTable[31]	GEESE.
	65535
Dem_DTCNumberTable[32]	65535
Dem_DTCNumberTable[32] Dem_DTCNumberTable[33]	
	65535
Dem_DTCNumberTable[33]	65535 65535
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34]	65535 65535
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34] Dem_DTCNumberTable[35]	65535 65535 65535
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34] Dem_DTCNumberTable[35] Dem_DTCNumberTable[36]	65535 65535 65535 65535 65535
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34] Dem_DTCNumberTable[35] Dem_DTCNumberTable[36] Dem_DTCNumberTable[37]	65535 65535 65535 65535 65535 65535
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34] Dem_DTCNumberTable[35] Dem_DTCNumberTable[36] Dem_DTCNumberTable[37] Dem_DTCNumberTable[38]	65535 65535 65535 65535 65535 65535

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Demlf_DTCStatusChanged	MACIL
Name	Input Value
Dem_DTCNumberTable[41]	65535
Dem_DTCNumberTable[42]	65535
Dem_DTCNumberTable[43]	65535
Dem_DTCNumberTable[44]	65535
Dem_DTCNumberTable[45]	65535
Dem_DTCNumberTable[46]	65535
Dem_DTCNumberTable[47]	65535
Dem_DTCNumberTable[48]	65535
Dem_DTCNumberTable[49]	65535
Dem_DTCNumberTable[50]	65535
Dem_DTCNumberTable[51]	65535
Dem_DTCNumberTable[52]	65535
Dem_DTCNumberTable[53]	65535
Dem_DTCNumberTable[54]	65535
Dem_DTCNumberTable[55]	65535
Dem_DTCNumberTable[56]	65535
Dem_DTCNumberTable[57]	65535
Dem_DTCNumberTable[58]	65535
Dem_DTCNumberTable[59]	65535
Dem_DTCNumberTable[60]	65535
Dem_DTCNumberTable[61]	65535
Dem_DTCNumberTable[62]	65535
Dem_DTCNumberTable[63]	65535
Dem_DTCNumberTable[64]	65535
Dem_DTCNumberTable[65]	65535
Dem_DTCNumberTable[66]	65535
Dem_DTCNumberTable[67]	65535
Dem_DTCNumberTable[68]	65535
Dem_DTCNumberTable[69]	65535
Dem_DTCNumberTable[70]	65535
Dem_DTCNumberTable[71]	65535
Dem_DTCNumberTable[72]	65535
Dem_DTCNumberTable[73]	65535
Dem_DTCNumberTable[74]	65535
Dem_DTCNumberTable[75]	65535
Dem_DTCNumberTable[76]	65535
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[11]	255
Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem DTC FTB Table[14]	255
Dem_DTC_FTB_Table[15]	255
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem DTC FTB Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[27]	255
	255
Dem_DTC_FTB_Table[29]	
Dem_DTC_FTB_Table[30]	255
Dem_DTC_FTB_Table[31]	255
Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[33]	255
Dem_DTC_FTB_Table[34]	255
Dem_DTC_FTB_Table[35] Dem_DTC_FTB_Table[36]	255 255

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Name	Input Value		
Dem_DTC_FTB_Table[37]	255		
Dem_DTC_FTB_Table[38]	255		
Dem_DTC_FTB_Table[39]	255		
Dem_DTC_FTB_Table[40] Dem_DTC_FTB_Table[41]	255 255		
Dem_DTC_FTB_Table[42]	255		
Dem_DTC_FTB_Table[43]	255		
Dem_DTC_FTB_Table[44]	255		
Dem_DTC_FTB_Table[45]	255		
Dem_DTC_FTB_Table[46]	255		
Dem_DTC_FTB_Table[47]	255		
Dem_DTC_FTB_Table[48]	255		
Dem_DTC_FTB_Table[49] Dem_DTC_FTB_Table[50]	255 255		
Dem_DTC_FTB_Table[51]	255		
Dem_DTC_FTB_Table[52]	255		
Dem_DTC_FTB_Table[53]	255		
Dem_DTC_FTB_Table[54]	255		
Dem_DTC_FTB_Table[55]	255		
Dem_DTC_FTB_Table[56]	255		
Dem_DTC_FTB_Table[57]	255		
Dem_DTC_FTB_Table[58]	255		
Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60]	255 255		
Dem_DTC_FTB_Table[61]	255		
Dem_DTC_FTB_Table[62]	255		
Dem_DTC_FTB_Table[63]	255		
Dem_DTC_FTB_Table[64]	255		
Dem_DTC_FTB_Table[65]	255		
Dem_DTC_FTB_Table[66]	255		
Dem_DTC_FTB_Table[67]	255		
Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69]	255 255		
Dem_DTC_FTB_Table[70]	255		
Dem_DTC_FTB_Table[71]	255		
Dem_DTC_FTB_Table[72]	255		
D DT0 FTD T 11 F00			
Dem_DTC_FTB_Table[73]	255		
Dem_DTC_FTB_Table[74]	255		
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75]	255 255		
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	255 255 255	Function Volum	Passid
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	255 255 255 Actual Value	Expected Value	Resul
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	255 255 255 <b>Actual Value</b>	1	•
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]	255 255 255 Actual Value	· ·	•
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]	255 255 255 <b>Actual Value</b> 1	1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]	255 255 255 <b>Actual Value</b> 1 1	1 1 1	Resul
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	255 255 Actual Value  1 1 1 1 1 1	1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6]	255 255 Actual Value  1 1 1 1 1 1 1 1	1 1 1 1 1 1	•
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	•
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	•
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11]	255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[77] CTCFailedBuf_Cnt_M_lgc[77] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[18]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	255 255  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[26]	255 255  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28]	255 255  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	255 255 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[34]	1	1	~
CTCFailedBuf_Cnt_M_lgc[35]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[36]	1	1	~
CTCFailedBuf_Cnt_M_lgc[37]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	1	1	~
CTCFailedBuf_Cnt_M_lgc[39]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[40]	1	1	~
CTCFailedBuf_Cnt_M_lgc[41]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[42]	1	1	~
CTCFailedBuf_Cnt_M_Igc[43]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	1	1	~
CTCFailedBuf_Cnt_M_lgc[45]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	1	1	~
CTCFailedBuf_Cnt_M_lgc[47]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	1	1	~
CTCFailedBuf_Cnt_M_Igc[49]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	1	1	~
CTCFailedBuf_Cnt_M_lgc[51]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	1	1	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>~</b>
CTCFailedBuf Cnt M Igc[54]	1	1	~
CTCFailedBuf Cnt M Igc[55]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	
CTCFailedBuf_Cnt_M_lgc[65]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[66]	1	1	~
CTCFailedBuf_Cnt_M_lgc[67]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[68]	1	1	~
CTCFailedBuf_Cnt_M_lgc[69]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[70]	1	1	_
CTCFailedBuf_Cnt_M_lgc[71]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[72]	1	1	
CTCFailedBuf_Cnt_M_lgc[73]	1	1	<b>V</b>
CTCFailedBuf Cnt M Igc[74]	1	1	•
CTCFailedBuf_Cnt_M_lgc[75]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_Igc[76]	1	1	~
CTCFailed_Cnt_M_lgc	1	1	<b>~</b>
Demlf_DTCStatusChanged()	0	0	_
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	<b>V</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	_

Test Step 2.3 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1

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Name	Input Value
CTCFailedBuf Cnt M Igc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_Igc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf Cnt M lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_Igc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	0
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68] CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf Cnt M lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[72] CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	0
DTCKind	1
DTCStatusNew	148
DTCStatusOld	39
Dem_DTCNumberTable[0]	181
Dem_DTCNumberTable[1]	1
Dem_DTCNumberTable[2]	41
Dem_DTCNumberTable[3]	22
	24
Dem_DTCNumberTable[4]	24

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Demlf\_DTCStatusChanged Input Value Dem DTCNumberTable[6] 209 Dem\_DTCNumberTable[7] 209 Dem DTCNumberTable[8] 181 Dem\_DTCNumberTable[9] 1 Dem DTCNumberTable[10] 209 Dem\_DTCNumberTable[11] 128 Dem\_DTCNumberTable[12] 1 Dem\_DTCNumberTable[13] 209 Dem\_DTCNumberTable[14] 181 Dem\_DTCNumberTable[15] 1 Dem\_DTCNumberTable[16] Dem\_DTCNumberTable[17] 209 Dem\_DTCNumberTable[18] 33 Dem\_DTCNumberTable[19] 181 Dem\_DTCNumberTable[20] Dem\_DTCNumberTable[21] 209 Dem\_DTCNumberTable[22] 181 Dem\_DTCNumberTable[23] 41 Dem\_DTCNumberTable[24] 22 Dem\_DTCNumberTable[25] 24 Dem\_DTCNumberTable[26] 254 Dem\_DTCNumberTable[27] 1 Dem\_DTCNumberTable[28] 181 Dem\_DTCNumberTable[29] Dem\_DTCNumberTable[30] 181 Dem\_DTCNumberTable[31] 181 Dem DTCNumberTable[32] 1 Dem\_DTCNumberTable[33] Dem DTCNumberTable[34] 181 Dem\_DTCNumberTable[35] Dem DTCNumberTable[36] 181 Dem\_DTCNumberTable[37] 181 Dem DTCNumberTable[38] 181 Dem\_DTCNumberTable[39] 1 Dem\_DTCNumberTable[40] Dem\_DTCNumberTable[41] 41 Dem\_DTCNumberTable[42] 22 24 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 254 Dem\_DTCNumberTable[45] 209 Dem\_DTCNumberTable[46] 181 Dem\_DTCNumberTable[47] 1 Dem\_DTCNumberTable[48] 22 Dem\_DTCNumberTable[49] 181 Dem\_DTCNumberTable[50] Dem\_DTCNumberTable[51] 181 Dem DTCNumberTable[52] 181 Dem\_DTCNumberTable[53] 1 Dem DTCNumberTable[54] 22 Dem\_DTCNumberTable[55] 209 Dem\_DTCNumberTable[56] 181 Dem\_DTCNumberTable[57] Dem\_DTCNumberTable[58] 181 Dem\_DTCNumberTable[59] 209 Dem\_DTCNumberTable[60] 181 Dem\_DTCNumberTable[61] 1 Dem\_DTCNumberTable[62] 22 41 Dem\_DTCNumberTable[63] Dem\_DTCNumberTable[64] 22 Dem\_DTCNumberTable[65] 24 Dem\_DTCNumberTable[66] 254 181 Dem\_DTCNumberTable[67] Dem\_DTCNumberTable[68] 181 Dem\_DTCNumberTable[69] 1 Dem\_DTCNumberTable[70] 22 Dem\_DTCNumberTable[71] 209 Dem\_DTCNumberTable[72] 22 Dem DTCNumberTable[73] 41 Dem\_DTCNumberTable[74] 22 Dem\_DTCNumberTable[75] 24 Dem\_DTCNumberTable[76] 254

245

151

Dem\_DTC\_FTB\_Table[0]

Dem\_DTC\_FTB\_Table[1]

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		- I GAZ I GAZ
Name	Input Value	
Dem_DTC_FTB_Table[2]	199	
Dem_DTC_FTB_Table[3]	160	
Dem_DTC_FTB_Table[4]	30	
Dem_DTC_FTB_Table[5]	136	
Dem_DTC_FTB_Table[6]	178	
Dem_DTC_FTB_Table[7]	178	
Dem_DTC_FTB_Table[8]	245	
Dem_DTC_FTB_Table[9]	151	
Dem_DTC_FTB_Table[10]	178	
Dem_DTC_FTB_Table[11]	31	
Dem_DTC_FTB_Table[12]	151	
Dem_DTC_FTB_Table[13]	178	
Dem_DTC_FTB_Table[14]	245	
Dem_DTC_FTB_Table[15]	151	
Dem_DTC_FTB_Table[16]	151	
Dem_DTC_FTB_Table[17]	178	
Dem_DTC_FTB_Table[18]	234	
Dem_DTC_FTB_Table[19]	245	
Dem_DTC_FTB_Table[20]	151	
Dem_DTC_FTB_Table[21]	178	
Dem_DTC_FTB_Table[22]	245	
Dem_DTC_FTB_Table[23]	199	
Dem_DTC_FTB_Table[24]	160	
Dem_DTC_FTB_Table[25]	30	
Dem_DTC_FTB_Table[26]	136	
Dem_DTC_FTB_Table[27]	151	
Dem_DTC_FTB_Table[28]	245	
Dem_DTC_FTB_Table[29]	151	
Dem_DTC_FTB_Table[30]	245	
Dem_DTC_FTB_Table[31]	245	
Dem_DTC_FTB_Table[32]	151	
Dem_DTC_FTB_Table[33]	151	
Dem_DTC_FTB_Table[34]	245	
Dem_DTC_FTB_Table[35]	151 245	
Dem_DTC_FTB_Table[36]	245	
Dem_DTC_FTB_Table[37] Dem_DTC_FTB_Table[38]	245	
Dem_DTC_FTB_Table[39]	151	
Dem_DTC_FTB_Table[40]	151	
Dem_DTC_FTB_Table[41]	199	
Dem_DTC_FTB_Table[42]	160	
Dem_DTC_FTB_Table[43]	30	
Dem_DTC_FTB_Table[44]	136	
Dem_DTC_FTB_Table[45]	178	
Dem_DTC_FTB_Table[46]	245	
Dem_DTC_FTB_Table[47]	151	
Dem_DTC_FTB_Table[48]	160	
Dem_DTC_FTB_Table[49]	245	
Dem_DTC_FTB_Table[50]	151	
Dem_DTC_FTB_Table[51]	245	
Dem_DTC_FTB_Table[52]	245	
Dem_DTC_FTB_Table[53]	151	
Dem_DTC_FTB_Table[54]	160	
Dem_DTC_FTB_Table[55]	178	
Dem_DTC_FTB_Table[56]	245	
Dem_DTC_FTB_Table[57]	151	
Dem_DTC_FTB_Table[58]	245	
Dem_DTC_FTB_Table[59]	178	
Dem_DTC_FTB_Table[60]	245	
Dem_DTC_FTB_Table[61]	151	
Dem_DTC_FTB_Table[62]	160	
Dem_DTC_FTB_Table[63]	199	
Dem_DTC_FTB_Table[64]	160	
Dem_DTC_FTB_Table[65]	30	
Dem_DTC_FTB_Table[66]	136	
Dem_DTC_FTB_Table[67]	245	
Dem_DTC_FTB_Table[68]	245	
Dem_DTC_FTB_Table[69]	151	
Dem_DTC_FTB_Table[70]	160	
Dem_DTC_FTB_Table[71]	178	
Dem_DTC_FTB_Table[72]	160	
Dem_DTC_FTB_Table[73]	199	

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Name	Input Value		
Dem_DTC_FTB_Table[75]	30		
Dem_DTC_FTB_Table[76]	136	Forms at ad Malors	D it
Name  CTCFailedBuf_Cnt_M_lgc[0]	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[1]	1	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	1	•
CTCFailedBuf_Cnt_M_lgc[4]	1	1	-
CTCFailedBuf_Cnt_M_lgc[5]	0	0	•
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CTCFailedBuf_Cnt_M_lgc[7]	1	1	•
CTCFailedBuf_Cnt_M_lgc[8]	1	1	•
CTCFailedBuf_Cnt_M_lgc[9]	1	1	
CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11]	1	1	
CTCFailedBuf_Cnt_M_lgc[12]	1	1	
CTCFailedBuf_Cnt_M_lgc[13]	1	1	•
CTCFailedBuf_Cnt_M_lgc[14]	1	1	-
CTCFailedBuf_Cnt_M_lgc[15]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[16]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	•
CTCFailedBuf_Cnt_M_lgc[19]	1	1	•
CTCFailedBuf_Cnt_M_lgc[20]	0	0	<b>→</b>
CTCFailedBuf_Cnt_M_lgc[21]	0	0	•
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[24]	1	1	
CTCFailedBuf_Cnt_M_lgc[25]	0	0	•
CTCFailedBuf_Cnt_M_lgc[26]	1	1	-
CTCFailedBuf_Cnt_M_lgc[27]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[28]	1	1	•
CTCFailedBuf_Cnt_M_lgc[29]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[30]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[31]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[33]	1	1	•
CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	0	0	Ž
CTCFalledBuf_Cnt_M_lgc[36]	0	0	
CTCFailedBuf_Cnt_M_lgc[37]	0	0	
CTCFailedBuf_Cnt_M_lgc[38]	0	0	-
CTCFailedBuf_Cnt_M_Igc[39]	0	0	•
CTCFailedBuf_Cnt_M_lgc[40]	0	0	-
CTCFailedBuf_Cnt_M_lgc[41]	0	0	•
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	•
CTCFailedBuf_Cnt_M_lgc[44]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[45]	0	0	•
CTCFailedBuf_Cnt_M_lgc[46] CTCFailedBuf Cnt M lgc[47]	0	0	
CTCFailedBuf_Cnt_M_igc[47] CTCFailedBuf_Cnt_M_igc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	
CTCFailedBuf_Cnt_M_lgc[50]	0	0	
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	•
CTCFailedBuf_Cnt_M_lgc[53]	1	1	•
CTCFailedBuf_Cnt_M_lgc[54]	1	1	•
CTCFailedBuf_Cnt_M_lgc[55]	1	1	•
CTCFailedBuf_Cnt_M_lgc[56]	1	1	•
CTCFailedBuf_Cnt_M_lgc[57]	1	1	•
CTCFailedBuf_Cnt_M_lgc[58]	1	1	•
CTCFailedBuf_Cnt_M_lgc[59] CTCFailedBuf_Cnt_M_lgc[60]	1	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	1	
CTCFailedBuf_Cnt_M_lgc[62]	1	1	
CTCFailedBuf_Cnt_M_lgc[63]	0	0	
CTCFailedBuf_Cnt_M_lgc[64]	1	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	0	•
CTCFailedBuf_Cnt_M_lgc[66]	0	0	•
CTCFailedBuf_Cnt_M_lgc[67]	0	0	•
CTCFailedBuf_Cnt_M_lgc[68]	0	0	•
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>

Demlf\_DTCStatusChanged

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✓
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
DemIf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.4 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf Cnt M lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1.
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf Cnt M Igc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M Igc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
TCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
TCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
TCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M Igc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
TCFailedBuf_Cnt_M_lgc[41]	0
TCFalledBut_Crit_ivi_igc[41] TCFalledBuf_Crit_M_lgc[42]	0
TCFalledBuf_Cnt_M_lgc[42]	0
TCFalledBuf_Cnt_M_lgc[43]	0
TCFalledBuf_Cnt_M_lgc[44]	0
TCFalledBut_Cnt_M_lgc[45]	0
TCFailedBuf_Crit_M_igc[46]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFalledBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0

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Demlf_DTCStatusChanged	TAACILAU
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66] CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCF alledBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	1
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	1
OTC	4294967295
DTCKind	2
DTCStatusNew	126
DTCStatusOld	203
Dem_DTCNumberTable[0]	182
Dem_DTCNumberTable[1]	221
Dem_DTCNumberTable[2]	159
Dem_DTCNumberTable[3]	164
Dem_DTCNumberTable[4]	34
Dem_DTCNumberTable[5]	166
Dem_DTCNumberTable[6]	237
Dem_DTCNumberTable[7]	237
Dem_DTCNumberTable[8]	182
Dem_DTCNumberTable[9]	221
Dem_DTCNumberTable[10]	237
Dem_DTCNumberTable[11]	123
Dem_DTCNumberTable[12]	221
Dem_DTCNumberTable[13]	237
Dem_DTCNumberTable[14]	182
Dem_DTCNumberTable[15]	221
Dem_DTCNumberTable[16]	221
Dem_DTCNumberTable[17]	237
Dem_DTCNumberTable[18]	239
Dem_DTCNumberTable[19]	182
Dem_DTCNumberTable[20] Dem DTCNumberTable[21]	221 237
Dem_DTCNumberTable[21] Dem_DTCNumberTable[22]	182
Dem DTCNumberTable[22]	159
Dem_DTCNumberTable[23] Dem_DTCNumberTable[24]	164
Dem_DTCNumberTable[24]	34
Dem_DTCNumberTable[25]	166
Dem DTCNumberTable[27]	221
Dem_DTCNumberTable[28]	182
Dem_DTCNumberTable[29]	221
Dem_DTCNumberTable[30]	182
Dem_DTCNumberTable[31]	182
Dem_DTCNumberTable[32]	221
Dem_DTCNumberTable[33]	221
Dem_DTCNumberTable[34]	182
Dem_DTCNumberTable[35]	221
Dem_DTCNumberTable[36]	182
Dem_DTCNumberTable[37]	182
Dem_DTCNumberTable[38]	182
Dem_DTCNumberTable[39]	221
Dem_DTCNumberTable[40]	221
	221   159
Dem_DTCNumberTable[40] Dem_DTCNumberTable[41] Dem_DTCNumberTable[42]	

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Demii_DTCStatusCrianged		- TOLOTON
lame	Input Value	
Dem_DTCNumberTable[44]	166	
Dem_DTCNumberTable[45]	237	
Dem_DTCNumberTable[46]	182	
Dem_DTCNumberTable[47]	221	
Dem_DTCNumberTable[48]	164	
Dem_DTCNumberTable[49]	182	
Dem_DTCNumberTable[50]	221	
Dem_DTCNumberTable[51]	182	
pem_DTCNumberTable[52]	182	
em_DTCNumberTable[53]	221	
em_DTCNumberTable[54]	164	
em_DTCNumberTable[54]	237	
em_DTCNumberTable[56]	182	
em_DTCNumberTable[57]	221	
em_DTCNumberTable[58]	182	
em_DTCNumberTable[59]	237	
em_DTCNumberTable[60]	182	
em_DTCNumberTable[61]	221	
em_DTCNumberTable[62]	164	
em_DTCNumberTable[63]	159	
em_DTCNumberTable[64]	164	
em_DTCNumberTable[65]	34	
em_DTCNumberTable[66]	166	
em_DTCNumberTable[67]	182	
em_DTCNumberTable[68]	182	
em_DTCNumberTable[69]	221	
em_DTCNumberTable[70]	164	
em_DTCNumberTable[71]	237	
em_DTCNumberTable[72]	164	
em_DTCNumberTable[73]	159	
em_DTCNumberTable[74]	164	
em_DTCNumberTable[75]	34	
em_DTCNumberTable[76]	166	
em_DTC_FTB_Table[0]	100	
em_DTC_FTB_Table[1]	77	
em_DTC_FTB_Table[2]	185	
em_DTC_FTB_Table[3]	93	
em_DTC_TTB_Table[3] em DTC FTB Table[4]	72	
em_DTC_TTB_Table[4] em DTC FTB Table[5]	20	
em_DTC_FTB_Table[6]	13	
em_DTC_FTB_Table[7]	13	
em_DTC_FTB_Table[8]	100	
em_DTC_FTB_Table[9]	77	
em_DTC_FTB_Table[10]	13	
em_DTC_FTB_Table[11]	191	
em_DTC_FTB_Table[12]	77	
em_DTC_FTB_Table[13]	13	
em_DTC_FTB_Table[14]	100	
em_DTC_FTB_Table[15]	77	
em_DTC_FTB_Table[16]	77	
em_DTC_FTB_Table[17]	13	
em_DTC_FTB_Table[18]	69	
em_DTC_FTB_Table[19]	100	
em_DTC_FTB_Table[20]	77	
em_DTC_FTB_Table[21]	13	
em_DTC_FTB_Table[22]	100	
em_DTC_FTB_Table[23]	185	
em_DTC_FTB_Table[24]	93	
em_DTC_FTB_Table[25]	72	
em_DTC_FTB_Table[26]	20	
em_DTC_FTB_Table[27]	77	
em_DTC_FTB_Table[27] em_DTC_FTB_Table[28]	100	
	77	
em_DTC_FTB_Table[29]		
em_DTC_FTB_Table[30]	100	
em_DTC_FTB_Table[31]	100	
em_DTC_FTB_Table[32]	77	
em_DTC_FTB_Table[33]	77	
em_DTC_FTB_Table[34]	100	
em_DTC_FTB_Table[35]	77	
em_DTC_FTB_Table[36]	100	
em_DTC_FTB_Table[37]	100	
em_DTC_FTB_Table[38]	100	
	77	

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			-
Name	Input Value		
Dem_DTC_FTB_Table[40]	77		
Dem_DTC_FTB_Table[41]	185		
Dem_DTC_FTB_Table[42]	93		
Dem_DTC_FTB_Table[43]	72		
Dem_DTC_FTB_Table[44]	20		
Dem_DTC_FTB_Table[45]	13		
Dem_DTC_FTB_Table[46] Dem_DTC_FTB_Table[47]	77		
Dem_DTC_FTB_Table[47]	93		
Dem_DTC_FTB_Table[49]	100		
Dem_DTC_FTB_Table[50]	77		
Dem_DTC_FTB_Table[51]	100		
Dem_DTC_FTB_Table[52]	100		
Dem_DTC_FTB_Table[53]	77		
Dem_DTC_FTB_Table[54]	93		
Dem_DTC_FTB_Table[55]	13		
Dem_DTC_FTB_Table[56]	100		
Dem_DTC_FTB_Table[57]	77		
Dem_DTC_FTB_Table[58]	100		
Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60]	100		
Dem_DTC_FTB_Table[61]	77		
Dem_DTC_FTB_Table[62]	93		
Dem DTC FTB Table[63]	185		
Dem_DTC_FTB_Table[64]	93		
Dem_DTC_FTB_Table[65]	72		
Dem_DTC_FTB_Table[66]	20		
Dem_DTC_FTB_Table[67]	100		
Dem_DTC_FTB_Table[68]	100		
Dem_DTC_FTB_Table[69]	77		
Dem_DTC_FTB_Table[70]	93		
Dem_DTC_FTB_Table[71]	93		
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	185		
Dem_DTC_FTB_Table[73]	93		
= a= . a= a=			
Dem DTC FTB Table[75]	72		
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	72 20		
		Expected Value	Result
Dem_DTC_FTB_Table[76]	20	Expected Value	Result
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]	20 Actual Value 1	1	· ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]	20 Actual Value  1 1 1	1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]	Actual Value  1 1 1 1	1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]	20 Actual Value  1 1 1 1 1	1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]	20 Actual Value  1 1 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]	20 Actual Value 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]	20 Actual Value 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[17]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]	20 Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[9]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[26]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[31]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]  CTCFailedBuf_Cnt_M_lgc[3]  CTCFailedBuf_Cnt_M_lgc[4]  CTCFailedBuf_Cnt_M_lgc[5]  CTCFailedBuf_Cnt_M_lgc[6]  CTCFailedBuf_Cnt_M_lgc[7]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[8]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[10]  CTCFailedBuf_Cnt_M_lgc[11]  CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  CTCFailedBuf_Cnt_M_lgc[14]  CTCFailedBuf_Cnt_M_lgc[15]  CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[20]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]  CTCFailedBuf_Cnt_M_lgc[29]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1	
Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[231] CTCFailedBuf_Cnt_M_lgc[231] CTCFailedBuf_Cnt_M_lgc[232]	20  Actual Value  1  1  1  1  1  1  1  1  1  1  1  1  1	1	

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[35]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	_
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	•
CTCFailedBuf_Cnt_M_Igc[39]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	✓
CTCFailedBuf_Cnt_M_Igc[55]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[56]	1	1	✓
CTCFailedBuf_Cnt_M_Igc[57]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_Igc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	~
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[68]	0	0	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	<b>y</b>
CTCFailedBuf_Cnt_M_lgc[73]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>~</b>
CTCFailed_Cnt_M_lgc	1	1	
Demlf_DTCStatusChanged()	0	0	<b>*</b>
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt loc	1	Rte Write An Demlf CTCFailed Cnt loc	1	_

Test Step 2.5 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_Igc[21] CTCFailedBuf_Cnt_M_Igc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0 0
CTCFailedBuf_Cnt_M_lgc[42] CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51] CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59] CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68] CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailed Cnt_M_lgc[76]	0 1
CTCFailed_Cnt_M_lgc DTC	256327693
DTCKind	1
DTCStatusNew	30
DTCStatusOld	178
Dem_DTCNumberTable[0]	99
Dem_DTCNumberTable[1]	143
Dem_DTCNumberTable[2]	36
Dem_DTCNumberTable[3]	85
Dem_DTCNumberTable[4] Dem_DTCNumberTable[5]	238 62
	217
Dem DTCNumberTableibi	
Dem_DTCNumberTable[6] Dem_DTCNumberTable[7]	217

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Demii_D1CStatusChanged		- GACTUAL
Name	Input Value	
Dem_DTCNumberTable[9]	143	
Dem_DTCNumberTable[10]	217	
Dem_DTCNumberTable[11]	101	
Dem_DTCNumberTable[12]	143	
Dem_DTCNumberTable[13]	217	
Dem_DTCNumberTable[14]	99	
Dem_DTCNumberTable[15]	143	
Dem_DTCNumberTable[16]	143	
Dem_DTCNumberTable[17]	217	
Dem_DTCNumberTable[18]	236	
Dem_DTCNumberTable[19]	99	
Dem_DTCNumberTable[20]	143	
Dem_DTCNumberTable[21]	217	
Dem_DTCNumberTable[22]	99	
Dem_DTCNumberTable[23]	36	
Dem_DTCNumberTable[24]	85	
Dem_DTCNumberTable[25]	238	
Dem_DTCNumberTable[26]	62	
Dem_DTCNumberTable[27]	143	
Dem_DTCNumberTable[28]	99	
Dem_DTCNumberTable[29]	143	
Dem_DTCNumberTable[30]	99	
Dem_DTCNumberTable[31]	99	
Dem_DTCNumberTable[32]	143	
Dem_DTCNumberTable[33]	143	
Dem_DTCNumberTable[34]	99	
Dem_DTCNumberTable[35]	143	
Dem_DTCNumberTable[36]	99	
Dem_DTCNumberTable[37]	99	
Dem_DTCNumberTable[38]	99	
Dem_DTCNumberTable[39]	143	
Dem_DTCNumberTable[40]	143	
Dem_DTCNumberTable[41]	36	
Dem_DTCNumberTable[42]	85 238	
Dem_DTCNumberTable[43] Dem_DTCNumberTable[44]	62	
Dem_DTCNumberTable[44]	217	
Dem_DTCNumberTable[46]	99	
Dem DTCNumberTable[47]	143	
Dem_DTCNumberTable[48]	85	
Dem DTCNumberTable[49]	99	
Dem_DTCNumberTable[50]	143	
Dem_DTCNumberTable[51]	99	
Dem_DTCNumberTable[52]	99	
Dem_DTCNumberTable[53]	143	
Dem_DTCNumberTable[54]	85	
Dem_DTCNumberTable[55]	217	
Dem DTCNumberTable[56]	99	
Dem_DTCNumberTable[57]	143	
Dem_DTCNumberTable[58]	99	
Dem_DTCNumberTable[59]	217	
Dem_DTCNumberTable[60]	99	
Dem_DTCNumberTable[61]	143	
Dem_DTCNumberTable[62]	85	
Dem_DTCNumberTable[63]	36	
Dem_DTCNumberTable[64]	85	
Dem_DTCNumberTable[65]	238	
Dem_DTCNumberTable[66]	62	
Dem_DTCNumberTable[67]	99	
Dem_DTCNumberTable[68]	99	
Dem_DTCNumberTable[69]	143	
Dem_DTCNumberTable[70]	85	
Dem_DTCNumberTable[71]	217	
Dem_DTCNumberTable[72]	85	
Dem_DTCNumberTable[73]	36	
Dem_DTCNumberTable[74]	85	
Dem_DTCNumberTable[75]	238	
Dem_DTCNumberTable[76]	62	
Dem_DTC_FTB_Table[0]	161	
Dem_DTC_FTB_Table[1]	211	
Dem_DTC_FTB_Table[2]	7	
Dem_DTC_FTB_Table[3]	239	
	206	

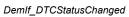
Demlf\_DTCStatusChanged

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Input Value Dem\_DTC\_FTB\_Table[5] 70 Dem\_DTC\_FTB\_Table[6] 84 Dem DTC\_FTB\_Table[7] 84 Dem\_DTC\_FTB\_Table[8] 161 Dem\_DTC\_FTB\_Table[9] 211 Dem\_DTC\_FTB\_Table[10] 84 Dem\_DTC\_FTB\_Table[11] 193 Dem\_DTC\_FTB\_Table[12] 211 Dem\_DTC\_FTB\_Table[13] 84 Dem\_DTC\_FTB\_Table[14] 161 Dem\_DTC\_FTB\_Table[15] 211 Dem\_DTC\_FTB\_Table[16] 211 Dem\_DTC\_FTB\_Table[17] 84 Dem\_DTC\_FTB\_Table[18] 108 Dem\_DTC\_FTB\_Table[19] 161 211 Dem\_DTC\_FTB\_Table[20] Dem\_DTC\_FTB\_Table[21] 84 Dem\_DTC\_FTB\_Table[22] 161 Dem\_DTC\_FTB\_Table[23] Dem\_DTC\_FTB\_Table[24] 239 Dem\_DTC\_FTB\_Table[25] 206 Dem\_DTC\_FTB\_Table[26] 70 Dem\_DTC\_FTB\_Table[27] 211 Dem\_DTC\_FTB\_Table[28] 161 Dem\_DTC\_FTB\_Table[29] 211 Dem\_DTC\_FTB\_Table[30] 161 Dem\_DTC\_FTB\_Table[31] 161 Dem\_DTC\_FTB\_Table[32] 211 Dem DTC FTB Table[33] 211 Dem\_DTC\_FTB\_Table[34] 161 Dem DTC FTB Table[35] 211 Dem\_DTC\_FTB\_Table[36] 161 Dem DTC FTB Table[37] 161 Dem\_DTC\_FTB\_Table[38] 161 Dem\_DTC\_FTB\_Table[39] 211 Dem\_DTC\_FTB\_Table[40] 211 Dem\_DTC\_FTB\_Table[41] Dem\_DTC\_FTB\_Table[42] 239 Dem\_DTC\_FTB\_Table[43] 206 Dem\_DTC\_FTB\_Table[44] 70 Dem\_DTC\_FTB\_Table[45] 84 Dem\_DTC\_FTB\_Table[46] 161 Dem\_DTC\_FTB\_Table[47] 211 Dem\_DTC\_FTB\_Table[48] 239 Dem\_DTC\_FTB\_Table[49] 161 Dem\_DTC\_FTB\_Table[50] 211 Dem\_DTC\_FTB\_Table[51] 161 Dem\_DTC\_FTB\_Table[52] 161 Dem\_DTC\_FTB\_Table[53] 211 Dem\_DTC\_FTB\_Table[54] 239 Dem DTC FTB Table[55] 84 Dem\_DTC\_FTB\_Table[56] 161 Dem\_DTC\_FTB\_Table[57] 211 Dem\_DTC\_FTB\_Table[58] 161 Dem\_DTC\_FTB\_Table[59] 84 Dem\_DTC\_FTB\_Table[60] 161 Dem\_DTC\_FTB\_Table[61] 211 Dem\_DTC\_FTB\_Table[62] 239 Dem\_DTC\_FTB\_Table[63] Dem\_DTC\_FTB\_Table[64] 239 Dem\_DTC\_FTB\_Table[65] 206 Dem\_DTC\_FTB\_Table[66] 70 Dem\_DTC\_FTB\_Table[67] 161 Dem\_DTC\_FTB\_Table[68] 161 Dem\_DTC\_FTB\_Table[69] 211 Dem DTC FTB Table[70] 239 Dem\_DTC\_FTB\_Table[71] 84 239 Dem DTC FTB Table[72] Dem\_DTC\_FTB\_Table[73] Dem\_DTC\_FTB\_Table[74] 239 Dem\_DTC\_FTB\_Table[75] 206 Dem\_DTC\_FTB\_Table[76] 70

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[1]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[2]	1	1	
CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	1	1	
CTCFailedBuf Cnt M lgc[5]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[6]	1	1	
CTCFailedBuf_Cnt_M_lgc[7]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[10]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	0	0	~
CTCFailedBuf_Cnt_M_Igc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[15]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_Igc[17] CTCFailedBuf_Cnt_M_Igc[18]	1	1	
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	_
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_Igc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[29]	1	1	<b>v</b>
CTCFailedBuf_Cnt_M_lgc[30]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_Igc[31] CTCFailedBuf_Cnt_M_Igc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[32]	1	1	_
CTCFailedBuf_Cnt_M_lgc[34]	0	0	_
CTCFailedBuf_Cnt_M_lgc[35]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_Igc[37]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[43]	0	0	
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0	0	-
CTCFailedBuf_Cnt_M_lgc[46]	0	0	
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_Igc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	~
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[54]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_Igc[57] CTCFailedBuf_Cnt_M_Igc[58]	1	1	
CTCFailedBuf_Cnt_M_lgc[59]	1	1	_
CTCFailedBuf_Cnt_M_lgc[60]	1	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	~
CTCFailedBuf_Cnt_M_lgc[66]	0	0	~
CTCFailedBuf_Cnt_M_lgc[67]	0	0	~
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[72]	0	0	<b>✓</b>

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[74]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>✓</b>
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
DemIf_DTCStatusChanged()	0	0	<b>✓</b>
Rte Write Ap Demlf CTCFailed Cnt lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.6 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf Cnt M lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	1
	1
CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
	1
CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	1
	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1.
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_Igc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	O .
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1

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Demlf_DTCStatusChanged		MACILAL
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[56]	1	
CTCFailedBuf_Cnt_M_lgc[57]	1	
CTCFailedBuf_Cnt_M_lgc[58]	1	
CTCFailedBuf_Cnt_M_lgc[59]	1	
CTCFailedBuf_Cnt_M_lgc[60]	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	
CTCFailedBuf_Cnt_M_lgc[62]	1	
CTCFailedBuf_Cnt_M_lgc[63]	1	
CTCFailedBuf_Cnt_M_lgc[64]	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	
CTCFailedBuf_Cnt_M_lgc[69] CTCFailedBuf_Cnt_M_lgc[70]	0	
CTCFailedBut_Cnt_M_lgc[71]	0	
CTCFailedBuf_Cnt_M_lgc[72]	0	
CTCFailedBuf_Cnt_M_lgc[73]	0	
CTCFailedBuf Cnt M lgc[74]	0	
CTCFailedBuf_Cnt_M_lgc[75]	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	
CTCFailed_Cnt_M_lgc	1	
DTC	3061213468	
DTCKind	1	
DTCStatusNew	72	
DTCStatusOld	13	
Dem_DTCNumberTable[0]	31	
Dem_DTCNumberTable[1]	227	
Dem_DTCNumberTable[2]	66	
Dem_DTCNumberTable[3]	96	
Dem_DTCNumberTable[4]	130	
Dem_DTCNumberTable[5]	24	
Dem_DTCNumberTable[6]	240	
Dem_DTCNumberTable[7]	240	
Dem_DTCNumberTable[8]	31 227	
Dem_DTCNumberTable[9] Dem_DTCNumberTable[10]	240	
Dem DTCNumberTable[11]	151	
Dem DTCNumberTable[12]	227	
Dem DTCNumberTable[13]	240	
Dem_DTCNumberTable[14]	31	
Dem_DTCNumberTable[15]	227	
Dem_DTCNumberTable[16]	227	
Dem_DTCNumberTable[17]	240	
Dem_DTCNumberTable[18]	241	
Dem_DTCNumberTable[19]	31	
Dem_DTCNumberTable[20]	227	
Dem_DTCNumberTable[21]	240	
Dem_DTCNumberTable[22]	31	
Dem_DTCNumberTable[23]	66	
Dem_DTCNumberTable[24]	96	
Dem_DTCNumberTable[25]	130	
Dem_DTCNumberTable[26]	24	
Dem_DTCNumberTable[27]	227	
Dem_DTCNumberTable[28]	31	
Dem_DTCNumberTable[29]	227	
Dem_DTCNumberTable[30]	31	
Dem_DTCNumberTable[31]	31	
Dem_DTCNumberTable[32] Dem_DTCNumberTable[33]	227 227	
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34]	31	
Dem_DTCNumberTable[34]	227	
Dem_DTCNumberTable[36]	31	
Dem_DTCNumberTable[37]	31	
Dem_DTCNumberTable[38]	31	
Dem_DTCNumberTable[39]	227	
Dem_DTCNumberTable[40]	227	
Dem_DTCNumberTable[41]	66	
Dem_DTCNumberTable[42]	96	
Dem_DTCNumberTable[43]	130	
Dem_DTCNumberTable[44]	24	
Dem_DTCNumberTable[45]	240	
Delli_DTCNulliberrable[45]	240	

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Demii_D1CStatusChanged		T GALCITON
Name	Input Value	
Dem_DTCNumberTable[47]	227	
Dem_DTCNumberTable[48]	96	
Dem_DTCNumberTable[49]	31	
Dem_DTCNumberTable[50]	227	
Dem_DTCNumberTable[51]	31	
Dem_DTCNumberTable[52]	31	
Dem_DTCNumberTable[53]	227	
Dem_DTCNumberTable[54]	96	
Dem_DTCNumberTable[55]	240	
Dem_DTCNumberTable[56]	31	
Dem_DTCNumberTable[57]	227	
Dem_DTCNumberTable[58]	31	
Dem_DTCNumberTable[59]	240	
Dem_DTCNumberTable[60]	31	
Dem_DTCNumberTable[61]	227	
Dem_DTCNumberTable[62]	96	
Dem_DTCNumberTable[63]	66	
Dem_DTCNumberTable[64]	96	
Dem_DTCNumberTable[65]	130	
Dem_DTCNumberTable[66]	24	
	31	
Dem_DTCNumberTable[67]		
Dem_DTCNumberTable[68]	31	
Dem_DTCNumberTable[69]	227	
Dem_DTCNumberTable[70]	96	
Dem_DTCNumberTable[71]	240	
Dem_DTCNumberTable[72]	96	
Dem_DTCNumberTable[73]	66	
Dem_DTCNumberTable[74]	96	
Dem_DTCNumberTable[75]	130	
Dem_DTCNumberTable[76]	24	
Dem_DTC_FTB_Table[0]	181	
Dem_DTC_FTB_Table[1]	1	
Dem_DTC_FTB_Table[2]	41	
Dem_DTC_FTB_Table[3]	22	
Dem_DTC_FTB_Table[4]	24	
Dem_DTC_FTB_Table[5]	254	
Dem_DTC_FTB_Table[6]	209	
Dem_DTC_FTB_Table[7]	209	
Dem_DTC_FTB_Table[8]	181	
Dem_DTC_FTB_Table[9]	1	
Dem_DTC_FTB_Table[10]	209	
Dem_DTC_FTB_Table[11]	128	
Dem_DTC_FTB_Table[12]	1	
Dem_DTC_FTB_Table[13]	209	
Dem_DTC_FTB_Table[14]	181	
Dem_DTC_FTB_Table[15]	1	
Dem_DTC_FTB_Table[16]	1	
Dem_DTC_FTB_Table[17]	209	
Dem_DTC_FTB_Table[18]	33	
Dem_DTC_FTB_Table[19]	181	
Dem DTC FTB Table[20]	1	
Dem_DTC_FTB_Table[21]	209	
Dem_DTC_FTB_Table[21]	181	
Dem_DTC_FTB_Table[22]	41	
	22	
Dem_DTC_FTB_Table[24]		
Dem_DTC_FTB_Table[25]	24	
Dem_DTC_FTB_Table[26]	254	
Dem_DTC_FTB_Table[27]	1	
Dem_DTC_FTB_Table[28]	181	
Dem_DTC_FTB_Table[29]	1	
Dem_DTC_FTB_Table[30]	181	
Dem_DTC_FTB_Table[31]	181	
Dem_DTC_FTB_Table[32]	1	
Dem_DTC_FTB_Table[33]	1	
Dem_DTC_FTB_Table[34]	181	
Dem_DTC_FTB_Table[35]	1	
Dem_DTC_FTB_Table[36]	181	
Dem_DTC_FTB_Table[37]	181	
Dem_DTC_FTB_Table[38]	181	
Dem_DTC_FTB_Table[39]	1	
Dem_DTC_FTB_Table[40]	1	
	41	
Dem_DTC_FTB_Table[41]		

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Name	Input Value		
Dem_DTC_FTB_Table[43]	24		
Dem_DTC_FTB_Table[44]	254		
Dem_DTC_FTB_Table[45]	209		
Dem_DTC_FTB_Table[46]	181		
Dem_DTC_FTB_Table[47]	1 22		
Dem_DTC_FTB_Table[48] Dem_DTC_FTB_Table[49]	181		
Dem_DTC_FTB_Table[49]	1		
Dem_DTC_FTB_Table[51]	181		
Dem_DTC_FTB_Table[52]	181		
Dem DTC FTB Table[53]	1		
Dem_DTC_FTB_Table[54]	22		
Dem_DTC_FTB_Table[55]	209		
Dem_DTC_FTB_Table[56]	181		
Dem_DTC_FTB_Table[57]	1		
Dem_DTC_FTB_Table[58]	181		
Dem_DTC_FTB_Table[59]	209		
Dem_DTC_FTB_Table[60]	181		
Dem_DTC_FTB_Table[61]	1		
Dem_DTC_FTB_Table[62]	22		
Dem_DTC_FTB_Table[63]	41		
Dem_DTC_FTB_Table[64]	22		
Dem_DTC_FTB_Table[65]	24		
Dem_DTC_FTB_Table[66]	254		
Dem_DTC_FTB_Table[67]	181 181		
Dem_DTC_FTB_Table[68]	181		
Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70]	22		
Dell_DTC_FTB_Table[70]	22 209		
Dom DTC ETR Table[71]			
Dem_DTC_FTB_Table[71]			
Dem_DTC_FTB_Table[72]	22		
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	22 41		
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	22 41 22		
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75]	22 41		
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	22 41 22 24 254	Expected Value	Result
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	22 41 22 24 254 Actual Value	Expected Value	Result
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	22 41 22 24 254	Expected Value 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	22 41 22 24 254 Actual Value	1	•
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	22 41 22 24 254 Actual Value 1	1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	22 41 22 24 254 Actual Value 1 1	1 1 0	•
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	22 41 22 24 254 Actual Value 1 1 0	1 1 0 1	•
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	22 41 22 24 254 Actual Value 1 1 0 1	1 1 0 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6]	22 41 22 24 254 Actual Value 1 1 0 1 1 1 1	1 1 0 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	22 41 22 24 254 Actual Value 1 1 0 1 1 1 1 1	1 1 0 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8]	22 41 22 24 254  Actual Value  1 0 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	22 41 22 24 254  Actual Value  1 0 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11]	22 41 22 24 254  Actual Value  1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13]	22 41 22 24 254  Actual Value  1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	22 41 22 24 254  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
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Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	
Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[10] CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34]	22 41 22 24 254  Actual Value  1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[47]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[59]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[60]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[68]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>✓</b>
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	<b>✓</b>
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	~

Test Step 2.7 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1 0
CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0 0
CTCFailedBuf_Cnt_M_lgc[43] CTCFailedBuf Cnt M lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52] CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61] CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0 0
CTCFailedBuf_Cnt_M_lgc[70] CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	1
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	3405792142
DTCKind DTCStatusNew	2 206
DTCStatusNew DTCStatusOld	84
Dem_DTCNumberTable[0]	83
Dem_DTCNumberTable[1]	99
Dem_DTCNumberTable[2]	240
Dem_DTCNumberTable[3]	233
Dem_DTCNumberTable[4]	31
Dem_DTCNumberTable[5]	75
Dem_DTCNumberTable[6]	164
Dem_DTCNumberTable[7]	164
Dem_DTCNumberTable[8]	83
Dem_DTCNumberTable[9]	
Dem_DTCNumberTable[9] Dem_DTCNumberTable[10]	99 164

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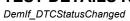
Demlf_DTCStatusChanged		TOLO (LAG
Name	Input Value	
Dem_DTCNumberTable[12]	99	
Dem_DTCNumberTable[13]	164	
Dem_DTCNumberTable[14]	83	
Dem_DTCNumberTable[15]	99	
Dem_DTCNumberTable[16]	99	
Dem_DTCNumberTable[17]	164	
Dem_DTCNumberTable[18]	74	
Dem_DTCNumberTable[19]	83	
Dem_DTCNumberTable[20]	99	
Dem_DTCNumberTable[21]	164	
Dem_DTCNumberTable[22]	83	
Dem_DTCNumberTable[23]	240	
Dem_DTCNumberTable[24]	233	
Dem_DTCNumberTable[25]	31	
Dem_DTCNumberTable[26]	75	
Dem_DTCNumberTable[27]	99	
Dem_DTCNumberTable[28]	83	
Dem_DTCNumberTable[29]	99	
Dem_DTCNumberTable[30]	83	
Dem_DTCNumberTable[31]	83	
Dem_DTCNumberTable[32]	99	
Dem_DTCNumberTable[33]	99	
Dem_DTCNumberTable[34]	83	
Dem_DTCNumberTable[35]	99	
Dem_DTCNumberTable[36]	83	
Dem_DTCNumberTable[37]	83	
Dem_DTCNumberTable[38]	83	
Dem_DTCNumberTable[39]	99	
Dem_DTCNumberTable[40]	99	
Dem_DTCNumberTable[41]	240	
Dem_DTCNumberTable[42]	233	
Dem_DTCNumberTable[43]	31	
Dem_DTCNumberTable[44]	75	
Dem_DTCNumberTable[45]	164	
Dem_DTCNumberTable[46]	83	
Dem_DTCNumberTable[47]	99	
Dem_DTCNumberTable[48]	233	
Dem_DTCNumberTable[49]	83	
Dem_DTCNumberTable[50]	99	
Dem_DTCNumberTable[51]	83	
Dem_DTCNumberTable[52]	83	
Dem_DTCNumberTable[53]	99	
Dem_DTCNumberTable[54]	233	
Dem_DTCNumberTable[55]	164	
Dem_DTCNumberTable[56]	83	
Dem_DTCNumberTable[57]	99	
Dem_DTCNumberTable[58]	83	
Dem_DTCNumberTable[59]	164	
Dem_DTCNumberTable[60]	83	
Dem_DTCNumberTable[61]	99	
Dem_DTCNumberTable[62]	233	
Dem_DTCNumberTable[63]	240	
Dem_DTCNumberTable[64]	233	
Dem_DTCNumberTable[65]	31	
Dem_DTCNumberTable[66]	75	
Dem_DTCNumberTable[67]	83	
Dem_DTCNumberTable[68]	83	
Dem_DTCNumberTable[69]	99	
Dem_DTCNumberTable[70]	233	
Dem_DTCNumberTable[71]	164	
Dem_DTCNumberTable[72]	233	
Dem_DTCNumberTable[73]	240	
Dem_DTCNumberTable[74]	233	
Dem_DTCNumberTable[75]	31	
Dem_DTCNumberTable[76]	75	
Dem_DTC_FTB_Table[0]	182	
Dem_DTC_FTB_Table[1]	221	
Dem_DTC_FTB_Table[2]	159	
Dem_DTC_FTB_Table[3]	164	
Dem_DTC_FTB_Table[4]	34	
Dem_DTC_FTB_Table[5]	166	
Dem_DTC_FTB_Table[6]	237	
	237	

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		TOLE !!	
Name	Input Value		
Dem_DTC_FTB_Table[8]	182		
Dem_DTC_FTB_Table[9]	221		
Dem_DTC_FTB_Table[10]	237		
Dem_DTC_FTB_Table[11]	123		
Dem_DTC_FTB_Table[12]	221		
Dem_DTC_FTB_Table[13]	237		
Dem_DTC_FTB_Table[14]	182		
Dem_DTC_FTB_Table[15]	221		
Dem_DTC_FTB_Table[16]	221		
Dem_DTC_FTB_Table[17]	237		
Dem_DTC_FTB_Table[18]	239		
Dem_DTC_FTB_Table[19]	182		
Dem_DTC_FTB_Table[20]	221 237		
Dem_DTC_FTB_Table[21] Dem_DTC_FTB_Table[22]	182		
Dem_DTC_FTB_Table[23]	159		
Dem_DTC_FTB_Table[24]	164		
Dem_DTC_FTB_Table[25]	34		
Dem_DTC_FTB_Table[26]	166		
Dem_DTC_FTB_Table[27]	221		
Dem_DTC_FTB_Table[28]	182		
Dem_DTC_FTB_Table[29]	221		
Dem_DTC_FTB_Table[30]	182		
Dem_DTC_FTB_Table[31]	182		
Dem_DTC_FTB_Table[32]	221		
Dem_DTC_FTB_Table[33]	221		
Dem_DTC_FTB_Table[34]	182		
Dem_DTC_FTB_Table[35]	221		
Dem_DTC_FTB_Table[36]	182		
Dem_DTC_FTB_Table[37]	182		
Dem_DTC_FTB_Table[38]	182		
Dem_DTC_FTB_Table[39]	221		
Dem_DTC_FTB_Table[40]	159		
Dem_DTC_FTB_Table[41] Dem_DTC_FTB_Table[42]	164		
Dem_DTC_FTB_Table[43]	34		
Dem_DTC_FTB_Table[44]	166		
Dem_DTC_FTB_Table[45]	237		
Dem_DTC_FTB_Table[46]	182		
Dem_DTC_FTB_Table[47]	221		
Dem_DTC_FTB_Table[48]	164		
Dem_DTC_FTB_Table[49]	182		
Dem_DTC_FTB_Table[50]	221		
Dem_DTC_FTB_Table[51]	182		
Dem_DTC_FTB_Table[52]	182		
Dem_DTC_FTB_Table[53]	221		
Dem_DTC_FTB_Table[54]	164		
Dem_DTC_FTB_Table[55]	237		
Dem_DTC_FTB_Table[56]	182		
Dem_DTC_FTB_Table[57]	221		
Dem_DTC_FTB_Table[58]	182		
Dem_DTC_FTB_Table[59]	237 182		
Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61]	221		
Dem_DTC_FTB_Table[62]	164		
Dem_DTC_FTB_Table[63]	159		
Dem_DTC_FTB_Table[65]	164		
Dem_DTC_FTB_Table[65]	34		
Dem_DTC_FTB_Table[66]	166		
Dem_DTC_FTB_Table[67]	182		
Dem_DTC_FTB_Table[68]	182		
Dem_DTC_FTB_Table[69]	221		
Dem_DTC_FTB_Table[70]	164		
Dem_DTC_FTB_Table[71]	237		
Dem_DTC_FTB_Table[72]	164		
Dem_DTC_FTB_Table[73]	159		
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	164		
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75]	164 34		
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	164 34 166		
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	164 34 166 Actual Value	Expected Value	Result
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name CTCFailedBuf_Cnt_M_lgc[0]	164 34 166 <b>Actual Value</b> 1	1	Result
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name	164 34 166 Actual Value	-	

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CTCFailedBuf_Cnt_M_lgc[7]	1	1	•
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[14]	1	1	~
CTCFailedBuf_Cnt_M_lgc[15]	1	1	•
CTCFailedBuf_Cnt_M_lgc[16]	1	1	~
CTCFailedBuf_Cnt_M_lgc[17]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[28]	1	1	~
CTCFailedBuf_Cnt_M_lgc[29]	0	0	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_Igc[47]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_Igc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	•
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_Igc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_Igc[55]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	•
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_Igc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[67]	0	0	•
CTCFailedBuf_Cnt_M_lgc[68]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[69]	0	0	•
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	1 0	1	
CTCFailedBuf_Cnt_M_lgc[75]	U	U	~

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Demlf	DTCS	tatus(	Changed

Name	Actual Value	Expected Value	Result
CTCFailedBuf Cnt M Igc[76]	0	0	✓ ×
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Stan 2.9 (Beneat Count = 4)	
Test Step 2.8 (Repeat Count = 1) Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_igc[17] CTCFailedBuf_Cnt_M_igc[18]	0
CTCFailedBuf Cnt M Igc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
	1
CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25]	1
	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0 0
CTCFailedBuf_Cnt_M_lgc[37]	
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64] CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76] CTCFailed_Cnt_M_lgc	1
DTC	20
DTCKind	1
DTCStatusNew	24
DTCStatusOld	0
Dem_DTCNumberTable[0]	67
Dem_DTCNumberTable[1]	177
Dem_DTCNumberTable[2]	247
Dem_DTCNumberTable[3]	156
Dem_DTCNumberTable[4]	178
Dem_DTCNumberTable[5]	171
Dem_DTCNumberTable[6]	176 176
Dem_DTCNumberTable[7] Dem_DTCNumberTable[8]	67
Dem_DTCNumberTable[9]	177
Dem_DTCNumberTable[10]	176
Dem_DTCNumberTable[11]	116
Dem_DTCNumberTable[12]	177
Dem_DTCNumberTable[13]	176
Dem_DTCNumberTable[14]	67
Dem_DTCNumberTable[15]	177
Dem_DTCNumberTable[16]	177
Dem_DTCNumberTable[17] Dem DTCNumberTable[18]	176 171
Dem DTCNumberTable[19]	67
Dem DTCNumberTable[20]	177
Dem_DTCNumberTable[21]	176
Dem_DTCNumberTable[22]	67
Dem_DTCNumberTable[23]	247
Dem_DTCNumberTable[24]	156
Dem_DTCNumberTable[25]	178
Dem_DTCNumberTable[26]	171
Dem_DTCNumberTable[27]	177
Dem_DTCNumberTable[28] Dem_DTCNumberTable[29]	67 177
Dem_DTCNumberTable[30]	67
Dem_DTCNumberTable[30]	67
Dem_DTCNumberTable[32]	177
Dem_DTCNumberTable[33]	177
Dem_DTCNumberTable[34]	67
Dem_DTCNumberTable[35]	177
Dem_DTCNumberTable[36]	67
Dem_DTCNumberTable[37]	67
Dem_DTCNumberTable[38]	67
Dem_DTCNumberTable[39]	177
Dem_DTCNumberTable[40] Dem_DTCNumberTable[41]	177 247
Dem_DTCNumberTable[41] Dem_DTCNumberTable[42]	156
Dem_DTCNumberTable[42]	178
Dem_DTCNumberTable[43] Dem_DTCNumberTable[44]	171
Dem_DTCNumberTable[45]	176
	67
Dem_DTCNumberTable[46]	
Dem_DTCNumberTable[47]	177
	177 156

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Name	Input Value	
Dem_DTCNumberTable[50]	177	
Dem_DTCNumberTable[51]	67	
Dem_DTCNumberTable[52]	67	
Dem_DTCNumberTable[53]	177	
Dem_DTCNumberTable[54]	156	
Dem_DTCNumberTable[55]	176	
Dem_DTCNumberTable[56]	67	
Dem_DTCNumberTable[57]	177	
Dem_DTCNumberTable[58]	67	
Dem_DTCNumberTable[59]	176	
Dem_DTCNumberTable[60]	67	
Dem_DTCNumberTable[61]	177	
Dem_DTCNumberTable[62]	156	
Dem_DTCNumberTable[63]	247	
Dem_DTCNumberTable[64]	156	
Dem_DTCNumberTable[65]	178	
Dem_DTCNumberTable[66]	171	
Dem_DTCNumberTable[67]	67	
Dem_DTCNumberTable[68]	67	
Dem_DTCNumberTable[69]	177	
Dem_DTCNumberTable[70]	156	
Dem_DTCNumberTable[71]	176	
Dem_DTCNumberTable[72]	156	
Dem_DTCNumberTable[73]	247	
Dem_DTCNumberTable[74]	156	
Dem_DTCNumberTable[75]	178	
Dem_DTCNumberTable[76]	171	
Dem_DTC_FTB_Table[0]	99	
Dem_DTC_FTB_Table[1]	143	
Dem_DTC_FTB_Table[2]	36	
Dem_DTC_FTB_Table[3]	85	
Dem_DTC_FTB_Table[4]	238	
Dem_DTC_FTB_Table[5]	62	
Dem_DTC_FTB_Table[6]	217	
Dem_DTC_FTB_Table[7]	217	
Dem_DTC_FTB_Table[8]	99	
Dem_DTC_FTB_Table[9]	143	
Dem_DTC_FTB_Table[10]	217	
Dem_DTC_FTB_Table[11]	101	
Dem_DTC_FTB_Table[12]	143	
Dem_DTC_FTB_Table[13]	217	
Dem_DTC_FTB_Table[14]	99	
Dem_DTC_FTB_Table[15]	143	
Dem_DTC_FTB_Table[16]	143	
Dem_DTC_FTB_Table[17]	217	
Dem_DTC_FTB_Table[18]	236	
Dem_DTC_FTB_Table[19]	99	
Dem_DTC_FTB_Table[20]	143	
Dem_DTC_FTB_Table[21]	217	
Dem_DTC_FTB_Table[22]	99	
Dem_DTC_FTB_Table[23]	36	
Dem_DTC_FTB_Table[24]	85	
Dem_DTC_FTB_Table[25]	238	
Dem_DTC_FTB_Table[26]	62	
Dem_DTC_FTB_Table[27]	143	
Dem_DTC_FTB_Table[28]	99	
Dem_DTC_FTB_Table[29]	143	
Dem_DTC_FTB_Table[30]	99	
Dem_DTC_FTB_Table[31]	99	
Dem_DTC_FTB_Table[32]	143	
Dem_DTC_FTB_Table[33]	143	
Dem_DTC_FTB_Table[34]	99	
Dem_DTC_FTB_Table[35]	143	
Dem_DTC_FTB_Table[36]	99	
Dem_DTC_FTB_Table[37]	99	
Dem_DTC_FTB_Table[38]	99	
Dem_DTC_FTB_Table[39]	143	
Dem_DTC_FTB_Table[40]	143	
Dem_DTC_FTB_Table[41]	36	
Dem_DTC_FTB_Table[42]	85	
Dem_DTC_FTB_Table[43]	238	
Dem_DTC_FTB_Table[44]	62	

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		( 10	,0
Name	Input Value		
Dem_DTC_FTB_Table[46]	99		
Dem_DTC_FTB_Table[47]	143		
Dem_DTC_FTB_Table[48]	85		
Dem_DTC_FTB_Table[49] Dem_DTC_FTB_Table[50]	99 143		
Dem_DTC_FTB_Table[51]	99		
Dem_DTC_FTB_Table[52]	99		
Dem_DTC_FTB_Table[53]	143		
Dem_DTC_FTB_Table[54]	85		
Dem_DTC_FTB_Table[55]	217		
Dem_DTC_FTB_Table[56]	99		
Dem_DTC_FTB_Table[57]	143		
Dem_DTC_FTB_Table[58]	99 217		
Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60]	99		
Dem_DTC_FTB_Table[61]	143		
Dem_DTC_FTB_Table[62]	85		
Dem_DTC_FTB_Table[63]	36		
Dem_DTC_FTB_Table[64]	85		
Dem_DTC_FTB_Table[65]	238		
Dem_DTC_FTB_Table[66]	62		
Dem_DTC_FTB_Table[67]	99		
Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69]	143		
Dem_DTC_FTB_Table[70]	85		
Dem_DTC_FTB_Table[71]	217		
Dem_DTC_FTB_Table[72]	85		
Dem_DTC_FTB_Table[73]	36		
Dem_DTC_FTB_Table[74]	85		
Dem_DTC_FTB_Table[75]	238		
Dem_DTC_FTB_Table[76]	62	I	1
Name	Actual Value	Expected Value	Resul
CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	1	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	1	
CTCFailedBuf_Cnt_M_lgc[4]	0	0	
CTCFailedBuf_Cnt_M_lgc[5]	1	1	•
CTCFailedBuf_Cnt_M_lgc[6]	1	1	•
CTCFailedBuf_Cnt_M_lgc[7]	1	1	•
CTCFailedBuf_Cnt_M_lgc[8]	1	1	
CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	1	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	1	
CTCFailedBuf_Cnt_M_lgc[12]	0	0	•
CTCFailedBuf_Cnt_M_lgc[13]	1	1	•
CTCFailedBuf_Cnt_M_lgc[14]	1	1	•
CTCFailedBuf_Cnt_M_lgc[15]	1	1	•
CTCFailedBuf_Cnt_M_lgc[16]	1	1	•
CTCFailedBuf_Cnt_M_lgc[17]	0	1	•
CTCFailedBuf_Cnt_M_lgc[18] CTCFailedBuf_Cnt_M_lgc[19]	1	0	
CTCFailedBuf Cnt M lgc[20]	0	0	
CTCFailedBuf_Cnt_M_lgc[21]			
	0	0	
CTCFailedBuf_Cnt_M_lgc[22]			
	0	0	•
CTCFailedBuf_Cnt_M_lgc[22]	0	0 0 1 1	•
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25]	0 0 1 1	0 0 1 1	•
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	0 0 1 1 1	0 0 1 1 1 1	•
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	0 0 1 1 1 1 1	0 0 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	0 0 1 1 1 1 1	0 0 1 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28]	0 0 1 1 1 1 1	0 0 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	0 0 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1	•
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30]	0 0 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31]	0 0 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33]	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36]	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 0	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[37]	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23] CTCFailedBuf_Cnt_M_lgc[24] CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29] CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31] CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0 0 1 1 1 1 1 1 1 1 1 1 1 1 0 0	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	

Demlf\_DTCStatusChanged

Demlf DTCStatusChanged()

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

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**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[48]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] n 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] n 0 **>** > > > CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf\_Cnt\_M\_lgc[56] 1 CTCFailedBuf\_Cnt\_M\_lgc[57] CTCFailedBuf\_Cnt\_M\_lgc[58] 1 CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] n 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 1 1

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	•

0

0

Test Step 2.9 (Repeat Count = 1)	✓
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46] CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBur_Cnt_M_igc[47] CTCFailedBur_Cnt_M_igc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56] CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64] CTCFailedBuf_Cnt_M_lgc[65]	1
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74] CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	1692840925
DTCKind	1
DTCStatusNew	34
DTCStatusOld	255
Dem_DTCNumberTable[0] Dem_DTCNumberTable[1]	89 78
Dem_DTCNumberTable[1] Dem_DTCNumberTable[2]	204
Dem_DTCNumberTable[3]	103
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	77
Dem_DTCNumberTable[6]	228
Dem_DTCNumberTable[7]	228
Dem_DTCNumberTable[8]	89
Dem_DTCNumberTable[9]	78
Dom DTCNumberTeble[10]	228
Dem_DTCNumberTable[10]	00
Dem_DTCNumberTable[11]	90
	90 78 228

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Demlf_DTCStatusChanged		MACILAL
Name	Input Value	
Dem_DTCNumberTable[15]	78	
Dem_DTCNumberTable[16]	78	
Dem_DTCNumberTable[17]	228	
Dem_DTCNumberTable[18]	228	
Dem_DTCNumberTable[19]	89	
Dem_DTCNumberTable[20]	78	
Dem_DTCNumberTable[21]	228	
Dem_DTCNumberTable[22]	89	
Dem_DTCNumberTable[23]	204	
Dem_DTCNumberTable[24]	103	
Dem_DTCNumberTable[25]	238	
Dem_DTCNumberTable[26]	77	
Dem_DTCNumberTable[27] Dem_DTCNumberTable[28]	78 89	
Dem_DTCNumberTable[29]	78	
Dem_DTCNumberTable[29]	89	
Dem_DTCNumberTable[31]	89	
Dem_DTCNumberTable[32]	78	
Dem_DTCNumberTable[33]	78	
Dem_DTCNumberTable[34]	89	
DTCNumberTable[35]	78	
DTCNumberTable[36]	89	
DTCNumberTable[37]	89	
Dem_DTCNumberTable[38]	89	
Dem_DTCNumberTable[39]	78	
Dem_DTCNumberTable[40]	78	
Dem_DTCNumberTable[41]	204	
Dem_DTCNumberTable[42]	103	
Dem_DTCNumberTable[43]	238	
Dem_DTCNumberTable[44]	77	
Dem_DTCNumberTable[45]	228	
Dem_DTCNumberTable[46]	89	
Dem_DTCNumberTable[47]	78	
Dem_DTCNumberTable[48]	103	
Dem_DTCNumberTable[49]	89	
Dem_DTCNumberTable[50] Dem_DTCNumberTable[51]	78 89	
Dem_DTCNumberTable[51]	89	
Dem_DTCNumberTable[52]	78	
Dem_DTCNumberTable[54]	103	
Dem_DTCNumberTable[55]	228	
Dem DTCNumberTable[56]	89	
Dem_DTCNumberTable[57]	78	
Dem_DTCNumberTable[58]	89	
Dem_DTCNumberTable[59]	228	
Dem_DTCNumberTable[60]	89	
Dem_DTCNumberTable[61]	78	
Dem_DTCNumberTable[62]	103	
Dem_DTCNumberTable[63]	204	
Dem_DTCNumberTable[64]	103	
0em_DTCNumberTable[65]	238	
Dem_DTCNumberTable[66]	77	
em_DTCNumberTable[67]	89	
Dem_DTCNumberTable[68]	89	
Dem_DTCNumberTable[69]	78	
Dem_DTCNumberTable[70]	103	
Dem_DTCNumberTable[71]	228	
Dem_DTCNumberTable[72]	103	
Dem_DTCNumberTable[73]	204	
pem_DTCNumberTable[74] pem_DTCNumberTable[75]	103 238	
rem_DTCNumberTable[75]  Dem_DTCNumberTable[76]	77	
Dem_DTC_FTB_Table[0]	31	
pem_DTC_FTB_Table[0]	227	
Dem_DTC_FTB_Table[1]	66	
Dem_DTC_FTB_Table[3]	96	
Dem_DTC_FTB_Table[4]	130	
Dem_DTC_FTB_Table[5]	24	
Dem_DTC_FTB_Table[6]	240	
Dem_DTC_FTB_Table[7]	240	
Dem_DTC_FTB_Table[8]	31	
Dem_DTC_FTB_Table[8] Dem_DTC_FTB_Table[9]	31 227	

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		( 10	,0
Name	Input Value		
Dem_DTC_FTB_Table[11]	151		
Dem_DTC_FTB_Table[12]	227		
Dem_DTC_FTB_Table[13]	240		
Dem_DTC_FTB_Table[14]	31		
Dem_DTC_FTB_Table[15]	227		
Dem_DTC_FTB_Table[16]	227		
Dem_DTC_FTB_Table[17]	240		
Dem_DTC_FTB_Table[18]	241		
Dem_DTC_FTB_Table[19]	31		
Dem_DTC_FTB_Table[20]	227		
Dem_DTC_FTB_Table[21]	240		
Dem_DTC_FTB_Table[22]	31		
Dem_DTC_FTB_Table[23]	66		
Dem_DTC_FTB_Table[24] Dem_DTC_FTB_Table[25]	96		
Dem_DTC_FTB_Table[26]	130 24		
Dem_DTC_FTB_Table[20] Dem_DTC_FTB_Table[27]	227		
Dem_DTC_FTB_Table[28]	31		
Dem_DTC_FTB_Table[29]	227		
Dem_DTC_FTB_Table[30]	31		
Dem_DTC_FTB_Table[31]	31		
Dem_DTC_FTB_Table[31]	227		
Dem_DTC_FTB_Table[32]	227		
Dem DTC FTB Table[34]	31		
Dem_DTC_FTB_Table[35]	227		
Dem_DTC_FTB_Table[36]	31		
Dem_DTC_FTB_Table[37]	31		
Dem_DTC_FTB_Table[38]	31		
Dem_DTC_FTB_Table[39]	227		
Dem_DTC_FTB_Table[40]	227		
Dem_DTC_FTB_Table[41]	66		
Dem_DTC_FTB_Table[42]	96		
Dem_DTC_FTB_Table[43]	130		
Dem_DTC_FTB_Table[44]	24		
Dem_DTC_FTB_Table[45]	240		
Dem_DTC_FTB_Table[46]	31		
Dem_DTC_FTB_Table[47]	227		
Dem_DTC_FTB_Table[48]	96		
Dem_DTC_FTB_Table[49]	31		
Dem_DTC_FTB_Table[50]	227		
Dem_DTC_FTB_Table[51]	31		
Dem_DTC_FTB_Table[52]	31		
Dem_DTC_FTB_Table[53]	227		
Dem_DTC_FTB_Table[54]	96		
Dem_DTC_FTB_Table[55]	240		
Dem_DTC_FTB_Table[56]	31		
Dem_DTC_FTB_Table[57]	227		
Dem_DTC_FTB_Table[58]	31		
Dem_DTC_FTB_Table[59]	240		
Dem_DTC_FTB_Table[60]	31		
Dem_DTC_FTB_Table[61]	227		
Dem_DTC_FTB_Table[62]	96		
Dem_DTC_FTB_Table[63]	66		
Dem_DTC_FTB_Table[64]	96		
Dem_DTC_FTB_Table[65]	130		
Dem_DTC_FTB_Table[66]	24		
Dem_DTC_FTB_Table[67]	31		
Dem_DTC_FTB_Table[68]	31		
Dem_DTC_FTB_Table[69]	227		
Dem_DTC_FTB_Table[70]	96		
Dem_DTC_FTB_Table[71]	240		
Dem_DTC_FTB_Table[72]	96		
Dem_DTC_FTB_Table[73]	66		
Dem_DTC_FTB_Table[74]	96		
Dem_DTC_FTB_Table[75]	130		
Dom DTC FTD Toble[76]	24	E-marked Mar	
		Expected Value	Resu
Name	Actual Value		
Name CTCFailedBuf_Cnt_M_lgc[0]	1	1	
Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]	1	1	•
Name CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	1 1 1	1	
Name CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	1	1	

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Demlf\_DTCStatusChanged **Actual Value Expected Value** Result CTCFailedBuf Cnt M Iqc[6] CTCFailedBuf\_Cnt\_M\_lgc[7] CTCFailedBuf Cnt M lqc[8] CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf Cnt M lqc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] CTCFailedBuf Cnt M lqc[12] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[13] 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] 1 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 0 CTCFailedBuf Cnt M lqc[23] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[24] 1 **v** CTCFailedBuf\_Cnt\_M\_lgc[25] 1 CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[28] CTCFailedBuf\_Cnt\_M\_lgc[29] 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] CTCFailedBuf\_Cnt\_M\_lgc[32]  $CTCFailedBuf\_Cnt\_M\_lgc[33]$ CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf Cnt M Igc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf Cnt M Igc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf Cnt M Iqc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 • CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] n n CTCFailedBuf\_Cnt\_M\_Igc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] n 0 CTCFailedBuf\_Cnt\_M\_Igc[53] 0 CTCFailedBuf\_Cnt\_M\_lgc[54] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[55] CTCFailedBuf Cnt M Igc[56] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[57] CTCFailedBuf Cnt M lqc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60]  $CTCFailedBuf\_Cnt\_M\_lgc[61]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 n **✓** CTCFailedBuf Cnt M lqc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] n 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0

0

0

0

0

CTCFailed\_Cnt\_M\_lgc

Demlf\_DTCStatusChanged

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Name	Actual Value	Expected Value	Result
Rte Write Ap Demlf CTCFailed Cnt lgc(data)	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Contractional Control   Miles   Section   Se	T4-04	
CICP-anisetts, Com. M. 19400 CICP-anisetts, Com. M. 19410 CICP-anisetts, Com. M. 19420 CICP-anisetts, Com. M. 19440 CICP-anisetts, C	Test Step 2.10 (Repeat Count = 1)	·
CICTRAISMENT, ON M. 19021  CICTRAISMENT, ON M. 19030  CICTRAISMENT, ON M. 190410  CICTRAISMENT, ON M. 190420  CICTRAISMENT,		•
CICS-anisettal_Cort.M.get3		
CITCFaiesdud, Cal. M, 19619 CTCFaiesdud, Cal. M, 19610 CTCFaiesdud, Cal. M, 19620 CTCFaiesdud, Cal. M,		
CTOFalested CM, M, 1954  CTOFalested CM, M, 1959  CTOFalested CM, CM, 1		
CICFaleadu, Col. M. 1968 1		
CICFaireaged, Cott, Mig-198  1 CTCFaireaged, Cott, Mig-198  1		
CICFallesBuff Cost M, 19671  CICFallesBuff Cost M, 19670  CICFallesBuff Cost M, 19670  CICFallesBuff Cost M, 19671  CICFallesBuff Cost M, 19672  CICFallesBuff Cost M, 19674  CICFallesBuff Cost M, 19678  CICFallesBuff Cost M, 19678  CICFallesBuff Cost M, 19678  CICFallesBuff Co		
CICFaiesded Cent M, 1909  1 CICFaiesded Cent M, 19010  1 CICFaiesded Cent M, 19010  1 CICFaiesded Cent M, 19010  1 CICFaiesded Cent M, 19011  1 CICFaiesded Cent M, 19012  1 CICFaiesded Cent M, 19013		
CCFaleabud Cnt. M. jugdi)  CCFaleabud Cnt. M. jugdi)  CCFaleabud Cnt. M. jugdi)  CCFaleabud Cnt. M. jugdii  CCFaleabud Cnt. M. jugdiii  CCFaleabud Cnt. M. jugdiii  CCFaleabud Cnt. M. jugdiii  CCFaleabud Cnt. M.		
CTG-RiesBud Cot M 19210 1 CTG-RiesBud Cot M 19212 1 CTG-RiesBud Cot M 19212 1 CTG-RiesBud Cot M 19214 1 CTG-RiesBud Cot M 19218 1 CTG-RiesBud Cot M 19220 0 CTG-RiesBud Cot M 19220 0 CTG-RiesBud Cot M 19220 0 CTG-RiesBud Cot M 19222 0 CTG-RiesBud Cot M 19223 1 CTG-RiesBud Cot M 19228 1 CTG-RiesBud Cot M 19239 1 CTG-RiesBud Cot M		
CICFaleadury Cont M. pgd13	CTCFailedBuf_Cnt_M_lgc[10]	1
CICFaleadsu Cnt M, pdf19 CICFaleadsu Cnt M, pdf20 CICFaleadsu Cnt M, pdf40 CICFaleadsu Cnt M, pd	CTCFailedBuf_Cnt_M_lgc[11]	1.
CTCFaieBull Cnt M, pgt19 TCTGaieBull Cnt M, pgt29 OCTGAieBull Cnt M, pgt29 OCTGAieBull Cnt M, pgt29 OCTGAieBull Cnt M, pgt29 TCTGaieBull Cnt M, pgt49 TCTGaieBull Cnt M, pg	CTCFailedBuf_Cnt_M_lgc[12]	0
CICFIarledtus Cott, M. 19415 CICFIarledtus Cott, M. 19417 CICFIarledtus Cott, M. 19427 CICFIarledtus Cott, M. 19427 CICFIarledtus Cott, M. 19427 CICFIarledtus Cott, M. 19427 CICFIarledtus Cott, M. 19428 CICFIarledtus Cott, M. 19438 CICFIarledtus Cott, M. 19448 CICFIarledtus Cott, M. 19449 CICFIarledtus Co	CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFaledBufL Crt. M. Jeg(19)	CTCFailedBuf_Cnt_M_lgc[14]	1
CICFaledBut_Crt, M_ lgd(18)	CTCFailedBuf_Cnt_M_lgc[15]	
CICFaledBuf, Cnt, M, Igct19  CICFaledBuf, Cnt, M, Igct20  CICFaledBuf, Cnt		
CCF alledBuf_Cnt_M_lgq213		
CICFaledBuf, Cnt, M, 19ct20 CICFaledBuf, Cnt, M, 19ct22 CICFaledBuf, Cnt, M, 19ct22 CICFaledBuf, Cnt, M, 19ct23 CICFaledBuf, Cnt, M, 19ct23 CICFaledBuf, Cnt, M, 19ct25 CICFaledBuf, Cnt, M, 19ct25 CICFaledBuf, Cnt, M, 19ct25 CICFaledBuf, Cnt, M, 19ct25 CICFaledBuf, Cnt, M, 19ct27 CICFaledBuf, Cnt, M, 19ct27 CICFaledBuf, Cnt, M, 19ct28 CICFaledBuf, Cnt, M, 19ct29 CICFaledBuf, Cnt, M, 19ct30 CICFaledBuf, Cnt, M, 19ct30 CICFaledBuf, Cnt, M, 19ct32 CICFaledBuf, Cnt, M, 19ct32 CICFaledBuf, Cnt, M, 19ct33 CICFaledBuf, Cnt, M, 19ct33 CICFaledBuf, Cnt, M, 19ct33 CICFaledBuf, Cnt, M, 19ct35 CICFaledBuf, Cnt, M, 19ct35 CICFaledBuf, Cnt, M, 19ct35 CICFaledBuf, Cnt, M, 19ct37 CICFaledBuf, Cnt, M, 19ct39 CICFaledBuf, Cnt, M, 19ct39 CICFaledBuf, Cnt, M, 19ct39 CICFaledBuf, Cnt, M, 19ct39 CICFaledBuf, Cnt, M, 19ct40 CICFaledBuf, Cnt, M, 19ct50 CI	CTCFailedBuf_Cnt_M_lgc[18]	
CTCFaiedBuf_Cn_M_igct21 CTCFaiedBuf_Cn_M_igct22 CTCFaiedBuf_Cn_M_igct23 1 CTCFaiedBuf_Cn_M_igct24 1 CTCFaiedBuf_Cn_M_igct26 CTCFaiedBuf_Cn_M_igct26 CTCFaiedBuf_Cn_M_igct26 CTCFaiedBuf_Cn_M_igct26 CTCFaiedBuf_Cn_M_igct27 1 CTCFaiedBuf_Cn_M_igct28 CTCFaiedBuf_Cn_M_igct28 CTCFaiedBuf_Cn_M_igct28 CTCFaiedBuf_Cn_M_igct28 1 CTCFaiedBuf_Cn_M_igct28 CTCFaiedBuf_Cn_M_igct28 CTCFaiedBuf_Cn_M_igct28 CTCFaiedBuf_Cn_M_igct28 1 CTCFaiedBuf_Cn_M_igct31 CTCFaiedBuf_Cn_M_igct31 1 CTCFaiedBuf_Cn_M_igct31 1 CTCFaiedBuf_Cn_M_igct33 1 CTCFaiedBuf_Cn_M_igct33 1 CTCFaiedBuf_Cn_M_igct38 CTCFaiedBuf_Cn_M_igct38 CTCFaiedBuf_Cn_M_igct38 CTCFaiedBuf_Cn_M_igct48 CTCFaiedBuf_Cn_M_igct58 CTCFaiedBuf_		
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CTCFailedBuf_Cnt_M_lgct28    1		
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CTCFailedBuf_Cnt_M_lgc[40]       0         CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       0         CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[46]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1 <t< td=""><td></td><td></td></t<>		
CTCFailedBuf_Cnt_M_lgc[40]       0         CTCFailedBuf_Cnt_M_lgc[42]       0         CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[46]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[58]       1 <td></td> <td></td>		
CTCFailedBuf_Cnt_M_lgc[41]       1         CTCFailedBuf_Cnt_M_lgc[42]       0         CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1 <td></td> <td></td>		
CTCFailedBuf_Cnt_M_lgc[42]         0           CTCFailedBuf_Cnt_M_lgc[43]         0           CTCFailedBuf_Cnt_M_lgc[44]         0           CTCFailedBuf_Cnt_M_lgc[45]         0           CTCFailedBuf_Cnt_M_lgc[46]         0           CTCFailedBuf_Cnt_M_lgc[47]         0           CTCFailedBuf_Cnt_M_lgc[48]         0           CTCFailedBuf_Cnt_M_lgc[49]         0           CTCFailedBuf_Cnt_M_lgc[50]         0           CTCFailedBuf_Cnt_M_lgc[51]         0           CTCFailedBuf_Cnt_M_lgc[52]         0           CTCFailedBuf_Cnt_M_lgc[53]         1           CTCFailedBuf_Cnt_M_lgc[53]         1           CTCFailedBuf_Cnt_M_lgc[54]         1           CTCFailedBuf_Cnt_M_lgc[56]         1           CTCFailedBuf_Cnt_M_lgc[56]         1           CTCFailedBuf_Cnt_M_lgc[56]         1           CTCFailedBuf_Cnt_M_lgc[58]         1		
CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[46]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[46]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[46]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[49]	
CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[52]	
CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_Igc[53]	
CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[54]	
CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[55]	
CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1	CTCFailedBuf_Cnt_M_lgc[56]	
CTCFailedBuf_Cnt_M_lgc[59]         1           CTCFailedBuf_Cnt_M_lgc[60]         1	CTCFailedBuf_Cnt_M_lgc[57]	
CTCFailedBuf_Cnt_M_lgc[60] 1		
CTOFalledBut_Cnt_m_igc[b1]		
	CTCFalledBut_Cnt_M_Igc[61]	1

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Demlf_DTCStatusChanged		MACILAG
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[62]	0	
CTCFailedBuf_Cnt_M_lgc[63]	1	
CTCFailedBuf_Cnt_M_lgc[64]	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	
CTCFailedBuf_Cnt_M_lgc[70]	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	
CTCFailedBuf_Cnt_M_lgc[72]	0	
CTCFailedBuf_Cnt_M_lgc[73]	0	
CTCFailedBuf_Cnt_M_lgc[74]	0	
CTCFailedBuf_Cnt_M_lgc[75]	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	
CTCFailed_Cnt_M_lgc	1	
DTC	1392997139	
DTCKind	2	
OTCStatusNew	238	
DTCStatusOld	217	
Dem_DTCNumberTable[0]	170	
Dem_DTCNumberTable[1]	194	
Dem_DTCNumberTable[2]	13	
Dem_DTCNumberTable[3]	32	
Dem_DTCNumberTable[4]	172	
Dem_DTCNumberTable[5]	241	
Dem_DTCNumberTable[6]	91	
Dem_DTCNumberTable[7]	91	
Dem_DTCNumberTable[8]	170	
Dem_DTCNumberTable[9]	194	
Dem_DTCNumberTable[10]	91	
Dem_DTCNumberTable[11]	82	
Dem_DTCNumberTable[12]	194	
Dem_DTCNumberTable[13]	91	
Dem_DTCNumberTable[14]	170	
Dem_DTCNumberTable[15]	194	
Dem_DTCNumberTable[16]	194	
Dem_DTCNumberTable[17]	91	
Dem_DTCNumberTable[18]	55	
Dem_DTCNumberTable[19]	170	
Dem_DTCNumberTable[20]	194	
Dem_DTCNumberTable[21]	91 170	
Dem_DTCNumberTable[22]		
Dem_DTCNumberTable[23]	13	
Dem_DTCNumberTable[24]	32 172	
Dem_DTCNumberTable[25] Dem_DTCNumberTable[26]	241	
Dem_DTCNumberTable[27] Dem_DTCNumberTable[28]	194 170	
Dem_DTCNumberTable[28] Dem_DTCNumberTable[29]	194	
Dem_DTCNumberTable[29] Dem_DTCNumberTable[30]	170	
Dem_DTCNumberTable[30]	170	
Dem_DTCNumberTable[31]	194	
Dem_DTCNumberTable[32]	194	
Dem DTCNumberTable[33]	170	
Dem DTCNumberTable[34]	194	
Dem_DTCNumberTable[35]	170	
Dem_DTCNumberTable[30]	170	
Dem_DTCNumberTable[37]	170	
Dem_DTCNumberTable[39]	194	
Dem_DTCNumberTable[40]	194	
Dem_DTCNumberTable[40]	13	
Dem_DTCNumberTable[41]	32	
Dem_DTCNumberTable[42]	172	
Dem_DTCNumberTable[44]	241	
Dem_DTCNumberTable[45]	91	
Dem_DTCNumberTable[46]	170	
Dem_DTCNumberTable[40]	194	
Dem_DTCNumberTable[47]	32	
Dem_DTCNumberTable[40]	170	
Dem DTCNumberTable[50]	194	
Dem_DTCNumberTable[50] Dem_DTCNumberTable[51]	194 170	

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[53] 194 Dem\_DTCNumberTable[54] 32 Dem\_DTCNumberTable[55] 91 Dem\_DTCNumberTable[56] 170 Dem\_DTCNumberTable[57] 194 Dem\_DTCNumberTable[58] 170 Dem\_DTCNumberTable[59] 91 Dem\_DTCNumberTable[60] 170 Dem\_DTCNumberTable[61] 194 Dem DTCNumberTable[62] 32 Dem\_DTCNumberTable[63] 13 Dem\_DTCNumberTable[64] 32 Dem\_DTCNumberTable[65] 172 Dem DTCNumberTable[66] 241 Dem\_DTCNumberTable[67] 170 Dem\_DTCNumberTable[68] 170 Dem\_DTCNumberTable[69] 194 Dem\_DTCNumberTable[70] 32 Dem\_DTCNumberTable[71] 91 Dem\_DTCNumberTable[72] 32 Dem\_DTCNumberTable[73] 13 Dem\_DTCNumberTable[74] 32 Dem\_DTCNumberTable[75] 172 Dem\_DTCNumberTable[76] 241 Dem\_DTC\_FTB\_Table[0] 83 Dem\_DTC\_FTB\_Table[1] 99 Dem\_DTC\_FTB\_Table[2] 240 Dem\_DTC\_FTB\_Table[3] 233 Dem\_DTC\_FTB\_Table[4] 31 Dem\_DTC\_FTB\_Table[5] 75 Dem\_DTC\_FTB\_Table[6] 164 Dem\_DTC\_FTB\_Table[7] 164 Dem DTC FTB Table[8] 83 Dem\_DTC\_FTB\_Table[9] 99 Dem\_DTC\_FTB\_Table[10] 164 Dem DTC FTB Table[11] 40 Dem\_DTC\_FTB\_Table[12] 99 Dem\_DTC\_FTB\_Table[13] 164 Dem\_DTC\_FTB\_Table[14] 83 Dem DTC\_FTB\_Table[15] 99 Dem\_DTC\_FTB\_Table[16] 99 Dem DTC FTB Table[17] 164 Dem\_DTC\_FTB\_Table[18] 74 Dem\_DTC\_FTB\_Table[19] 83 Dem\_DTC\_FTB\_Table[20] 99 Dem\_DTC\_FTB\_Table[21] 164 83 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 240 Dem\_DTC\_FTB\_Table[24] 233 Dem\_DTC\_FTB\_Table[25] 31 Dem\_DTC\_FTB\_Table[26] 75 Dem\_DTC\_FTB\_Table[27] 99 Dem\_DTC\_FTB\_Table[28] 83 Dem\_DTC\_FTB\_Table[29] 99 Dem\_DTC\_FTB\_Table[30] 83 Dem\_DTC\_FTB\_Table[31] 83 Dem\_DTC\_FTB\_Table[32] 99 Dem\_DTC\_FTB\_Table[33] 99 Dem\_DTC\_FTB\_Table[34] 83 Dem\_DTC\_FTB\_Table[35] 99 Dem\_DTC\_FTB\_Table[36] 83 Dem\_DTC\_FTB\_Table[37] 83 Dem\_DTC\_FTB\_Table[38] 83 Dem\_DTC\_FTB\_Table[39] 99 Dem\_DTC\_FTB\_Table[40] 99 Dem DTC FTB Table[41] 240

233

31

75

164

83

99

233

Dem\_DTC\_FTB\_Table[42]

Dem DTC FTB Table[43]

Dem\_DTC\_FTB\_Table[44]

Dem\_DTC\_FTB\_Table[45]

Dem\_DTC\_FTB\_Table[46]

Dem\_DTC\_FTB\_Table[47]

Dem\_DTC\_FTB\_Table[48]

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		•	
Name	Input Value		
Dem_DTC_FTB_Table[49]	83		
Dem_DTC_FTB_Table[50]	99		
Dem_DTC_FTB_Table[51]	83		
Dem_DTC_FTB_Table[52]	83		
Dem_DTC_FTB_Table[53]	99 233		
Dem_DTC_FTB_Table[54] Dem_DTC_FTB_Table[55]	164		
Dem_DTC_FTB_Table[56]	83		
Dem_DTC_FTB_Table[57]	99		
Dem_DTC_FTB_Table[58]	83		
Dem_DTC_FTB_Table[59]	164		
Dem_DTC_FTB_Table[60]	83		
Dem_DTC_FTB_Table[61]	99		
Dem_DTC_FTB_Table[62]	233		
Dem_DTC_FTB_Table[63]	240		
Dem_DTC_FTB_Table[64]	233		
Dem_DTC_FTB_Table[65]	31   75		
Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67]	83		
Dem_DTC_FTB_Table[68]	83		
Dem_DTC_FTB_Table[69]	99		
Dem_DTC_FTB_Table[70]	233		
Dem_DTC_FTB_Table[71]	164		
Dem_DTC_FTB_Table[72]	233		
Dem_DTC_FTB_Table[73]	240		
Dem_DTC_FTB_Table[74]	233		
Dem_DTC_FTB_Table[75]	31		
Dem_DTC_FTB_Table[76]	75		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	1	1	
CTCFailedBuf_Cnt_M_lgc[5]	1	1	_
CTCFailedBuf_Cnt_M_lgc[6]	1	1	_
CTCFailedBuf_Cnt_M_lgc[7]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[12]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[13]	1	1	
CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	0	0	
CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[20]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[21]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	1	1	_
CTCFailedBuf_Cnt_M_lgc[28]	1	1	
CTCFailedBuf_Cnt_M_lgc[29]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[30]	1	1	_
CTCFailedBuf_Cnt_M_lgc[31]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	•
CTCFailedBuf_Cnt_M_lgc[36]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	•
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40] CTCFailedBuf_Cnt_M_lgc[41]	1	1	~
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	0	0	
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>V</b>
,			

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[44]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[45]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[46]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[62]	0	0	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[68]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	1	1	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.11 (Repeat Count = 1)		
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	1	
CTCFailedBuf_Cnt_M_lgc[1]	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	
CTCFailedBuf_Cnt_M_lgc[4]	1	
CTCFailedBuf_Cnt_M_lgc[5]	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	
CTCFailedBuf_Cnt_M_lgc[7]	1	
CTCFailedBuf_Cnt_M_lgc[8]	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	
CTCFailedBuf_Cnt_M_lgc[12]	1	
CTCFailedBuf_Cnt_M_lgc[13]	1	
CTCFailedBuf_Cnt_M_lgc[14]	1	
CTCFailedBuf_Cnt_M_lgc[15]	1	
CTCFailedBuf_Cnt_M_lgc[16]	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	
CTCFailedBuf_Cnt_M_lgc[18]	1	
CTCFailedBuf_Cnt_M_lgc[19]	1	
CTCFailedBuf_Cnt_M_lgc[20]	0	
CTCFailedBuf_Cnt_M_lgc[21]	0	
CTCFailedBuf_Cnt_M_lgc[22]	0	
CTCFailedBuf_Cnt_M_lgc[23]	1	
CTCFailedBuf_Cnt_M_lgc[24]	1	
CTCFailedBuf_Cnt_M_lgc[25]	1	
CTCFailedBuf_Cnt_M_lgc[26]	1	

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Demii_DTCStatusChanged	(WAC)
Name	Input Value
CTCFailedBuf Cnt M Igc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf Cnt M Igc[39]	0
	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	0
	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	983749041
DTCKind	2
DTCStatusNew	0
DTCStatusOld	240
Dem DTCNumberTable[0]	161
Dem DTCNumberTable[0]	211
Dem_DTCNumberTable[1] Dem_DTCNumberTable[2]	7
	239
Dem_DTCNumberTable[3]	
Dem_DTCNumberTable[4]	206
Dem_DTCNumberTable[5]	70
Dem_DTCNumberTable[6]	84
Dem_DTCNumberTable[7]	84
Dem_DTCNumberTable[8]	161
Dem_DTCNumberTable[9]	211
Dem_DTCNumberTable[10]	84
Dem_DTCNumberTable[11]	193
Dem_DTCNumberTable[12]	211
Dem_DTCNumberTable[13]	84
Dem_DTCNumberTable[14]	161
Dem_DTCNumberTable[15]	211
Dem_DTCNumberTable[16]	211

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[18] 108 Dem\_DTCNumberTable[19] 161 Dem DTCNumberTable[20] 211 Dem\_DTCNumberTable[21] 84 Dem DTCNumberTable[22] 161 Dem\_DTCNumberTable[23] 7 Dem\_DTCNumberTable[24] 239 Dem\_DTCNumberTable[25] 206 Dem\_DTCNumberTable[26] 70 Dem\_DTCNumberTable[27] 211 Dem\_DTCNumberTable[28] 161 Dem\_DTCNumberTable[29] 211 Dem\_DTCNumberTable[30] 161 Dem\_DTCNumberTable[31] 161 Dem\_DTCNumberTable[32] 211 Dem\_DTCNumberTable[33] 211 Dem\_DTCNumberTable[34] 161 Dem\_DTCNumberTable[35] 211 Dem\_DTCNumberTable[36] 161 Dem\_DTCNumberTable[37] 161 Dem\_DTCNumberTable[38] 161 Dem\_DTCNumberTable[39] 211 Dem\_DTCNumberTable[40] 211 Dem\_DTCNumberTable[41] Dem\_DTCNumberTable[42] 239 Dem\_DTCNumberTable[43] 206 Dem DTCNumberTable[44] 70 Dem\_DTCNumberTable[45] 84 Dem DTCNumberTable[46] 161 Dem\_DTCNumberTable[47] 211 Dem DTCNumberTable[48] 239 Dem\_DTCNumberTable[49] 161 Dem DTCNumberTable[50] 211 Dem\_DTCNumberTable[51] 161 Dem\_DTCNumberTable[52] 161 Dem\_DTCNumberTable[53] 211 Dem\_DTCNumberTable[54] 239 Dem\_DTCNumberTable[55] 84 Dem\_DTCNumberTable[56] 161 Dem\_DTCNumberTable[57] 211 Dem\_DTCNumberTable[58] 161 Dem\_DTCNumberTable[59] 84 Dem\_DTCNumberTable[60] 161 Dem\_DTCNumberTable[61] 211 Dem\_DTCNumberTable[62] 239 Dem\_DTCNumberTable[63] 7 Dem DTCNumberTable[64] 239 Dem\_DTCNumberTable[65] 206 Dem DTCNumberTable[66] 70 Dem\_DTCNumberTable[67] 161 Dem\_DTCNumberTable[68] 161 Dem\_DTCNumberTable[69] 211 Dem\_DTCNumberTable[70] 239 Dem\_DTCNumberTable[71] 84 Dem\_DTCNumberTable[72] 239 Dem\_DTCNumberTable[73] 7 Dem\_DTCNumberTable[74] 239 Dem\_DTCNumberTable[75] 206 Dem\_DTCNumberTable[76] 70 Dem\_DTC\_FTB\_Table[0] 46 Dem\_DTC\_FTB\_Table[1] 245 Dem\_DTC\_FTB\_Table[2] 24 Dem\_DTC\_FTB\_Table[3] 143 Dem\_DTC\_FTB\_Table[4] 13 Dem\_DTC\_FTB\_Table[5] 12

209

209

46

245

209

145

245

209

Dem DTC FTB Table[6]

Dem\_DTC\_FTB\_Table[7]

Dem DTC FTB Table[8]

Dem\_DTC\_FTB\_Table[9]

Dem\_DTC\_FTB\_Table[10]

Dem\_DTC\_FTB\_Table[11]

Dem\_DTC\_FTB\_Table[12]

Dem\_DTC\_FTB\_Table[13]

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		(	,0
Name	Input Value		
Dem_DTC_FTB_Table[14]	46		
Dem_DTC_FTB_Table[15]	245		
Dem_DTC_FTB_Table[16]	245		
Dem_DTC_FTB_Table[17]	209		
Dem_DTC_FTB_Table[18]	239		
Dem_DTC_FTB_Table[19]	46		
Dem_DTC_FTB_Table[20]	245		
Dem_DTC_FTB_Table[21]	209		
Dem_DTC_FTB_Table[22]	46		
Dem_DTC_FTB_Table[23]	24		
Dem_DTC_FTB_Table[24]	143		
Dem_DTC_FTB_Table[25]	13		
Dem_DTC_FTB_Table[26]	12		
Dem_DTC_FTB_Table[27]	245		
Dem_DTC_FTB_Table[28]	46		
Dem_DTC_FTB_Table[29]	245		
Dem_DTC_FTB_Table[30]	46		
Dem_DTC_FTB_Table[31]	46		
Dem_DTC_FTB_Table[32]	245		
Dem_DTC_FTB_Table[33]	245		
Dem_DTC_FTB_Table[34]	46		
Dem_DTC_FTB_Table[35]	245		
Dem_DTC_FTB_Table[36]	46		
Dem_DTC_FTB_Table[37]	46		
Dem_DTC_FTB_Table[38]	46		
Dem_DTC_FTB_Table[39]	245		
Dem_DTC_FTB_Table[40]	245		
Dem_DTC_FTB_Table[41]	24		
Dem_DTC_FTB_Table[42]	143		
Dem_DTC_FTB_Table[43]	13		
Dem_DTC_FTB_Table[44]	12		
Dem_DTC_FTB_Table[45]	209		
Dem_DTC_FTB_Table[46]	46 245		
Dem_DTC_FTB_Table[47] Dem_DTC_FTB_Table[48]	143		
Dem_DTC_FTB_Table[49]	46		
Dem_DTC_FTB_Table[50]	245		
Dem_DTC_FTB_Table[51]	46		
Dem_DTC_FTB_Table[52]	46		
Dem_DTC_FTB_Table[53]	245		
Dem_DTC_FTB_Table[54]	143		
Dem_DTC_FTB_Table[55]	209		
Dem_DTC_FTB_Table[56]	46		
Dem_DTC_FTB_Table[57]	245		
Dem_DTC_FTB_Table[58]	46		
Dem_DTC_FTB_Table[59]	209		
Dem_DTC_FTB_Table[60]	46		
Dem_DTC_FTB_Table[61]	245		
Dem_DTC_FTB_Table[62]	143		
Dem_DTC_FTB_Table[63]	24		
Dem_DTC_FTB_Table[64]	143		
Dem_DTC_FTB_Table[65]	13		
Dem_DTC_FTB_Table[66]	12		
Dem_DTC_FTB_Table[67]	46		
Dem_DTC_FTB_Table[68]	46		
Dem_DTC_FTB_Table[69]	245		
Dem_DTC_FTB_Table[70]	143		
Dem_DTC_FTB_Table[71]	209		
Dem_DTC_FTB_Table[72]	143		
Dem_DTC_FTB_Table[73]	24		
Dem_DTC_FTB_Table[74]	143		
Dem_DTC_FTB_Table[75]	13		
Dem_DTC_FTB_Table[76]	12		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	•
CTCFailedBuf_Cnt_M_lgc[6]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	1	1	

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Name	Actual Value	Expected Value	Resul
CTCFailedBuf_Cnt_M_lgc[9] CTCFailedBuf_Cnt_M_lgc[10]	1	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	1	
CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12]	1	1	
CTCFailedBuf_Cnt_M_lgc[13]	1	1	
CTCFailedBuf_Cnt_M_lgc[14]	1	1	
CTCFailedBuf_Cnt_M_lgc[15]	1	1	
CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	
CTCFailedBuf_Cnt_M_lgc[18]	1	1	
CTCFailedBuf_Cnt_M_lgc[19]	1	1	
CTCFailedBuf_Cnt_M_lgc[20]	0	0	•
CTCFailedBuf_Cnt_M_lgc[21]	0	0	•
CTCFailedBuf_Cnt_M_lgc[22]	0	0	
CTCFailedBuf_Cnt_M_lgc[23]	1	1	•
CTCFailedBuf_Cnt_M_lgc[24]	1	1	•
CTCFailedBuf_Cnt_M_lgc[25]	1	1	•
CTCFailedBuf_Cnt_M_lgc[26]	1	1	•
CTCFailedBuf_Cnt_M_lgc[27]	1	1	•
CTCFailedBuf_Cnt_M_lgc[28]	1	1	•
CTCFailedBuf_Cnt_M_lgc[29]	1	1	•
CTCFailedBuf_Cnt_M_lgc[30]	1	1	•
CTCFailedBuf_Cnt_M_lgc[31]	1	1	•
CTCFailedBuf_Cnt_M_lgc[32]	1	1	•
CTCFailedBuf_Cnt_M_lgc[33]	1	1	•
CTCFailedBuf_Cnt_M_lgc[34]	1	1	•
CTCFailedBuf_Cnt_M_lgc[35]	0	0	•
CTCFailedBuf_Cnt_M_lgc[36]	0	0	•
CTCFailedBuf_Cnt_M_lgc[37]	0	0	•
CTCFailedBuf_Cnt_M_lgc[38]	0	0	•
CTCFailedBuf_Cnt_M_lgc[39]	0	0	•
CTCFailedBuf_Cnt_M_lgc[40]	0	0	•
CTCFailedBuf_Cnt_M_lgc[41]	0	0	•
CTCFailedBuf_Cnt_M_lgc[42]	0	0	•
CTCFailedBuf_Cnt_M_lgc[43]	0	0	•
CTCFailedBuf_Cnt_M_lgc[44]	0	0	•
CTCFailedBuf_Cnt_M_lgc[45]	0	0	
CTCFailedBuf_Cnt_M_lgc[46]	0	0	
CTCFailedBuf_Cnt_M_lgc[47]	0 0	0	
CTCFailedBuf_Cnt_M_lgc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	
CTCFailedBuf_Cnt_M_lgc[50] CTCFailedBuf_Cnt_M_lgc[51]	0	0	
CTCFailedBuf_Cnt_M_lgc[52]	0	0	
CTCFailedBuf_Cnt_M_lgc[53]	1	1	
CTCFailedBuf_Cnt_M_lgc[54]	1	1	
CTCFailedBuf Cnt M lgc[55]	1	1	
CTCFailedBuf_Cnt_M_lgc[56]	1	1	
CTCFailedBuf_Cnt_M_lgc[57]	1	1	
CTCFailedBuf_Cnt_M_lgc[58]	1	1	
CTCFailedBuf_Cnt_M_lgc[59]	1	1	
CTCFailedBuf_Cnt_M_lgc[60]	1	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	1	
CTCFailedBuf_Cnt_M_lgc[62]	1	1	
CTCFailedBuf_Cnt_M_lgc[63]	1	1	
CTCFailedBuf Cnt M Igc[64]	1	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	0	•
CTCFailedBuf_Cnt_M_lgc[70]	0	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	0	•
CTCFailedBuf_Cnt_M_lgc[72]	0	0	•
CTCFailedBuf_Cnt_M_lgc[73]	0	0	
CTCFailedBuf_Cnt_M_lgc[74]	0	0	•
CTCFailedBuf_Cnt_M_lgc[75]	0	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	0	
CTCFailed_Cnt_M_lgc	0	0	
Demlf_DTCStatusChanged()	0	0	•
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	





- 101 010 15 10 10	
Test Step 2.12 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11] CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_Igc[22] CTCFailedBuf_Cnt_M_Igc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33] CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43] CTCFailedBuf Cnt M lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54] CTCFailedBuf_Cnt_M_lgc[55]	1   1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[50]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

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		- TOLOTON
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[64]	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	
CTCFailedBuf_Cnt_M_lgc[70]	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	
	0	
CTCFailedBuf_Cnt_M_lgc[72] CTCFailedBuf_Cnt_M_lgc[73]	0	
	0	
CTCFailedBuf_Cnt_M_lgc[74]		
CTCFailedBuf_Cnt_M_lgc[75]	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	
CTCFailed_Cnt_M_lgc	0	
DTC	56	
DTCKind	1	
DTCStatusNew	255	
DTCStatusOld	164	
Dem_DTCNumberTable[0]	181	
Dem_DTCNumberTable[1]	1	
Dem_DTCNumberTable[2]	41	
Dem_DTCNumberTable[3]	22	
Dem_DTCNumberTable[4]	24	
Dem_DTCNumberTable[5]	254	
Dem_DTCNumberTable[6]	209	
Dem_DTCNumberTable[7]	209	
Dem_DTCNumberTable[8]	181	
Dem_DTCNumberTable[9]	1	
Dem_DTCNumberTable[10]	209	
Dem_DTCNumberTable[11]	128	
Dem_DTCNumberTable[12]	1	
Dem_DTCNumberTable[13]	209	
Dem_DTCNumberTable[14]	181	
Dem_DTCNumberTable[15]	1	
Dem_DTCNumberTable[16]	1	
Dem_DTCNumberTable[17]	209	
Dem_DTCNumberTable[18]	33	
Dem DTCNumberTable[19]	181	
	1	
Dem_DTCNumberTable[20]		
Dem_DTCNumberTable[21]	209	
Dem_DTCNumberTable[22]	181	
Dem_DTCNumberTable[23]	41	
Dem_DTCNumberTable[24]	22	
Dem_DTCNumberTable[25]	24	
Dem_DTCNumberTable[26]	254	
Dem_DTCNumberTable[27]	1	
Dem_DTCNumberTable[28]	181	
Dem_DTCNumberTable[29]	1	
Dem_DTCNumberTable[30]	181	
Dem_DTCNumberTable[31]	181	
Dem_DTCNumberTable[32]	1	
Dem_DTCNumberTable[33]	1	
Dem_DTCNumberTable[34]	181	
Dem_DTCNumberTable[35]	1	
Dem_DTCNumberTable[36]	181	
Dem_DTCNumberTable[37]	181	
Dem_DTCNumberTable[38]	181	
Dem_DTCNumberTable[39]	1	
Dem_DTCNumberTable[40]	1	
Dem_DTCNumberTable[41]	41	
Dem_DTCNumberTable[42]	22	
Dem_DTCNumberTable[43]	24	
Dem_DTCNumberTable[44]	254	
Dem_DTCNumberTable[45]	209	
=		
Dem_DTCNumberTable[46]	181	
Dem_DTCNumberTable[47]	1	
Dem_DTCNumberTable[48]	22	
Dem_DTCNumberTable[49]	181	
Dem_DTCNumberTable[50]	1	
Dem_DTCNumberTable[51]	181	
	l.a.a.	
Dem_DTCNumberTable[52]	181	
Dem_DTCNumberTable[52] Dem_DTCNumberTable[53]	181   1	

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[55] 209 Dem\_DTCNumberTable[56] 181 Dem\_DTCNumberTable[57] 1 Dem\_DTCNumberTable[58] 181 Dem\_DTCNumberTable[59] 209 Dem\_DTCNumberTable[60] 181 Dem\_DTCNumberTable[61] 1 Dem\_DTCNumberTable[62] 22 Dem\_DTCNumberTable[63] 41 Dem DTCNumberTable[64] 22 Dem\_DTCNumberTable[65] 24 Dem\_DTCNumberTable[66] 254 Dem\_DTCNumberTable[67] 181 Dem DTCNumberTable[68] 181 Dem\_DTCNumberTable[69] 1 Dem\_DTCNumberTable[70] 22 Dem\_DTCNumberTable[71] 209 Dem\_DTCNumberTable[72] 22 Dem\_DTCNumberTable[73] 41 Dem\_DTCNumberTable[74] 22 Dem\_DTCNumberTable[75] 24 Dem\_DTCNumberTable[76] 254 Dem\_DTC\_FTB\_Table[0] 112 Dem\_DTC\_FTB\_Table[1] 227 Dem\_DTC\_FTB\_Table[2] 76 Dem\_DTC\_FTB\_Table[3] 252 Dem\_DTC\_FTB\_Table[4] 240 Dem\_DTC\_FTB\_Table[5] 206 Dem\_DTC\_FTB\_Table[6] 62 Dem\_DTC\_FTB\_Table[7] 62 Dem\_DTC\_FTB\_Table[8] 112 Dem\_DTC\_FTB\_Table[9] 227 Dem DTC FTB Table[10] 62 Dem\_DTC\_FTB\_Table[11] 80 Dem\_DTC\_FTB\_Table[12] 227 Dem DTC FTB Table[13] 62 Dem\_DTC\_FTB\_Table[14] 112 Dem\_DTC\_FTB\_Table[15] 227 Dem\_DTC\_FTB\_Table[16] 227 Dem DTC\_FTB\_Table[17] 62 Dem\_DTC\_FTB\_Table[18] 57 Dem DTC FTB Table[19] 112 Dem\_DTC\_FTB\_Table[20] 227 Dem\_DTC\_FTB\_Table[21] 62 112 Dem\_DTC\_FTB\_Table[22] Dem\_DTC\_FTB\_Table[23] 76

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227 252

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227

Dem\_DTC\_FTB\_Table[24]
Dem\_DTC\_FTB\_Table[25]

Dem\_DTC\_FTB\_Table[26]

Dem\_DTC\_FTB\_Table[27]

Dem\_DTC\_FTB\_Table[28]

Dem\_DTC\_FTB\_Table[29]

Dem\_DTC\_FTB\_Table[30]

Dem\_DTC\_FTB\_Table[31]

Dem\_DTC\_FTB\_Table[32]

Dem\_DTC\_FTB\_Table[33]

Dem\_DTC\_FTB\_Table[34]

Dem\_DTC\_FTB\_Table[35]

Dem\_DTC\_FTB\_Table[36]

Dem\_DTC\_FTB\_Table[37]

Dem\_DTC\_FTB\_Table[38]

Dem\_DTC\_FTB\_Table[39]

Dem\_DTC\_FTB\_Table[40]

Dem\_DTC\_FTB\_Table[41]

Dem\_DTC\_FTB\_Table[42]

Dem DTC FTB Table[43]

Dem\_DTC\_FTB\_Table[44]

Dem DTC FTB Table[45]

Dem\_DTC\_FTB\_Table[46]

Dem\_DTC\_FTB\_Table[47]

Dem\_DTC\_FTB\_Table[48]
Dem\_DTC\_FTB\_Table[49]

Dem\_DTC\_FTB\_Table[50]

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	Input Value		
Dem_DTC_FTB_Table[51]	112		
Dem_DTC_FTB_Table[52]	112		
Dem_DTC_FTB_Table[53]	227		
Dem_DTC_FTB_Table[54]	252		
Dem_DTC_FTB_Table[55] Dem DTC FTB Table[56]	62 112		
Dem_DTC_FTB_Table[50]	227		
Dem_DTC_FTB_Table[57] Dem_DTC_FTB_Table[58]	112		
Dem_DTC_FTB_Table[59]	62		
Dem_DTC_FTB_Table[60]	112		
Dem_DTC_FTB_Table[61]	227		
Dem_DTC_FTB_Table[62]	252		
Dem_DTC_FTB_Table[63]	76		
Dem_DTC_FTB_Table[64]	252		
Dem_DTC_FTB_Table[65]	240		
Dem_DTC_FTB_Table[66]	206		
Dem_DTC_FTB_Table[67]	112		
Dem_DTC_FTB_Table[68]	112		
Dem_DTC_FTB_Table[69]	227		
Dem_DTC_FTB_Table[70]	252		
Dem_DTC_FTB_Table[71]	62		
Dem_DTC_FTB_Table[72]	252		
Dem_DTC_FTB_Table[73]	76		
Dem_DTC_FTB_Table[74]	252		
Dem_DTC_FTB_Table[75]	240		
Dem_DTC_FTB_Table[76]	206		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[2]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[3]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[4]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[5]	1	1	Ž
CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CTCFailedBuf_Cnt_M_lgc[8]	0	0	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[14]	1	1	~
CTCFailedBuf_Cnt_M_lgc[15]	1	1	~
CTCFailedBuf_Cnt_M_lgc[16]	1	1	~
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	~
CTCFailedBuf_Cnt_M_lgc[21]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[22]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[24]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_Igc[25] CTCFailedBuf_Cnt_M_Igc[26]	1	1	Ž
CTCFailedBuf_Cnt_M_lgc[27]	1	1	<b>✓</b>
CTCFailedBuf Cnt M Igc[28]	1	1	_
CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_Igc[45]	U	0	~

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	•
CTCFailedBuf_Cnt_M_lgc[49]	0	0	•
CTCFailedBuf_Cnt_M_lgc[50]	0	0	•
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	•
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	•
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	•
CTCFailedBuf_Cnt_M_lgc[60]	1	1	•
CTCFailedBuf_Cnt_M_lgc[61]	1	1	•
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	~
CTCFailedBuf_Cnt_M_lgc[67]	0	0	•
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	•
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_Igc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	•
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	•
Demlf_DTCStatusChanged()	0	0	•
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	~

Test Step 2.13 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_Igc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

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	(
Name	Input Value
CTCFailedBuf_Cnt_M_Igc[29]	1
CTCFailedBuf Cnt M Igc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	1
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_Igc[64]	1
CTCFailedBuf_Cnt_M_Igc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	1
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
	0
CTCFailedBuf_Cnt_M_lgc[75]	
CTCFailed Cpt M lea	0
CTCFailed_Cnt_M_lgc	0
DTC	180560374
DTCKind	1
DTCStatusNew	13
DTCStatusOld	209
Dem_DTCNumberTable[0]	182
Dem_DTCNumberTable[1]	221
Dem_DTCNumberTable[2]	159
Dem_DTCNumberTable[3]	164
Dem_DTCNumberTable[4]	34
Dem_DTCNumberTable[5]	166
Dem_DTCNumberTable[6]	237
Dem_DTCNumberTable[7]	237
Dem_DTCNumberTable[8]	182
Dem_DTCNumberTable[9]	221
Dem_DTCNumberTable[10]	237
Dem_DTCNumberTable[11]	123
Dem_DTCNumberTable[12]	221
Dem_DTCNumberTable[13]	237
Dem_DTCNumberTable[14]	182
Dem_DTCNumberTable[15]	221
Dem_DTCNumberTable[16]	221
	237
Dem_DTCNumberTable[17]	237 239
	237 239 182

Demlf\_DTCStatusChanged

Dem\_DTCNumberTable[29]

Dem\_DTCNumberTable[30]

Dem\_DTCNumberTable[31]

Dem\_DTCNumberTable[32]

Dem\_DTCNumberTable[33]

Dem\_DTCNumberTable[34]

Dem\_DTCNumberTable[35]

Dem\_DTCNumberTable[36]

Dem\_DTCNumberTable[37]

Dem\_DTCNumberTable[38]

Dem\_DTCNumberTable[39]

Dem\_DTCNumberTable[40]

Dem\_DTCNumberTable[41]

Dem\_DTCNumberTable[42]

Dem\_DTCNumberTable[43]

Dem\_DTCNumberTable[44]

Dem\_DTCNumberTable[45]

Dem DTCNumberTable[46]

Dem\_DTCNumberTable[47]

Dem DTCNumberTable[48]

Dem\_DTCNumberTable[49]

Dem DTCNumberTable[50]

Dem\_DTCNumberTable[51]

Dem DTCNumberTable[52]

Dem\_DTCNumberTable[53]

Dem\_DTCNumberTable[54]

Dem\_DTCNumberTable[55]

Dem\_DTCNumberTable[56]

Dem\_DTCNumberTable[57]

Dem\_DTCNumberTable[58]

Dem\_DTCNumberTable[59]
Dem\_DTCNumberTable[60]

Dem\_DTCNumberTable[61]

Dem\_DTCNumberTable[62]

Dem\_DTCNumberTable[63]

Dem\_DTCNumberTable[64]

Dem\_DTCNumberTable[65]

Dem DTCNumberTable[66]

Dem\_DTCNumberTable[67]

Dem DTCNumberTable[68]

Dem\_DTCNumberTable[69]

Dem DTCNumberTable[70]

Dem\_DTCNumberTable[71]

Dem\_DTCNumberTable[72]

Dem\_DTCNumberTable[73]

Dem\_DTCNumberTable[74]

Dem\_DTCNumberTable[75]

Dem\_DTCNumberTable[76]

Dem\_DTC\_FTB\_Table[0]

Dem\_DTC\_FTB\_Table[1]

Dem\_DTC\_FTB\_Table[2]

Dem\_DTC\_FTB\_Table[3]

Dem\_DTC\_FTB\_Table[4]

Dem\_DTC\_FTB\_Table[5]

Dem\_DTC\_FTB\_Table[6]

Dem\_DTC\_FTB\_Table[7]

Dem DTC FTB Table[8]

Dem\_DTC\_FTB\_Table[9]

Dem DTC FTB Table[10]

Dem\_DTC\_FTB\_Table[11]

Dem\_DTC\_FTB\_Table[12]

Dem\_DTC\_FTB\_Table[13]

Dem\_DTC\_FTB\_Table[14]

Dem\_DTC\_FTB\_Table[15]

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173

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122



Input Value Dem\_DTCNumberTable[20] 221 Dem\_DTCNumberTable[21] 237 Dem DTCNumberTable[22] 182 Dem\_DTCNumberTable[23] 159 Dem DTCNumberTable[24] 164 Dem\_DTCNumberTable[25] 34 Dem\_DTCNumberTable[26] 166 Dem\_DTCNumberTable[27] 221 Dem\_DTCNumberTable[28] 182

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Name	Input Value		
Dem_DTC_FTB_Table[16]	122		
Dem_DTC_FTB_Table[17]	172		
Dem_DTC_FTB_Table[18]	117		
Dem_DTC_FTB_Table[19]	252		
Dem_DTC_FTB_Table[20]	122		
Dem_DTC_FTB_Table[21]	172		
Dem_DTC_FTB_Table[22]	252		
Dem_DTC_FTB_Table[23]	173		
Dem_DTC_FTB_Table[24]	253		
Dem_DTC_FTB_Table[25]	78		
Dem_DTC_FTB_Table[26]	251		
Dem_DTC_FTB_Table[27]	122		
Dem DTC FTB Table[28]	252		
Dem_DTC_FTB_Table[29]	122		
Dem_DTC_FTB_Table[30]	252		
Dem_DTC_FTB_Table[31]	252		
Dem_DTC_FTB_Table[32]	122		
Dem_DTC_FTB_Table[33]	122		
Dem_DTC_FTB_Table[34]	252		
Dem_DTC_FTB_Table[35]	122		
Dem_DTC_FTB_Table[36]	252		
Dem_DTC_FTB_Table[37]	252		
Dem_DTC_FTB_Table[38]	252		
Dem_DTC_FTB_Table[39]	122		
Dem_DTC_FTB_Table[40]	122		
Dem_DTC_FTB_Table[41]	173		
Dem_DTC_FTB_Table[42]	253		
Dem_DTC_FTB_Table[43]	78		
Dem_DTC_FTB_Table[44]	251		
Dem_DTC_FTB_Table[45]	172		
Dem_DTC_FTB_Table[46]	252		
Dem_DTC_FTB_Table[47]	122		
Dem_DTC_FTB_Table[48]	253		
Dem_DTC_FTB_Table[49]	252		
Dem_DTC_FTB_Table[50]	122		
Dem_DTC_FTB_Table[51]	252		
Dem_DTC_FTB_Table[52]	252		
Dem_DTC_FTB_Table[53]	122		
Dem_DTC_FTB_Table[54]	253		
Dem_DTC_FTB_Table[55]	172		
Dem_DTC_FTB_Table[56]	122 122		
Dem_DTC_FTB_Table[57] Dem_DTC_FTB_Table[58]	252		
Dem_DTC_FTB_Table[59]	172		
Dem_DTC_FTB_Table[60]	252		
Dem_DTC_FTB_Table[61]	122		
Dem_DTC_FTB_Table[62]	253		
Dem_DTC_FTB_Table[63]	173		
Dem DTC FTB Table[64]	253		
Dem_DTC_FTB_Table[65]	78		
Dem_DTC_FTB_Table[66]	251		
Dem_DTC_FTB_Table[67]	252		
Dem_DTC_FTB_Table[68]	252		
Dem_DTC_FTB_Table[69]	122		
Dem_DTC_FTB_Table[70]	253		
Dem_DTC_FTB_Table[71]	172		
Dem_DTC_FTB_Table[72]	253		
Dem_DTC_FTB_Table[73]	173		
Dem_DTC_FTB_Table[74]	253		
Dem_DTC_FTB_Table[75]	78		
Dem_DTC_FTB_Table[76]	251		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	0	0	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	0	0	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	~
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~

2018-04-10, 18:44:44+0530



COTAMEND, COL M, 19878  COTAME	Name	Actual Value	Expected Value	Result
CICRIANDLO COM Ng 153				
CCCRandonia Cret Mugetia CCCRandonia Cret Muge		1	1	~
CICRIAISMA CAM, Mg/18 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
COTOR-BORDED, COM, My BORTH 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				-
CICS-laterial_Col_M_got19				
CCTORAIGNUL CHM, Mg019 1 1 1 1 1 CCTORAIGNUL CHM, Mg019 1 1 1 1 1 CCTORAIGNUL CHM, Mg019 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CCF-Bai-Bail (고에 보 ) 무리의  CCF-Bail-Bail (고에 보		0	0	~
CICF alles GV CM M 19623  O	CTCFailedBuf_Cnt_M_lgc[19]			
CTCFaledud Cot M 1962점 1 1 1 1				
CTCFalesBuff_CM_M_M_Depth				
COFFailed Coff M 1 1 1 1				
CICPained Cont. M. 19628				
CICFaledbull_Crit_M_popts	CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CICFairabell Crit M, 19628				
CICFailed   Citty   Migray				
CTCFaledfull_CM_M_jog130  1				
CITCPainedBuf, Crit, M, Jug423				
CICFoliaelduf, Cit, M, Jeg(33)   1				~
CICFailedBuf_Cnt_M_gq838			1	
CTCFalesBut_CM_M_gq(55)				
CICFaleadbuf, Crit, M. Igc358)  CTCFaleadbuf, Crit, M. Igc358)  CTCFaleadbuf, Crit, M. Igc458)  CTCFaleadbuf, Crit, M. Igc458)  CTCFaleadbuf, Crit, M. Igc458)  CTCFaleadbuf, Crit, M. Igc458)  CTCFaleadbuf, Crit, M. Igc451  CTCFaleadbuf, Crit, M. Igc451  CTCFaleadbuf, Crit, M. Igc451  CTCFaleadbuf, Crit, M. Igc453  CTCFaleadbuf, Crit, M. Igc453  CTCFaleadbuf, Crit, M. Igc454  CTCFaleadbuf, Crit, M. Igc458  CTCFaleadbuf, Crit, M. Igc559  TTCFaleadbuf, Crit, M. Igc569  TTCFaleadbuf, Crit, M. Igc577  TTCFaleadbuf, Crit, M. Ig				
CTCFaledBut_CTM_M_sq253				
CTCFaledbuf_Cn_M_logids)  O O O O O O O O O O O O O O O O O O O				
CTCFaiedBut_Cnt_M lgc[41] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFailedBut_Cnt_M_igcl41] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		0	0	<b>✓</b>
CTCFaledBuf_Cnt_M_lgc(42)  O O O O CTCFaledBuf_Cnt_M_lgc(43)  O O O O O CTCFaledBuf_Cnt_M_lgc(44)  O O O O O O CTCFaledBuf_Cnt_M_lgc(45)  O O O O O O O O O O O O O O O O O O O	CTCFailedBuf_Cnt_M_lgc[40]			
CTCFaledBuf_Cnt_M_lgc(43)  CTCFaledBuf_Cnt_M_lgc(45)  O  O  CTCFaledBuf_Cnt_M_lgc(45)  O  O  CTCFaledBuf_Cnt_M_lgc(45)  O  O  CTCFaledBuf_Cnt_M_lgc(46)  O  CTCFaledBuf_Cnt_M_lgc(47)  O  CTCFaledBuf_Cnt_M_lgc(48)  O  CTCFaledBuf_Cnt_M_lgc(48)  O  CTCFaledBuf_Cnt_M_lgc(48)  O  CTCFaledBuf_Cnt_M_lgc(48)  O  CTCFaledBuf_Cnt_M_lgc(50)  O  CTCFaledBuf_Cnt_M_lgc(50)  O  CTCFaledBuf_Cnt_M_lgc(51)  O  CTCFaledBuf_Cnt_M_lgc(51)  O  CTCFaledBuf_Cnt_M_lgc(53)  I  I  I  CTCFaledBuf_Cnt_M_lgc(53)  CTCFaledBuf_Cnt_M_lgc(55)  I  CTCFaledBuf_Cnt_M_lgc(55)  I  CTCFaledBuf_Cnt_M_lgc(55)  I  CTCFaledBuf_Cnt_M_lgc(56)  CTCFaledBuf_Cnt_M_lgc(56)  CTCFaledBuf_Cnt_M_lgc(56)  I  CTCFaledBuf_Cnt_M_lgc(56)  CTCFaledBuf_Cnt_M_lgc(66)  CTCFaledBuf_Cnt_M_lgc(66)  CTCFaledBuf_Cnt_M_lgc(66)  CTCFaledBuf_Cnt_M_lgc(66)  CTCFaledBuf_Cnt_M_lgc(66)  CTCFaledBuf_Cnt_M_lgc(67)  CTCFAl				
CTCFaledBuf_Cnt_M_lgcl43   O O O O CTCFaledBuf_Cnt_M_lgcl45   O O O O O CTCFaledBuf_Cnt_M_lgcl46   O O O O O O CTCFaledBuf_Cnt_M_lgcl47   O O O O O O O O O O O O O O O O O O O				
CTCFaledBuf_Cnt_M_lgcl45] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFailedBuf_Cnt_M_lgcf49				~
CTCFailedBuf_Cnt_M_lgd49] 0 0 0 0		0	0	
CTCFailedBut_Cnt_M_lgc[49]				
CTCFailedBuf_Cnt_M_lgc[51]         0         0           CTCFailedBuf_Cnt_M_lgc[52]         0         0           CTCFailedBuf_Cnt_M_lgc[52]         0         0           CTCFailedBuf_Cnt_M_lgc[53]         1         1           CTCFailedBuf_Cnt_M_lgc[55]         1         1           CTCFailedBuf_Cnt_M_lgc[55]         1         1           CTCFailedBuf_Cnt_M_lgc[56]         1         1           CTCFailedBuf_Cnt_M_lgc[58]         0         0           CTCFailedBuf_Cnt_M_lgc[58]         0         0           CTCFailedBuf_Cnt_M_lgc[59]         1         1           CTCFailedBuf_Cnt_M_lgc[69]         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1           CTCFailedBuf_Cnt_M_lgc[62]         1         1           CTCFailedBuf_Cnt_M_lgc[62]         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1           CTCFailedBuf_Cnt_M_lgc[64]         1         1           CTCFailedBuf_Cnt_M_lgc[65]         0         0           CTCFailedBuf_Cnt_M_lgc[65]         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0           CTCFailedBuf_Cnt_M_lgc[68]         0         0           CTC				
CTCFailedBuf_Cnt_M_lgc[51]         0         0         V           CTCFailedBuf_Cnt_M_lgc[53]         1         1         V           CTCFailedBuf_Cnt_M_lgc[54]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[54]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[56]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[57]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0         V           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[64]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[64]         0         0         0         V           CTCFailedBuf_Cnt_M_lgc[67]         0         0         0         V <td></td> <td></td> <td></td> <td></td>				
CTCFailedBuf_Cnt_M_lgc[52]         0         0           CTCFailedBuf_Cnt_M_lgc[54]         1         1           CTCFailedBuf_Cnt_M_lgc[54]         1         1           CTCFailedBuf_Cnt_M_lgc[55]         1         1           CTCFailedBuf_Cnt_M_lgc[57]         1         1           CTCFailedBuf_Cnt_M_lgc[58]         0         0           CTCFailedBuf_Cnt_M_lgc[58]         0         0           CTCFailedBuf_Cnt_M_lgc[58]         1         1           CTCFailedBuf_Cnt_M_lgc[69]         1         1           CTCFailedBuf_Cnt_M_lgc[60]         1         1           CTCFailedBuf_Cnt_M_lgc[61]         1         1           CTCFailedBuf_Cnt_M_lgc[62]         1         1           CTCFailedBuf_Cnt_M_lgc[63]         1         1           CTCFailedBuf_Cnt_M_lgc[64]         1         1           CTCFailedBuf_Cnt_M_lgc[65]         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0           CTCFailedBuf_Cnt_M_lgc[68]         0         0           CTCFailedBuf_Cnt_M_lgc[68]         0         0           CTCFailedBuf_Cnt_M_lgc[70]         1         1           CTCFailedBuf_Cnt_M_lgc[70]         0         0           CTC				
CTCFailedBut_Cnt_M_lgc[54]         1         1         1           CTCFailedBut_Cnt_M_lgc[56]         1         1         1           CTCFailedBut_Cnt_M_lgc[57]         1         1         1           CTCFailedBut_Cnt_M_lgc[57]         1         1         1           CTCFailedBut_Cnt_M_lgc[58]         0         0         0           CTCFailedBut_Cnt_M_lgc[60]         1         1         1           CTCFailedBut_Cnt_M_lgc[61]         1         1         1           CTCFailedBut_Cnt_M_lgc[62]         1         1         1           CTCFailedBut_Cnt_M_lgc[63]         1         1         1           CTCFailedBut_Cnt_M_lgc[64]         1         1         1           CTCFailedBut_Cnt_M_lgc[65]         0         0         0           CTCFailedBut_Cnt_M_lgc[66]         0         0         0           CTCFailedBut_Cnt_M_lgc[67]         0         0         0           CTCFailedBut_Cnt_M_lgc[68]         0         0         0           CTCFailedBut_Cnt_M_lgc[68]         0         0         0           CTCFailedBut_Cnt_M_lgc[68]         0         0         0           CTCFailedBut_Cnt_M_lgc[68]         0         0         0			0	~
CTCFailedBuf_Cnt_M_lgc[55]         1         1         4           CTCFailedBuf_Cnt_M_lgc[56]         1         1         4           CTCFailedBuf_Cnt_M_lgc[57]         1         1         4           CTCFailedBuf_Cnt_M_lgc[58]         0         0         0         V           CTCFailedBuf_Cnt_M_lgc[69]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[60]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[61]         1         1         1         V           CTCFailedBuf_Cnt_M_lgc[62]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[63]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[64]         1         1         1         V         CTCFailedBuf_Cnt_M_lgc[65]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[65]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[66]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[66]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[68]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[68]         0         0         0         V         CTCFailedBuf_Cnt_M_lgc[69]<				
CTCFailedBuf_Cnt_M_lgc[56]       1       1       1				
CTCFailedBuf_Cnt_M_lgc[57]         1         1				
CTCFailedBuf_Cnt_M_lgc[58]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[69]       1       1        ✓         CTCFailedBuf_Cnt_M_lgc[60]       1       1       1        ✓         CTCFailedBuf_Cnt_M_lgc[61]       1       1       1        ✓         CTCFailedBuf_Cnt_M_lgc[62]       1       1       1        ✓         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1        ✓         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0        ✓         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0        ✓         CTCFailedBuf_Cnt_M_lgc[68]       0       0        ✓       ✓        ✓         ✓        ✓         ✓          ✓          ✓        <				
CTCFailedBuf_Cnt_M_lgc[60]       1       1       1         CTCFailedBuf_Cnt_M_lgc[61]       1       1       1         CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[69]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0 <td< td=""><td></td><td></td><td></td><td></td></td<>				
CTCFailedBuf_Cnt_M_lgc[61]       1       1       4         CTCFailedBuf_Cnt_M_lgc[62]       1       1       4         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFai			1	~
CTCFailedBuf_Cnt_M_lgc[62]       1       1       1         CTCFailedBuf_Cnt_M_lgc[63]       1       1       1         CTCFailedBuf_Cnt_M_lgc[64]       1       1       1         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[69]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0 <td< td=""><td></td><td></td><td></td><td></td></td<>				
CTCFailedBuf_Cnt_M_lgc[63]       1       1       4         CTCFailedBuf_Cnt_M_lgc[64]       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0         CTCFailedBuf_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc <td></td> <td></td> <td></td> <td></td>				
CTCFailedBuf_Cnt_M_lgc[64]       1       1       4         CTCFailedBuf_Cnt_M_lgc[65]       0       0       0         CTCFailedBuf_Cnt_M_lgc[66]       0       0       0         CTCFailedBuf_Cnt_M_lgc[67]       0       0       0         CTCFailedBuf_Cnt_M_lgc[68]       0       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         CTCFailed_Cnt_M_lgc       0       0       0         Demlf_DTCStatusChanged()       0       0       0				
CTCFailedBuf_Cnt_M_lgc[65]       0       0       •         CTCFailedBuf_Cnt_M_lgc[67]       0       0       •         CTCFailedBuf_Cnt_M_lgc[68]       0       0       •         CTCFailedBuf_Cnt_M_lgc[69]       0       0       •         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0       •         CTCFailedBuf_Cnt_M_lgc[72]       0       0       •         CTCFailedBuf_Cnt_M_lgc[73]       0       0       •         CTCFailedBuf_Cnt_M_lgc[74]       0       0       •         CTCFailedBuf_Cnt_M_lgc[75]       0       0       •         CTCFailedBuf_Cnt_M_lgc[76]       0       0       •         CTCFailed_Cnt_M_lgc       0       0       •         CTCFailed_Cnt_M_lgc       0       0       •         Demlf_DTCStatusChanged()       0       0       •				
CTCFailedBuf_Cnt_M_lgc[67]       0       0       •         CTCFailedBuf_Cnt_M_lgc[68]       0       0       •         CTCFailedBuf_Cnt_M_lgc[69]       0       0       •         CTCFailedBuf_Cnt_M_lgc[70]       1       1       1       •         CTCFailedBuf_Cnt_M_lgc[71]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[72]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[73]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[74]       0       0       •       •         CTCFailedBuf_Cnt_M_lgc[75]       0       0       •       •         CTCFailed_Cnt_M_lgc[76]       0       0       •       •         CTCFailed_Cnt_M_lgc       0       0       •       •         Demlf_DTCStatusChanged()       0       0       •       •			0	<b>v</b>
CTCFailedBuf_Cnt_M_lgc[68]       0       0       •         CTCFailedBuf_Cnt_M_lgc[79]       0       0       •         CTCFailedBuf_Cnt_M_lgc[71]       0       0       •         CTCFailedBuf_Cnt_M_lgc[72]       0       0       •         CTCFailedBuf_Cnt_M_lgc[73]       0       0       •         CTCFailedBuf_Cnt_M_lgc[74]       0       0       •         CTCFailedBuf_Cnt_M_lgc[75]       0       0       •         CTCFailedBuf_Cnt_M_lgc[76]       0       0       •         CTCFailed_Cnt_M_lgc       0       0       •         Demlf_DTCStatusChanged()       0       0       •				
CTCFailedBuf_Cnt_M_lgc[69]       0       0         CTCFailedBuf_Cnt_M_lgc[70]       1       1         CTCFailedBuf_Cnt_M_lgc[71]       0       0         CTCFailedBuf_Cnt_M_lgc[72]       0       0         CTCFailedBuf_Cnt_M_lgc[73]       0       0         CTCFailedBuf_Cnt_M_lgc[74]       0       0         CTCFailedBuf_Cnt_M_lgc[75]       0       0         CTCFailedBuf_Cnt_M_lgc[76]       0       0         CTCFailed_Cnt_M_lgc       0       0         Demlf_DTCStatusChanged()       0       0				
CTCFailedBuf_Cnt_M_lgc[70]       1       1       9         CTCFailedBuf_Cnt_M_lgc[71]       0       0       •         CTCFailedBuf_Cnt_M_lgc[72]       0       0       •         CTCFailedBuf_Cnt_M_lgc[73]       0       0       •         CTCFailedBuf_Cnt_M_lgc[74]       0       0       •         CTCFailedBuf_Cnt_M_lgc[75]       0       0       •         CTCFailedBuf_Cnt_M_lgc[76]       0       0       •         CTCFailed_Cnt_M_lgc       0       0       •         Demlf_DTCStatusChanged()       0       0       •				
CTCFailedBuf_Cnt_M_lgc[71]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[72]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[73]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[74]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[75]       0       0       ✓         CTCFailedBuf_Cnt_M_lgc[76]       0       0       ✓         CTCFailed_Cnt_M_lgc       0       0       ✓         Demlf_DTCStatusChanged()       0       0       ✓				
CTCFailedBuf_Cnt_M_lgc[75]         0         0         ✓           CTCFailedBuf_Cnt_M_lgc[76]         0         0         ✓           CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
CTCFailedBuf_Cnt_M_lgc[76]         0         0         ✓           CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
CTCFailed_Cnt_M_lgc         0         0         ✓           Demlf_DTCStatusChanged()         0         0         ✓				
Demlf_DTCStatusChanged() 0 0				
	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	<b>✓</b>



Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 2.14 (Repeat Count = 1)	<b>√</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf Cnt M lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0
CTCFailedBuf_Cnt_M_lgc[6]	0
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf_Cnt_M_lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	0
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	0
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_lgc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61]	0
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_Igc[63]	0

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Demii_DTC3tatusChanged	- Turk turk turk turk turk turk turk turk t
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	1
DTC	2534667367
DTCKind	2
DTCStatusNew	240
DTCStatusOld	62
Dem_DTCNumberTable[0]	99
Dem_DTCNumberTable[1]	143
Dem_DTCNumberTable[2]	36
Dem_DTCNumberTable[3]	85
Dem_DTCNumberTable[4]	238
Dem_DTCNumberTable[5]	62
Dem_DTCNumberTable[6]	217
Dem_DTCNumberTable[7]	217
Dem_DTCNumberTable[8]	99
Dem_DTCNumberTable[9]	143
Dem_DTCNumberTable[10]	217
Dem_DTCNumberTable[11]	101
Dem_DTCNumberTable[12]	143
Dem_DTCNumberTable[13]	217
Dem_DTCNumberTable[14]	99
Dem_DTCNumberTable[15]	143
Dem_DTCNumberTable[16]	143
Dem_DTCNumberTable[17]	217
Dem_DTCNumberTable[18]	236
Dem DTCNumberTable[19]	99
Dem_DTCNumberTable[20]	143
	217
Dem_DTCNumberTable[21]	
Dem_DTCNumberTable[22]	99
Dem_DTCNumberTable[23]	36
Dem_DTCNumberTable[24]	85
Dem_DTCNumberTable[25]	238
Dem_DTCNumberTable[26]	62
Dem_DTCNumberTable[27]	143
Dem_DTCNumberTable[28]	99
Dem_DTCNumberTable[29]	143
Dem_DTCNumberTable[30]	99
Dem_DTCNumberTable[31]	99
Dem_DTCNumberTable[32]	143
Dem_DTCNumberTable[33]	143
Dem_DTCNumberTable[34]	99
Dem_DTCNumberTable[35]	143
Dem_DTCNumberTable[36]	99
Dem_DTCNumberTable[37]	99
Dem_DTCNumberTable[38]	99
Dem_DTCNumberTable[39]	143
Dem_DTCNumberTable[40]	143
Dem_DTCNumberTable[41]	36
Dem_DTCNumberTable[42]	85
Dem_DTCNumberTable[43]	238
Dem_DTCNumberTable[44]	62
Dem_DTCNumberTable[44] Dem_DTCNumberTable[45]	217
Dem_DTCNumberTable[46]	99
Dem_DTCNumberTable[47]	143
	05
Dem_DTCNumberTable[48]	85
Dem_DTCNumberTable[49]	99
Dem_DTCNumberTable[49] Dem_DTCNumberTable[50]	99 143
Dem_DTCNumberTable[49] Dem_DTCNumberTable[50] Dem_DTCNumberTable[51]	99 143 99
Dem_DTCNumberTable[49] Dem_DTCNumberTable[50]	99 143 99 99
Dem_DTCNumberTable[49] Dem_DTCNumberTable[50] Dem_DTCNumberTable[51]	99 143 99

Demlf\_DTCStatusChanged

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Name	Input Value
Dem_DTCNumberTable[55]	217
Dem DTCNumberTable[56]	99
Dem_DTCNumberTable[57]	143
	99
Dem_DTCNumberTable[58]	
Dem_DTCNumberTable[59]	217
Dem_DTCNumberTable[60]	99
Dem_DTCNumberTable[61]	143
Dem_DTCNumberTable[62]	85
Dem_DTCNumberTable[63]	36
Dem_DTCNumberTable[64]	85
Dem_DTCNumberTable[65]	238
Dem_DTCNumberTable[66]	62
Dem_DTCNumberTable[67]	99
Dem_DTCNumberTable[68]	99
Dem_DTCNumberTable[69]	143
Dem_DTCNumberTable[70]	85
Dem_DTCNumberTable[71]	217
Dem_DTCNumberTable[72]	85
Dem_DTCNumberTable[73]	36
Dem DTCNumberTable[74]	85
Dem_DTCNumberTable[74] Dem_DTCNumberTable[75]	238
Dem_DTC.ETP_Table[76]	62 67
Dem_DTC_FTB_Table[0]	
Dem_DTC_FTB_Table[1]	177
Dem_DTC_FTB_Table[2]	247
Dem_DTC_FTB_Table[3]	156
Dem_DTC_FTB_Table[4]	178
Dem_DTC_FTB_Table[5]	171
Dem_DTC_FTB_Table[6]	176
Dem_DTC_FTB_Table[7]	176
Dem_DTC_FTB_Table[8]	67
Dem_DTC_FTB_Table[9]	177
Dem_DTC_FTB_Table[10]	176
Dem_DTC_FTB_Table[11]	116
Dem_DTC_FTB_Table[12]	177
Dem_DTC_FTB_Table[13]	176
Dem_DTC_FTB_Table[14]	67
Dem_DTC_FTB_Table[15]	177
Dem_DTC_FTB_Table[16]	177
Dem_DTC_FTB_Table[17]	176
Dem_DTC_FTB_Table[18]	171
	67
Dem_DTC_FTB_Table[19]	
Dem_DTC_FTB_Table[20]	177
Dem_DTC_FTB_Table[21]	176
Dem_DTC_FTB_Table[22]	67
Dem_DTC_FTB_Table[23]	247
Dem_DTC_FTB_Table[24]	156
Dem_DTC_FTB_Table[25]	178
Dem_DTC_FTB_Table[26]	171
Dem_DTC_FTB_Table[27]	177
Dem_DTC_FTB_Table[28]	67
Dem_DTC_FTB_Table[29]	177
Dem_DTC_FTB_Table[30]	67
Dem_DTC_FTB_Table[31]	67
Dem_DTC_FTB_Table[32]	177
Dem_DTC_FTB_Table[33]	177
Dem_DTC_FTB_Table[34]	67
Dem_DTC_FTB_Table[35]	177
Dem_DTC_FTB_Table[36]	67
Dem_DTC_FTB_Table[37]	67
Dem_DTC_FTB_Table[38]	67
	177
Dem_DTC_FTB_Table[39]	
Dem_DTC_FTB_Table[40]	177
Dem_DTC_FTB_Table[41]	247
Dem_DTC_FTB_Table[42]	156
Dem_DTC_FTB_Table[43]	178
Dem_DTC_FTB_Table[44]	171
Dem_DTC_FTB_Table[45]	176
Dem_DTC_FTB_Table[46]	67
Dem_DTC_FTB_Table[47]	177
Dem_DTC_FTB_Table[48]	156
Dem_DTC_FTB_Table[49]	67
Dem_DTC_FTB_Table[50]	177

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Name				
Den DIC FIR TeleSide   97	Name	Input Value		
Den Dig   File   Table   Sign   Sign   Den Dig   File   Table   Sign   S	Dem_DTC_FTB_Table[51]			
Descript Page   1986				
Dest   DTC_FTR_Table[5]   FF   Dest   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FT   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FF   DTC_FTR_Table[6]   FT   DTC_FTR_Table[6]   FT   DTC_FTR_Table[6]   FT   DTC_FTR_Table[6]   FT   DTC_FTR_Table[6]   FT   DTC_FTR_Table[6]   F				
Dest   DEC   FIRST   Jackson   DEC				
Dest   DTC   FIRS   Table   ST				
Dem   DTC_FTB_ Table[90]   F7				
Den DTC_FTR_Table(9) Den DTC_				
Den DTC_FTB_Table(5) Den DTC_FTB_Table(5) Den DTC_FTB_Table(6) Den DTC_FTB_Table(7) Den DTC_		176		
Dest. DTC_FTB_Table[5]   247	Dem_DTC_FTB_Table[60]	67		
Den DTC_FRE_Table(4) Den DTC_FRE_Table(4) Den DTC_FRE_Table(5) Den DTC_FRE_Table(5) Den DTC_FRE_Table(6) Den DTC_FRE_Table(6) Den DTC_FRE_Table(6) Den DTC_FRE_Table(6) Den DTC_FRE_Table(6) Den DTC_FRE_Table(6) Den DTC_FRE_Table(7) Den DTC_				
Dem_DTC_FFS_Table(9)   176				
Dem, DTC_FFB_Table(9)   778   Dem DTC_FFB_Table(9)   771   Dem DTC_FFB_Table(9)   771   Dem DTC_FFB_Table(9)   775   Dem DTC_FFB_				
Dem. DTC.FTB_Table(98)				
Den. DTC.FTB.Table(9)   67				
Dem. DIG. FTR. Tabel600				
Dem. DTC_FTE_Table[7]   79   Dem. DTC_FTE_T				
Den.   Dic.   File.   Table   File.   Den.   Dic.		177		
Dem, DTC, FTE, Table(F2)   247	Dem_DTC_FTB_Table[70]	156		
Dem, DTC, FTB, Table(F3)   158   1	Dem_DTC_FTB_Table[71]	176		
Dem. DTC. FTB_Table[74]   156 Dem. DTC. FTB_Table[75]   175 Dem.				
Dem_DTC_FTB_Table(PS)   176				
Dem_DTC_FTB_Table(Pe)				
Name				
CTCFaledBut_Cnt_M_gqt1			Evacated Value	Popult
CTCFaledBut_Crit_M_gat2			The state of the s	Result
CTCFaledBuf_Crit_M_lgct3  CTCFaledBuf_Crit_M_lgct3  CTCFaledBuf_Crit_M_lgct4  CTCFaledBuf_Crit_M_lgct6  CTCFaledBuf_Crit_M_lgct6  CTCFaledBuf_Crit_M_lgct6  CTCFaledBuf_Crit_M_lgct7  CTCFaledBuf_Crit_M_lgct9  CTCFaledBuf_Crit_M_lgct19  CTCFaledBuf_Crit_M_lgct29  CTCFaledBuf_Crit_M_lgct39  CTCFaledBuf_Crit_M_lgct49  CTCFaledBuf_Crit_M_lgct49  CTCFaledBuf_Crit_M_lgct49  CTCFaledBuf_Crit_M_lgct49  CTCFaledBuf				~
CTCFaledBuf_Cnt_M_logis				_
CTCFaledBuf_Cnt_M_lgc[5]  CTCFaledBuf_Cnt_M_lgc[7]  CTCFaledBuf_Cnt_M_lgc[7]  CTCFaledBuf_Cnt_M_lgc[7]  CTCFaledBuf_Cnt_M_lgc[8]  O  CTCFaledBuf_Cnt_M_lgc[9]  CTCFaledBuf_Cnt_M_lgc[9]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  CTCFaledBuf_Cnt_M_lgc[1]  O  CTCFaledBuf_Cnt_M_lgc[2]		0	0	<b>✓</b>
CTCFaledBuf_Cnt_M_gqtPl OCTCFaledBuf_Cnt_M_gqtPl OCTCFaledBuf_Cnt_M_gqtPl OCTCFaledBuf_Cnt_M_gqtPl OCTCFaledBuf_Cnt_M_gqtPl OCTCFaledBuf_Cnt_M_gqtPl OCTCFaledBuf_Cnt_M_gqt10 OCTCFaledBuf_Cnt_M_gqt11 OCTCFaledBuf_Cnt_M_gqt13 OCTCFaledBuf_Cnt_M_gqt13 OCTCFaledBuf_Cnt_M_gqt13 OCTCFaledBuf_Cnt_M_gqt13 OCTCFaledBuf_Cnt_M_gqt14 OCTCFaledBuf_Cnt_M_gqt15 OCTCFaledBuf_Cnt_M_gqt16 OCTCFaledBuf_Cnt_M_gqt16 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt18 OCTCFaledBuf_Cnt_M_gqt19 OCTCFaledBuf_Cnt_M_gqt20 OCTCFaledBuf_Cnt_M_gqt21 OCTCFaledBuf_Cnt_M_gqt21 OCTCFaledBuf_Cnt_M_gqt21 OCTCFaledBuf_Cnt_M_gqt23 OCTCFaledBuf_Cnt_M_gqt24 OCTCFaledBuf_Cnt_M_gqt28 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt39 OCTCFaledBuf_Cnt_M_gqt49 OCTCFaledBuf_Cnt_M_gqt		0	0	~
CTCFaledBuf_Cnt_M_lgq(7)	CTCFailedBuf_Cnt_M_lgc[5]	0	0	✓
CTCFaledBuf_Cnt_M_lgq8  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq8  0 0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq10  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq11  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq11  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq12  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq13  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq13  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq14  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq16  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq16  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq16  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq17  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq19  0 0 0 0 0 CTCFaledBuf_Cnt_M_lgq20  0 0 0 CTCFaledBuf_Cnt_M_lgq30  0 0 CTCFaledBuf_Cnt_M_lgq30  0 0 CTCFaledBuf_Cnt_M_lgq30  0 CTCFaledBuf_Cnt_M_lgq40  0 CTCFaledBuf_	CTCFailedBuf_Cnt_M_lgc[6]			~
CTCFailedBut_Cnt_M_lgc[9]				<b>~</b>
CTCFaledBut_Cnt_M_lgct10  CTCFaledBut_Cnt_M_lgct12  O  O  CTCFaledBut_Cnt_M_lgct12  O  O  CTCFaledBut_Cnt_M_lgct13  O  CTCFaledBut_Cnt_M_lgct13  O  CTCFaledBut_Cnt_M_lgct14  O  CTCFaledBut_Cnt_M_lgct15  O  O  CTCFaledBut_Cnt_M_lgct15  O  O  CTCFaledBut_Cnt_M_lgct16  CTCFaledBut_Cnt_M_lgct17  O  O  CTCFaledBut_Cnt_M_lgct17  O  O  CTCFaledBut_Cnt_M_lgct18  O  CTCFaledBut_Cnt_M_lgct18  O  CTCFaledBut_Cnt_M_lgct19  O  CTCFaledBut_Cnt_M_lgct20  O  CTCFaledBut_Cnt_M_lgct20  O  CTCFaledBut_Cnt_M_lgct21  O  CTCFaledBut_Cnt_M_lgct21  O  CTCFaledBut_Cnt_M_lgct21  O  CTCFaledBut_Cnt_M_lgct23  O  CTCFaledBut_Cnt_M_lgct23  O  CTCFaledBut_Cnt_M_lgct28  O  CTCFaledBut_Cnt_M_lgct39  O  CTCFaledBut_Cnt_M_lgct39  O  CTCFaledBut_Cnt_M_lgct39  O  CTCFaledBut_Cnt_M_lgct39  O  CTCFaledBut_Cnt_M_lgct39  O  CTCFaledBut_Cnt_M_lgct39  O  CTCFaledBut_Cnt_M_lgct38  O  CTCFaledBut_Cnt_M_lgct38  O  CTCFaledBut_Cnt_M_lgct38  O  CTCFaledBut_Cnt_M_lgct38  O  CTCFaledBut_Cnt_M_lgct38  O  CTCFaledBut_Cnt_M_lgct39  CTCFaledBut_Cnt_M_lgct49  O  CTCFaledBut_Cnt_M_lgct49  O  CTCFaledBut_Cnt_M_lgct41  O  CTCFale				~
CTCFailedBuf_Cnt_M_lgc 11				
CTCFailedBuf_Cnt_M_lgc[12]  CTCFailedBuf_Cnt_M_lgc[13]  O  O  CTCFailedBuf_Cnt_M_lgc[14]  O  O  CTCFailedBuf_Cnt_M_lgc[15]  O  O  CTCFailedBuf_Cnt_M_lgc[15]  O  O  CTCFailedBuf_Cnt_M_lgc[17]  O  O  CTCFailedBuf_Cnt_M_lgc[18]  O  O  CTCFailedBuf_Cnt_M_lgc[18]  O  O  CTCFailedBuf_Cnt_M_lgc[18]  O  O  CTCFailedBuf_Cnt_M_lgc[20]  O  CTCFailedBuf_Cnt_M_lgc[20]  O  CTCFailedBuf_Cnt_M_lgc[21]  O  CTCFailedBuf_Cnt_M_lgc[21]  O  CTCFailedBuf_Cnt_M_lgc[22]  O  CTCFailedBuf_Cnt_M_lgc[23]  O  CTCFailedBuf_Cnt_M_lgc[23]  O  CTCFailedBuf_Cnt_M_lgc[24]  O  CTCFailedBuf_Cnt_M_lgc[24]  O  CTCFailedBuf_Cnt_M_lgc[26]  O  CTCFailedBuf_Cnt_M_lgc[26]  O  CTCFailedBuf_Cnt_M_lgc[28]  O  CTCFailedBuf_Cnt_M_lgc[38]  O  CTCFailedBuf_Cnt_M_lgc[40]  O  CTCFailedBuf_Cnt_M_lgc[40]  CTCFailedBuf_Cnt_M_lgc[40]  O  CTCFailedBuf_				
CTCFailedBuf_Cnt_M_lgc[13] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFailedBuf_Cnt_M_lgq15  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				•
CTCFailedBuf_Cnt_M_lgc[16]  CTCFailedBuf_Cnt_M_lgc[17]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[18]  CTCFailedBuf_Cnt_M_lgc[19]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[21]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[22]  CTCFailedBuf_Cnt_M_lgc[23]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[25]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[27]  CTCFailedBuf_Cnt_M_lgc[28]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[24]  CTCFailedBuf_Cnt_M_lgc[48]  CT		0	0	•
CTCFailedBuf_Cnt_M_lgc[18] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[18] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[18] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[20] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[21] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[22] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[23] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[23] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[24] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[28] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[28] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[28] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[28] 0 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[28] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[33] 0 0 0 0 CTCFailedBuf_Cnt_M_lgc[33] 0 0 0 CTCFailedBuf_Cnt_M_lgc[34] 0 CTCFailedBuf_Cnt	CTCFailedBuf_Cnt_M_lgc[15]	0	0	~
CTCFailedBut_Cnt_M_lgc[18]         0         0           CTCFailedBut_Cnt_M_lgc[19]         0         0           CTCFailedBut_Cnt_M_lgc[20]         0         0           CTCFailedBut_Cnt_M_lgc[21]         0         0           CTCFailedBut_Cnt_M_lgc[22]         0         0           CTCFailedBut_Cnt_M_lgc[23]         0         0           CTCFailedBut_Cnt_M_lgc[24]         0         0           CTCFailedBut_Cnt_M_lgc[25]         0         0           CTCFailedBut_Cnt_M_lgc[27]         0         0           CTCFailedBut_Cnt_M_lgc[27]         0         0           CTCFailedBut_Cnt_M_lgc[28]         0         0           CTCFailedBut_Cnt_M_lgc[28]         0         0           CTCFailedBut_Cnt_M_lgc[30]         0         0           CTCFailedBut_Cnt_M_lgc[31]         0         0           CTCFailedBut_Cnt_M_lgc[33]         0         0           CTCFailedBut_Cnt_M_lgc[33]         0         0           CTCFailedBut_Cnt_M_lgc[36]         0         0           CTCFailedBut_Cnt_M_lgc[36]         0         0           CTCFailedBut_Cnt_M_lgc[36]         0         0           CTCFailedBut_Cnt_M_lgc[39]         0         0           CTC	CTCFailedBuf_Cnt_M_lgc[16]	0	0	~
CTCFailedBuf_Cnt_M_lgc[20]         0         0           CTCFailedBuf_Cnt_M_lgc[21]         0         0           CTCFailedBuf_Cnt_M_lgc[21]         0         0           CTCFailedBuf_Cnt_M_lgc[22]         0         0           CTCFailedBuf_Cnt_M_lgc[23]         0         0           CTCFailedBuf_Cnt_M_lgc[25]         0         0           CTCFailedBuf_Cnt_M_lgc[26]         0         0           CTCFailedBuf_Cnt_M_lgc[27]         0         0           CTCFailedBuf_Cnt_M_lgc[28]         0         0           CTCFailedBuf_Cnt_M_lgc[28]         0         0           CTCFailedBuf_Cnt_M_lgc[29]         0         0           CTCFailedBuf_Cnt_M_lgc[30]         0         0           CTCFailedBuf_Cnt_M_lgc[31]         0         0           CTCFailedBuf_Cnt_M_lgc[32]         0         0           CTCFailedBuf_Cnt_M_lgc[33]         0         0           CTCFailedBuf_Cnt_M_lgc[33]         0         0           CTCFailedBuf_Cnt_M_lgc[36]         0         0           CTCFailedBuf_Cnt_M_lgc[36]         0         0           CTCFailedBuf_Cnt_M_lgc[39]         0         0           CTCFailedBuf_Cnt_M_lgc[40]         0         0           CTC				<b>~</b>
CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       0       0         CTCFailedBuf_Cnt_M_lgc[24]       0       0         CTCFailedBuf_Cnt_M_lgc[25]       0       0         CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_l				
CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       0       0         CTCFailedBuf_Cnt_M_lgc[24]       0       0         CTCFailedBuf_Cnt_M_lgc[25]       0       0         CTCFailedBuf_Cnt_M_lgc[26]       0       0         CTCFailedBuf_Cnt_M_lgc[26]       0       0         CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_l				
CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       0       0         CTCFailedBuf_Cnt_M_lgc[24]       0       0         CTCFailedBuf_Cnt_M_lgc[25]       0       0         CTCFailedBuf_Cnt_M_lgc[26]       0       0         CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[29]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_l				
CTCFailedBuf_Cnt_M_lgc[23] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
CTCFailedBuf_Cnt_M_lgc[24]       0       0         CTCFailedBuf_Cnt_M_lgc[25]       0       0         CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[29]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0          CTCFailedBu				•
CTCFailedBuf_Cnt_M_lgc[25]       0       0         CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[29]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0         CTCFailedBuf_Cnt_M_l				-
CTCFailedBuf_Cnt_M_lgc[27]       0       0         CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[29]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0	CTCFailedBuf_Cnt_M_lgc[25]	0	Ö	•
CTCFailedBuf_Cnt_M_lgc[28]       0       0         CTCFailedBuf_Cnt_M_lgc[29]       0       0         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0	CTCFailedBuf_Cnt_M_lgc[26]	0	0	~
CTCFailedBuf_Cnt_M_lgc[29]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0	CTCFailedBuf_Cnt_M_lgc[27]			~
CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				<b>~</b>
CTCFailedBuf_Cnt_M_lgc[31]       0       0         CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[32]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				<b>•</b>
CTCFailedBuf_Cnt_M_lgc[33]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				
CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				
CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				
CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[37]       0       0         CTCFailedBuf_Cnt_M_lgc[38]       0       0         CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0				·
CTCFailedBuf_Cnt_M_lgc[39]       0       0         CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0		0	0	•
CTCFailedBuf_Cnt_M_lgc[40]       0       0         CTCFailedBuf_Cnt_M_lgc[41]       0       0         CTCFailedBuf_Cnt_M_lgc[42]       0       0         CTCFailedBuf_Cnt_M_lgc[43]       0       0         CTCFailedBuf_Cnt_M_lgc[44]       0       0	CTCFailedBuf_Cnt_M_lgc[38]			~
CTCFailedBuf_Cnt_M_lgc[41]         0         0           CTCFailedBuf_Cnt_M_lgc[42]         0         0           CTCFailedBuf_Cnt_M_lgc[43]         0         0           CTCFailedBuf_Cnt_M_lgc[44]         0         0				<b>~</b>
CTCFailedBuf_Cnt_M_lgc[42]         0         0           CTCFailedBuf_Cnt_M_lgc[43]         0         0           CTCFailedBuf_Cnt_M_lgc[44]         0         0				~
CTCFailedBuf_Cnt_M_lgc[43]         0         0           CTCFailedBuf_Cnt_M_lgc[44]         0         0				<b>V</b>
CTCFailedBuf_Cnt_M_lgc[44] 0 0				<b>V</b>

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[50]	0	0	•
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[53]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[55]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	0	0	~
CTCFailedBuf_Cnt_M_lgc[57]	0	0	•
CTCFailedBuf_Cnt_M_lgc[58]	0	0	~
CTCFailedBuf_Cnt_M_lgc[59]	0	0	•
CTCFailedBuf_Cnt_M_lgc[60]	0	0	~
CTCFailedBuf_Cnt_M_lgc[61]	0	0	•
CTCFailedBuf_Cnt_M_lgc[62]	0	0	~
CTCFailedBuf_Cnt_M_lgc[63]	0	0	~
CTCFailedBuf_Cnt_M_lgc[64]	0	0	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	~
CTCFailedBuf_Cnt_M_lgc[66]	0	0	~
CTCFailedBuf_Cnt_M_Igc[67]	0	0	~
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_Igc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_Igc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	•
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	1	1	•
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	~

Test Step 2.15 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

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Input Value
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1
1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1
1
1
1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1
1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 3261627242 1 1 78 172 31 227 66 96 130 24 240
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 3261627242 1 1 78 172 31 227 66 96 130 24 240
1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 3261627242 1 1 78 172 31 227 66 96 130 24 240
1 1 1 1 1 1 1 1 1 1 1 1 0 3261627242 1 1 78 172 31 227 66 96 130 24 240
1 1 1 1 1 1 1 1 1 0 3261627242 1 78 172 31 227 66 96 130 24 240
1 1 1 1 1 1 0 3261627242 1 78 172 31 227 66 96 130 24 240
1 1 1 1 0 3261627242 1 78 172 31 227 66 96 130 24 240
1 1 1 0 3261627242 1 78 172 31 227 66 96 130 24
1 1 0 3261627242 1 78 172 31 227 66 96 130 24
1 0 3261627242 1 78 172 31 227 66 96 130 24 240
0 3261627242 1 78 172 31 227 66 96 130 24 240
3261627242 1 78 172 31 227 66 96 130 24 240
1 78 172 31 227 66 96 130 24 240
78 172 31 227 66 96 130 24
172 31 227 66 96 130 24 240
31 227 66 96 130 24 240
227 66 96 130 24 240
66 96 130 24 240
96 130 24 240
24 240
240
240
31
227
240
151
227
240
221
240 241
227

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[20] 227 Dem\_DTCNumberTable[21] 240 Dem DTCNumberTable[22] 31 Dem\_DTCNumberTable[23] 66 Dem DTCNumberTable[24] 96 Dem\_DTCNumberTable[25] 130 Dem\_DTCNumberTable[26] 24 Dem\_DTCNumberTable[27] 227 Dem\_DTCNumberTable[28] 31 Dem\_DTCNumberTable[29] 227 Dem\_DTCNumberTable[30] 31 Dem\_DTCNumberTable[31] 31 Dem\_DTCNumberTable[32] 227 Dem\_DTCNumberTable[33] 227 Dem\_DTCNumberTable[34] 31 Dem\_DTCNumberTable[35] 227 Dem\_DTCNumberTable[36] 31 Dem\_DTCNumberTable[37] 31 Dem\_DTCNumberTable[38] 31 Dem\_DTCNumberTable[39] 227 Dem\_DTCNumberTable[40] 227 Dem\_DTCNumberTable[41] 66 Dem\_DTCNumberTable[42] 96 Dem\_DTCNumberTable[43] 130 Dem\_DTCNumberTable[44] 24 Dem\_DTCNumberTable[45] 240 Dem DTCNumberTable[46] 31 Dem\_DTCNumberTable[47] 227 Dem DTCNumberTable[48] 96 Dem\_DTCNumberTable[49] 31 Dem DTCNumberTable[50] 227 Dem\_DTCNumberTable[51] 31 Dem DTCNumberTable[52] 31 Dem\_DTCNumberTable[53] 227 Dem\_DTCNumberTable[54] 96 Dem\_DTCNumberTable[55] 240 Dem\_DTCNumberTable[56] 31 Dem\_DTCNumberTable[57] 227 Dem\_DTCNumberTable[58] Dem\_DTCNumberTable[59] 240 Dem\_DTCNumberTable[60] 31 Dem\_DTCNumberTable[61] 227 Dem\_DTCNumberTable[62] 96 Dem\_DTCNumberTable[63] 66 Dem\_DTCNumberTable[64] 96 Dem\_DTCNumberTable[65] 130 Dem DTCNumberTable[66] 24 Dem\_DTCNumberTable[67] 31 Dem DTCNumberTable[68] 31 Dem\_DTCNumberTable[69] 227 Dem\_DTCNumberTable[70] 96 Dem\_DTCNumberTable[71] 240 Dem\_DTCNumberTable[72] 96 Dem\_DTCNumberTable[73] 66

96

130

24

89

78

204

103 238

77

228

228

89

78

228

90

78

228

89

78

Dem\_DTCNumberTable[74]

Dem\_DTCNumberTable[75]

Dem\_DTCNumberTable[76]

Dem\_DTC\_FTB\_Table[0]

Dem\_DTC\_FTB\_Table[1]

Dem\_DTC\_FTB\_Table[2]

Dem\_DTC\_FTB\_Table[3]

Dem\_DTC\_FTB\_Table[4]
Dem\_DTC\_FTB\_Table[5]

Dem\_DTC\_FTB\_Table[6]

Dem\_DTC\_FTB\_Table[7]

Dem DTC FTB Table[8]

Dem\_DTC\_FTB\_Table[9]

Dem DTC FTB Table[10]

Dem\_DTC\_FTB\_Table[11]

Dem\_DTC\_FTB\_Table[12]

Dem\_DTC\_FTB\_Table[13]

Dem\_DTC\_FTB\_Table[14]

Dem\_DTC\_FTB\_Table[15]

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Demii_DTCStatusChangeu		( MAC)	
Name	Input Value		
Dem_DTC_FTB_Table[16]	78		
Dem_DTC_FTB_Table[17]	228		
Dem_DTC_FTB_Table[18]	228		
Dem_DTC_FTB_Table[19]	89		
Dem_DTC_FTB_Table[20]	78		
Dem_DTC_FTB_Table[21]	228		
Dem_DTC_FTB_Table[22]	89		
Dem_DTC_FTB_Table[23]	204		
Dem_DTC_FTB_Table[24]	103		
Dem_DTC_FTB_Table[25]	238		
Dem_DTC_FTB_Table[26]	77		
Dem_DTC_FTB_Table[27]	78		
Dem_DTC_FTB_Table[28]	89		
Dem_DTC_FTB_Table[29]	78		
Dem_DTC_FTB_Table[30]	89		
Dem_DTC_FTB_Table[31]	89		
Dem_DTC_FTB_Table[32]	78		
Dem_DTC_FTB_Table[33]	78		
Dem_DTC_FTB_Table[34]	89		
Dem_DTC_FTB_Table[35]	78		
Dem_DTC_FTB_Table[36]	89		
Dem_DTC_FTB_Table[37]	89		
Dem_DTC_FTB_Table[38]	89		
Dem_DTC_FTB_Table[39]	78		
Dem DTC FTB Table[40]	78		
Dem_DTC_FTB_Table[41]	204		
Dem_DTC_FTB_Table[42]	103		
Dem_DTC_FTB_Table[43]	238		
Dem_DTC_FTB_Table[44]	77		
Dem_DTC_FTB_Table[45]	228		
Dem_DTC_FTB_Table[46]	89		
Dem_DTC_FTB_Table[47]	78		
Dem_DTC_FTB_Table[48]	103		
Dem_DTC_FTB_Table[49]	89		
Dem_DTC_FTB_Table[50]	78		
Dem_DTC_FTB_Table[51]	89		
Dem_DTC_FTB_Table[52]	89		
Dem_DTC_FTB_Table[53]	78		
Dem_DTC_FTB_Table[54]	103		
Dem_DTC_FTB_Table[55]	228		
Dem_DTC_FTB_Table[56]	89		
Dem_DTC_FTB_Table[57]	78		
Dem_DTC_FTB_Table[58]	89		
Dem_DTC_FTB_Table[59]	228		
Dem_DTC_FTB_Table[60]	89		
Dem_DTC_FTB_Table[61]	78		
Dem_DTC_FTB_Table[62]	103		
Dem_DTC_FTB_Table[63]	204		
Dem_DTC_FTB_Table[64]	103		
Dem_DTC_FTB_Table[65]	238		
Dem_DTC_FTB_Table[66]	77		
Dem_DTC_FTB_Table[67]	89		
Dem_DTC_FTB_Table[68]	89		
Dem_DTC_FTB_Table[69]	78		
Dem_DTC_FTB_Table[70]	103		
Dem_DTC_FTB_Table[71]	228		
Dem_DTC_FTB_Table[72]	103		
Dem_DTC_FTB_Table[73]	204		
Dem_DTC_FTB_Table[74]	103		
Dem_DTC_FTB_Table[75]	238		
Dem_DTC_FTB_Table[76]	77		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	-
CTCFailedBuf_Cnt_M_lgc[1]	1	1	-
CTCFailedBuf_Cnt_M_lgc[2]	1	1	-
CTCFailedBuf_Cnt_M_lgc[3]	1	1	-
CTCFailedBuf_Cnt_M_lgc[4]	1	1	•
CTCFailedBuf_Cnt_M_lgc[5]	1	1	-
	1	1	-
CTCFalledBut_Cftt_lvt_lgc[0]	· ·		1
CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	1	1	-
CTCFailedBuf_Cnt_M_lgc[7]	1	1	

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	v ✓
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[14]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf Cnt M lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_Igc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22]	1	1	
CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_Igc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[26]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[27]	1	1	<b>y</b>
CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29]	1	1	·
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	✓
CTCFailedBuf_Cnt_M_Igc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[35]	1	1	
CTCFailedBuf_Cnt_M_Igc[37]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[38]	1	1	~
CTCFailedBuf_Cnt_M_Igc[39]	1	1	~
CTCFailedBuf_Cnt_M_lgc[40]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	1	1	
CTCFailedBuf_Cnt_M_lgc[43]	1	1	~
CTCFailedBuf_Cnt_M_lgc[44]	1	1	~
CTCFailedBuf_Cnt_M_Igc[45]	1	1	~
CTCFailedBuf_Cnt_M_lgc[46]	1	1	~
CTCFailedBuf_Cnt_M_lgc[47] CTCFailedBuf_Cnt_M_lgc[48]	1	1	
CTCFailedBuf_Cnt_M_lgc[49]	1	1	~
CTCFailedBuf_Cnt_M_lgc[50]	1	1	~
CTCFailedBuf_Cnt_M_lgc[51]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[52]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53] CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_Igc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[58]	1	1	•
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60] CTCFailedBuf_Cnt_M_lgc[61]	1	1	-
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	1	1	~
CTCFailedBuf_Cnt_M_lgc[66] CTCFailedBuf_Cnt_M_lgc[67]	1	1	~
CTCFailedBuf_Cnt_M_lgc[68]	1	1	~
CTCFailedBuf_Cnt_M_lgc[69]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[70]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[72] CTCFailedBuf_Cnt_M_lgc[73]	1	1	<b>V</b>
CTCFalledBut_Cnt_M_lgc[73] CTCFalledBuf_Cnt_M_lgc[74]	1	1	
CTCFailedBuf_Cnt_M_lgc[75]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	1	1	~
CTCFailed_Cnt_M_lgc	0	0	<b>~</b>
Demlf_DTCStatusChanged()	0	0	<b>Y</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	U	•

Demlf\_DTCStatusChanged

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Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt Inc	1	Rte Write An Demlf CTCFailed Cnt Igc	1	_

Test Step 2.16 (Repeat Count = 1)	ن ا
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27] CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf Cnt M Igc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53] CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62] CTCFailedBuf_Cnt_M_lgc[63]	1
o. o. asabal_ont_m_gotooj	

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	- Tacitat
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	1
TC	4231674622
DTCKind	2
DTCStatusNew	178
DTCStatusOld	176
Dem DTCNumberTable[0]	83
Dem_DTCNumberTable[1]	99
Dem_DTCNumberTable[2]	240
Dem DTCNumberTable[3]	233
Dem_DTCNumberTable[3]	31
Dem_DTCNumberTable[4]	75
Dem_DTCNumberTable[6]	164
Dem_DTCNumberTable[7]	164
Dem_DTCNumberTable[7]	83
	99
Dem_DTCNumberTable[9]	
Dem_DTCNumberTable[10]	164
Dem_DTCNumberTable[11]	40
Dem_DTCNumberTable[12]	99
Dem_DTCNumberTable[13]	164
Dem_DTCNumberTable[14]	83
Dem_DTCNumberTable[15]	99
Dem_DTCNumberTable[16]	99
Dem_DTCNumberTable[17]	164
Dem_DTCNumberTable[18]	74
Dem_DTCNumberTable[19]	83
Dem_DTCNumberTable[20]	99
Dem_DTCNumberTable[21]	164
Dem_DTCNumberTable[22]	83
Dem_DTCNumberTable[23]	240
Dem_DTCNumberTable[24]	233
Dem_DTCNumberTable[25]	31
Dem_DTCNumberTable[26]	75
Dem_DTCNumberTable[27]	99
Dem_DTCNumberTable[28]	83
Dem_DTCNumberTable[29]	99
Dem_DTCNumberTable[30]	83
Dem_DTCNumberTable[31]	83
Dem_DTCNumberTable[32]	99
Dem_DTCNumberTable[33]	99
Dem_DTCNumberTable[34]	83
Dem_DTCNumberTable[35]	99
Dem_DTCNumberTable[36]	83
Dem_DTCNumberTable[37]	83
Dem_DTCNumberTable[38]	83
Dem_DTCNumberTable[39]	99
Dem_DTCNumberTable[40]	99
Dem_DTCNumberTable[41]	240
Dem_DTCNumberTable[42]	233
Dem_DTCNumberTable[43]	31
Dem_DTCNumberTable[44]	75
Dem_DTCNumberTable[45]	164
Dem_DTCNumberTable[46]	83
	99
rem DTCNumberrable(47)	233
Dem_DTCNumberTable[47]  Dem_DTCNumberTable[48]	
Dem_DTCNumberTable[48]	83
Dem_DTCNumberTable[48] Dem_DTCNumberTable[49]	83
Dem_DTCNumberTable[48] Dem_DTCNumberTable[49] Dem_DTCNumberTable[50]	99
Dem_DTCNumberTable[48] Dem_DTCNumberTable[49] Dem_DTCNumberTable[50] Dem_DTCNumberTable[51]	99 83
Dem_DTCNumberTable[48] Dem_DTCNumberTable[49] Dem_DTCNumberTable[50]	99

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Demlf_DTCStatusChanged		MACICAL
Name	Input Value	
Dem_DTCNumberTable[55]	164	
Dem_DTCNumberTable[56]	83	
Dem_DTCNumberTable[57]	99	
Dem_DTCNumberTable[58]	83	
Dem_DTCNumberTable[59]	164	
Dem_DTCNumberTable[60]	83	
Dem_DTCNumberTable[61]	99	
Dem_DTCNumberTable[62] Dem_DTCNumberTable[63]	233 240	
Dem_DTCNumberTable[63]	233	
Dem_DTCNumberTable[65]	31	
Dem_DTCNumberTable[66]	75	
Dem DTCNumberTable[67]	83	
Dem_DTCNumberTable[68]	83	
Dem_DTCNumberTable[69]	99	
em_DTCNumberTable[70]	233	
em_DTCNumberTable[71]	164	
em_DTCNumberTable[72]	233	
em_DTCNumberTable[73]	240	
em_DTCNumberTable[74]	233	
em_DTCNumberTable[75]	31	
em_DTCNumberTable[76]	75	
em_DTC_FTB_Table[0]	170	
em_DTC_FTB_Table[1]	194	
em_DTC_FTB_Table[2]	13	
em_DTC_FTB_Table[3]	32	
em_DTC_FTB_Table[4]	172	
em_DTC_FTB_Table[5]	241	
pem_DTC_FTB_Table[6]	91	
em_DTC_FTB_Table[7]	91	
rem_DTC_FTB_Table[8]	170	
em_DTC_FTB_Table[9]	194 91	
em_DTC_FTB_Table[10] em_DTC_FTB_Table[11]	82	
Dem_DTC_FTB_Table[11]	194	
em_DTC_FTB_Table[13]	91	
Dem_DTC_FTB_Table[14]	170	
Dem DTC FTB Table[15]	194	
em_DTC_FTB_Table[16]	194	
Dem_DTC_FTB_Table[17]	91	
em_DTC_FTB_Table[18]	55	
em_DTC_FTB_Table[19]	170	
em_DTC_FTB_Table[20]	194	
em_DTC_FTB_Table[21]	91	
em_DTC_FTB_Table[22]	170	
em_DTC_FTB_Table[23]	13	
em_DTC_FTB_Table[24]	32	
em_DTC_FTB_Table[25]	172	
em_DTC_FTB_Table[26]	241	
em_DTC_FTB_Table[27]	194	
em_DTC_FTB_Table[28]	170	
em_DTC_FTB_Table[29]	194	
em_DTC_FTB_Table[30]	170	
em_DTC_FTB_Table[31]	170	
em_DTC_FTB_Table[32]	194 194	
em_DTC_FTB_Table[33] em_DTC_FTB_Table[34]	194	
em_DTC_FTB_Table[34] em_DTC_FTB_Table[35]	194	
em_DTC_FTB_Table[36]	170	
em_DTC_FTB_Table[37]	170	
em_DTC_FTB_Table[38]	170	
em_DTC_FTB_Table[39]	194	
em_DTC_FTB_Table[40]	194	
em_DTC_FTB_Table[41]	13	
em_DTC_FTB_Table[42]	32	
em_DTC_FTB_Table[43]	172	
em_DTC_FTB_Table[44]	241	
em_DTC_FTB_Table[45]	91	
em_DTC_FTB_Table[46]	170	
em_DTC_FTB_Table[47]	194	
em_DTC_FTB_Table[48]	32	
em_DTC_FTB_Table[49]	170	
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Name	Input Value		
Dem_DTC_FTB_Table[51]	170		
Dem_DTC_FTB_Table[52]	170 194		
Dem_DTC_FTB_Table[53] Dem_DTC_FTB_Table[54]	32		
Dem_DTC_FTB_Table[54]	91		
Dem_DTC_FTB_Table[56]	170		
Dem_DTC_FTB_Table[57]	194		
Dem_DTC_FTB_Table[58]	170		
Dem_DTC_FTB_Table[59]	91		
Dem_DTC_FTB_Table[60]	170		
Dem_DTC_FTB_Table[61]	194		
Dem_DTC_FTB_Table[62]	32		
Dem_DTC_FTB_Table[63]	13		
Dem_DTC_FTB_Table[64]	32		
Dem_DTC_FTB_Table[65]	172		
Dem_DTC_FTB_Table[66]	241		
Dem_DTC_FTB_Table[67]	170 170		
Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69]	194		
Dem_DTC_FTB_Table[70]	32		
Dem DTC FTB Table[71]	91		
Dem DTC FTB Table[72]	32		
Dem_DTC_FTB_Table[73]	13		
Dem_DTC_FTB_Table[74]	32		
Dem_DTC_FTB_Table[75]	172		
Dem_DTC_FTB_Table[76]	241		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[4]	1	1	· · · · · ·
CTCFailedBuf_Cnt_M_lgc[5]	1	1	
CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	1	1	
CTCFailedBuf_Cnt_M_lgc[8]	1	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	1	•
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	•
CTCFailedBuf_Cnt_M_lgc[14]	1	1	~
CTCFailedBuf_Cnt_M_lgc[15]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[16]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[17]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[18]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[19]	1 0	0	
CTCFailedBuf_Cnt_M_lgc[20] CTCFailedBuf_Cnt_M_lgc[21]	0	0	
CTCFailedBuf_Cnt_M_lgc[22]	0	0	
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<u> </u>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[28]	1	1	~
CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[33]	1	1	
CTCFailedBuf_Cnt_M_lgc[34]	0	0	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[35] CTCFailedBuf_Cnt_M_lgc[36]	0	0	
CTCFailedBuf_Cnt_M_igc[36] CTCFailedBuf_Cnt_M_igc[37]	0	0	
CTCFailedBuf_Cnt_M_lgc[38]	0	0	
CTCFailedBuf_Cnt_M_Igc[39]	0	0	·
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[42]	0	0	•
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~

Demlf\_DTCStatusChanged

CTCFailedBuf\_Cnt\_M\_lgc[73]

CTCFailedBuf\_Cnt\_M\_lgc[74]

CTCFailedBuf\_Cnt\_M\_lgc[75]

CTCFailedBuf\_Cnt\_M\_lgc[76]

Demlf DTCStatusChanged()

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

CTCFailed\_Cnt\_M\_lgc

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Actual Value **Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[53]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ CTCFailedBuf\_Cnt\_M\_lgc[65] ソソソソソソ 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[66]$ CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	~

0

0

0

0

1

0

0

0

0

0

1

0

Test Step 2.17 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	0
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

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Demii_DTCStatusChanged	- Talcitat
Name	Input Value
CTCFailedBuf Cnt M lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1.
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	1673189688
DTCKind	1
DTCStatusNew	238
DTCStatusOld	228
Dem_DTCNumberTable[0]	46
Dem_DTCNumberTable[1]	245
Dem_DTCNumberTable[2]	24
Dem_DTCNumberTable[3]	143
Dem_DTCNumberTable[4]	13
Dem_DTCNumberTable[5]	12
Dem_DTCNumberTable[6]	209
Dem_DTCNumberTable[7]	209
Dem_DTCNumberTable[8]	46
Dem_DTCNumberTable[9]	245
Dem_DTCNumberTable[10]	209
Dem_DTCNumberTable[11]	145
Dem_DTCNumberTable[12]	245
Dem_DTCNumberTable[13]	209
Dem_DTCNumberTable[14]	46
Dem_DTCNumberTable[15]	245
Dem_DTCNumberTable[16]	245
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Dem_DTCNumberTable[17]	209
Dem_DTCNumberTable[17] Dem_DTCNumberTable[18]	239

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Name	Input Value	
Dem_DTCNumberTable[20]	245	
Dem_DTCNumberTable[21]	209	
Dem_DTCNumberTable[22]	46	
Dem_DTCNumberTable[23]	24	
Dem_DTCNumberTable[24]	143	
Dem_DTCNumberTable[25]	13	
Dem_DTCNumberTable[26]	12	
Dem_DTCNumberTable[20]	245	
Dem_DTCNumberTable[28]	46	
Dem_DTCNumberTable[29]	245	
Dem_DTCNumberTable[30]	46	
Dem_DTCNumberTable[31]	46	
Dem_DTCNumberTable[32]	245	
Dem_DTCNumberTable[33]	245	
Dem_DTCNumberTable[34]	46	
Dem_DTCNumberTable[35]	245	
Dem_DTCNumberTable[36]	46	
Dem_DTCNumberTable[37]	46	
Dem_DTCNumberTable[38]	46	
Dem_DTCNumberTable[39]	245	
Dem_DTCNumberTable[40]	245	
Dem_DTCNumberTable[41]	24	
Dem_DTCNumberTable[42]	143	
Dem_DTCNumberTable[43]	13	
Dem_DTCNumberTable[44]	12	
Dem_DTCNumberTable[45]	209	
Dem_DTCNumberTable[46]	46	
Dem_DTCNumberTable[47]	245	
Dem_DTCNumberTable[48]	143	
Dem_DTCNumberTable[49]	46	
Dem_DTCNumberTable[50]	245	
Dem_DTCNumberTable[51]	46	
Dem_DTCNumberTable[52]	46	
Dem_DTCNumberTable[53]	245	
Dem_DTCNumberTable[54]	143	
Dem_DTCNumberTable[55]	209	
Dem_DTCNumberTable[56]	46	
Dem_DTCNumberTable[57]	245	
Dem_DTCNumberTable[58]	46	
Dem DTCNumberTable[59]	209	
Dem_DTCNumberTable[60]	46	
Dem_DTCNumberTable[61]	245	
Dem_DTCNumberTable[62]	143	
Dem DTCNumberTable[63]	24	
Dem_DTCNumberTable[64]	143	
Dem_DTCNumberTable[65]	13	
Dem_DTCNumberTable[66]	12	
Dem_DTCNumberTable[67]	46	
Dem_DTCNumberTable[68]	46	
Dem_DTCNumberTable[69]	245	
Dem_DTCNumberTable[70]	143	
Dem_DTCNumberTable[71]	209	
Dem_DTCNumberTable[72]	143	
Dem_DTCNumberTable[73]	24	
Dem_DTCNumberTable[74]	143	
Dem_DTCNumberTable[75]	13	
Dem_DTCNumberTable[76]	12	
Dem_DTC_FTB_Table[0]	107	
Dem_DTC_FTB_Table[1]	156	
Dem_DTC_FTB_Table[2]	5	
Dem_DTC_FTB_Table[3]	166	
Dem_DTC_FTB_Table[4]	182	
Dem_DTC_FTB_Table[5]	118	
Dem_DTC_FTB_Table[6]	237	
Dem_DTC_FTB_Table[7]	237	
Dem_DTC_FTB_Table[8]	107	
Dem_DTC_FTB_Table[9]	156	
Dem_DTC_FTB_Table[10]	237	
Dem_DTC_FTB_Table[11]	66	
Dem_DTC_FTB_Table[12]	156	
	237	
Dem_DTC_FTB_Table[13] Dem_DTC_FTB_Table[14]	237 107	

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Name	Input Value		
Dem_DTC_FTB_Table[16]	156		
Dem_DTC_FTB_Table[17]	237		
Dem_DTC_FTB_Table[18]	106		
Dem_DTC_FTB_Table[19]	107		
Dem_DTC_FTB_Table[20]	156		
Dem_DTC_FTB_Table[21]	237		
Dem_DTC_FTB_Table[22]	107		
Dem_DTC_FTB_Table[23]	5 166		
Dem_DTC_FTB_Table[24] Dem_DTC_FTB_Table[25]	182		
Dem_DTC_FTB_Table[26]	118		
Dem_DTC_FTB_Table[27]	156		
Dem_DTC_FTB_Table[28]	107		
Dem_DTC_FTB_Table[29]	156		
Dem_DTC_FTB_Table[30]	107		
Dem_DTC_FTB_Table[31]	107		
Dem_DTC_FTB_Table[32]	156		
Dem_DTC_FTB_Table[33]	156		
Dem_DTC_FTB_Table[34]	107		
Dem_DTC_FTB_Table[35]	156		
Dem_DTC_FTB_Table[36]	107		
Dem_DTC_FTB_Table[37]	107		
Dem_DTC_FTB_Table[38]	107		
Dem_DTC_FTB_Table[39]	156		
Dem_DTC_FTB_Table[40]	156		
Dem_DTC_FTB_Table[41]	5 166		
Dem_DTC_FTB_Table[42] Dem_DTC_FTB_Table[43]	182		
Dem_DTC_FTB_Table[44]	118		
Dem_DTC_FTB_Table[45]	237		
Dem_DTC_FTB_Table[46]	107		
Dem_DTC_FTB_Table[47]	156		
Dem_DTC_FTB_Table[48]	166		
Dem_DTC_FTB_Table[49]	107		
Dem_DTC_FTB_Table[50]	156		
Dem_DTC_FTB_Table[51]	107		
Dem_DTC_FTB_Table[52]	107		
Dem_DTC_FTB_Table[53]	156		
Dem_DTC_FTB_Table[54]	166		
Dem_DTC_FTB_Table[55]	237		
Dem_DTC_FTB_Table[56]	107		
D. DTO FTD T II IFT	156		
Dem_DTC_FTB_Table[57]	107		
Dem_DTC_FTB_Table[58]	107		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59]	237		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60]	237 107		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61]	237 107 156		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62]	237 107		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61]	237 107 156 166		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63]	237 107 156 166 5		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64]	237 107 156 166 5 166		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65]	237 107 156 166 5 166 182		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66]	237 107 156 166 5 166 182		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[68]	237 107 156 166 5 166 182 118		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69]	237 107 156 166 5 166 182 118 107 107 156		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71]	237 107 156 166 5 166 182 118 107 107 156 166 237		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	237 107 156 166 5 166 182 118 107 107 156 166 237		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[74]	237 107 156 166 5 166 182 118 107 107 107 156 166 237 166 5 166 182		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118 Actual Value	Expected Value	Result
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value	1	~
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1	1	~
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[76] Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1	1 1 1	* *
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1	1 1 1 1	\rightarrow \right
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1 1	1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1 1 1	1 1 1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1 1 1 1	1 1 1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 118  Actual Value 1 1 1 1 1	1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	237 107 156 166 5 166 182 118 107 107 156 166 237 166 5 166 182 1118  Actual Value 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 0	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	•
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_Igc[15] CTCFailedBuf_Cnt_M_Igc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	-
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	•
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	1	1	
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	•
CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0	0	-
CTCFailedBuf_Cnt_M_lgc[38]	0	0	
CTCFailedBuf_Cnt_M_lgc[39]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	•
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47] CTCFailedBuf_Cnt_M_lgc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	-
CTCFailedBuf_Cnt_M_lgc[50]	0	0	•
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	•
CTCFailedBuf_Cnt_M_lgc[56]	0	0	· ·
CTCFailedBuf_Cnt_M_lgc[57] CTCFailedBuf_Cnt_M_lgc[58]	1	1	
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[68] CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	•
Demlf_DTCStatusChanged()  Pto Write An Demlf_CTCEailed_Cnt_lac/data\	0	0	<b>*</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	l o	U	

Demlf\_DTCStatusChanged

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Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write An Demlf CTCFailed Cnt Inc	1	Rte Write An Demlf CTCFailed Cnt Igc	1	_

Test Step 2.18 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17] CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34] CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43] CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50] CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59] CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

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Demii_DTC3tatusChanged		- Table (Mar)
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[64]	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	
CTCFailedBuf_Cnt_M_lgc[70]	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	
	0	
CTCFailedBuf_Cnt_M_lgc[72]	0	
CTCFailedBuf_Cnt_M_lgc[73]	1	
CTCFailedBuf_Cnt_M_lgc[74]		
CTCFailedBuf_Cnt_M_lgc[75]	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	
CTCFailed_Cnt_M_lgc	1	
DTC	3302797192	
DTCKind	1	
DTCStatusNew	172	
DTCStatusOld	91	
Dem_DTCNumberTable[0]	112	
Dem_DTCNumberTable[1]	227	
Dem_DTCNumberTable[2]	76	
Dem_DTCNumberTable[3]	252	
Dem_DTCNumberTable[4]	240	
Dem_DTCNumberTable[5]	206	
Dem_DTCNumberTable[6]	62	
Dem_DTCNumberTable[7]	62	
Dem_DTCNumberTable[8]	112	
Dem_DTCNumberTable[9]	227	
Dem_DTCNumberTable[10]	62	
Dem_DTCNumberTable[11]	80	
Dem_DTCNumberTable[12]	227	
Dem_DTCNumberTable[13]	62	
Dem_DTCNumberTable[14]	112	
Dem_DTCNumberTable[15]	227	
Dem_DTCNumberTable[16]	227	
Dem_DTCNumberTable[17]	62	
Dem_DTCNumberTable[18]	57	
Dem DTCNumberTable[19]	112	
Dem DTCNumberTable[19] Dem DTCNumberTable[20]	227	
Dem_DTCNumberTable[21]	62	
Dem_DTCNumberTable[22]	112	
Dem_DTCNumberTable[23]	76	
Dem_DTCNumberTable[24]	252	
Dem_DTCNumberTable[25]	240	
Dem_DTCNumberTable[26]	206	
Dem_DTCNumberTable[27]	227	
Dem_DTCNumberTable[28]	112	
Dem_DTCNumberTable[29]	227	
Dem_DTCNumberTable[30]	112	
Dem_DTCNumberTable[31]	112	
Dem_DTCNumberTable[32]	227	
Dem_DTCNumberTable[33]	227	
Dem_DTCNumberTable[34]	112	
Dem_DTCNumberTable[35]	227	
Dem_DTCNumberTable[36]	112	
Dem_DTCNumberTable[37]	112	
Dem_DTCNumberTable[38]	112	
Dem_DTCNumberTable[39]	227	
Dem_DTCNumberTable[40]	227	
Dem_DTCNumberTable[41]	76	
Dem_DTCNumberTable[42]	252	
Dem_DTCNumberTable[43]	240	
Dem_DTCNumberTable[44]	206	
Dem_DTCNumberTable[44]	62	
Dem_DTCNumberTable[45] Dem_DTCNumberTable[46]	112	
Dem_DTCNumberTable[47]	227	
Dem_DTCNumberTable[48]	252	
Dem_DTCNumberTable[49]	112	
Dem_DTCNumberTable[50]	227	
Dem_DTCNumberTable[51]	112	
Dem_DTCNumberTable[52]	112	
Dem_DTCNumberTable[53]	227	
Delli_D i Civalibei rabie[55]	252	

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Denni_D1CStatusChanged		T GALCITON
Name	Input Value	
Dem_DTCNumberTable[55]	62	
Dem_DTCNumberTable[56]	112	
Dem_DTCNumberTable[57]	227	
Dem_DTCNumberTable[58]	112	
Dem_DTCNumberTable[59]	62	
Dem_DTCNumberTable[60]	112	
Dem_DTCNumberTable[61]	227	
Dem_DTCNumberTable[62]	252	
Dem_DTCNumberTable[63]	76	
Dem_DTCNumberTable[64]	252	
Dem_DTCNumberTable[65]	240	
Dem_DTCNumberTable[66]	206	
Dem_DTCNumberTable[67]	112	
Dem_DTCNumberTable[68]	112	
Dem_DTCNumberTable[69]	227	
Dem_DTCNumberTable[70]	252	
Dem_DTCNumberTable[71]	62	
Dem_DTCNumberTable[72]	252	
Dem_DTCNumberTable[73]	76	
Dem_DTCNumberTable[74]	252	
Dem_DTCNumberTable[75]	240	
Dem_DTCNumberTable[76]	206	
Dem_DTC_FTB_Table[0]	219	
Dem_DTC_FTB_Table[1]	237	
Dem_DTC_FTB_Table[2]	46	
Dem_DTC_FTB_Table[3]	187	
Dem_DTC_FTB_Table[4]	250	
Dem_DTC_FTB_Table[5]	36	
Dem_DTC_FTB_Table[6]	202	
Dem_DTC_FTB_Table[7]	202	
Dem_DTC_FTB_Table[8]	219	
Dem_DTC_FTB_Table[9]	237	
Dem_DTC_FTB_Table[10]	202	
Dem_DTC_FTB_Table[11]	126	
Dem_DTC_FTB_Table[12]	237	
Dem_DTC_FTB_Table[13]	202	
Dem_DTC_FTB_Table[14]	219	
Dem_DTC_FTB_Table[15]	237	
Dem_DTC_FTB_Table[16]	237	
Dem_DTC_FTB_Table[17]	202	
Dem_DTC_FTB_Table[18]	86	
Dem_DTC_FTB_Table[19]	219	
Dem_DTC_FTB_Table[20]	237	
Dem_DTC_FTB_Table[21]	202	
Dem_DTC_FTB_Table[22]	219	
Dem_DTC_FTB_Table[23]	46	
Dem_DTC_FTB_Table[24]	187	
Dem_DTC_FTB_Table[25]	250	
Dem_DTC_FTB_Table[26]	36	
Dem_DTC_FTB_Table[27]	237	
Dem_DTC_FTB_Table[28]	219	
Dem_DTC_FTB_Table[29]	237	
Dem_DTC_FTB_Table[30]	219	
Dem_DTC_FTB_Table[31]	219	
Dem_DTC_FTB_Table[32]	237	
Dem_DTC_FTB_Table[33]	237	
Dem_DTC_FTB_Table[34]	219	
Dem_DTC_FTB_Table[35]	237	
Dem_DTC_FTB_Table[36]	219	
Dem_DTC_FTB_Table[37]	219	
Dem_DTC_FTB_Table[38]	219	
Dem_DTC_FTB_Table[39]	237	
Dem_DTC_FTB_Table[40]	237	
Dem_DTC_FTB_Table[41]	46	
Dem_DTC_FTB_Table[42]	187	
Dem_DTC_FTB_Table[43]	250	
Dem_DTC_FTB_Table[44]	36	
Dem_DTC_FTB_Table[45]	202	
Dem_DTC_FTB_Table[46]	219	
Dem_DTC_FTB_Table[47]	237	
Dem_DTC_FTB_Table[48]	187	
	219	
Dem_DTC_FTB_Table[49]		

Demlf\_DTCStatusChanged

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Input Value Dem\_DTC\_FTB\_Table[51] 219 Dem\_DTC\_FTB\_Table[52] 219 Dem DTC\_FTB\_Table[53] 237 Dem\_DTC\_FTB\_Table[54] 187 Dem\_DTC\_FTB\_Table[55] 202 Dem\_DTC\_FTB\_Table[56] 219 Dem\_DTC\_FTB\_Table[57] 237 Dem\_DTC\_FTB\_Table[58] 219 Dem\_DTC\_FTB\_Table[59] 202 Dem\_DTC\_FTB\_Table[60] 219 Dem\_DTC\_FTB\_Table[61] 237 Dem\_DTC\_FTB\_Table[62] 187 46 Dem\_DTC\_FTB\_Table[63] Dem\_DTC\_FTB\_Table[64] 187 Dem\_DTC\_FTB\_Table[65] 250 Dem DTC FTB Table[66] 36 Dem\_DTC\_FTB\_Table[67] 219 Dem\_DTC\_FTB\_Table[68] 219 Dem\_DTC\_FTB\_Table[69] 237 Dem\_DTC\_FTB\_Table[70] 187 Dem\_DTC\_FTB\_Table[71] 202 Dem\_DTC\_FTB\_Table[72] 187 Dem\_DTC\_FTB\_Table[73] 46 Dem\_DTC\_FTB\_Table[74] 187 Dem\_DTC\_FTB\_Table[75] 250 Dem\_DTC\_FTB\_Table[76] 36 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf Cnt M lgc[4] 1 CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[8] 1 CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf\_Cnt\_M\_lgc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_Igc[19] 1 1 V CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf Cnt M lqc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	•
CTCFailedBuf_Cnt_M_lgc[50]	0	0	•
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	•
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[55]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[56]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[57]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[59]	1	1	•
CTCFailedBuf_Cnt_M_lgc[60]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[61]	1	1	•
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	•
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	•
CTCFailedBuf_Cnt_M_lgc[66]	0	0	~
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_Igc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	1	1	~
CTCFailedBuf_Cnt_M_Igc[75]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	1	1	~
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	~

Test Step 2.19 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

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	- Contraction of the contraction
Name	Input Value
CTCFailedBuf Cnt M Igc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	0
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	3645660753
DTCKind	1
DTCStatusNew	182
DTCStatusOld	237
Dem_DTCNumberTable[0]	0
Dem DTCNumberTable[1]	0
Dem_DTCNumberTable[1] Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[2]	0
Dem_DTCNumberTable[4]	0
	0
Dem_DTCNumberTable[5]	
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11]	0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12]	0 0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13]	0 0 0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14]	0 0 0 0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15]	0 0 0 0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16]	0 0 0 0 0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16] Dem_DTCNumberTable[17]	0 0 0 0 0 0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12] Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16]	0 0 0 0 0

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[20] 0 Dem\_DTCNumberTable[21] 0 Dem DTCNumberTable[22] 0 Dem\_DTCNumberTable[23] 0 Dem DTCNumberTable[24] 0 Dem\_DTCNumberTable[25] 0 Dem\_DTCNumberTable[26] 0 Dem\_DTCNumberTable[27] 0 Dem\_DTCNumberTable[28] 0 Dem\_DTCNumberTable[29] 0 Dem\_DTCNumberTable[30] 0 Dem\_DTCNumberTable[31] 0 Dem\_DTCNumberTable[32] 0 0 Dem\_DTCNumberTable[33] Dem\_DTCNumberTable[34] 0 0 Dem\_DTCNumberTable[35] Dem\_DTCNumberTable[36] 0 Dem\_DTCNumberTable[37] 0 Dem\_DTCNumberTable[38] 0 Dem\_DTCNumberTable[39] 0 Dem\_DTCNumberTable[40] 0 Dem\_DTCNumberTable[41] 0 Dem\_DTCNumberTable[42] 0 Dem\_DTCNumberTable[43] 0 Dem\_DTCNumberTable[44] 0 Dem\_DTCNumberTable[45] 0 Dem DTCNumberTable[46] 0 Dem\_DTCNumberTable[47] 0 Dem DTCNumberTable[48] 0 Dem\_DTCNumberTable[49] 0 Dem DTCNumberTable[50] 0 Dem\_DTCNumberTable[51] 0 Dem DTCNumberTable[52] 0 Dem\_DTCNumberTable[53] 0 Dem\_DTCNumberTable[54] 0 Dem\_DTCNumberTable[55] 0 Dem\_DTCNumberTable[56] 0 Dem\_DTCNumberTable[57] 0 Dem\_DTCNumberTable[58] 0 Dem\_DTCNumberTable[59] 0 Dem\_DTCNumberTable[60] 0 0 Dem\_DTCNumberTable[61] Dem\_DTCNumberTable[62] 0 Dem\_DTCNumberTable[63] 0 Dem\_DTCNumberTable[64] n Dem\_DTCNumberTable[65] 0 Dem\_DTCNumberTable[66] n Dem\_DTCNumberTable[67] 0 Dem DTCNumberTable[68] n Dem\_DTCNumberTable[69] 0 Dem\_DTCNumberTable[70] 0 Dem\_DTCNumberTable[71] 0 Dem\_DTCNumberTable[72] 0 Dem\_DTCNumberTable[73] 0 Dem\_DTCNumberTable[74] 0 Dem\_DTCNumberTable[75] 0 Dem\_DTCNumberTable[76] 0 Dem\_DTC\_FTB\_Table[0] 69 Dem\_DTC\_FTB\_Table[1] 30 Dem\_DTC\_FTB\_Table[2] 148 Dem\_DTC\_FTB\_Table[3] 120 135 Dem\_DTC\_FTB\_Table[4] Dem\_DTC\_FTB\_Table[5] 193 Dem\_DTC\_FTB\_Table[6] 53 Dem\_DTC\_FTB\_Table[7] 53 Dem DTC FTB Table[8] 69 Dem\_DTC\_FTB\_Table[9] 30 Dem DTC FTB Table[10] 53 Dem\_DTC\_FTB\_Table[11] 189 Dem\_DTC\_FTB\_Table[12] 30

53

69

30

Dem\_DTC\_FTB\_Table[13]

Dem\_DTC\_FTB\_Table[14]

Dem\_DTC\_FTB\_Table[15]

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		• • • • • • • • • • • • • • • • • • • •	
Name	Input Value		
Dem_DTC_FTB_Table[16]	30		
Dem_DTC_FTB_Table[17]	53		
Dem_DTC_FTB_Table[18]	127		
Dem_DTC_FTB_Table[19]	69		
Dem_DTC_FTB_Table[20]	30		
Dem_DTC_FTB_Table[21]	53		
Dem_DTC_FTB_Table[22]	69		
Dem_DTC_FTB_Table[23]	148		
Dem_DTC_FTB_Table[24]	120		
Dem_DTC_FTB_Table[25]	135		
Dem_DTC_FTB_Table[26]	193		
Dem_DTC_FTB_Table[27]	30		
Dem_DTC_FTB_Table[28]	69		
Dem_DTC_FTB_Table[29]	30		
Dem_DTC_FTB_Table[30]	69		
Dem_DTC_FTB_Table[31]	69		
Dem_DTC_FTB_Table[32]	30		
Dem_DTC_FTB_Table[33]	30		
Dem_DTC_FTB_Table[34]	69		
Dem_DTC_FTB_Table[35]	30		
Dem_DTC_FTB_Table[36]	69		
Dem_DTC_FTB_Table[37]	69		
Dem_DTC_FTB_Table[38]	69		
Dem_DTC_FTB_Table[39]	30		
Dem_DTC_FTB_Table[40]	30		
Dem_DTC_FTB_Table[41]	148		
Dem_DTC_FTB_Table[42]	120		
Dem_DTC_FTB_Table[43]	135		
Dem_DTC_FTB_Table[44]	193		
Dem_DTC_FTB_Table[45]	53		
Dem_DTC_FTB_Table[46]	69		
Dem_DTC_FTB_Table[47]	30		
Dem_DTC_FTB_Table[48]	120		
Dem_DTC_FTB_Table[49]	69		
Dem_DTC_FTB_Table[50]	30		
Dem_DTC_FTB_Table[51]	69		
Dem_DTC_FTB_Table[52]	69		
Dem_DTC_FTB_Table[53]	30		
Dem_DTC_FTB_Table[54]	120		
Dem_DTC_FTB_Table[55]	53		
Dem_DTC_FTB_Table[56]	69   30		
Dem_DTC_FTB_Table[57] Dem_DTC_FTB_Table[58]	69		
Dem_DTC_FTB_Table[59]	53		
Dem_DTC_FTB_Table[60]	69		
Dem_DTC_FTB_Table[61]	30		
Dem DTC FTB Table[62]	120		
Dem_DTC_FTB_Table[63]	148		
Dem DTC FTB Table[64]	120		
Dem DTC FTB Table[65]	135		
Dem_DTC_FTB_Table[66]	193		
Dem_DTC_FTB_Table[67]	69		
Dem_DTC_FTB_Table[68]	69		
Dem_DTC_FTB_Table[69]	30		
Dem_DTC_FTB_Table[70]	120		
Dem_DTC_FTB_Table[71]	53		
Dem_DTC_FTB_Table[72]	120		
Dem_DTC_FTB_Table[73]	148		
Dem_DTC_FTB_Table[74]	120		
Dem_DTC_FTB_Table[75]	135		
Dem_DTC_FTB_Table[76]	193		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	~
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_Igc[12] CTCFailedBuf_Cnt_M_Igc[13]	1	1	
CTCFailedBuf_Cnt_M_lgc[14]	1	1	
CTCFailedBuf_Cnt_M_lgc[15]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[18]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<u> </u>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	~
CTCFailedBuf_Cnt_M_lgc[25]	1	1	
CTCFailedBuf_Cnt_M_lgc[26] CTCFailedBuf_Cnt_M_lgc[27]	1	1	
CTCFailedBuf_Cnt_M_lgc[28]	1	1	
CTCFailedBuf_Cnt_M_lgc[29]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[30]	1	1	
CTCFailedBuf_Cnt_M_lgc[31]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40]	0	0	
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	0	0	
CTCFailedBuf_Cnt_M_lgc[42]	0	0	·
CTCFailedBuf_Cnt_M_lgc[44]	0	0	
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[46]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[49]	0	0	~
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[51]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53] CTCFailedBuf_Cnt_M_lgc[54]	1	1	
CTCFailedBuf_Cnt_M_lgc[55]	1	1	
CTCFailedBuf_Cnt_M_lgc[56]	1	1	
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[60]	0	0	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[67] CTCFailedBuf_Cnt_M_lgc[68]	0	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	0	_
CTCFailedBuf_Cnt_M_lgc[70]	0	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	•
CTCFailed_Cnt_M_lgc	0	0	~
Demlf_DTCStatusChanged()	0	0	<b>~</b>
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✓



Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt Igc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	-

Total Std Dr. 200 (Repeat Count = 1)		
COTAMISMO, COM, Majority  COTAMISMO, COM, Ma	Test Step 2.20 (Repeat Count = 1)	<b>✓</b>
COTABIOSUL ON M [022]  COTABIOSUL ON M [022]  COTABIOSUL ON M [023]		•
CTCR-selbal, Crit. M, 1902  1 CTCR-selbal, Crit. M, 1904  1 CTCR-s		
CCFanished, Col. M. 1903    1		
CCFCareach, Cot M, 1958 1 CCFCareach, Cot M, 1958 1 CCFCareach, Cot M, 1959 1 CCFCareach, Cot M,		
CFG-Biaseld Col. M. 1985    1   1   1   1   1   1   1   1   1		
CICFainabilla (Cat M, 1978) 1 CICFainabilla (Cat M, 1971) 1 CICFainabilla (Cat M, 1972) 1 CICFainabilla (Cat M, 1973) 1 CICFainabilla (Cat M, 1973) 1 CICFainabilla (Cat M, 1973) 1 CICFainabilla (Cat M, 1974) 1 CICFai		
CICTaleadid, Cim, My, 1987		1
CCCFailandian, Com, M, Mg49    1	CTCFailedBuf_Cnt_M_lgc[7]	1
CICFaiedby Citt, M. jord 1  CICFaiedby Citt, M. jord 2  CICFaiedby Citt, M. jord 2  CICFaiedby Citt, M. jord 2  CICFaiedby Citt, M. jord 3  CICFaiedby Citt, M. jord 4  CICFaiedby Citt, M. jord 4  CICFaiedby Citt, M. jord 9  CI	CTCFailedBuf_Cnt_M_lgc[8]	
CCTRAINSUL COL M. 19513  CTCTANESUL COL M. 19513  CTCTANESUL COL M. 19513  CTCTANESUL COL M. 19513  CTCTANESUL COL M. 19515  CTCTANESUL COL M. 19517  CTCTANESUL COL M. 19512  TCTCTANESUL COL M. 19513  TCTCTANESUL COL		
CTCFalesBull Cost M Mgd19  CTCFalesBull Cost M Mgd29  CTCFalesBull Cost M M		
CICFaleadBuf Cett, M. jog/13   1   1   1   1   1   1   1   1   1		
CICFaleadedy Cort M. Jogf19		
CCFCaladed Cort   M. pdf 19		
CICFORIAGEMED, CM, Major 19 CI		
CICFaiedBuff_CR_M_log(18) 1 CICFaiedBuf_CR_M_log(18) 1 CICFaiedBuf_CR_M_log(19) 1 CICFaiedBuf_CR_M_log(20) 0 CICFaiedBuf_CR_M_log(20) 0 CICFaiedBuf_CR_M_log(20) 1 CICFaiedBuf_CR_M_log(20) 0 CICFaiedBuf_CR_M_log		
CICPaiedBuf, Crt, M. Jgd(18) CICPaiedBuf, Crt, M. Jgd(20) CICPaiedBuf, Crt		
CTCFaledBuf_CR_M_log20	CTCFailedBuf_Cnt_M_lgc[18]	1
CICFairedBuf_Cnt_M_gq22]  O CTGFairedBuf_Cnt_M_gq22]  O CTGFairedBuf_Cnt_M_gq24]  O CTGFairedBuf_Cnt_M_gq24]  O CTGFairedBuf_Cnt_M_gq24]  O CTGFairedBuf_Cnt_M_gq24]  O CTGFairedBuf_Cnt_M_gq28]  O CTGFairedBuf_Cnt_M_gq38]  O CTGFairedBuf_Cnt_M_gq48]  O CTGFairedBuf_Cnt_M_gq58]		
CICFaiedBuf, Cnt, M, 19c223 CICFaiedBuf, Cnt, M, 19c224 CICFaiedBuf, Cnt, M, 19c255 CICFaiedBuf, Cnt, M, 19c255 CICFaiedBuf, Cnt, M, 19c255 CICFaiedBuf, Cnt, M, 19c269 CICFaiedBuf, Cnt, M, 19c277 CICFaiedBuf, Cnt, M, 19c277 CICFaiedBuf, Cnt, M, 19c293 CICFaiedBuf, Cnt, M, 19c293 CICFaiedBuf, Cnt, M, 19c293 CICFaiedBuf, Cnt, M, 19c203 CICFaiedBuf, Cnt, M, 19c204 CICFaiedBuf, Cnt, M, 19c204 CICFaiedBuf, Cnt, M, 19c203 CI		
CTCFailedBut_Cnt_M_gd23    TCTFailedBut_Cnt_M_gd24    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd28    TCTFailedBut_Cnt_M_gd30    TCTFailedBut_Cnt_M_gd31    TCTFailedBut_Cnt_M_gd31    TCTFailedBut_Cnt_M_gd31    TCTFailedBut_Cnt_M_gd31    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd33    TCTFailedBut_Cnt_M_gd34    TCTFailedBut_Cnt_M_gd34    TCTFailedBut_Cnt_M_gd34    TCTFailedBut_Cnt_M_gd34    TCTFailedBut_Cnt_M_gd34    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd44    TCTFailedBut_Cnt_M_gd46    TCTFailedBut_Cnt_M_gd46    TCTFailedBut_Cnt_M_gd46    TCTFailedBut_Cnt_M_gd48    TCTFailedBut_Cnt_M_gd68    TCTFAIledBut_Cnt_M_		
CTCFailedBuf_Cnt_M_gct24]  CTCFailedBuf_Cnt_M_gct26]  CTCFailedBuf_Cnt_M_gct27]  CTCFailedBuf_Cnt_M_gct27]  CTCFailedBuf_Cnt_M_gct28]  CTCFailedBuf_Cnt_M_gct28]  CTCFailedBuf_Cnt_M_gct28]  CTCFailedBuf_Cnt_M_gct28]  CTCFailedBuf_Cnt_M_gct28]  CTCFailedBuf_Cnt_M_gct31]  CTCFailedBuf_Cnt_M_gct31]  CTCFailedBuf_Cnt_M_gct31]  CTCFailedBuf_Cnt_M_gct33]  CTCFailedBuf_Cnt_M_gct33]  CTCFailedBuf_Cnt_M_gct34]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct38]  CTCFailedBuf_Cnt_M_gct48]  CTCFailedBuf_Cnt_M_gct69]		
CTCFailedBuf_Crt_M_lgct28] 1 CTCFailedBuf_Crt_M_lgct28] 1 CTCFailedBuf_Crt_M_lgct28] 1 CTCFailedBuf_Crt_M_lgct28] 1 CTCFailedBuf_Crt_M_lgct28] 1 CTCFailedBuf_Crt_M_lgct30] 1 CTCFailedBuf_Crt_M_lgct30] 1 CTCFailedBuf_Crt_M_lgct31] 1 CTCFailedBuf_Crt_M_lgct31] 1 CTCFailedBuf_Crt_M_lgct33] 1 CTCFailedBuf_Crt_M_lgct33] 1 CTCFailedBuf_Crt_M_lgct33] 1 CTCFailedBuf_Crt_M_lgct33] 1 CTCFailedBuf_Crt_M_lgct38] 0 CTCFailedBuf_Crt_M_lgct48] 1 CTCFailedBuf_Crt_M_lgct58] 1 CTCFailedBuf_Crt		
CTCFailedBuf, Cnt, M, Jgc(28) 1 CTCFailedBuf, Cnt, M, Jgc(30) 1 CTCFailedBuf, Cnt, M, Jgc(31) 1 CTCFailedBuf, Cnt, M, Jgc(31) 1 CTCFailedBuf, Cnt, M, Jgc(32) 1 CTCFailedBuf, Cnt, M, Jgc(33) 1 CTCFailedBuf, Cnt, M, Jgc(33) 1 CTCFailedBuf, Cnt, M, Jgc(38) 1 CTCFailedBuf, Cnt, M, Jgc(48) 1 CTCFailedBuf, Cnt, M, Jgc(58) 1 CTCFailedBuf, Cnt, M, Jgc(59) 1		
CTCFailedBuf, Cnt, M, Jgc(28) 1 CTCFailedBuf, Cnt, M, Jgc(28) 1 CTCFailedBuf, Cnt, M, Jgc(30) 1 CTCFailedBuf, Cnt, M, Jgc(30) 1 CTCFailedBuf, Cnt, M, Jgc(31) 1 CTCFailedBuf, Cnt, M, Jgc(31) 1 CTCFailedBuf, Cnt, M, Jgc(32) 1 CTCFailedBuf, Cnt, M, Jgc(33) 1 CTCFailedBuf, Cnt, M, Jgc(33) 1 CTCFailedBuf, Cnt, M, Jgc(34) 0 CTCFailedBuf, Cnt, M, Jgc(38) 0 CTCFailedBuf, Cnt, M, Jgc(40) 0 CTCFailedBuf, Cnt, M, Jgc(40) 0 CTCFailedBuf, Cnt, M, Jgc(44) 0 CTCFailedBuf, Cnt, M, Jgc(44) 0 CTCFailedBuf, Cnt, M, Jgc(48) 0 CTCFailedBuf, Cnt, M, Jgc(58) 1		
CTCFailedBuf_Cnt_M_lgct28		
CTCFailedBuf_Cnt_M_lgc(30)         1           CTCFailedBuf_Cnt_M_lgc(32)         1           CTCFailedBuf_Cnt_M_lgc(33)         1           CTCFailedBuf_Cnt_M_lgc(34)         0           CTCFailedBuf_Cnt_M_lgc(34)         0           CTCFailedBuf_Cnt_M_lgc(36)         0           CTCFailedBuf_Cnt_M_lgc(37)         0           CTCFailedBuf_Cnt_M_lgc(38)         0           CTCFailedBuf_Cnt_M_lgc(38)         0           CTCFailedBuf_Cnt_M_lgc(40)         0           CTCFailedBuf_Cnt_M_lgc(41)         0           CTCFailedBuf_Cnt_M_lgc(42)         0           CTCFailedBuf_Cnt_M_lgc(43)         0           CTCFailedBuf_Cnt_M_lgc(44)         0           CTCFailedBuf_Cnt_M_lgc(46)         0           CTCFailedBuf_Cnt_M_lgc(46)         0           CTCFailedBuf_Cnt_M_lgc(46)         0           CTCFailedBuf_Cnt_M_lgc(46)         0           CTCFailedBuf_Cnt_M_lgc(47)         0           CTCFailedBuf_Cnt_M_lgc(48)         0           CTCFailedBuf_Cnt_M_lgc(50)         0           CTCFailedBuf_Cnt_M_lgc(50)         0           CTCFailedBuf_Cnt_M_lgc(50)         1           CTCFailedBuf_Cnt_M_lgc(51)         1           CTCFailedBuf_Cnt_M_lgc(50)         1		
CTCFailedBuf_Cnt_M_lgcj31         1           CTCFailedBuf_Cnt_M_lgcj32         1           CTCFailedBuf_Cnt_M_lgcj33         1           CTCFailedBuf_Cnt_M_lgcj33         0           CTCFailedBuf_Cnt_M_lgcj35         0           CTCFailedBuf_Cnt_M_lgcj36         0           CTCFailedBuf_Cnt_M_lgcj37         0           CTCFailedBuf_Cnt_M_lgcj38         0           CTCFailedBuf_Cnt_M_lgcj39         0           CTCFailedBuf_Cnt_M_lgcj40         0           CTCFailedBuf_Cnt_M_lgcj41         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj53         1           CTCFailedBuf_Cnt_M_lgcj63         1 <t< td=""><td>CTCFailedBuf_Cnt_M_lgc[29]</td><td>1</td></t<>	CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgcj32]         1           CTCFailedBuf_Cnt_M_lgcj33]         1           CTCFailedBuf_Cnt_M_lgcj34]         0           CTCFailedBuf_Cnt_M_lgcj35]         0           CTCFailedBuf_Cnt_M_lgcj37]         0           CTCFailedBuf_Cnt_M_lgcj37]         0           CTCFailedBuf_Cnt_M_lgcj38]         0           CTCFailedBuf_Cnt_M_lgcj40]         0           CTCFailedBuf_Cnt_M_lgcj40]         0           CTCFailedBuf_Cnt_M_lgcj41]         0           CTCFailedBuf_Cnt_M_lgcj43]         0           CTCFailedBuf_Cnt_M_lgcj43]         0           CTCFailedBuf_Cnt_M_lgcj43]         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj44         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj54         0           CTCFailedBuf_Cnt_M_lgcj54         0           CTCFailedBuf_Cnt_M_lgcj54         1           CTCFailedBuf_Cnt_M_lgcj54         1 <t< td=""><td>CTCFailedBuf_Cnt_M_lgc[30]</td><td>1</td></t<>	CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgcj33         1           CTCFailedBuf_Cnt_M_lgcj35         0           CTCFailedBuf_Cnt_M_lgcj35         0           CTCFailedBuf_Cnt_M_lgcj36         0           CTCFailedBuf_Cnt_M_lgcj38         0           CTCFailedBuf_Cnt_M_lgcj38         0           CTCFailedBuf_Cnt_M_lgcj40         0           CTCFailedBuf_Cnt_M_lgcj41         0           CTCFailedBuf_Cnt_M_lgcj41         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj43         0           CTCFailedBuf_Cnt_M_lgcj44         0           CTCFailedBuf_Cnt_M_lgcj45         0           CTCFailedBuf_Cnt_M_lgcj46         0           CTCFailedBuf_Cnt_M_lgcj48         0           CTCFailedBuf_Cnt_M_lgcj49         0           CTCFailedBuf_Cnt_M_lgcj49         0           CTCFailedBuf_Cnt_M_lgcj49         0           CTCFailedBuf_Cnt_M_lgcj50         0           CTCFailedBuf_Cnt_M_lgcj51         0           CTCFailedBuf_Cnt_M_lgcj52         0           CTCFailedBuf_Cnt_M_lgcj53         1           CTCFailedBuf_Cnt_M_lgcj50         1           CTCFailedBuf_Cnt_M_lgcj56         1           CTCFailedBuf_Cnt_M_lgcj58         1 <t< td=""><td>CTCFailedBuf_Cnt_M_lgc[31]</td><td></td></t<>	CTCFailedBuf_Cnt_M_lgc[31]	
CTCFailedBuf_Cnt_M_lgq34         0           CTCFailedBuf_Cnt_M_lgq35         0           CTCFailedBuf_Cnt_M_lgq37         0           CTCFailedBuf_Cnt_M_lgq37         0           CTCFailedBuf_Cnt_M_lgq39         0           CTCFailedBuf_Cnt_M_lgq40         0           CTCFailedBuf_Cnt_M_lgq41         0           CTCFailedBuf_Cnt_M_lgq42         0           CTCFailedBuf_Cnt_M_lgq43         0           CTCFailedBuf_Cnt_M_lgq43         0           CTCFailedBuf_Cnt_M_lgq43         0           CTCFailedBuf_Cnt_M_lgq44         0           CTCFailedBuf_Cnt_M_lgq46         0           CTCFailedBuf_Cnt_M_lgq46         0           CTCFailedBuf_Cnt_M_lgq48         0           CTCFailedBuf_Cnt_M_lgq49         0           CTCFailedBuf_Cnt_M_lgq49         0           CTCFailedBuf_Cnt_M_lgq50         0           CTCFailedBuf_Cnt_M_lgq53         1           CTCFailedBuf_Cnt_M_lgq53         1           CTCFailedBuf_Cnt_M_lgq55         1           CTCFailedBuf_Cnt_M_lgq56         1           CTCFailedBuf_Cnt_M_lgq56         1           CTCFailedBuf_Cnt_M_lgq56         1           CTCFailedBuf_Cnt_M_lgq56         1           CTCFailedBuf_Cnt_M_lgq5		
CTCFailedBuf_Cnl_M]gc[35]         0           CTCFailedBuf_Cnl_M]gc[37]         0           CTCFailedBuf_Cnl_M]gc[38]         0           CTCFailedBuf_Cnl_M]gc[38]         0           CTCFailedBuf_Cnl_M]gc[40]         0           CTCFailedBuf_Cnl_M]gc[41]         0           CTCFailedBuf_Cnl_M]gc[42]         0           CTCFailedBuf_Cnl_M]gc[43]         0           CTCFailedBuf_Cnl_M]gc[44]         0           CTCFailedBuf_Cnl_M]gc[44]         0           CTCFailedBuf_Cnl_M]gc[45]         0           CTCFailedBuf_Cnl_M]gc[47]         0           CTCFailedBuf_Cnl_M_gc[47]         0           CTCFailedBuf_Cnl_M_gc[48]         1           CTCFailedBuf_Cnl_M_gc[48]         1           CTCFailedBuf_Cnl_M_gc[48]         1           CTCFailedBuf_Cnl_M_gc[48]         1           CTCFailedBuf_Cnl_M_gc[48]         1           CTCFailedBuf_Cnl_M_gc[48]         1 <t< td=""><td></td><td></td></t<>		
CTCFailedBuf_Cnt_M_lgc[38]         0           CTCFailedBuf_Cnt_M_lgc[38]         0           CTCFailedBuf_Cnt_M_lgc[38]         0           CTCFailedBuf_Cnt_M_lgc[38]         0           CTCFailedBuf_Cnt_M_lgc[41]         0           CTCFailedBuf_Cnt_M_lgc[42]         0           CTCFailedBuf_Cnt_M_lgc[42]         0           CTCFailedBuf_Cnt_M_lgc[44]         0           CTCFailedBuf_Cnt_M_lgc[44]         0           CTCFailedBuf_Cnt_M_lgc[48]         0           CTCFailedBuf_Cnt_M_lgc[48]         0           CTCFailedBuf_Cnt_M_lgc[48]         0           CTCFailedBuf_Cnt_M_lgc[49]         0           CTCFailedBuf_Cnt_M_lgc[49]         0           CTCFailedBuf_Cnt_M_lgc[51]         0           CTCFailedBuf_Cnt_M_lgc[52]         0           CTCFailedBuf_Cnt_M_lgc[52]         1           CTCFailedBuf_Cnt_M_lgc[53]         1		
CTCFailedBuf_Cnt_M_lgcl371         0           CTCFailedBuf_Cnt_M_lgcl391         0           CTCFailedBuf_Cnt_M_lgcl401         0           CTCFailedBuf_Cnt_M_lgcl401         0           CTCFailedBuf_Cnt_M_lgcl411         0           CTCFailedBuf_Cnt_M_lgcl431         0           CTCFailedBuf_Cnt_M_lgcl431         0           CTCFailedBuf_Cnt_M_lgcl441         0           CTCFailedBuf_Cnt_M_lgcl461         0           CTCFailedBuf_Cnt_M_lgcl461         0           CTCFailedBuf_Cnt_M_lgcl481         0           CTCFailedBuf_Cnt_M_lgcl481         0           CTCFailedBuf_Cnt_M_lgcl481         0           CTCFailedBuf_Cnt_M_lgcl501         0           CTCFailedBuf_Cnt_M_lgcl501         0           CTCFailedBuf_Cnt_M_lgcl501         0           CTCFailedBuf_Cnt_M_lgcl501         0           CTCFailedBuf_Cnt_M_lgcl501         1           CTCFailedBuf_Cnt_M_lgcl601         1		
CTCFailedBuf_Cmt_M_lgc[38]         0           CTCFailedBuf_Cmt_M_lgc[40]         0           CTCFailedBuf_Cmt_M_lgc[41]         0           CTCFailedBuf_Cmt_M_lgc[42]         0           CTCFailedBuf_Cmt_M_lgc[43]         0           CTCFailedBuf_Cmt_M_lgc[44]         0           CTCFailedBuf_Cmt_M_lgc[44]         0           CTCFailedBuf_Cmt_M_lgc[48]         0           CTCFailedBuf_Cmt_M_lgc[48]         0           CTCFailedBuf_Cmt_M_lgc[48]         0           CTCFailedBuf_Cmt_M_lgc[48]         0           CTCFailedBuf_Cmt_M_lgc[48]         0           CTCFailedBuf_Cmt_M_lgc[49]         0           CTCFailedBuf_Cmt_M_lgc[50]         0           CTCFailedBuf_Cmt_M_lgc[51]         0           CTCFailedBuf_Cmt_M_lgc[52]         0           CTCFailedBuf_Cmt_M_lgc[53]         1           CTCFailedBuf_Cmt_M_lgc[54]         1           CTCFailedBuf_Cmt_M_lgc[56]         1           CTCFailedBuf_Cmt_M_lgc[56]         1           CTCFailedBuf_Cmt_M_lgc[58]         1           CTCFailedBuf_Cmt_M_lgc[66]         1           CTCFailedBuf_Cmt_M_lgc[60]         1           CTCFailedBuf_Cmt_M_lgc[60]         1           CTCFailedBuf_Cmt_M_lgc[60]         1		
CTCFailedBut_Cnt_M_lgc[40]         0           CTCFailedBut_Cnt_M_lgc[41]         0           CTCFailedBut_Cnt_M_lgc[42]         0           CTCFailedBut_Cnt_M_lgc[42]         0           CTCFailedBut_Cnt_M_lgc[43]         0           CTCFailedBut_Cnt_M_lgc[44]         0           CTCFailedBut_Cnt_M_lgc[45]         0           CTCFailedBut_Cnt_M_lgc[46]         0           CTCFailedBut_Cnt_M_lgc[47]         0           CTCFailedBut_Cnt_M_lgc[48]         0           CTCFailedBut_Cnt_M_lgc[49]         0           CTCFailedBut_Cnt_M_lgc[50]         0           CTCFailedBut_Cnt_M_lgc[50]         0           CTCFailedBut_Cnt_M_lgc[51]         0           CTCFailedBut_Cnt_M_lgc[52]         0           CTCFailedBut_Cnt_M_lgc[53]         1           CTCFailedBut_Cnt_M_lgc[54]         1           CTCFailedBut_Cnt_M_lgc[55]         1           CTCFailedBut_Cnt_M_lgc[56]         1           CTCFailedBut_Cnt_M_lgc[57]         1           CTCFailedBut_Cnt_M_lgc[58]         1           CTCFailedBut_Cnt_M_lgc[67]         1           CTCFailedBut_Cnt_M_lgc[60]         1           CTCFailedBut_Cnt_M_lgc[60]         1           CTCFailedBut_Cnt_M_lgc[60]         1		
CTCFailedBuf_Cnt_M_lgc[41]       0         CTCFailedBuf_Cnt_M_lgc[42]       0         CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[69]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		0
CTCFailedBuf_Cnt_M_lgc[42]       0         CTCFailedBuf_Cnt_M_lgc[43]       0         CTCFailedBuf_Cnt_M_lgc[44]       0         CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[68]       1 <td>CTCFailedBuf_Cnt_M_lgc[40]</td> <td>0</td>	CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[43] 0 CTCFailedBuf_Cnt_M_lgc[44] 0 CTCFailedBuf_Cnt_M_lgc[45] 0 CTCFailedBuf_Cnt_M_lgc[46] 0 CTCFailedBuf_Cnt_M_lgc[47] 0 CTCFailedBuf_Cnt_M_lgc[48] 0 CTCFailedBuf_Cnt_M_lgc[48] 0 CTCFailedBuf_Cnt_M_lgc[48] 0 CTCFailedBuf_Cnt_M_lgc[49] 0 CTCFailedBuf_Cnt_M_lgc[50] 0 CTCFailedBuf_Cnt_M_lgc[50] 0 CTCFailedBuf_Cnt_M_lgc[50] 1 CTCFailedBuf_Cnt_M_lgc[51] 1 CTCFailedBuf_Cnt_M_lgc[52] 1 CTCFailedBuf_Cnt_M_lgc[53] 1 CTCFailedBuf_Cnt_M_lgc[53] 1 CTCFailedBuf_Cnt_M_lgc[56] 1 CTCFailedBuf_Cnt_M_lgc[56] 1 CTCFailedBuf_Cnt_M_lgc[56] 1 CTCFailedBuf_Cnt_M_lgc[56] 1 CTCFailedBuf_Cnt_M_lgc[56] 1 CTCFailedBuf_Cnt_M_lgc[58] 1 CTCFailedBuf_Cnt_M_lgc[58] 1 CTCFailedBuf_Cnt_M_lgc[58] 1 CTCFailedBuf_Cnt_M_lgc[60] 1 CTCFailedBuf_Cnt_M_lgc[60] 1 CTCFailedBuf_Cnt_M_lgc[60] 1 CTCFailedBuf_Cnt_M_lgc[60] 1 CTCFailedBuf_Cnt_M_lgc[60] 1 CTCFailedBuf_Cnt_M_lgc[60] 1	CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[44]         0           CTCFailedBuf_Cnt_M_lgc[45]         0           CTCFailedBuf_Cnt_M_lgc[47]         0           CTCFailedBuf_Cnt_M_lgc[48]         0           CTCFailedBuf_Cnt_M_lgc[48]         0           CTCFailedBuf_Cnt_M_lgc[49]         0           CTCFailedBuf_Cnt_M_lgc[50]         0           CTCFailedBuf_Cnt_M_lgc[51]         0           CTCFailedBuf_Cnt_M_lgc[52]         0           CTCFailedBuf_Cnt_M_lgc[53]         1           CTCFailedBuf_Cnt_M_lgc[53]         1           CTCFailedBuf_Cnt_M_lgc[56]         1           CTCFailedBuf_Cnt_M_lgc[56]         1           CTCFailedBuf_Cnt_M_lgc[56]         1           CTCFailedBuf_Cnt_M_lgc[58]         1           CTCFailedBuf_Cnt_M_lgc[58]         1           CTCFailedBuf_Cnt_M_lgc[58]         1           CTCFailedBuf_Cnt_M_lgc[58]         1           CTCFailedBuf_Cnt_M_lgc[68]         1           CTCFailedBuf_Cnt_M_lgc[68]         1           CTCFailedBuf_Cnt_M_lgc[68]         1           CTCFailedBuf_Cnt_M_lgc[61]         1           CTCFailedBuf_Cnt_M_lgc[61]         1           CTCFailedBuf_Cnt_M_lgc[61]         1		i a constant a constan
CTCFailedBuf_Cnt_M_lgc[45]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[46]       0         CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[47]       0         CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1		
CTCFailedBuf_Cnt_M_lgc[48]       0         CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[49]       0         CTCFailedBuf_Cnt_M_lgc[50]       0         CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[51]       0         CTCFailedBuf_Cnt_M_lgc[52]       0         CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[53]       1         CTCFailedBuf_Cnt_M_lgc[54]       1         CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		0
CTCFailedBuf_Cnt_M_igc[54]       1         CTCFailedBuf_Cnt_M_igc[55]       1         CTCFailedBuf_Cnt_M_igc[56]       1         CTCFailedBuf_Cnt_M_igc[57]       1         CTCFailedBuf_Cnt_M_igc[58]       1         CTCFailedBuf_Cnt_M_igc[69]       1         CTCFailedBuf_Cnt_M_igc[60]       1         CTCFailedBuf_Cnt_M_igc[61]       1         CTCFailedBuf_Cnt_M_igc[62]       1		
CTCFailedBuf_Cnt_M_lgc[55]       1         CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[56]       1         CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[57]       1         CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[58]       1         CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[59]       1         CTCFailedBuf_Cnt_M_lgc[60]       1         CTCFailedBuf_Cnt_M_lgc[61]       1         CTCFailedBuf_Cnt_M_lgc[62]       1		
CTCFailedBuf_Cnt_M_lgc[60]         1           CTCFailedBuf_Cnt_M_lgc[61]         1           CTCFailedBuf_Cnt_M_lgc[62]         1		
CTCFailedBuf_Cnt_M_lgc[61]         1           CTCFailedBuf_Cnt_M_lgc[62]         1		
CTCFailedBuf_Cnt_M_lgc[62] 1		
CTCFailedBuf_Cnt_M_lgc[63] 1		
	CTCFailedBuf_Cnt_M_lgc[63]	1

Demlf\_DTCStatusChanged

2018-04-10, 18:44:44+0530



Input Value CTCFailedBuf\_Cnt\_M\_lgc[64] CTCFailedBuf\_Cnt\_M\_lgc[65] 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 CTCFailedBuf Cnt M lqc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 1 DTC 4137755052 DTCKind 2 DTCStatusNew 250 DTCStatusOld 202 Dem\_DTCNumberTable[0] 65535 Dem\_DTCNumberTable[1] 65535 Dem\_DTCNumberTable[2] 65535 Dem\_DTCNumberTable[3] 65535 Dem\_DTCNumberTable[4] 65535 Dem\_DTCNumberTable[5] 65535 Dem DTCNumberTable[6] 65535 Dem\_DTCNumberTable[7] 65535 Dem DTCNumberTable[8] 65535 Dem\_DTCNumberTable[9] 65535 Dem DTCNumberTable[10] 65535 Dem\_DTCNumberTable[11] 65535 Dem DTCNumberTable[12] 65535 Dem\_DTCNumberTable[13] 65535 Dem DTCNumberTable[14] 65535 Dem\_DTCNumberTable[15] 65535 Dem\_DTCNumberTable[16] 65535 Dem\_DTCNumberTable[17] 65535 Dem\_DTCNumberTable[18] 65535 Dem\_DTCNumberTable[19] 65535 Dem\_DTCNumberTable[20] 65535 Dem\_DTCNumberTable[21] 65535 Dem\_DTCNumberTable[22] 65535 Dem\_DTCNumberTable[23] 65535 Dem\_DTCNumberTable[24] 65535 Dem\_DTCNumberTable[25] 65535 Dem\_DTCNumberTable[26] 65535 Dem\_DTCNumberTable[27] 65535 Dem DTCNumberTable[28] 65535 Dem\_DTCNumberTable[29] 65535 Dem DTCNumberTable[30] 65535 Dem\_DTCNumberTable[31] 65535 Dem DTCNumberTable[32] 65535 Dem\_DTCNumberTable[33] 65535 Dem\_DTCNumberTable[34] 65535 Dem\_DTCNumberTable[35] 65535 Dem\_DTCNumberTable[36] 65535 Dem\_DTCNumberTable[37] 65535 Dem\_DTCNumberTable[38] 65535 Dem\_DTCNumberTable[39] 65535 Dem\_DTCNumberTable[40] 65535 Dem\_DTCNumberTable[41] 65535 Dem\_DTCNumberTable[42] 65535 65535 Dem\_DTCNumberTable[43] Dem\_DTCNumberTable[44] 65535 Dem\_DTCNumberTable[45] 65535 Dem\_DTCNumberTable[46] 65535 Dem DTCNumberTable[47] 65535 Dem\_DTCNumberTable[48] 65535 Dem DTCNumberTable[49] 65535 Dem DTCNumberTable[50] 65535 Dem\_DTCNumberTable[51] 65535 Dem DTCNumberTable[52] 65535 Dem\_DTCNumberTable[53] 65535 Dem\_DTCNumberTable[54] 65535

2018-04-10, 18:44:44+0530



Denni_D1CStatusChangeu	- Talcitat
Name	Input Value
Dem_DTCNumberTable[55]	65535
Dem DTCNumberTable[56]	65535
Dem_DTCNumberTable[57]	65535
Dem_DTCNumberTable[58]	65535
Dem DTCNumberTable[59]	65535
Dem_DTCNumberTable[60]	65535
Dem_DTCNumberTable[61]	65535
	65535
Dem_DTCNumberTable[62]	
Dem_DTCNumberTable[63]	65535
Dem_DTCNumberTable[64]	65535
Dem_DTCNumberTable[65]	65535
Dem_DTCNumberTable[66]	65535
Dem_DTCNumberTable[67]	65535
Dem_DTCNumberTable[68]	65535
Dem_DTCNumberTable[69]	65535
Dem_DTCNumberTable[70]	65535
Dem_DTCNumberTable[71]	65535
Dem_DTCNumberTable[72]	65535
Dem_DTCNumberTable[73]	65535
Dem_DTCNumberTable[74]	65535
Dem_DTCNumberTable[75]	65535
Dem_DTCNumberTable[76]	65535
Dem_DTC_FTB_Table[0]	254
Dem_DTC_FTB_Table[1]	153
Dem_DTC_FTB_Table[2]	91
Dem_DTC_FTB_Table[3]	138
Dem_DTC_FTB_Table[4]	54
Dem_DTC_FTB_Table[5]	108
Dem_DTC_FTB_Table[6]	239
Dem_DTC_FTB_Table[7]	239
Dem_DTC_FTB_Table[8]	254
Dem_DTC_FTB_Table[9]	153
Dem_DTC_FTB_Table[10]	239
Dem_DTC_FTB_Table[11]	200
Dem_DTC_FTB_Table[11]	153
	239
Dem_DTC_FTB_Table[13] Dem_DTC_FTB_Table[14]	254
Dem_DTC_FTB_Table[15]	153
Dem_DTC_FTB_Table[16]	153
Dem_DTC_FTB_Table[17]	239
Dem_DTC_FTB_Table[18]	33
Dem_DTC_FTB_Table[19]	254
Dem_DTC_FTB_Table[20]	153
Dem_DTC_FTB_Table[21]	239
Dem_DTC_FTB_Table[22]	254
Dem_DTC_FTB_Table[23]	91
Dem_DTC_FTB_Table[24]	138
Dem_DTC_FTB_Table[25]	54
Dem_DTC_FTB_Table[26]	108
Dem_DTC_FTB_Table[27]	153
Dem_DTC_FTB_Table[28]	254
Dem_DTC_FTB_Table[29]	153
Dem_DTC_FTB_Table[30]	254
Dem_DTC_FTB_Table[31]	254
Dem_DTC_FTB_Table[32]	153
Dem_DTC_FTB_Table[33]	153
Dem_DTC_FTB_Table[34]	254
Dem_DTC_FTB_Table[35]	153
Dem_DTC_FTB_Table[36]	254
Dem_DTC_FTB_Table[37]	254
Dem_DTC_FTB_Table[38]	254
Dem_DTC_FTB_Table[39]	153
Dem_DTC_FTB_Table[49]	153
Dem_DTC_FTB_Table[40] Dem_DTC_FTB_Table[41]	91
Dem_DTC_FTB_Table[42]	138
Dem_DTC_FTB_Table[43]	54
Dem_DTC_FTB_Table[44]	108
Dem_DTC_FTB_Table[45]	239
Dem_DTC_FTB_Table[46]	254
Dem_DTC_FTB_Table[47]	153
Dem_DTC_FTB_Table[48]	138
	138 254

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	l		
Name	Input Value 254		
Dem_DTC_FTB_Table[51] Dem_DTC_FTB_Table[52]	254		
Dem_DTC_FTB_Table[53]	153		
Dem_DTC_FTB_Table[54]	138		
Dem_DTC_FTB_Table[55]	239		
Dem_DTC_FTB_Table[56]	254		
Dem_DTC_FTB_Table[57]	153		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59]	254 239		
Dem_DTC_FTB_Table[60]	259		
Dem_DTC_FTB_Table[61]	153		
Dem_DTC_FTB_Table[62]	138		
Dem_DTC_FTB_Table[63]	91		
Dem_DTC_FTB_Table[64]	138		
Dem_DTC_FTB_Table[65]	54		
Dem_DTC_FTB_Table[66]	108		
Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68]	254 254		
Dem_DTC_FTB_Table[69]	153		
Dem_DTC_FTB_Table[70]	138		
Dem_DTC_FTB_Table[71]	239		
Dem_DTC_FTB_Table[72]	138		
Dem_DTC_FTB_Table[73]	91		
Dem_DTC_FTB_Table[74]	138		
Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	54 108		
Name	Actual Value	Expected Value	Result
CTCFailedBuf Cnt M lgc[0]	1	1	result
CTCFailedBuf_Cnt_M_lgc[1]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	1	1	· · · · · ·
CTCFailedBuf_Cnt_M_lgc[8]	1	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[14] CTCFailedBuf_Cnt_M_lgc[15]	1	1	· · · · · ·
CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[21]	0	0	· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23]	0	1	
CTCFailedBuf Cnt M lgc[24]	1	1	
CTCFailedBuf_Cnt_M_lgc[25]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[29]	1	1	· ·
CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31]	1	1	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[33]	1	1	·
CTCFailedBuf_Cnt_M_lgc[34]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[38]	0	0	<b>Y</b>
CTCFailedBuf_Cnt_M_lgc[39] CTCFailedBuf_Cnt_M_lgc[40]	0	0	- Y
CTCFailedBuf_Cnt_M_lgc[40] CTCFailedBuf_Cnt_M_lgc[41]	0	0	
CTCFailedBuf_Cnt_M_lgc[42]	0	0	
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	<b>~</b>

Demlf\_DTCStatusChanged

CTCFailedBuf\_Cnt\_M\_lgc[74]

CTCFailedBuf\_Cnt\_M\_lgc[75]

CTCFailedBuf\_Cnt\_M\_lgc[76]

Demlf DTCStatusChanged()

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

CTCFailed\_Cnt\_M\_lgc

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**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] **> > > > >** CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[66]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	~

0

0

0

1

0

0

0

0

1

0

Test Step 2.21 (Repeat Count = 1)	🗸
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	0
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_Igc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_Igc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	1
	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	1
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf Cnt M Igc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	2969842604
DTCKind	1
DTCStatusNew	135
DTCStatusOld	53
Dem DTCNumberTable[0]	219
Dem_DTCNumberTable[1]	237
Dem_DTCNumberTable[1] Dem_DTCNumberTable[2]	46
Dem_DTCNumberTable[3]	187
Dem_DTCNumberTable[3] Dem_DTCNumberTable[4]	250
	36
Dem_DTCNumberTable[5]	
Dem_DTCNumberTable[6]	202 202
Dem_DTCNumberTable[7]	219
Dem_DTCNumberTable[8] Dem_DTCNumberTable[9]	237
Dem_DTCNumberTable[10]	202
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12]	126
	237
	202
Dem_DTCNumberTable[13]	202
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14]	219
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15]	219 237
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16]	219 237 237
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16] Dem_DTCNumberTable[17]	219 237 237 202
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14] Dem_DTCNumberTable[15] Dem_DTCNumberTable[16]	219 237 237

Demlf\_DTCStatusChanged

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		(
Name	Input Value	
Dem_DTCNumberTable[20]	237	
Dem_DTCNumberTable[21]	202	
Dem_DTCNumberTable[22]	219	
Dem_DTCNumberTable[23]	46	
Dem_DTCNumberTable[24]	187	
Dem_DTCNumberTable[25]	250	
Dem_DTCNumberTable[26]	36	
Dem_DTCNumberTable[27]	237	
Dem_DTCNumberTable[28]	219	
Dem_DTCNumberTable[29]	237	
Dem_DTCNumberTable[30]	219	
Dem_DTCNumberTable[31]	219	
Dem_DTCNumberTable[32]	237	
Dem_DTCNumberTable[33]	237	
Dem_DTCNumberTable[34]	219	
Dem_DTCNumberTable[35]	237	
Dem_DTCNumberTable[36]	219	
Dem_DTCNumberTable[37]	219	
Dem_DTCNumberTable[38]	219	
Dem_DTCNumberTable[39]	237	
Dem_DTCNumberTable[40]	237	
Dem_DTCNumberTable[41] Dem_DTCNumberTable[42]	46 187	
Dem_DTCNumberTable[42] Dem_DTCNumberTable[43]	250	
Dem_DTCNumberTable[43] Dem_DTCNumberTable[44]	36	
Dem_DTCNumberTable[45]	202	
Dem_DTCNumberTable[45]	219	
Dem DTCNumberTable[47]	237	
Dem_DTCNumberTable[48]	187	
Dem_DTCNumberTable[49]	219	
Dem_DTCNumberTable[50]	237	
Dem_DTCNumberTable[51]	219	
Dem_DTCNumberTable[52]	219	
Dem_DTCNumberTable[53]	237	
Dem_DTCNumberTable[54]	187	
Dem_DTCNumberTable[55]	202	
Dem_DTCNumberTable[56]	219	
Dem_DTCNumberTable[57]	237	
Dem_DTCNumberTable[58]	219	
Dem_DTCNumberTable[59]	202	
Dem_DTCNumberTable[60]	219	
Dem_DTCNumberTable[61]	237	
Dem_DTCNumberTable[62]	187	
Dem_DTCNumberTable[63]	46	
Dem_DTCNumberTable[64]	187	
Dem_DTCNumberTable[65]	250	
Dem_DTCNumberTable[66]	36	
Dem_DTCNumberTable[67]	219	
Dem_DTCNumberTable[68]	219	
Dem_DTCNumberTable[69]	237	
Dem_DTCNumberTable[70] Dem_DTCNumberTable[71]	187 202	
Dem DTCNumberTable[71]	187	
Dem_DTCNumberTable[72] Dem_DTCNumberTable[73]	46	
Dem_DTCNumberTable[73] Dem_DTCNumberTable[74]	187	
Dem_DTCNumberTable[74] Dem_DTCNumberTable[75]	250	
Dem_DTCNumberTable[75] Dem_DTCNumberTable[76]	36	
Dem_DTC_FTB_Table[0]	157	
Dem_DTC_FTB_Table[1]	1	
Dem_DTC_FTB_Table[2]	112	
Dem_DTC_FTB_Table[3]	195	
Dem_DTC_FTB_Table[4]	200	
Dem_DTC_FTB_Table[5]	99	
Dem_DTC_FTB_Table[6]	203	
Dem_DTC_FTB_Table[7]	203	
Dem_DTC_FTB_Table[8]	157	
Dem_DTC_FTB_Table[9]	1	
Dem_DTC_FTB_Table[10]	203	
Dem_DTC_FTB_Table[11]	201	
Dem_DTC_FTB_Table[12]	1	
Dem_DTC_FTB_Table[13]	203	
Dem_DTC_FTB_Table[14]	157	
Dem_DTC_FTB_Table[15]	1	

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Name	Input Value		
Dem_DTC_FTB_Table[16]	1		
Dem_DTC_FTB_Table[17]	203		
Dem_DTC_FTB_Table[18]	101		
Dem_DTC_FTB_Table[19]	157		
Dem_DTC_FTB_Table[20]	1		
Dem_DTC_FTB_Table[21]	203		
Dem_DTC_FTB_Table[22]	157		
Dem_DTC_FTB_Table[23]	112 195		
Dem_DTC_FTB_Table[24] Dem_DTC_FTB_Table[25]	200		
Dem_DTC_FTB_Table[26]	99		
Dem_DTC_FTB_Table[27]	1		
Dem_DTC_FTB_Table[28]	157		
Dem_DTC_FTB_Table[29]	1		
Dem_DTC_FTB_Table[30]	157		
Dem_DTC_FTB_Table[31]	157		
Dem_DTC_FTB_Table[32]	1		
Dem_DTC_FTB_Table[33]	1		
Dem_DTC_FTB_Table[34]	157		
Dem_DTC_FTB_Table[35]	1		
Dem_DTC_FTB_Table[36]	157		
Dem_DTC_FTB_Table[37]	157		
Dem_DTC_FTB_Table[38]	157		
Dem_DTC_FTB_Table[39] Dem_DTC_FTB_Table[40]	1		
Dem_DTC_FTB_Table[40] Dem_DTC_FTB_Table[41]	112		
Dem_DTC_FTB_Table[42]	195		
Dem_DTC_FTB_Table[43]	200		
Dem_DTC_FTB_Table[44]	99		
Dem_DTC_FTB_Table[45]	203		
Dem_DTC_FTB_Table[46]	157		
Dem_DTC_FTB_Table[47]	1		
Dem_DTC_FTB_Table[48]	195		
Dem_DTC_FTB_Table[49]	157		
Dem_DTC_FTB_Table[50]	1		
Dem_DTC_FTB_Table[51]	157		
Dem_DTC_FTB_Table[52]	157		
Dem_DTC_FTB_Table[53]	1		
Dem_DTC_FTB_Table[54] Dem_DTC_FTB_Table[55]	195 203		
Dem_DTC_FTB_Table[55]	157		
Dem_DTC_FTB_Table[57]	1		
Dem_DTC_FTB_Table[58]	157		
Dem_DTC_FTB_Table[59]	203		
Dem_DTC_FTB_Table[60]	157		
Dem_DTC_FTB_Table[61]	1		
Dem_DTC_FTB_Table[62]	195		
Dem_DTC_FTB_Table[63]	112		
Dem_DTC_FTB_Table[64]	195		
Dem_DTC_FTB_Table[65]	200		
Dem_DTC_FTB_Table[66]	99		
Dem_DTC_FTB_Table[67]	157 157		
Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69]	157		
Dem_DTC_FTB_Table[09]  Dem_DTC_FTB_Table[70]	195		
Dem_DTC_FTB_Table[70]	203		
Dem_DTC_FTB_Table[72]	195		
	112		
Dem_DTC_FTB_Table[73]			
Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74]	195		
	195 200		
Dem_DTC_FTB_Table[74]			
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name	200	Expected Value	Result
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	200 99 <b>Actual Value</b>	Expected Value	Result
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name	200 99 <b>Actual Value</b>	1 0	Result
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0]  CTCFailedBuf_Cnt_M_lgc[1]  CTCFailedBuf_Cnt_M_lgc[2]	200 99 <b>Actual Value</b> 1 0	1 0 1	<b>*</b>
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	200 99 <b>Actual Value</b> 1 0 1	1 0 1 1	\ \ \ \
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4]	200 99 <b>Actual Value</b> 1 0 1 1	1 0 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5]	200 99 <b>Actual Value</b> 1 0 1 1 1	1 0 1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[6]	200 99  Actual Value  1 0 1 1 1 1 1	1 0 1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	200 99  Actual Value  1 0 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	200 99  Actual Value  1 0 1 1 1 1 1 1 0	1 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	200 99  Actual Value  1 0 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·

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Name	Result
CTCFailedBuf_Cnt_M_lgc[13] 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[14]       1       1         CTCFailedBuf_Cnt_M_lgc[15]       1       1         CTCFailedBuf_Cnt_M_lgc[16]       1       1         CTCFailedBuf_Cnt_M_lgc[17]       1       1         CTCFailedBuf_Cnt_M_lgc[18]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_l	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[15] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[16]       1       1         CTCFailedBuf_Cnt_M_lgc[17]       1       1         CTCFailedBuf_Cnt_M_lgc[18]       1       1         CTCFailedBuf_Cnt_M_lgc[19]       1       1         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_l	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[17]       1       1         CTCFailedBuf_Cnt_M_lgc[18]       1       1         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_l	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[18]       1       1         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[20]       0       0         CTCFailedBuf_Cnt_M_lgc[21]       0       0         CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[22]       0       0         CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[23]       1       1         CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[24]       1       1         CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[25]       1       1         CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[26]       1       1         CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	> > > > > > > > > > > > > > > > > > >
CTCFailedBuf_Cnt_M_lgc[27]       1       1         CTCFailedBuf_Cnt_M_lgc[28]       1       1         CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[29]       1       1         CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	-
CTCFailedBuf_Cnt_M_lgc[30]       0       0         CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	· · · · · · · · · · · · · · · · · · ·
CTCFailedBuf_Cnt_M_lgc[31]       1       1         CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	~
CTCFailedBuf_Cnt_M_lgc[32]       1       1         CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	~
CTCFailedBuf_Cnt_M_lgc[33]       1       1         CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	<b>v</b>
CTCFailedBuf_Cnt_M_lgc[34]       0       0         CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	~
CTCFailedBuf_Cnt_M_lgc[35]       0       0         CTCFailedBuf_Cnt_M_lgc[36]       0       0         CTCFailedBuf_Cnt_M_lgc[37]       1       1	
CTCFailedBuf_Cnt_M_lgc[37] 1 1	✓
	~
CTCFailedBuf Cnt M lgc[38] 0 0	~
	~
CTCFailedBuf_Cnt_M_lgc(39) 0 0	~
CTCFailedBuf_Cnt_M_lgc[40]         0         0           CTCFailedBuf_Cnt_M_lgc[41]         0         0	
CTCFailedBuf_Cnt_M_lgc[42]	
CTCFailedBuf_Cnt_M_lgc[43] 0 0	_
CTCFailedBuf_Cnt_M_lgc[44] 0 0	~
CTCFailedBuf_Cnt_M_lgc[45] 0 0	~
CTCFailedBuf_Cnt_M_lgc[46] 0	~
CTCFailedBuf_Cnt_M_lgc[47] 0 0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[48]         0         0           CTCFailedBuf_Cnt_M_lgc[49]         0         0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[50] 0 0	
CTCFailedBuf_Cnt_M_lgc[51] 1 1	~
CTCFailedBuf_Cnt_M_lgc[52] 0 0	~
CTCFailedBuf_Cnt_M_lgc[53] 1 1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[54] 1 1	~
CTCFailedBuf_Cnt_M_lgc[55] 0	~
CTCFailedBuf_Cnt_M_lgc[56] 1 1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[57]       1       1         CTCFailedBuf_Cnt_M_lgc[58]       1       1	
CTCFailedBuf_Cnt_M_lgc[59] 1 1	·
CTCFailedBuf_Cnt_M_lgc[60] 1 1	_
CTCFailedBuf_Cnt_M_lgc[61] 1 1	✓
CTCFailedBuf_Cnt_M_lgc[62] 1 1	~
CTCFailedBuf_Cnt_M_lgc[63] 1 1	~
CTCFailedBuf_Cnt_M_lgc[64] 1 1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[65]         0         0           CTCFailedBuf_Cnt_M_lgc[66]         0         0	~
CTCFailedBuf_Cnt_M_lgc[66]         0         0           CTCFailedBuf_Cnt_M_lgc[67]         0         0	~
CTCFailedBuf_Cnt_M_lgc[68] 0 0	
CTCFailedBuf_Cnt_M_lgc[69] 0 0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70] 0 0	~
CTCFailedBuf_Cnt_M_lgc[71] 0 0	✓
CTCFailedBuf_Cnt_M_lgc[72] 0 0	<b>v</b>
CTCFailedBuf_Cnt_M_lgc[73] 0 0	<b>v</b>
CTCFailedBuf_Cnt_M_lgc[74]         0         0           CTCFailedBuf_Cnt_M_lgc[75]         0         0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[75]         0         0           CTCFailedBuf_Cnt_M_lgc[76]         0         0	
CTCFailed_Cnt_M_lgc 0 0	·
Demlf_DTCStatusChanged() 0 0	<b>~</b>
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data) 0	<b>✓</b>

Demlf\_DTCStatusChanged

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Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt Igc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	-

Test Step 2.22 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	
CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12] CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21] CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32] CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40] CTCFailedBuf Cnt M lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	1
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50] CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60] CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

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		Tazertat.
Name	Input Value	
CTCFailedBuf_Cnt_M_Igc[64]	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	
CTCFailedBuf_Cnt_M_lgc[66]	1	
CTCFailedBuf_Cnt_M_lgc[67]	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	
CTCFailedBuf_Cnt_M_lgc[70]	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	
CTCFailedBuf_Cnt_M_lgc[72]	0	
CTCFailedBuf_Cnt_M_lgc[73]	0	
CTCFailedBuf_Cnt_M_lgc[74]	0	
	0	
CTCFailedBuf_Cnt_M_lgc[75]		
CTCFailedBuf_Cnt_M_lgc[76]	0	
CTCFailed_Cnt_M_lgc	1	
DTC	598152539	
DTCKind	1	
DTCStatusNew	54	
DTCStatusOld	239	
Dem_DTCNumberTable[0]	69	
Dem_DTCNumberTable[1]	30	
Dem_DTCNumberTable[2]	148	
Dem_DTCNumberTable[3]	120	
Dem_DTCNumberTable[4]	135	
Dem_DTCNumberTable[5]	193	
Dem_DTCNumberTable[6]	53	
Dem_DTCNumberTable[7]	53	
Dem_DTCNumberTable[8]	69	
Dem_DTCNumberTable[9]	30	
Dem_DTCNumberTable[10]	53	
Dem_DTCNumberTable[11]	189	
Dem_DTCNumberTable[12]	30	
Dem_DTCNumberTable[13]	53	
Dem_DTCNumberTable[14]	69	
Dem_DTCNumberTable[15]	30	
Dem_DTCNumberTable[16]	30	
Dem_DTCNumberTable[17]	53	
Dem_DTCNumberTable[18]	127	
Dem_DTCNumberTable[19]	69	
Dem_DTCNumberTable[19] Dem_DTCNumberTable[20]	30	
Dem_DTCNumberTable[21]	53	
Dem_DTCNumberTable[22]	69	
Dem_DTCNumberTable[23]	148	
Dem_DTCNumberTable[24]	120	
Dem_DTCNumberTable[25]	135	
Dem_DTCNumberTable[26]	193	
Dem_DTCNumberTable[27]	30	
Dem_DTCNumberTable[28]	69	
Dem_DTCNumberTable[29]	30	
Dem_DTCNumberTable[30]	69	
Dem_DTCNumberTable[31]	69	
Dem_DTCNumberTable[32]	30	
Dem_DTCNumberTable[33]	30	
Dem_DTCNumberTable[34]	69	
Dem_DTCNumberTable[35]	30	
Dem_DTCNumberTable[36]	69	
Dem_DTCNumberTable[37]	69	
Dem DTCNumberTable[38]	69	
Dem_DTCNumberTable[39]	30	
Dem_DTCNumberTable[40]	30	
Dem_DTCNumberTable[40] Dem_DTCNumberTable[41]	148	
Dem_DTCNumberTable[41] Dem_DTCNumberTable[42]	120	
Dem_DTCNumberTable[42] Dem_DTCNumberTable[43]	135	
	193	
Dem_DTCNumberTable[44]		
Dem_DTCNumberTable[45]	53	
Dem_DTCNumberTable[46]	69	
Dem_DTCNumberTable[47]	30	
Dem_DTCNumberTable[48]	120	
Dem_DTCNumberTable[49]	69	
Dem_DTCNumberTable[50]	30	
Dem_DTCNumberTable[51]	69	
Dem_DTCNumberTable[52]	69	
Dem_DTCNumberTable[53]	30	
Dem_DTCNumberTable[54]	120	

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	(
Name	Input Value
Dem_DTCNumberTable[55]	53
Dem_DTCNumberTable[56]	69
Dem_DTCNumberTable[57]	30
Dem_DTCNumberTable[57] Dem_DTCNumberTable[58]	69
Dem_DTCNumberTable[59]	53
Dem_DTCNumberTable[60]	69
Dem_DTCNumberTable[61]	30
Dem_DTCNumberTable[62]	120
Dem_DTCNumberTable[63]	148
Dem_DTCNumberTable[64]	120
Dem_DTCNumberTable[65]	135
Dem_DTCNumberTable[66]	193
Dem_DTCNumberTable[67]	69
Dem_DTCNumberTable[68]	69
Dem_DTCNumberTable[69]	30
Dem_DTCNumberTable[70]	120
Dem_DTCNumberTable[71]	53
Dem_DTCNumberTable[72]	120
Dem_DTCNumberTable[73]	148
Dem_DTCNumberTable[74]	120
Dem_DTCNumberTable[75]	135
Dem_DTCNumberTable[76]	193
Dem_DTC_FTB_Table[0]	0
Dem_DTC_FTB_Table[1]	0
Dem_DTC_FTB_Table[2]	0
Dem_DTC_FTB_Table[3]	0
Dem_DTC_FTB_Table[4]	0
Dem DTC FTB Table[5]	0
Dem_DTC_FTB_Table[6]	0
Dem_DTC_FTB_Table[7]	0
Dem_DTC_FTB_Table[8]	0
Dem_DTC_FTB_Table[9]	0
Dem_DTC_FTB_Table[10]	0
Dem_DTC_FTB_Table[11]	0
Dem_DTC_FTB_Table[12]	0
	0
Dem_DTC_FTB_Table[13] Dem_DTC_FTB_Table[14]	0
	0
Dem_DTC_FTB_Table[15]	
Dem_DTC_FTB_Table[16]	0
Dem_DTC_FTB_Table[17]	0
Dem_DTC_FTB_Table[18]	0
Dem_DTC_FTB_Table[19]	0
Dem_DTC_FTB_Table[20]	0
Dem_DTC_FTB_Table[21]	0
Dem_DTC_FTB_Table[22]	0
Dem_DTC_FTB_Table[23]	0
Dem_DTC_FTB_Table[24]	0
Dem_DTC_FTB_Table[25]	0
Dem_DTC_FTB_Table[26]	0
Dem_DTC_FTB_Table[27]	0
Dem_DTC_FTB_Table[28]	0
Dem_DTC_FTB_Table[29]	0
Dem_DTC_FTB_Table[30]	0
Dem_DTC_FTB_Table[31]	0
Dem_DTC_FTB_Table[32]	0
Dem_DTC_FTB_Table[33]	0
Dem_DTC_FTB_Table[34]	0
Dem_DTC_FTB_Table[35]	0
Dem_DTC_FTB_Table[36]	0
Dem_DTC_FTB_Table[37]	0
Dem_DTC_FTB_Table[38]	0
Dem_DTC_FTB_Table[39]	0
Dem_DTC_FTB_Table[40]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[41]	0
Dem_DTC_FTB_Table[43]	0
Dem_DTC_FTB_Table[45] Dem_DTC_FTB_Table[44]	0
	0
Dem_DTC_FTB_Table[45]	Į <b>v</b>
Dam DTC FTD Table[46]	
Dem_DTC_FTB_Table[46]	0
Dem_DTC_FTB_Table[47]	0
Dem_DTC_FTB_Table[47] Dem_DTC_FTB_Table[48]	0
Dem_DTC_FTB_Table[47]	0

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Nome	Immut Value		
Name Dem_DTC_FTB_Table[51]	Input Value		
Dem_DTC_FTB_Table[51]	0		
Dem_DTC_FTB_Table[53]	0		
Dem_DTC_FTB_Table[54]	0		
Dem DTC FTB Table[55]	0		
Dem_DTC_FTB_Table[56]	0		
Dem_DTC_FTB_Table[57]	0		
Dem_DTC_FTB_Table[58]	0		
Dem_DTC_FTB_Table[59]	0		
Dem_DTC_FTB_Table[60]	0		
Dem_DTC_FTB_Table[61]	0		
Dem_DTC_FTB_Table[62]	0		
Dem_DTC_FTB_Table[63]	0		
Dem_DTC_FTB_Table[64]	0		
Dem_DTC_FTB_Table[65]	0		
Dem_DTC_FTB_Table[66]	0		
Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68]	0		
Dem_DTC_FTB_Table[69]	0		
Dem_DTC_FTB_Table[70]	0		
Dem_DTC_FTB_Table[71]	0		
Dem_DTC_FTB_Table[72]	0		
Dem_DTC_FTB_Table[73]	0		
Dem_DTC_FTB_Table[74]	0		
Dem_DTC_FTB_Table[75]	0		
Dem_DTC_FTB_Table[76]	0		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[6]	1	1	•
CTCFailedBuf_Cnt_M_lgc[7]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[8] CTCFailedBuf_Cnt_M_lgc[9]	1	1	•
CTCFailedBuf_Cnt_M_lgc[10]	1	1	-
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14]	1	1	•
CTCFailedBuf_Cnt_M_lgc[15]	1	1	~
CTCFailedBuf_Cnt_M_lgc[16]	1	1	~
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	~
CTCFailedBuf_Cnt_M_lgc[20]	0	0	•
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22] CTCFailedBuf_Cnt_M_lgc[23]	1	1	~
CTCFailedBuf_Cnt_M_lgc[24]	1	1	,
CTCFailedBuf_Cnt_M_lgc[25]	1	1	~
CTCFailedBuf Cnt M lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	~
CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	~
CTCFailedBuf_Cnt_M_lgc[35]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[36]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[37]	0	0	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[38] CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40]	0	0	Ž
CTCFailedBuf_Cnt_M_lgc[41]	0	0	-
CTCFailedBuf_Cnt_M_lgc[42]	0	0	,
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~

Rte\_Write\_Ap\_DemIf\_CTCFailed\_Cnt\_lgc(data)

Demlf\_DTCStatusChanged

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Actual Value **Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[53]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] CTCFailedBuf\_Cnt\_M\_lgc[63] 1 1  $CTCFailedBuf\_Cnt\_M\_lgc[64]$ ソソソソソ CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[66]$ CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[68]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 1 1 Demlf DTCStatusChanged() 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt Igc	1	~

Test Step 2.23 (Repeat Count = 1)   ✓		
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	1	
CTCFailedBuf_Cnt_M_lgc[1]	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	
CTCFailedBuf_Cnt_M_lgc[4]	1	
CTCFailedBuf_Cnt_M_lgc[5]	1	
CTCFailedBuf_Cnt_M_lgc[6]	1	
CTCFailedBuf_Cnt_M_lgc[7]	0	
CTCFailedBuf_Cnt_M_lgc[8]	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	
CTCFailedBuf_Cnt_M_lgc[12]	1	
CTCFailedBuf_Cnt_M_lgc[13]	1	
CTCFailedBuf_Cnt_M_lgc[14]	1	
CTCFailedBuf_Cnt_M_lgc[15]	1	
CTCFailedBuf_Cnt_M_lgc[16]	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	
CTCFailedBuf_Cnt_M_lgc[18]	1	
CTCFailedBuf_Cnt_M_lgc[19]	1	
CTCFailedBuf_Cnt_M_lgc[20]	0	
CTCFailedBuf_Cnt_M_lgc[21]	0	
CTCFailedBuf_Cnt_M_lgc[22]	0	
CTCFailedBuf_Cnt_M_Igc[23]	1	
CTCFailedBuf_Cnt_M_lgc[24]	1	
CTCFailedBuf_Cnt_M_lgc[25]	1	
CTCFailedBuf_Cnt_M_lgc[26]	1	
CTCFailedBuf_Cnt_M_lgc[27]	1	
CTCFailedBuf_Cnt_M_lgc[28]	1	

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[37] CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49] CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_igc[50] CTCFailedBuf_Cnt_M_igc[51]	0
CTCFailedBuf Cnt M lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63] CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75] CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	4118147944
DTCKind	2
DTCStatusNew	200
DTCStatusOld	203
Dem_DTCNumberTable[0]	254
Dem_DTCNumberTable[1]	153
Dem_DTCNumberTable[2]	91
Dem_DTCNumberTable[3]	138
Dem_DTCNumberTable[4]	54
Dem_DTCNumberTable[5]	108
Dem_DTCNumberTable[6] Dem_DTCNumberTable[7]	239 239
Dem_DTCNumberTable[8]	254
Dem_DTCNumberTable[9]	153
Dem_DTCNumberTable[10]	239
Dem_DTCNumberTable[11]	200
Dem_DTCNumberTable[12]	153
Dem_DTCNumberTable[13]	239
Dem_DTCNumberTable[14]	254
Dem_DTCNumberTable[15]	153
Dem_DTCNumberTable[16]	153
Dem_DTCNumberTable[17]	239
	33
Dem_DTCNumberTable[18] Dem_DTCNumberTable[19]	254

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Denni_D1C3tatusChanged		T GALCITON
Name	Input Value	
Dem_DTCNumberTable[20]	153	
Dem_DTCNumberTable[21]	239	
Dem_DTCNumberTable[22]	254	
Dem_DTCNumberTable[23]	91	
Dem_DTCNumberTable[24]	138	
Dem_DTCNumberTable[25]	54	
Dem_DTCNumberTable[26]	108	
Dem_DTCNumberTable[27]	153	
Dem_DTCNumberTable[28]	254	
Dem_DTCNumberTable[29]	153	
Dem_DTCNumberTable[30]	254	
Dem_DTCNumberTable[31]	254	
Dem_DTCNumberTable[32]	153	
Dem_DTCNumberTable[33]	153	
Dem_DTCNumberTable[34]	254	
Dem_DTCNumberTable[35]	153	
Dem_DTCNumberTable[36]	254	
Dem_DTCNumberTable[37] Dem_DTCNumberTable[38]	254 254	
Dem DTCNumberTable[39]	153	
	153	
Dem_DTCNumberTable[40] Dem_DTCNumberTable[41]	91	
Dem_DTCNumberTable[41]	138	
Dem_DTCNumberTable[42] Dem_DTCNumberTable[43]	54	
Dem_DTCNumberTable[43] Dem_DTCNumberTable[44]	108	
Dem_DTCNumberTable[44]	239	
Dem_DTCNumberTable[46]	254	
Dem_DTCNumberTable[47]	153	
Dem_DTCNumberTable[48]	138	
Dem_DTCNumberTable[49]	254	
Dem_DTCNumberTable[50]	153	
Dem_DTCNumberTable[51]	254	
Dem_DTCNumberTable[52]	254	
Dem_DTCNumberTable[53]	153	
Dem_DTCNumberTable[54]	138	
Dem_DTCNumberTable[55]	239	
Dem_DTCNumberTable[56]	254	
Dem_DTCNumberTable[57]	153	
Dem_DTCNumberTable[58]	254	
Dem_DTCNumberTable[59]	239	
Dem_DTCNumberTable[60]	254	
Dem_DTCNumberTable[61]	153	
Dem_DTCNumberTable[62]	138	
Dem_DTCNumberTable[63]	91	
Dem_DTCNumberTable[64]	138	
Dem_DTCNumberTable[65]	54	
Dem_DTCNumberTable[66]	108	
Dem_DTCNumberTable[67]	254	
Dem_DTCNumberTable[68]	254	
Dem_DTCNumberTable[69]	153	
Dem_DTCNumberTable[70]	138	
Dem_DTCNumberTable[71]	239	
Dem_DTCNumberTable[72]	138	
Dem_DTCNumberTable[73]	91	
Dem_DTCNumberTable[74]	138	
Dem_DTCNumberTable[75]	54	
Dem_DTC FTR_Table[76]	108	
Dem_DTC_FTB_Table[0]	255	
Dem_DTC_FTB_Table[1]	255	
Dem_DTC_FTB_Table[2]	255 255	
Dem_DTC_FTB_Table[3]	255	
Dem_DTC_FTB_Table[4] Dem_DTC_FTB_Table[5]	255	
Dem_DTC_FTB_Table[6]	255	
	255	
Dem_DTC_FTB_Table[7] Dem_DTC_FTB_Table[8]	255	
Dem_DTC_FTB_Table[8] Dem_DTC_FTB_Table[9]	255	
Dem_DTC_FTB_Table[10]	255 255	
Dem_DTC_FTB_Table[11]	255	
Dem_DTC_FTB_Table[12]		
Dem DTC FTB Table[13]	255	
Dem_DTC_FTB_Table[13] Dem_DTC_FTB_Table[14]	255 255	

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	le constitution of the con		
Name	Input Value		
Dem_DTC_FTB_Table[16] Dem_DTC_FTB_Table[17]	255 255		
Dem_DTC_FTB_Table[18]	255		
Dem_DTC_FTB_Table[19]	255		
Dem_DTC_FTB_Table[20]	255		
Dem_DTC_FTB_Table[21]	255		
Dem_DTC_FTB_Table[22]	255		
Dem_DTC_FTB_Table[23]	255		
Dem_DTC_FTB_Table[24] Dem_DTC_FTB_Table[25]	255 255		
Dem_DTC_FTB_Table[26]	255		
Dem_DTC_FTB_Table[27]	255		
Dem_DTC_FTB_Table[28]	255		
Dem_DTC_FTB_Table[29]	255		
Dem_DTC_FTB_Table[30]	255		
Dem_DTC_FTB_Table[31]	255 255		
Dem_DTC_FTB_Table[32] Dem_DTC_FTB_Table[33]	255		
Dem_DTC_FTB_Table[34]	255		
Dem_DTC_FTB_Table[35]	255		
Dem_DTC_FTB_Table[36]	255		
Dem_DTC_FTB_Table[37]	255		
Dem_DTC_FTB_Table[38]	255		
Dem_DTC_FTB_Table[39] Dem_DTC_FTB_Table[40]	255 255		
Dem_DTC_FTB_Table[40] Dem_DTC_FTB_Table[41]	255		
Dem_DTC_FTB_Table[42]	255		
Dem_DTC_FTB_Table[43]	255		
Dem_DTC_FTB_Table[44]	255		
Dem_DTC_FTB_Table[45]	255		
Dem_DTC_FTB_Table[46]	255		
Dem_DTC_FTB_Table[47]	255 255		
Dem_DTC_FTB_Table[48] Dem_DTC_FTB_Table[49]	255		
Dem_DTC_FTB_Table[50]	255		
Dem_DTC_FTB_Table[51]	255		
Dem_DTC_FTB_Table[52]	255		
Dem_DTC_FTB_Table[53]	255		
Dem_DTC_FTB_Table[54]	255		
Dem_DTC_FTB_Table[55] Dem_DTC_FTB_Table[56]	255 255		
Dem DTC FTB Table[57]			
	255		
Dem_DTC_FTB_Table[58]	255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60]	255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61]	255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62]	255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63]	255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62]	255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66]	255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[68]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[68]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[74]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]	255 255 255 255 255 255 255 255 255 255		
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[76] Name	255 255 255 255 255 255 255 255 255 255	Expected Value	
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name CTCFailedBuf_Cnt_M_lgc[0]	255 255 255 255 255 255 255 255 255 255	1	•
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1]	255 255 255 255 255 255 255 255 255 255	•	~
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76] Name CTCFailedBuf_Cnt_M_lgc[0]	255 255 255 255 255 255 255 255 255 255	1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[76] Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2]	255 255 255 255 255 255 255 255 255 255	1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5]	255 255 255 255 255 255 255 255 255 255	1 1 1 1 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6]	255 255 255 255 255 255 255 255 255 255	1 1 1 1 1 1	
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	255 255 255 255 255 255 255 255 255 255	1 1 1 1 1 1 1 1	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[59] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[67] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[72] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[1] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[7] CTCFailedBuf_Cnt_M_lgc[8]	255 255 255 255 255 255 255 255 255 255	1 1 1 1 1 1 1 1 0	· · · · · · · · · · · · · · · · · · ·
Dem_DTC_FTB_Table[58] Dem_DTC_FTB_Table[60] Dem_DTC_FTB_Table[61] Dem_DTC_FTB_Table[62] Dem_DTC_FTB_Table[63] Dem_DTC_FTB_Table[64] Dem_DTC_FTB_Table[65] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[66] Dem_DTC_FTB_Table[68] Dem_DTC_FTB_Table[69] Dem_DTC_FTB_Table[70] Dem_DTC_FTB_Table[71] Dem_DTC_FTB_Table[73] Dem_DTC_FTB_Table[74] Dem_DTC_FTB_Table[75] Dem_DTC_FTB_Table[76]  Name  CTCFailedBuf_Cnt_M_lgc[0] CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[4] CTCFailedBuf_Cnt_M_lgc[5] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[6] CTCFailedBuf_Cnt_M_lgc[7]	255 255 255 255 255 255 255 255 255 255	1 1 1 1 1 1 1 1	Result

2018-04-10, 18:44:44+0530



Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[11]	1	1	•
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[15] CTCFailedBuf_Cnt_M_lgc[16]	1	1	
CTCFailedBuf_Cnt_M_lgc[17]	1	1	~
CTCFailedBuf_Cnt_M_lgc[18]	1	1	-
CTCFailedBuf_Cnt_M_lgc[19]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[20]	0	0	•
CTCFailedBuf_Cnt_M_lgc[21]	0	0	~
CTCFailedBuf_Cnt_M_lgc[22]	0	0	~
CTCFailedBuf_Cnt_M_lgc[23]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[24]	1	1	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	1	1	
CTCFailedBuf_Cnt_M_lgc[27]	1	1	~
CTCFailedBuf_Cnt_M_lgc[28]	1	1	•
CTCFailedBuf_Cnt_M_lgc[29]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	•
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf_Cnt_M_lgc[36] CTCFailedBuf_Cnt_M_lgc[37]	0	0	-
CTCFailedBuf_Cnt_M_lgc[38]	0	0	
CTCFailedBuf_Cnt_M_lgc[39]	0	0	•
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	0	0	•
CTCFailedBuf_Cnt_M_lgc[43]	0	0	~
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46] CTCFailedBuf_Cnt_M_lgc[47]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[48]	0	0	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	•
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	•
CTCFailedBuf_Cnt_M_lgc[52]	0	0	•
CTCFailedBuf_Cnt_M_lgc[53]	1	1	•
CTCFailedBuf_Cnt_M_lgc[54]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56] CTCFailedBuf_Cnt_M_lgc[57]	1	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[58]	1	1	
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	•
CTCFailedBuf_Cnt_M_lgc[62]	1	1	~
CTCFailedBuf_Cnt_M_lgc[63]	1	1	~
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[66]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[67] CTCFailedBuf_Cnt_M_lgc[68]	0	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	~
CTCFailedBuf_Cnt_M_lgc[74]	0	0	~
CTCFailedBuf_Cnt_M_lgc[75]	0	0	~
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>V</b>
CTCFailed_Cnt_M_lgc  Demlf_DTCStatusChanged()	0	0	<b>V</b>
Demlf_DTCStatusChanged()  Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	~
	-	-	



Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt Igc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	-

Test Step 2.24 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2] CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16] CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf Cnt M Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	0
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30] CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	O .
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43] CTCFailedBuf Cnt M lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[44] CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58] CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1

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Demlf_DTCStatusChanged		MACICAL
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[64]	1	
CTCFailedBuf_Cnt_M_lgc[65]	0	
CTCFailedBuf_Cnt_M_lgc[66]	0	
CTCFailedBuf_Cnt_M_lgc[67]	0	
CTCFailedBuf_Cnt_M_lgc[68]	0	
CTCFailedBuf_Cnt_M_lgc[69]	0	
CTCFailedBuf_Cnt_M_lgc[70]	0	
CTCFailedBuf_Cnt_M_lgc[71]	0	
CTCFailedBuf_Cnt_M_lgc[72]	0	
CTCFailedBuf_Cnt_M_lgc[73]	0	
CTCFailedBuf_Cnt_M_lgc[74]	1	
CTCFailedBuf_Cnt_M_lgc[75]	0	
CTCFailedBuf_Cnt_M_lgc[76]	0	
CTCFailed_Cnt_M_lgc	0	
DTC	2120792415	
DTCKind	2	
DTCStatusNew	226	
DTCStatusOld	69	
Dem_DTCNumberTable[0]	157	
Dem_DTCNumberTable[1]	1	
Dem_DTCNumberTable[2]	112	
Dem_DTCNumberTable[3]	195	
Dem_DTCNumberTable[4]	200	
Dem_DTCNumberTable[5]	99	
Dem_DTCNumberTable[6]	203	
Dem_DTCNumberTable[7]	203	
Dem_DTCNumberTable[8]	157	
Dem_DTCNumberTable[9]	1	
Dem_DTCNumberTable[10]	203	
Dem_DTCNumberTable[11]	201	
Dem_DTCNumberTable[12]	1	
Dem_DTCNumberTable[13]	203	
Dem_DTCNumberTable[14]	157	
Dem_DTCNumberTable[15]	1	
Dem_DTCNumberTable[16]	1	
Dem_DTCNumberTable[17]	203	
Dem_DTCNumberTable[18]	101	
Dem_DTCNumberTable[19]	157	
Dem_DTCNumberTable[20]	1	
Dem DTCNumberTable[21]	203	
Dem_DTCNumberTable[22]	157	
Dem_DTCNumberTable[23]	112	
Dem_DTCNumberTable[24]	195	
Dem DTCNumberTable[25]	200	
Dem_DTCNumberTable[26]	99	
Dem_DTCNumberTable[27]	1	
Dem DTCNumberTable[28]	157	
	1	
Dem_DTCNumberTable[29]		
Dem_DTCNumberTable[30]	157	
Dem_DTCNumberTable[31]	157	
Dem_DTCNumberTable[32]	1	
Dem_DTCNumberTable[33]	1	
Dem_DTCNumberTable[34]	157	
Dem_DTCNumberTable[35]	1	
Dem_DTCNumberTable[36]	157	
Dem_DTCNumberTable[37]	157	
Dem_DTCNumberTable[38]	157	
Dem_DTCNumberTable[39]	1	
Dem_DTCNumberTable[40]	1	
Dem_DTCNumberTable[41]	112	
Dem_DTCNumberTable[42]	195	
Dem_DTCNumberTable[43]	200	
Dem_DTCNumberTable[44]	99	
Dem_DTCNumberTable[45]	203	
Dem_DTCNumberTable[46]	157	
Dem_DTCNumberTable[47]	1	
Dem_DTCNumberTable[48]	195	
Dem_DTCNumberTable[46]	157	
	1	
Dem_DTCNumberTable[50]		
Dem_DTCNumberTable[51]	157	
Dem_DTCNumberTable[52]	157	
Dem_DTCNumberTable[53]	1	
Dem_DTCNumberTable[54]	195	

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Imput Value	
m_DTCNumberTable[55]   203   157	
1	
157   203	
203   203   203   203   205	
Sem_DTCNumberTable[60]   157   158	
Sem_DTCNumberTable[61]   1   1   1   1   1   1   1   1   1	
195	
112   125	
195   200	
em_DTCNumberTable[65]       200         em_DTCNumberTable[66]       99         em_DTCNumberTable[67]       157         em_DTCNumberTable[68]       157         em_DTCNumberTable[69]       1         em_DTCNumberTable[70]       195         em_DTCNumberTable[71]       203         em_DTCNumberTable[72]       195         em_DTCNumberTable[73]       112         em_DTCNumberTable[74]       195         em_DTCNumberTable[75]       200         em_DTCNumberTable[76]       99         em_DTC_FTB_Table[0]       31         em_DTC_FTB_Table[1]       227         em_DTC_FTB_Table[2]       66         em_DTC_FTB_Table[3]       96	
grm_DTCNumberTable[66]       99         grm_DTCNumberTable[67]       157         grm_DTCNumberTable[68]       157         grm_DTCNumberTable[69]       1         grm_DTCNumberTable[70]       195         grm_DTCNumberTable[71]       203         grm_DTCNumberTable[72]       195         grm_DTCNumberTable[73]       112         grm_DTCNumberTable[74]       195         grm_DTCNumberTable[75]       200         grm_DTCNumberTable[76]       99         grm_DTC_FTB_Table[0]       31         grm_DTC_FTB_Table[1]       227         grm_DTC_FTB_Table[2]       66         grm_DTC_FTB_Table[3]       96	
em_DTCNumberTable[67]     157       em_DTCNumberTable[68]     157       em_DTCNumberTable[69]     1       em_DTCNumberTable[70]     195       em_DTCNumberTable[71]     203       em_DTCNumberTable[72]     195       em_DTCNumberTable[73]     112       em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[68]     157       em_DTCNumberTable[69]     1       em_DTCNumberTable[70]     195       em_DTCNumberTable[71]     203       em_DTCNumberTable[72]     195       em_DTCNumberTable[73]     112       em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
1	
em_DTCNumberTable[70]     195       em_DTCNumberTable[71]     203       em_DTCNumberTable[72]     195       em_DTCNumberTable[73]     112       em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[71]     203       em_DTCNumberTable[72]     195       em_DTCNumberTable[73]     112       em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[72]     195       em_DTCNumberTable[73]     112       em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[73]     112       em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[74]     195       em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[75]     200       em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTCNumberTable[76]     99       em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTC_FTB_Table[0]     31       em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTC_FTB_Table[1]     227       em_DTC_FTB_Table[2]     66       em_DTC_FTB_Table[3]     96	
em_DTC_FTB_Table[2] 66 em_DTC_FTB_Table[3] 96	
em_DTC_FTB_Table[3] 96	
em_DTC_FTB_Table[5] 24	
em_DTC_FTB_Table[6] 240	
em_DTC_FTB_Table[7] 240	
em_DTC_FTB_Table[8] 31	
em_DTC_FTB_Table[9] 227	
em_DTC_FTB_Table[10] 240	
em_DTC_FTB_Table[11] 151	
em_DTC_FTB_Table[12] 227	
em_DTC_FTB_Table[13] 240	
em_DTC_FTB_Table[14] 31	
em_DTC_FTB_Table[15] 227	
em_DTC_FTB_Table[16] 227	
em_DTC_FTB_Table[17] 240	
em_DTC_FTB_Table[18] 241	
em_DTC_FTB_Table[19] 31	
em_DTC_FTB_Table[20] 227	
em_DTC_FTB_Table[21] 240 em_DTC_FTB_Table[22] 31	
em_DTC_FTB_Table[22] 31 em_DTC_FTB_Table[23] 66	
em_DTC_FTB_Table[24] 96	
em_DTC_FTB_Table[25] 130	
em_DTC_FTB_Table[26] 24	
em_DTC_FTB_Table[27] 227	
em_DTC_FTB_Table[28] 31	
em_DTC_FTB_Table[29] 227	
em_DTC_FTB_Table[30] 31	
em_DTC_FTB_Table[31] 31	
em_DTC_FTB_Table[32] 227	
em_DTC_FTB_Table[33] 227	
em_DTC_FTB_Table[34] 31	
em_DTC_FTB_Table[35] 227	
em_DTC_FTB_Table[36] 31	
em_DTC_FTB_Table[37] 31	
em_DTC_FTB_Table[38] 31	
em_DTC_FTB_Table[39] 227	
em_DTC_FTB_Table[40] 227	
em_DTC_FTB_Table[41] 66	
em_DTC_FTB_Table[42] 96	
em_DTC_FTB_Table[43] 130	
em_DTC_FTB_Table[44] 24	
em_DTC_FTB_Table[45] 240	
em_DTC_FTB_Table[46] 31	
em_DTC_FTB_Table[47] 227	
em_DTC_FTB_Table[48] 96	
em_DTC_FTB_Table[49] 31	
em_DTC_FTB_Table[50] 227	

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Demlf\_DTCStatusChanged Input Value Dem\_DTC\_FTB\_Table[51] 31 Dem\_DTC\_FTB\_Table[52] 31 Dem DTC\_FTB\_Table[53] 227 Dem\_DTC\_FTB\_Table[54] 96 Dem\_DTC\_FTB\_Table[55] 240 Dem\_DTC\_FTB\_Table[56] 31 Dem\_DTC\_FTB\_Table[57] 227 Dem\_DTC\_FTB\_Table[58] 31 Dem\_DTC\_FTB\_Table[59] 240 Dem\_DTC\_FTB\_Table[60] 31 Dem\_DTC\_FTB\_Table[61] 227 Dem\_DTC\_FTB\_Table[62] 96 66 Dem\_DTC\_FTB\_Table[63] Dem\_DTC\_FTB\_Table[64] 96 Dem\_DTC\_FTB\_Table[65] 130 24 Dem DTC FTB Table[66] Dem\_DTC\_FTB\_Table[67] 31 Dem\_DTC\_FTB\_Table[68] 31 Dem\_DTC\_FTB\_Table[69] 227 Dem\_DTC\_FTB\_Table[70] 96 Dem\_DTC\_FTB\_Table[71] 240 Dem\_DTC\_FTB\_Table[72] 96 Dem\_DTC\_FTB\_Table[73] 66 Dem\_DTC\_FTB\_Table[74] 96 Dem\_DTC\_FTB\_Table[75] 130 Dem\_DTC\_FTB\_Table[76] 24 Name **Actual Value Expected Value** Result CTCFailedBuf Cnt M Igc[0] 1 CTCFailedBuf\_Cnt\_M\_lgc[1] CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 0 CTCFailedBuf Cnt M lgc[4] 1 CTCFailedBuf\_Cnt\_M\_lgc[5] 1 1 CTCFailedBuf Cnt M Igc[6] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[7] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[8] 1 CTCFailedBuf\_Cnt\_M\_lgc[9] CTCFailedBuf\_Cnt\_M\_lgc[10] CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] CTCFailedBuf\_Cnt\_M\_lgc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] **~** CTCFailedBuf\_Cnt\_M\_lgc[17] 1 CTCFailedBuf\_Cnt\_M\_lgc[18] 1 1 CTCFailedBuf\_Cnt\_M\_Igc[19] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[20] n 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[22] n n CTCFailedBuf\_Cnt\_M\_lgc[23] 1 CTCFailedBuf Cnt M lqc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25] CTCFailedBuf\_Cnt\_M\_lgc[26] CTCFailedBuf\_Cnt\_M\_lgc[27] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 1  $CTCFailedBuf\_Cnt\_M\_lgc[29]$ 1 CTCFailedBuf\_Cnt\_M\_lgc[30] CTCFailedBuf\_Cnt\_M\_lgc[31] 1 CTCFailedBuf\_Cnt\_M\_lgc[32] 1 CTCFailedBuf\_Cnt\_M\_lgc[33] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[38] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 0 CTCFailedBuf Cnt M Igc[41] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 V CTCFailedBuf\_Cnt\_M\_lgc[44] 0 0

0

0

CTCFailedBuf\_Cnt\_M\_lgc[45]



Demlf\_DTCStatusChanged

Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[50]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[51]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[52]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[53]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[54]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[55]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[56]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[57]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[58]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[59]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[60]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[61]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[62]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[63]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[64]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[65]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[66]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[67]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[68]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[69]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[70]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[71]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[72]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[73]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[74]	1	1	✓
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	✓
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	✓
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc(data)	0	0	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_DemIf_CTCFailed_Cnt_lgc	1	~

Test Step 3.1 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	0
CTCFailedBuf_Cnt_M_lgc[2]	0
CTCFailedBuf_Cnt_M_lgc[3]	0
CTCFailedBuf_Cnt_M_lgc[4]	0
CTCFailedBuf_Cnt_M_lgc[5]	0

Test Case 3: Path Test

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Input Value CTCFailedBuf\_Cnt\_M\_lgc[6] 0 CTCFailedBuf\_Cnt\_M\_lgc[7] 0 CTCFailedBuf Cnt M lqc[8] 0 CTCFailedBuf\_Cnt\_M\_lgc[9] 0 CTCFailedBuf Cnt M lqc[10] 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] 0 CTCFailedBuf\_Cnt\_M\_lgc[18] 0 CTCFailedBuf\_Cnt\_M\_lgc[19] 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 CTCFailedBuf\_Cnt\_M\_lgc[22] 0 CTCFailedBuf\_Cnt\_M\_lgc[23] 0 CTCFailedBuf\_Cnt\_M\_lgc[24] 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 CTCFailedBuf\_Cnt\_M\_lgc[27] 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 CTCFailedBuf\_Cnt\_M\_lgc[29] 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 CTCFailedBuf\_Cnt\_M\_lgc[31] 0 CTCFailedBuf\_Cnt\_M\_lgc[32] 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 CTCFailedBuf\_Cnt\_M\_lgc[35] 0 CTCFailedBuf Cnt M Igc[36] 0 CTCFailedBuf\_Cnt\_M\_lgc[37] 0 CTCFailedBuf Cnt M Igc[38] 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 CTCFailedBuf\_Cnt\_M\_lgc[40] 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 CTCFailedBuf\_Cnt\_M\_lgc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] CTCFailedBuf\_Cnt\_M\_lgc[44] 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 CTCFailedBuf\_Cnt\_M\_lgc[47] 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 CTCFailedBuf\_Cnt\_M\_lgc[50] n CTCFailedBuf\_Cnt\_M\_Igc[51] 0 CTCFailedBuf\_Cnt\_M\_lgc[52] n CTCFailedBuf\_Cnt\_M\_lgc[53] 0 CTCFailedBuf\_Cnt\_M\_lgc[54] n CTCFailedBuf\_Cnt\_M\_lgc[55] 0 CTCFailedBuf Cnt M Igc[56] 0 CTCFailedBuf\_Cnt\_M\_lgc[57] 0 CTCFailedBuf\_Cnt\_M\_lgc[58] 0 CTCFailedBuf\_Cnt\_M\_lgc[59] 0 CTCFailedBuf\_Cnt\_M\_lgc[60] 0 CTCFailedBuf\_Cnt\_M\_lgc[61] 0 CTCFailedBuf\_Cnt\_M\_lgc[62] 0 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 CTCFailedBuf\_Cnt\_M\_lgc[64] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[65] CTCFailedBuf\_Cnt\_M\_lgc[66] 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 CTCFailedBuf Cnt M Igc[73] 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 CTCFailed\_Cnt\_M\_lgc 0 DTC 0

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Demlf_DTCStatusChanged	TAZOICAL
Name	Input Value
DTCKind	1
DTCStatusNew	0
DTCStatusOld	0
Dem_DTCNumberTable[0]	0
Dem_DTCNumberTable[1]	0
Dem_DTCNumberTable[2] Dem_DTCNumberTable[3]	0
Dem_DTCNumberTable[4]	0
Dem_DTCNumberTable[5]	0
Dem_DTCNumberTable[6]	0
Dem_DTCNumberTable[7]	0
Dem_DTCNumberTable[8]	0
Dem_DTCNumberTable[9]	0
Dem_DTCNumberTable[10]	0
Dem_DTCNumberTable[11] Dem_DTCNumberTable[12]	0 0
Dem_DTCNumberTable[13]	0
Dem_DTCNumberTable[14]	0
Dem_DTCNumberTable[15]	0
Dem_DTCNumberTable[16]	0
Dem_DTCNumberTable[17]	0
Dem_DTCNumberTable[18]	0
Dem_DTCNumberTable[19]	0
Dem_DTCNumberTable[20]	0
Dem_DTCNumberTable[21] Dem_DTCNumberTable[22]	0
Dem_DTCNumberTable[23]	0
Dem_DTCNumberTable[24]	0
Dem_DTCNumberTable[25]	0
Dem_DTCNumberTable[26]	0
Dem_DTCNumberTable[27]	0
Dem_DTCNumberTable[28]	0
Dem_DTCNumberTable[29]	0
Dem_DTCNumberTable[30] Dem_DTCNumberTable[31]	0 0
Dem_DTCNumberTable[32]	0
Dem_DTCNumberTable[33]	0
Dem_DTCNumberTable[34]	0
Dem_DTCNumberTable[35]	0
Dem_DTCNumberTable[36]	0
Dem_DTCNumberTable[37]	0
Dem_DTCNumberTable[38]	0
Dem_DTCNumberTable[39] Dem_DTCNumberTable[40]	0
Dem_DTCNumberTable[41]	0
Dem_DTCNumberTable[42]	0
Dem_DTCNumberTable[43]	0
Dem_DTCNumberTable[44]	0
Dem_DTCNumberTable[45]	0
Dem_DTCNumberTable[46]	0
Dem_DTCNumberTable[47]	0 0
Dem_DTCNumberTable[48] Dem_DTCNumberTable[49]	0
Dem_DTCNumberTable[49] Dem_DTCNumberTable[50]	0
Dem_DTCNumberTable[51]	0
Dem_DTCNumberTable[52]	0
Dem_DTCNumberTable[53]	0
Dem_DTCNumberTable[54]	0
Dem_DTCNumberTable[55]	0
Dem_DTCNumberTable[56]	0
Dem_DTCNumberTable[57] Dem_DTCNumberTable[58]	0 0
Dem_DTCNumberTable[58] Dem_DTCNumberTable[59]	0
Dem_DTCNumberTable[69]	0
Dem_DTCNumberTable[61]	0
Dem_DTCNumberTable[62]	0
Dem_DTCNumberTable[63]	0
Dem_DTCNumberTable[64]	0
Dem_DTCNumberTable[65]	0
Dem_DTCNumberTable[66]	0
Dem_DTCNumberTable[67]	0
Dem_DTCNumberTable[68]	0
Dem_DTCNumberTable[69]	0

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Demlf_DTCStatusChanged	MACICAL
Name	Input Value
Dem_DTCNumberTable[70]	0
Dem_DTCNumberTable[71]	0
Dem_DTCNumberTable[72]	0
Dem_DTCNumberTable[73]	0
Dem_DTCNumberTable[74]	0
Dem_DTCNumberTable[75]	0
Dem_DTCNumberTable[76]	0
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem_DTC_FTB_Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem_DTC_FTB_Table[7]	255
Dem_DTC_FTB_Table[8] Dem_DTC_FTB_Table[9]	255 255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem_DTC_FTB_Table[12]	255
Dem DTC FTB Table[13]	255
Dem_DTC_FTB_Table[14]	255
Dem_DTC_FTB_Table[15]	255
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
Dem_DTC_FTB_Table[30]	255 255
Dem_DTC_FTB_Table[31] Dem_DTC_FTB_Table[32]	255
Dem_DTC_FTB_Table[32]	255
Dem DTC FTB Table[34]	255
Dem_DTC_FTB_Table[35]	255
Dem_DTC_FTB_Table[36]	255
Dem_DTC_FTB_Table[37]	255
Dem_DTC_FTB_Table[38]	255
Dem_DTC_FTB_Table[39]	255
Dem_DTC_FTB_Table[40]	255
Dem_DTC_FTB_Table[41]	255
Dem_DTC_FTB_Table[42]	255
Dem_DTC_FTB_Table[43]	255
Dem_DTC_FTB_Table[44]	255
Dem_DTC_FTB_Table[45]	255
Dem_DTC_FTB_Table[46]	255
Dem_DTC_FTB_Table[47]	255
Dem_DTC_FTB_Table[48]	255
Dem_DTC_FTB_Table[49]	255
Dem_DTC_FTB_Table[50]	255
Dem_DTC_FTB_Table[51]	255
Dem_DTC_FTB_Table[52]	255
Dem_DTC_FTB_Table[53]	255
Dem_DTC_FTB_Table[54]	255 255
Dem_DTC_FTB_Table[55] Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[57]	255
Dem_DTC_FTB_Table[56]	255
Dem_DTC_FTB_Table[60]	255
em DTC FTB Table[61]	
Dem_DTC_FTB_Table[61] Dem DTC FTB Table[62]	255
Dem_DTC_FTB_Table[62]	
	255 255

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Name	Input Value			
Dem_DTC_FTB_Table[66]	255			
Dem_DTC_FTB_Table[67]	255			
Dem_DTC_FTB_Table[68]	255			
Dem_DTC_FTB_Table[69]	255			
Dem_DTC_FTB_Table[70]	255			
Dem_DTC_FTB_Table[71]	255			
Dem_DTC_FTB_Table[72]	255			
Dem_DTC_FTB_Table[73]	255			
Dem_DTC_FTB_Table[74]	255			
Dem_DTC_FTB_Table[75]	255			
Dem_DTC_FTB_Table[76]	255			
		I		
Name	Actual Value	Expected Value	Result	
CTCFailedBuf_Cnt_M_lgc[0]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[1]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[2]	0	0	<b>✓</b>	
CTCFailedBuf_Cnt_M_lgc[3]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[4]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[5]	0	0	•	
	0	0	-	
CTCFailedBuf_Cnt_M_lgc[6]		0		
CTCFailedBuf_Cnt_M_lgc[7]	0		~	
CTCFailedBuf_Cnt_M_lgc[8]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[9]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[10]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[11]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[12]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[13]	0	0	<b>✓</b>	
CTCFailedBuf_Cnt_M_lgc[14]	0	0	_	
	0	0	~	
CTCFailedBuf_Cnt_M_lgc[15]				
CTCFailedBuf_Cnt_M_lgc[16]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[17]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[18]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[19]	0	0	~	
CTCFailedBuf_Cnt_M_Igc[20]	0	0	•	
CTCFailedBuf_Cnt_M_lgc[21]	0	0	<b>✓</b>	
CTCFailedBuf_Cnt_M_lgc[22]	0	0	_	
CTCFailedBuf_Cnt_M_lgc[23]	0	0	<b>✓</b>	
	0	0	-	
CTCFailedBuf_Cnt_M_lgc[24]				
CTCFailedBuf_Cnt_M_lgc[25]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[26]	0	0	~	
CTCFailedBuf_Cnt_M_Igc[27]	0	0	~	
CTCFailedBuf_Cnt_M_Igc[28]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[29]	0	0	~	
CTCFailedBuf Cnt M lgc[30]	0	0	~	
CTCFailedBuf Cnt M Igc[31]	0	0	<b>✓</b>	
CTCFailedBuf Cnt M Igc[32]	0	0	_	
CTCFailedBuf_Cnt_M_lgc[33]	0	0	•	
CTCFailedBuf_Cnt_M_lgc[34]	0	0		
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[36]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[37]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[41]	0	0	•	
	0	0	9	
CTCFailedBuf_Cnt_M_lgc[42]				
CTCFailedBuf_Cnt_M_lgc[43]	0	0	•	
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[49]	0	0	<b>V</b>	
CTCFailedBuf_Cnt_M_lgc[50]	0	0		
	0	0		
CTCFailedBuf_Cnt_M_lgc[51]				
CTCFailedBuf_Cnt_M_lgc[52]	0	0	•	
CTCFailedBuf_Cnt_M_lgc[53]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[54]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[55]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[56]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[57]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[58]	0	0	~	
CTCFailedBuf_Cnt_M_lgc[59]	0	0	-	
CTCFailedBuf_Cnt_M_lgc[60]	0	0		

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[61]	0	0	~
CTCFailedBuf_Cnt_M_lgc[62]	0	0	~
CTCFailedBuf_Cnt_M_lgc[63]	0	0	~
CTCFailedBuf_Cnt_M_lgc[64]	0	0	~
CTCFailedBuf_Cnt_M_lgc[65]	0	0	•
CTCFailedBuf_Cnt_M_lgc[66]	0	0	•
CTCFailedBuf_Cnt_M_lgc[67]	0	0	•
CTCFailedBuf_Cnt_M_lgc[68]	0	0	~
CTCFailedBuf_Cnt_M_lgc[69]	0	0	~
CTCFailedBuf_Cnt_M_lgc[70]	0	0	~
CTCFailedBuf_Cnt_M_lgc[71]	0	0	~
CTCFailedBuf_Cnt_M_lgc[72]	0	0	~
CTCFailedBuf_Cnt_M_lgc[73]	0	0	•
CTCFailedBuf_Cnt_M_lgc[74]	0	0	•
CTCFailedBuf_Cnt_M_lgc[75]	0	0	•
CTCFailedBuf_Cnt_M_lgc[76]	0	0	~
CTCFailed_Cnt_M_lgc	0	0	~
Demlf_DTCStatusChanged()	0	0	~
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 3.2 (Repeat Count = 1)	Innut Value
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	0
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
TCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf Cnt M lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
TCF alledBut_Crit_M_igc[20]	1
CTCFailedBut_Crit_ivi_igc[27]	1
	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	
TCFailedBuf_Cnt_M_lgc[31]	1
TCFailedBuf_Cnt_M_lgc[32]	1
TCFailedBuf_Cnt_M_lgc[33]	1
TCFailedBuf_Cnt_M_lgc[34]	1
TCFailedBuf_Cnt_M_lgc[35]	1
TCFailedBuf_Cnt_M_lgc[36]	1
TCFailedBuf_Cnt_M_lgc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf Cnt M lgc[43]	1

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Input Value CTCFailedBuf\_Cnt\_M\_lgc[44] CTCFailedBuf\_Cnt\_M\_lgc[45] CTCFailedBuf\_Cnt\_M\_lgc[46] CTCFailedBuf\_Cnt\_M\_lgc[47] CTCFailedBuf Cnt M lqc[48] CTCFailedBuf\_Cnt\_M\_lgc[49] CTCFailedBuf\_Cnt\_M\_lgc[50] 1 CTCFailedBuf\_Cnt\_M\_lgc[51] 1 CTCFailedBuf\_Cnt\_M\_lgc[52] CTCFailedBuf\_Cnt\_M\_lgc[53] 1 CTCFailedBuf\_Cnt\_M\_lgc[54] CTCFailedBuf\_Cnt\_M\_lgc[55] 1 CTCFailedBuf\_Cnt\_M\_lgc[56] CTCFailedBuf\_Cnt\_M\_lgc[57] 1 CTCFailedBuf\_Cnt\_M\_lgc[58] CTCFailedBuf\_Cnt\_M\_lgc[59] 1 CTCFailedBuf\_Cnt\_M\_lgc[60] CTCFailedBuf\_Cnt\_M\_lgc[61] 1 CTCFailedBuf\_Cnt\_M\_lgc[62] 1 CTCFailedBuf\_Cnt\_M\_lgc[63] 1 CTCFailedBuf\_Cnt\_M\_lgc[64] 1 CTCFailedBuf\_Cnt\_M\_lgc[65] 1 CTCFailedBuf\_Cnt\_M\_lgc[66] 1 CTCFailedBuf\_Cnt\_M\_lgc[67] 1 CTCFailedBuf\_Cnt\_M\_lgc[68] CTCFailedBuf\_Cnt\_M\_lgc[69] CTCFailedBuf\_Cnt\_M\_lgc[70] 1 CTCFailedBuf\_Cnt\_M\_lgc[71] 1 CTCFailedBuf\_Cnt\_M\_lgc[72] 1 CTCFailedBuf\_Cnt\_M\_lgc[73] 1 CTCFailedBuf Cnt M Igc[74] CTCFailedBuf\_Cnt\_M\_lgc[75] 1 CTCFailedBuf Cnt M Igc[76] 1 CTCFailed\_Cnt\_M\_lgc 0 DTC 0 DTCKind 1 DTCStatusNew 0 DTCStatusOld 0 Dem\_DTCNumberTable[0] 0 Dem\_DTCNumberTable[1] 0 Dem\_DTCNumberTable[2] 0 Dem\_DTCNumberTable[3] 0 Dem\_DTCNumberTable[4] 0 Dem\_DTCNumberTable[5] 0 Dem\_DTCNumberTable[6] n Dem\_DTCNumberTable[7] 0 Dem DTCNumberTable[8] n Dem\_DTCNumberTable[9] 0 Dem DTCNumberTable[10] n Dem\_DTCNumberTable[11] 0 Dem\_DTCNumberTable[12] 0 Dem\_DTCNumberTable[13] 0 Dem\_DTCNumberTable[14] 0 Dem\_DTCNumberTable[15] 0 Dem\_DTCNumberTable[16] 0 Dem\_DTCNumberTable[17] 0 Dem\_DTCNumberTable[18] 0 Dem\_DTCNumberTable[19] 0 Dem\_DTCNumberTable[20] 0 Dem\_DTCNumberTable[21] 0 Dem\_DTCNumberTable[22] 0 0 Dem\_DTCNumberTable[23] Dem\_DTCNumberTable[24] 0 Dem\_DTCNumberTable[25] 0 Dem\_DTCNumberTable[26] 0 Dem DTCNumberTable[27] 0 Dem\_DTCNumberTable[28] 0 0 Dem DTCNumberTable[29] Dem\_DTCNumberTable[30] 0 Dem\_DTCNumberTable[31] 0 Dem DTCNumberTable[32] 0 Dem\_DTCNumberTable[33] 0 Dem\_DTCNumberTable[34] 0

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Demlf_DTCStatusChanged		razoitat
Name	Input Value	
Dem_DTCNumberTable[35]	0	
Dem_DTCNumberTable[36]	0	
Dem_DTCNumberTable[37]	0	
Dem_DTCNumberTable[38]	0	
Dem_DTCNumberTable[39]	0	
Dem_DTCNumberTable[40]	0	
Dem_DTCNumberTable[41]	0	
Dem_DTCNumberTable[42]	0	
Dem_DTCNumberTable[43]	0	
Dem_DTCNumberTable[44]	0	
Dem_DTCNumberTable[45]	0	
Dem_DTCNumberTable[46]	0	
Dem_DTCNumberTable[47]	0	
Dem_DTCNumberTable[48] Dem_DTCNumberTable[49]	0	
Dem_DTCNumberTable[50]	0	
Dem_DTCNumberTable[51]	0	
Dem_DTCNumberTable[52]	0	
Dem_DTCNumberTable[53]	0	
Dem_DTCNumberTable[54]	0	
Dem_DTCNumberTable[55]	0	
Dem_DTCNumberTable[56]	0	
Dem_DTCNumberTable[57]	0	
Dem_DTCNumberTable[58]	0	
Dem_DTCNumberTable[59]	0	
Dem_DTCNumberTable[60]	0	
Dem_DTCNumberTable[61]	0	
Dem_DTCNumberTable[62]	0	
Dem_DTCNumberTable[63]	0	
Dem_DTCNumberTable[64]	0	
Dem_DTCNumberTable[65]	0	
Dem_DTCNumberTable[66]	0	
Dem_DTCNumberTable[67]	0	
Dem_DTCNumberTable[68]	0	
Dem_DTCNumberTable[69]	0	
Dem_DTCNumberTable[70] Dem_DTCNumberTable[71]	0	
Dem_DTCNumberTable[71]	0	
Dem DTCNumberTable[73]	0	
Dem_DTCNumberTable[74]	0	
Dem_DTCNumberTable[75]	0	
Dem_DTCNumberTable[76]	0	
Dem_DTC_FTB_Table[0]	0	
Dem_DTC_FTB_Table[1]	0	
Dem_DTC_FTB_Table[2]	0	
Dem_DTC_FTB_Table[3]	0	
Dem_DTC_FTB_Table[4]	0	
Dem_DTC_FTB_Table[5]	0	
Dem_DTC_FTB_Table[6]	0	
Dem_DTC_FTB_Table[7]	0	
Dem_DTC_FTB_Table[8]	0	
Dem_DTC_FTB_Table[9]	0	
Dem_DTC_FTB_Table[10]	0	
Dem_DTC_FTB_Table[11]	0	
Dem_DTC_FTB_Table[12]	0	
Dem_DTC_FTB_Table[13]	0	
Dem_DTC_FTB_Table[14] Dem_DTC_FTB_Table[15]	0	
Dem_DTC_F1B_Table[16]	0	
Dem_DTC_FTB_Table[16]	0	
Dem_DTC_FTB_Table[18]	0	
Dem_DTC_FTB_Table[19]	0	
Dem_DTC_FTB_Table[20]	0	
Dem_DTC_FTB_Table[21]	0	
Dem_DTC_FTB_Table[22]	0	
Dem_DTC_FTB_Table[23]	0	
Dem_DTC_FTB_Table[24]	0	
Dem_DTC_FTB_Table[25]	0	
Dem_DTC_FTB_Table[26]	0	
Dem_DTC_FTB_Table[27]	0	
Dem_DTC_FTB_Table[28]	0	
	1-	
Dem_DTC_FTB_Table[29] Dem_DTC_FTB_Table[30]	0	

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Input Value Dem\_DTC\_FTB\_Table[31] 0 Dem\_DTC\_FTB\_Table[32] 0 Dem DTC\_FTB\_Table[33] 0 Dem\_DTC\_FTB\_Table[34] 0 Dem\_DTC\_FTB\_Table[35] 0 Dem\_DTC\_FTB\_Table[36] 0 Dem\_DTC\_FTB\_Table[37] 0 Dem\_DTC\_FTB\_Table[38] 0 Dem\_DTC\_FTB\_Table[39] 0 Dem\_DTC\_FTB\_Table[40] 0 Dem\_DTC\_FTB\_Table[41] 0 Dem\_DTC\_FTB\_Table[42] 0 Dem\_DTC\_FTB\_Table[43] 0 Dem\_DTC\_FTB\_Table[44] 0 Dem\_DTC\_FTB\_Table[45] 0 0 Dem DTC FTB Table[46] Dem\_DTC\_FTB\_Table[47] 0 Dem\_DTC\_FTB\_Table[48] 0 Dem\_DTC\_FTB\_Table[49] 0 Dem\_DTC\_FTB\_Table[50] 0 Dem\_DTC\_FTB\_Table[51] 0 Dem\_DTC\_FTB\_Table[52] 0 Dem\_DTC\_FTB\_Table[53] 0 Dem\_DTC\_FTB\_Table[54] 0 Dem\_DTC\_FTB\_Table[55] 0 Dem\_DTC\_FTB\_Table[56] 0 Dem\_DTC\_FTB\_Table[57] 0 Dem\_DTC\_FTB\_Table[58] 0 Dem DTC FTB Table[59] 0 Dem\_DTC\_FTB\_Table[60] 0 Dem DTC FTB Table[61] 0 Dem\_DTC\_FTB\_Table[62] 0 Dem DTC FTB Table[63] 0 Dem\_DTC\_FTB\_Table[64] 0 Dem\_DTC\_FTB\_Table[65] 0 Dem\_DTC\_FTB\_Table[66] 0 Dem\_DTC\_FTB\_Table[67] 0 0 Dem\_DTC\_FTB\_Table[68] Dem\_DTC\_FTB\_Table[69] 0 Dem\_DTC\_FTB\_Table[70] 0 Dem\_DTC\_FTB\_Table[71] 0 Dem\_DTC\_FTB\_Table[72] 0 Dem\_DTC\_FTB\_Table[73] 0 Dem\_DTC\_FTB\_Table[74] 0 Dem\_DTC\_FTB\_Table[75] n Dem\_DTC\_FTB\_Table[76] 0 **Actual Value Expected Value** Result CTCFailedBuf\_Cnt\_M\_lgc[0] n 0 CTCFailedBuf\_Cnt\_M\_lgc[1] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[3] CTCFailedBuf\_Cnt\_M\_lgc[4] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[5] CTCFailedBuf\_Cnt\_M\_lgc[6] CTCFailedBuf\_Cnt\_M\_lgc[7] 1 CTCFailedBuf\_Cnt\_M\_lgc[8] 1 CTCFailedBuf\_Cnt\_M\_lgc[9] 1 CTCFailedBuf\_Cnt\_M\_lgc[10] 1 CTCFailedBuf\_Cnt\_M\_lgc[11] CTCFailedBuf\_Cnt\_M\_lgc[12] 1 CTCFailedBuf\_Cnt\_M\_lgc[13] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[14] **~** CTCFailedBuf\_Cnt\_M\_lgc[15] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[16] CTCFailedBuf\_Cnt\_M\_lgc[17] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[18] CTCFailedBuf\_Cnt\_M\_lgc[19] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[20] 1 1 CTCFailedBuf Cnt M Igc[21] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[22] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[23] 1 1 ~ CTCFailedBuf\_Cnt\_M\_lgc[24] 1 1 CTCFailedBuf\_Cnt\_M\_lgc[25]

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[26]	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[28]	1	1	~
CTCFailedBuf_Cnt_M_lgc[29]	1	1	•
CTCFailedBuf_Cnt_M_lgc[30]	1	1	~
CTCFailedBuf_Cnt_M_lgc[31]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[32]	1	1	~
CTCFailedBuf_Cnt_M_lgc[33]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[34]	1	1	_
CTCFailedBuf_Cnt_M_lgc[35]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[36]	1	1	_
CTCFailedBuf_Cnt_M_lgc[37]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[38]	1	1	
CTCFailedBuf_Cnt_M_lgc[39]	1	1	
CTCFailedBuf_Cnt_M_lgc[40]	1	1	
CTCFailedBuf_Cnt_M_lgc[41]	1	1	~
CTCFailedBuf_Cnt_M_lgc[42]	1	1	
CTCFailedBuf_Cnt_M_lgc[43]	1	1	-
	1	1	
CTCFailedBuf_Cnt_M_lgc[44]		1	
CTCFailedBuf_Cnt_M_lgc[45]	1		
CTCFailedBuf_Cnt_M_lgc[46]	1	1	
CTCFailedBuf_Cnt_M_lgc[47]	1	1	_
CTCFailedBuf_Cnt_M_lgc[48]	1	1	~
CTCFailedBuf_Cnt_M_lgc[49]	1	1	•
CTCFailedBuf_Cnt_M_lgc[50]	1	1	~
CTCFailedBuf_Cnt_M_lgc[51]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[52]	1	1	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	<b>~</b>
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	~
CTCFailedBuf_Cnt_M_lgc[62]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[63]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[64]	1	1	~
CTCFailedBuf_Cnt_M_lgc[65]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[66]	1	1	~
CTCFailedBuf_Cnt_M_lgc[67]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[68]	1	1	~
CTCFailedBuf Cnt M lgc[69]	1	1	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	1	1	_
CTCFailedBuf_Cnt_M_lgc[71]	1	1	~
CTCFailedBuf_Cnt_M_lgc[72]	1	1	~
CTCFailedBuf_Cnt_M_lgc[73]	1	1	•
CTCFailedBuf_Cnt_M_lgc[74]	1	1	
CTCFailedBuf_Cnt_M_lgc[75]	1	1	•
CTCFailedBuf Cnt M lgc[76]	1	1	
CTCFailed_Cnt_M_lgc	1	1	-
Demlf_DTCStatusChanged()	0	0	
	1	1	
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc(data)	1	1	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 3.3 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	0	
CTCFailedBuf_Cnt_M_lgc[1]	0	
CTCFailedBuf_Cnt_M_lgc[2]	0	
CTCFailedBuf_Cnt_M_lgc[3]	0	
CTCFailedBuf_Cnt_M_lgc[4]	0	
CTCFailedBuf_Cnt_M_lgc[5]	0	
CTCFailedBuf_Cnt_M_lgc[6]	0	
CTCFailedBuf_Cnt_M_lgc[7]	0	
CTCFailedBuf_Cnt_M_lgc[8]	0	

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	(
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[9]	0
CTCFailedBuf Cnt M lgc[10]	0
CTCFailedBuf_Cnt_M_lgc[11]	0
CTCFailedBuf_Cnt_M_lgc[12]	0
CTCFailedBuf_Cnt_M_lgc[13]	0
CTCFailedBuf_Cnt_M_lgc[14]	0
CTCFailedBuf_Cnt_M_lgc[15]	0
CTCFailedBuf_Cnt_M_lgc[16]	0
CTCFailedBuf_Cnt_M_lgc[17]	0
CTCFailedBuf_Cnt_M_lgc[18]	0
CTCFailedBuf_Cnt_M_lgc[19]	0
CTCFailedBuf_Cnt_M_Igc[20]	0
CTCFailedBuf_Cnt_M_Igc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_Igc[23]	0
CTCFailedBuf_Cnt_M_lgc[24]	0
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	0
	0
CTCFailedBuf_Cnt_M_lgc[27]	
CTCFailedBuf_Cnt_M_lgc[28]	0
CTCFailedBuf_Cnt_M_Igc[29]	0
CTCFailedBuf_Cnt_M_lgc[30]	0
CTCFailedBuf_Cnt_M_lgc[31]	0
CTCFailedBuf_Cnt_M_lgc[32]	0
CTCFailedBuf_Cnt_M_Igc[33]	0
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_Igc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_lgc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
	0
CTCFailedBuf_Cnt_M_lgc[44]	
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	0
CTCFailedBuf Cnt M Igc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	0
CTCFailedBuf_Cnt_M_lgc[54]	0
CTCFailedBuf_Cnt_M_Igc[55]	0
CTCFailedBuf_Cnt_M_lgc[56]	0
CTCFailedBuf_Cnt_M_Igc[57]	0
CTCFailedBuf_Cnt_M_lgc[58]	0
CTCFailedBuf_Cnt_M_lgc[59]	0
CTCFailedBuf_Cnt_M_lgc[60]	0
	0
CTCFailedBuf_Cnt_M_lgc[61]	
CTCFailedBuf_Cnt_M_lgc[62]	0
CTCFailedBuf_Cnt_M_lgc[63]	0
CTCFailedBuf_Cnt_M_lgc[64]	0
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_lgc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
	0
CTCFailedBuf_Cnt_M_lgc[70]	
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
	0
CTCFailedBuf Cnt M lgc[76]	
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
CTCFailed_Cnt_M_lgc DTC	0
CTCFailed_Cnt_M_lgc DTC DTCKind	0
CTCFailed_Cnt_M_lgc DTC	0

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Demlf_DTCStatusChanged		TAACILAG
Name	Input Value	
Dem_DTCNumberTable[0]	0	
Dem_DTCNumberTable[1]	0	
Dem_DTCNumberTable[2]	0	
Dem_DTCNumberTable[3]	0	
Dem_DTCNumberTable[4]	0	
Dem_DTCNumberTable[5]	0	
Dem_DTCNumberTable[6]	0	
Dem_DTCNumberTable[7]	0	
Dem_DTCNumberTable[8]	0	
Dem_DTCNumberTable[9]	0	
Dem_DTCNumberTable[10]	0	
Dem_DTCNumberTable[11]	0	
Dem_DTCNumberTable[12]	0	
Dem_DTCNumberTable[13]	0	
Dem_DTCNumberTable[14]	0	
Dem_DTCNumberTable[15]	0	
Dem_DTCNumberTable[16]	0	
Dem_DTCNumberTable[17]	0	
Dem_DTCNumberTable[18]	0	
Dem_DTCNumberTable[19]	0	
Dem_DTCNumberTable[20]	0	
Dem_DTCNumberTable[21]	0	
Dem_DTCNumberTable[22]	0	
Dem_DTCNumberTable[23]	0	
Dem_DTCNumberTable[24]	0	
Dem_DTCNumberTable[25]	0	
Dem_DTCNumberTable[26]	0	
Dem_DTCNumberTable[27]	0	
Dem_DTCNumberTable[28]	0	
Dem_DTCNumberTable[29]	0	
Dem_DTCNumberTable[30]	0	
Dem_DTCNumberTable[31]	0	
Dem_DTCNumberTable[32]	0	
Dem_DTCNumberTable[33]	0	
Dem_DTCNumberTable[34]	0	
Dem_DTCNumberTable[35]	0	
Dem_DTCNumberTable[36]	0	
Dem_DTCNumberTable[37]	0	
Dem DTCNumberTable[38]	0	
Dem_DTCNumberTable[39]	0	
Dem_DTCNumberTable[40]	0	
Dem DTCNumberTable[41]	0	
Dem DTCNumberTable[42]	0	
Dem DTCNumberTable[43]	0	
Dem_DTCNumberTable[44]	0	
Dem_DTCNumberTable[45]	0	
Dem_DTCNumberTable[46]	0	
Dem DTCNumberTable[47]	0	
Dem DTCNumberTable[48]	0	
Dem_DTCNumberTable[49]	0	
Dem DTCNumberTable[50]	0	
Dem_DTCNumberTable[51]	0	
Dem DTCNumberTable[52]	0	
Dem_DTCNumberTable[53]	0	
Dem_DTCNumberTable[54]	0	
Dem_DTCNumberTable[55]	0	
Dem_DTCNumberTable[56]	0	
Dem_DTCNumberTable[57]	0	
Dem_DTCNumberTable[57]	0	
Dem_DTCNumberTable[56]	0	
Dem_DTCNumberTable[59]	0	
Dem_DTCNumberTable[60]	0	
Dem_DTCNumberTable[62]	0	
Dem_DTCNumberTable[63]	0	
Dem_DTCNumberTable[63]	0	
	0	
Dem_DTCNumberTable[65]		
Dem_DTCNumberTable[66]	0	
Dem_DTCNumberTable[67]	0	
Dem_DTCNumberTable[68]	0	
Dem_DTCNumberTable[69]	0	
Dem_DTCNumberTable[70]	0	
Dem_DTCNumberTable[71]	0	
Dem_DTCNumberTable[72]	0	

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Demlf\_DTCStatusChanged Input Value Dem\_DTCNumberTable[73] 0 Dem\_DTCNumberTable[74] 0 Dem\_DTCNumberTable[75] 0 Dem\_DTCNumberTable[76] 0 Dem\_DTC\_FTB\_Table[0] 0 Dem\_DTC\_FTB\_Table[1] 0 Dem\_DTC\_FTB\_Table[2] 0 Dem\_DTC\_FTB\_Table[3] 0 Dem\_DTC\_FTB\_Table[4] 0 Dem\_DTC\_FTB\_Table[5] n Dem\_DTC\_FTB\_Table[6] 0 Dem\_DTC\_FTB\_Table[7] n Dem\_DTC\_FTB\_Table[8] 0 Dem DTC FTB Table[9] n Dem\_DTC\_FTB\_Table[10] 0 Dem\_DTC\_FTB\_Table[11] 0 Dem\_DTC\_FTB\_Table[12] 0 Dem\_DTC\_FTB\_Table[13] 0 Dem\_DTC\_FTB\_Table[14] 0 Dem\_DTC\_FTB\_Table[15] 0 Dem\_DTC\_FTB\_Table[16] 0 Dem\_DTC\_FTB\_Table[17] 0 Dem\_DTC\_FTB\_Table[18] 0 Dem\_DTC\_FTB\_Table[19] 0 Dem\_DTC\_FTB\_Table[20] 0 Dem\_DTC\_FTB\_Table[21] 0 Dem\_DTC\_FTB\_Table[22] 0 Dem\_DTC\_FTB\_Table[23] 0 Dem\_DTC\_FTB\_Table[24] 0 Dem\_DTC\_FTB\_Table[25] 0 Dem DTC FTB Table[26] 0 Dem\_DTC\_FTB\_Table[27] 0 Dem DTC FTB Table[28] 0 Dem\_DTC\_FTB\_Table[29] 0 Dem\_DTC\_FTB\_Table[30] 0 Dem\_DTC\_FTB\_Table[31] 0 Dem\_DTC\_FTB\_Table[32] 0 Dem\_DTC\_FTB\_Table[33] 0 Dem\_DTC\_FTB\_Table[34] 0 Dem DTC\_FTB\_Table[35] 0 Dem\_DTC\_FTB\_Table[36] 0 Dem DTC FTB Table[37] 0 Dem\_DTC\_FTB\_Table[38] 0 Dem\_DTC\_FTB\_Table[39] 0 Dem\_DTC\_FTB\_Table[40] 0 Dem\_DTC\_FTB\_Table[41] 0 Dem\_DTC\_FTB\_Table[42] 0 Dem\_DTC\_FTB\_Table[43] 0 Dem\_DTC\_FTB\_Table[44] 0 Dem\_DTC\_FTB\_Table[45] 0 Dem\_DTC\_FTB\_Table[46] 0 Dem\_DTC\_FTB\_Table[47] 0 Dem\_DTC\_FTB\_Table[48] 0 Dem\_DTC\_FTB\_Table[49] 0 Dem\_DTC\_FTB\_Table[50] 0 Dem\_DTC\_FTB\_Table[51] 0 0 Dem\_DTC\_FTB\_Table[52] Dem\_DTC\_FTB\_Table[53] 0 Dem\_DTC\_FTB\_Table[54] 0 Dem\_DTC\_FTB\_Table[55] 0 Dem\_DTC\_FTB\_Table[56] 0 Dem\_DTC\_FTB\_Table[57] 0 Dem\_DTC\_FTB\_Table[58] 0 Dem\_DTC\_FTB\_Table[59] 0 Dem\_DTC\_FTB\_Table[60] 0 Dem DTC FTB Table[61] 0 Dem\_DTC\_FTB\_Table[62] 0 Dem DTC FTB Table[63] 0 Dem\_DTC\_FTB\_Table[64] 0 Dem\_DTC\_FTB\_Table[65] 0 Dem\_DTC\_FTB\_Table[66] 0

0

0

Dem\_DTC\_FTB\_Table[67]

Dem\_DTC\_FTB\_Table[68]

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Input Value Dem\_DTC\_FTB\_Table[69] 0 Dem\_DTC\_FTB\_Table[70] 0 Dem DTC\_FTB\_Table[71] 0 Dem\_DTC\_FTB\_Table[72] 0 Dem\_DTC\_FTB\_Table[73] 0 Dem\_DTC\_FTB\_Table[74] 0 Dem\_DTC\_FTB\_Table[75] 0 Dem\_DTC\_FTB\_Table[76] 0 **Actual Value Expected Value** Name Result CTCFailedBuf\_Cnt\_M\_lgc[0] 0 CTCFailedBuf\_Cnt\_M\_lgc[1] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[2] 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[3] 0 CTCFailedBuf\_Cnt\_M\_lgc[4] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[5] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[6] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[7] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[8] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[9] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[10] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[11] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[12] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[13] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[14] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[15] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[16] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[17] 0 0 CTCFailedBuf Cnt M Igc[18] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[19] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[20] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[21] 0 0 CTCFailedBuf Cnt M Igc[22] 0 0 CTCFailedBuf\_Cnt\_M\_Igc[23] 0 0 CTCFailedBuf Cnt M Igc[24] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[25] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[26] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[27]$ 0 0 0 CTCFailedBuf\_Cnt\_M\_lgc[28] 0 CTCFailedBuf\_Cnt\_M\_lgc[29] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[30] 0 0 CTCFailedBuf Cnt M lqc[31] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[32] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[33] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[34] 0 0 **~** CTCFailedBuf\_Cnt\_M\_lgc[35] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[36] n n CTCFailedBuf\_Cnt\_M\_lgc[37] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[38] n 0 CTCFailedBuf\_Cnt\_M\_lgc[39] 0 0 CTCFailedBuf Cnt M Igc[40] n 0 CTCFailedBuf\_Cnt\_M\_lgc[41] 0 0 CTCFailedBuf Cnt M Igc[42] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[43] 0 0 CTCFailedBuf Cnt M lqc[44] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[45] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[46] 0 0  $CTCFailedBuf\_Cnt\_M\_lgc[47]$ 0 0 CTCFailedBuf\_Cnt\_M\_lgc[48] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[49] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[50] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[51] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[52] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[53] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[54] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[55] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[56] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[57] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[58] 0 0 CTCFailedBuf Cnt M lqc[59] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[60] n 0 CTCFailedBuf\_Cnt\_M\_lgc[61] 0 0 ~ CTCFailedBuf\_Cnt\_M\_lgc[62] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[63] 0 0

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**Actual Value Expected Value** CTCFailedBuf\_Cnt\_M\_lgc[64] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[65] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[66] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[67] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[68] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[69] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[70] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[71] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[72] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[73] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[74] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[75] 0 0 CTCFailedBuf\_Cnt\_M\_lgc[76] 0 0 CTCFailed\_Cnt\_M\_lgc 0 0 DemIf\_DTCStatusChanged() 0 0 Rte\_Write\_Ap\_Demlf\_CTCFailed\_Cnt\_lgc(data) 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	~

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value
CTCFailedBuf_Cnt_M_lgc[0]	1
CTCFailedBuf_Cnt_M_lgc[1]	1
CTCFailedBuf_Cnt_M_lgc[2]	1
CTCFailedBuf_Cnt_M_lgc[3]	1
CTCFailedBuf_Cnt_M_lgc[4]	1
CTCFailedBuf_Cnt_M_lgc[5]	1
CTCFailedBuf_Cnt_M_lgc[6]	1
CTCFailedBuf_Cnt_M_lgc[7]	1
CTCFailedBuf_Cnt_M_lgc[8]	1
CTCFailedBuf_Cnt_M_lgc[9]	1
CTCFailedBuf_Cnt_M_lgc[10]	1
CTCFailedBuf_Cnt_M_lgc[11]	1
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf Cnt M lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
CTCFailedBuf_Cnt_M_lgc[17]	1
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf Cnt M Igc[20]	1
CTCFailedBuf_Cnt_M_lgc[21]	1
CTCFailedBuf_Cnt_M_lgc[22]	1
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	1
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	1
CTCFailedBuf_Cnt_M_lgc[35]	1
CTCFailedBuf_Cnt_M_lgc[36]	1
CTCFailedBuf Cnt M Igc[37]	1
CTCFailedBuf_Cnt_M_lgc[38]	1
CTCFailedBuf_Cnt_M_lgc[39]	1
CTCFailedBuf_Cnt_M_lgc[40]	1
CTCFailedBuf_Cnt_M_lgc[41]	1
CTCFailedBuf_Cnt_M_lgc[41] CTCFailedBuf_Cnt_M_lgc[42]	1
CTCFailedBuf_Cnt_M_lgc[42] CTCFailedBuf_Cnt_M_lgc[43]	1
	1
CTCFailedBuf_Cnt_M_lgc[44]	1
CTCFailedBuf_Cnt_M_lgc[45]	1
CTCFailedBuf_Cnt_M_lgc[46]	<u>                                     </u>

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[47]	1
CTCFailedBuf_Cnt_M_lgc[48]	1
CTCFailedBuf_Cnt_M_lgc[49]	1
CTCFailedBuf_Cnt_M_lgc[50]	1
CTCFailedBuf_Cnt_M_lgc[51]	1.
CTCFailedBuf_Cnt_M_lgc[52]	1
CTCFailedBuf_Cnt_M_lgc[53]	1.
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1.
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_Igc[57]	1.
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_Igc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	1
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	1
CTCFailedBuf_Cnt_M_lgc[66]	1
CTCFailedBuf_Cnt_M_lgc[67]	1
CTCFailedBuf_Cnt_M_lgc[68]	1
CTCFailedBuf_Cnt_M_lgc[69]	1
CTCFailedBuf_Cnt_M_lgc[70]	1
CTCFailedBuf_Cnt_M_lgc[71]	1
CTCFailedBuf_Cnt_M_lgc[72]	1
CTCFailedBuf_Cnt_M_lgc[73]	1
CTCFailedBuf_Cnt_M_lgc[74]	1
CTCFailedBuf_Cnt_M_lgc[75]	1
CTCFailedBuf_Cnt_M_lgc[76]	1
CTCFailed_Cnt_M_lgc	1
DTC	4294967295
DTCKind	2
DTCStatusNew	255
DTCStatusOld	255
Dem_DTCNumberTable[0]	65535
Dem_DTCNumberTable[1]	65535
Dem_DTCNumberTable[2]	65535
Dem_DTCNumberTable[3]	65535
Dem_DTCNumberTable[4]	65535
Dem_DTCNumberTable[5]	65535
Dem_DTCNumberTable[6]	65535
Dem_DTCNumberTable[7]	65535 65535
Dem_DTCNumberTable[8]	
Dem_DTCNumberTable[9]	65535 65535
Dem_DTCNumberTable[10]	
Dem_DTCNumberTable[11]	65535
Dem_DTCNumberTable[12] Dem_DTCNumberTable[13]	65535 65535
Dem_DTCNumberTable[14] Dem_DTCNumberTable[15]	65535 65535
Dem_D1CNumber1able[15] Dem DTCNumberTable[16]	65535
Dem_DTCNumberTable[16] Dem_DTCNumberTable[17]	65535
Dem DTCNumberTable[17] Dem DTCNumberTable[18]	65535
Dem_DTCNumberTable[19]	65535
Dem DTCNumberTable[19] Dem DTCNumberTable[20]	65535
Dem_DTCNumberTable[20]	65535
Dem_DTCNumberTable[21] Dem_DTCNumberTable[22]	65535
Dem_DTCNumberTable[23]	65535
Dem_DTCNumberTable[24]	65535
Dem_DTCNumberTable[25]	65535
Dem_DTCNumberTable[26]	65535
Dem_DTCNumberTable[27]	65535
Dem_DTCNumberTable[28]	65535
Dem_DTCNumberTable[29]	65535
Dem_DTCNumberTable[29] Dem_DTCNumberTable[30]	65535
Dem_DTCNumberTable[30]	65535
Dem_DTCNumberTable[31] Dem_DTCNumberTable[32]	65535
Dem_DTCNumberTable[32] Dem_DTCNumberTable[33]	65535
Dem_DTCNumberTable[33] Dem_DTCNumberTable[34]	65535
Dem_DTCNumberTable[34] Dem_DTCNumberTable[35]	65535
	65535
Dem_DTCNumberTable[36] Dem_DTCNumberTable[37]	65535 65535

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	MACIMU
Name	Input Value
Dem_DTCNumberTable[38]	65535
Dem_DTCNumberTable[39]	65535
Dem_DTCNumberTable[40]	65535
Dem_DTCNumberTable[41]	65535
Dem_DTCNumberTable[42]	65535
Dem_DTCNumberTable[43]	65535
Dem_DTCNumberTable[44]	65535
Dem_DTCNumberTable[44]	65535
Dem_DTCNumberTable[46]	65535
Dem_DTCNumberTable[47]	65535
Dem_DTCNumberTable[48]	65535
Dem_DTCNumberTable[49]	65535
Dem_DTCNumberTable[50]	65535
Dem_DTCNumberTable[51]	65535
Dem_DTCNumberTable[52]	65535
Dem_DTCNumberTable[53]	65535
Dem_DTCNumberTable[54]	65535
Dem_DTCNumberTable[55]	65535
Dem_DTCNumberTable[56]	65535
Dem_DTCNumberTable[57]	65535
Dem_DTCNumberTable[58]	65535
Dem_DTCNumberTable[59]	65535
Dem_DTCNumberTable[60]	65535
Dem_DTCNumberTable[61]	65535
Dem_DTCNumberTable[62]	65535
Dem_DTCNumberTable[63]	65535
Dem_DTCNumberTable[64]	65535
Dem_DTCNumberTable[65]	65535
Dem_DTCNumberTable[66]	65535
Dem_DTCNumberTable[67]	65535
Dem_DTCNumberTable[68]	65535
Dem_DTCNumberTable[69]	65535
Dem_DTCNumberTable[70]	65535
Dem_DTCNumberTable[71]	65535
Dem_DTCNumberTable[72]	65535
Dem_DTCNumberTable[73]	65535
Dem_DTCNumberTable[74]	65535
Dem_DTCNumberTable[75]	65535
Dem_DTCNumberTable[76]	65535
Dem_DTC_FTB_Table[0]	255
Dem_DTC_FTB_Table[1]	255
Dem DTC FTB Table[2]	255
Dem_DTC_FTB_Table[3]	255
Dem_DTC_FTB_Table[4]	255
Dem_DTC_FTB_Table[5]	255
Dem_DTC_FTB_Table[6]	255
Dem DTC FTB Table[7]	255
Dem_DTC_FTB_Table[8]	255
Dem_DTC_FTB_Table[9]	255
Dem_DTC_FTB_Table[10]	255
Dem DTC FTB Table[11]	255
Dem_DTC_FTB_Table[11] Dem_DTC_FTB_Table[12]	255
Dem_DTC_FTB_Table[13]	255
Dem_DTC_FTB_Table[13]	255
	255
Dem_DTC_FTB_Table[15]	
Dem_DTC_FTB_Table[16]	255
Dem_DTC_FTB_Table[17]	255
Dem_DTC_FTB_Table[18]	255
Dem_DTC_FTB_Table[19]	255
Dem_DTC_FTB_Table[20]	255
Dem_DTC_FTB_Table[21]	255
Dem_DTC_FTB_Table[22]	255
Dem_DTC_FTB_Table[23]	255
Dem_DTC_FTB_Table[24]	255
Dem_DTC_FTB_Table[25]	255
Dem_DTC_FTB_Table[26]	255
Dem_DTC_FTB_Table[27]	255
Dem_DTC_FTB_Table[28]	255
Dem_DTC_FTB_Table[29]	255
D. DTO FTD T II 1991	255
Dem_DTC_FTB_Table[30]	
Dem_DTC_FTB_Table[30] Dem_DTC_FTB_Table[31]	255
	255 255

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lame	Input Value		
Dem_DTC_FTB_Table[34]	255		
em_DTC_FTB_Table[35]	255		
em_DTC_FTB_Table[36]	255		
em_DTC_FTB_Table[37]	255		
em_DTC_FTB_Table[38]	255		
Dem_DTC_FTB_Table[39]	255		
em_DTC_FTB_Table[40]	255		
Dem_DTC_FTB_Table[41]	255		
Dem_DTC_FTB_Table[42]	255		
em_DTC_FTB_Table[43]	255		
Dem_DTC_FTB_Table[44]	255		
em_DTC_FTB_Table[45]	255		
em_DTC_FTB_Table[46]	255		
em_DTC_FTB_Table[47]	255		
em_DTC_FTB_Table[48]	255		
em_DTC_FTB_Table[49]	255		
em_DTC_FTB_Table[50]	255		
em_DTC_FTB_Table[51]	255		
em_DTC_FTB_Table[52]	255		
em_DTC_FTB_Table[53]	255		
em_DTC_FTB_Table[54]	255		
em_DTC_FTB_Table[55]	255		
em_DTC_FTB_Table[56]	255		
em_DTC_FTB_Table[57]	255		
em_DTC_FTB_Table[58]	255		
em_DTC_FTB_Table[59]	255		
em_DTC_FTB_Table[60]	255		
em_DTC_FTB_Table[61]	255		
em_DTC_FTB_Table[62]	255		
em_DTC_FTB_Table[63]	255		
em_DTC_FTB_Table[64]	255		
em_DTC_FTB_Table[65]	255		
em_DTC_FTB_Table[66]	255		
em_DTC_FTB_Table[67]	255		
em_DTC_FTB_Table[68]	255		
em_DTC_FTB_Table[69]	255		
em_DTC_FTB_Table[70]	255		
em_DTC_FTB_Table[71]	255		
em_DTC_FTB_Table[71] em_DTC_FTB_Table[72]	255 255		
em_DTC_FTB_Table[72]			
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73]	255		
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74]	255 255		
	255 255 255		
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75]	255 255 255 255 255	Expected Value	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] ame	255 255 255 255 255 255 <b>Actual Value</b>	·	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] ame  TCFailedBuf_Cnt_M_lgc[0]	255 255 255 255 255 255 <b>Actual Value</b> 1	1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1]	255 255 255 255 255 255 <b>Actual Value</b> 1	·	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_CTC_FAiledBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2]	255 255 255 255 255 255 <b>Actual Value</b> 1 1	1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_CTC_FailedBuf_Cnt_M_lgc[0] "CFailedBuf_Cnt_M_lgc[1] "CFailedBuf_Cnt_M_lgc[2] "CFailedBuf_Cnt_M_lgc[3]	255 255 255 255 255 255 <b>Actual Value</b> 1 1 1	1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_CTC_FailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4]	255 255 255 255 255 <b>Actual Value</b> 1 1 1 1	1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 <b>Actual Value</b> 1 1 1 1 1 1	1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FTB_Table[72] em_DTC_FT	255 255 255 255 255 255 <b>Actual Value</b> 1 1 1 1 1 1 1	1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 <b>Actual Value</b> 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255 <b>Actual Value</b> 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 <b>Actual Value</b> 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	Rest
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_DTC_FTB_Table[76] em_DTC_FailedBuf_Cnt_M_lgc[0] rCFailedBuf_Cnt_M_lgc[1] rCFailedBuf_Cnt_M_lgc[3] rCFailedBuf_Cnt_M_lgc[4] rCFailedBuf_Cnt_M_lgc[6] rCFailedBuf_Cnt_M_lgc[6] rCFailedBuf_Cnt_M_lgc[7] rCFailedBuf_Cnt_M_lgc[8] rCFailedBuf_Cnt_M_lgc[9] rCFailedBuf_Cnt_M_lgc[10] rCFailedBuf_Cnt_M_lgc[11] rCFailedBuf_Cnt_M_lgc[12] rCFailedBuf_Cnt_M_lgc[13] rCFailedBuf_Cnt_M_lgc[13] rCFailedBuf_Cnt_M_lgc[13] rCFailedBuf_Cnt_M_lgc[14]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
m_DTC_FTB_Table[72] m_DTC_FTB_Table[73] m_DTC_FTB_Table[74] m_DTC_FTB_Table[75] m_DTC_FTB_Table[76] m_DTC_FTB_Table[76] m_DTC_FTB_Table[76] mme  CFailedBuf_Cnt_M_lgc[0] CFailedBuf_Cnt_M_lgc[1] CFailedBuf_Cnt_M_lgc[2] CFailedBuf_Cnt_M_lgc[3] CFailedBuf_Cnt_M_lgc[4] CFailedBuf_Cnt_M_lgc[6] CFailedBuf_Cnt_M_lgc[6] CFailedBuf_Cnt_M_lgc[7] CFailedBuf_Cnt_M_lgc[7] CFailedBuf_Cnt_M_lgc[8] CFailedBuf_Cnt_M_lgc[9] CFailedBuf_Cnt_M_lgc[10] CFailedBuf_Cnt_M_lgc[11] CFailedBuf_Cnt_M_lgc[12] CFailedBuf_Cnt_M_lgc[13] CFailedBuf_Cnt_M_lgc[14] CFailedBuf_Cnt_M_lgc[15] CFailedBuf_Cnt_M_lgc[16] CFailedBuf_Cnt_M_lgc[16] CFailedBuf_Cnt_M_lgc[17] CFailedBuf_Cnt_M_lgc[18] CFailedBuf_Cnt_M_lgc[18] CFailedBuf_Cnt_M_lgc[18] CFailedBuf_Cnt_M_lgc[18] CFailedBuf_Cnt_M_lgc[19]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] em_DTC_FT	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resi
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76]  ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4] TCFailedBuf_Cnt_M_lgc[5] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[8] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[11] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[15] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[17] TCFailedBuf_Cnt_M_lgc[18] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[20] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76]  ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4] TCFailedBuf_Cnt_M_lgc[5] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[8] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[11] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[13] TCFailedBuf_Cnt_M_lgc[14] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[17] TCFailedBuf_Cnt_M_lgc[18] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[20] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[22] TCFailedBuf_Cnt_M_lgc[23]	255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76]  ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4] TCFailedBuf_Cnt_M_lgc[5] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[9] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[11] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[13] TCFailedBuf_Cnt_M_lgc[14] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[20] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[22] TCFailedBuf_Cnt_M_lgc[23] TCFailedBuf_Cnt_M_lgc[23] TCFailedBuf_Cnt_M_lgc[24]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76]  ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4] TCFailedBuf_Cnt_M_lgc[5] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[8] TCFailedBuf_Cnt_M_lgc[9] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[11] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[14] TCFailedBuf_Cnt_M_lgc[15] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[17] TCFailedBuf_Cnt_M_lgc[18] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[20] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[22] TCFailedBuf_Cnt_M_lgc[23] TCFailedBuf_Cnt_M_lgc[24] TCFailedBuf_Cnt_M_lgc[25]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76] ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[8] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[11] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[13] TCFailedBuf_Cnt_M_lgc[13] TCFailedBuf_Cnt_M_lgc[15] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[17] TCFailedBuf_Cnt_M_lgc[18] TCFailedBuf_Cnt_M_lgc[18] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[20] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[22] TCFailedBuf_Cnt_M_lgc[23] TCFailedBuf_Cnt_M_lgc[25] TCFailedBuf_Cnt_M_lgc[25] TCFailedBuf_Cnt_M_lgc[25] TCFailedBuf_Cnt_M_lgc[25] TCFailedBuf_Cnt_M_lgc[26]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu
em_DTC_FTB_Table[72] em_DTC_FTB_Table[73] em_DTC_FTB_Table[74] em_DTC_FTB_Table[75] em_DTC_FTB_Table[76]  ame  TCFailedBuf_Cnt_M_lgc[0] TCFailedBuf_Cnt_M_lgc[1] TCFailedBuf_Cnt_M_lgc[2] TCFailedBuf_Cnt_M_lgc[3] TCFailedBuf_Cnt_M_lgc[4] TCFailedBuf_Cnt_M_lgc[5] TCFailedBuf_Cnt_M_lgc[6] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[7] TCFailedBuf_Cnt_M_lgc[8] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[10] TCFailedBuf_Cnt_M_lgc[11] TCFailedBuf_Cnt_M_lgc[12] TCFailedBuf_Cnt_M_lgc[13] TCFailedBuf_Cnt_M_lgc[14] TCFailedBuf_Cnt_M_lgc[15] TCFailedBuf_Cnt_M_lgc[16] TCFailedBuf_Cnt_M_lgc[17] TCFailedBuf_Cnt_M_lgc[18] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[19] TCFailedBuf_Cnt_M_lgc[20] TCFailedBuf_Cnt_M_lgc[21] TCFailedBuf_Cnt_M_lgc[22] TCFailedBuf_Cnt_M_lgc[23] TCFailedBuf_Cnt_M_lgc[23] TCFailedBuf_Cnt_M_lgc[24] TCFailedBuf_Cnt_M_lgc[25]	255 255 255 255 255 255  Actual Value  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Resu

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Name	Actual Value	Expected Value	Resul
CTCFailedBuf_Cnt_M_lgc[29]	1	1	
CTCFailedBuf_Cnt_M_lgc[30]	1	1	
CTCFailedBuf_Cnt_M_lgc[31]	1	1	•
CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[33]	1	1	
CTCFailedBuf_Cnt_M_lgc[34]	1	1	
CTCFailedBuf_Cnt_M_lgc[35]	1	1	
CTCFailedBuf_Cnt_M_lgc[36]	1	1	
CTCFailedBuf_Cnt_M_lgc[37]	1	1	
CTCFailedBuf_Cnt_M_lgc[38]	1	1	
CTCFailedBuf_Cnt_M_lgc[39]	1	1	
CTCFailedBuf Cnt M lgc[40]	1	1	
CTCFailedBuf_Cnt_M_lgc[41]	1	1	
CTCFailedBuf_Cnt_M_lgc[42]	1	1	
CTCFailedBuf_Cnt_M_lgc[42]	1	1	
	1	1	
CTCFailedBuf_Cnt_M_lgc[44]	1	1	
CTCFailedBuf_Cnt_M_lgc[45]	1	1	
CTCFailedBuf_Cnt_M_lgc[46]		1	
CTCFailedBuf_Cnt_M_lgc[47]	1		
CTCFailedBuf_Cnt_M_lgc[48]	1	1	
CTCFailedBuf_Cnt_M_lgc[49]	1	1	•
CTCFailedBuf_Cnt_M_lgc[50]	1	1	
CTCFailedBuf_Cnt_M_lgc[51]	1	1	•
CTCFailedBuf_Cnt_M_lgc[52]	1	1	•
CTCFailedBuf_Cnt_M_lgc[53]	1	1	•
CTCFailedBuf_Cnt_M_lgc[54]	1	1	•
CTCFailedBuf_Cnt_M_lgc[55]	1	1	•
CTCFailedBuf_Cnt_M_lgc[56]	1	1	•
CTCFailedBuf_Cnt_M_Igc[57]	1	1	•
CTCFailedBuf_Cnt_M_lgc[58]	1	1	•
CTCFailedBuf_Cnt_M_Igc[59]	1	1	•
CTCFailedBuf_Cnt_M_lgc[60]	1	1	
CTCFailedBuf_Cnt_M_lgc[61]	1	1	•
CTCFailedBuf_Cnt_M_lgc[62]	1	1	
CTCFailedBuf_Cnt_M_lgc[63]	1	1	•
CTCFailedBuf_Cnt_M_lgc[64]	1	1	
CTCFailedBuf_Cnt_M_lgc[65]	1	1	
CTCFailedBuf_Cnt_M_lgc[66]	1	1	
CTCFailedBuf_Cnt_M_lgc[67]	1	1	
CTCFailedBuf_Cnt_M_lgc[68]	1	1	
CTCFailedBuf_Cnt_M_lgc[69]	1	1	
CTCFailedBuf_Cnt_M_lgc[70]	1	1	
CTCFailedBuf_Cnt_M_lgc[71]	1	1	
CTCFailedBuf_Cnt_M_lgc[72]	1	1	
CTCFailedBuf_Cnt_M_lgc[73]	1	1	
CTCFailedBuf_Cnt_M_lgc[74]	1	1	
CTCFailedBuf_Cnt_M_lgc[75]	1	1	
CTCFailedBuf_Cnt_M_lgc[76]	1	1	
CTCFailed_Cnt_M_lgc	1	1	
Demlf_DTCStatusChanged()	0	0	
Delliii_D i OolalusOllaligeu()	U	U	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte Write Ap Demlf CTCFailed Cnt lgc	1	Rte Write Ap Demlf CTCFailed Cnt lgc	1	_

Test Step 3.5 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
CTCFailedBuf_Cnt_M_lgc[0]	1	
CTCFailedBuf_Cnt_M_lgc[1]	1	
CTCFailedBuf_Cnt_M_lgc[2]	1	
CTCFailedBuf_Cnt_M_lgc[3]	1	
CTCFailedBuf_Cnt_M_lgc[4]	1	
CTCFailedBuf_Cnt_M_lgc[5]	0	
CTCFailedBuf_Cnt_M_lgc[6]	1	
CTCFailedBuf_Cnt_M_lgc[7]	1	
CTCFailedBuf_Cnt_M_lgc[8]	1	
CTCFailedBuf_Cnt_M_lgc[9]	1	
CTCFailedBuf_Cnt_M_lgc[10]	1	
CTCFailedBuf_Cnt_M_lgc[11]	1	

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Name	Input Value
CTCFailedBuf_Cnt_M_lgc[12]	1
CTCFailedBuf_Cnt_M_lgc[13]	1
CTCFailedBuf_Cnt_M_lgc[14]	1
CTCFailedBuf_Cnt_M_lgc[15]	1
CTCFailedBuf_Cnt_M_lgc[16]	1
	1
CTCFailedBuf_Cnt_M_lgc[17]	
CTCFailedBuf_Cnt_M_lgc[18]	1
CTCFailedBuf_Cnt_M_lgc[19]	1
CTCFailedBuf_Cnt_M_lgc[20]	0
CTCFailedBuf_Cnt_M_lgc[21]	0
CTCFailedBuf_Cnt_M_lgc[22]	0
CTCFailedBuf_Cnt_M_lgc[23]	1
CTCFailedBuf_Cnt_M_lgc[24]	1
CTCFailedBuf_Cnt_M_lgc[25]	0
CTCFailedBuf_Cnt_M_lgc[26]	1
CTCFailedBuf_Cnt_M_lgc[27]	1
CTCFailedBuf_Cnt_M_lgc[28]	1
CTCFailedBuf_Cnt_M_lgc[29]	1
CTCFailedBuf_Cnt_M_lgc[30]	1
CTCFailedBuf_Cnt_M_lgc[31]	1
CTCFailedBuf_Cnt_M_lgc[32]	1
CTCFailedBuf_Cnt_M_lgc[33]	1
CTCFailedBuf_Cnt_M_lgc[34]	0
CTCFailedBuf_Cnt_M_lgc[35]	0
CTCFailedBuf_Cnt_M_lgc[36]	0
CTCFailedBuf_Cnt_M_lgc[37]	0
CTCFailedBuf_Cnt_M_lgc[38]	0
CTCFailedBuf_Cnt_M_Igc[39]	0
CTCFailedBuf_Cnt_M_lgc[40]	0
CTCFailedBuf_Cnt_M_lgc[41]	0
CTCFailedBuf_Cnt_M_lgc[42]	0
CTCFailedBuf_Cnt_M_lgc[43]	0
CTCFailedBuf_Cnt_M_lgc[44]	0
CTCFailedBuf_Cnt_M_lgc[45]	0
CTCFailedBuf_Cnt_M_lgc[46]	0
	0
CTCFailedBuf_Cnt_M_lgc[47]	0
CTCFailedBuf_Cnt_M_lgc[48]	0
CTCFailedBuf_Cnt_M_lgc[49]	0
CTCFailedBuf_Cnt_M_lgc[50]	
CTCFailedBuf_Cnt_M_lgc[51]	0
CTCFailedBuf_Cnt_M_lgc[52]	0
CTCFailedBuf_Cnt_M_lgc[53]	1
CTCFailedBuf_Cnt_M_lgc[54]	1
CTCFailedBuf_Cnt_M_lgc[55]	1
CTCFailedBuf_Cnt_M_lgc[56]	1
CTCFailedBuf_Cnt_M_lgc[57]	1
CTCFailedBuf_Cnt_M_lgc[58]	1
CTCFailedBuf_Cnt_M_lgc[59]	1
CTCFailedBuf_Cnt_M_lgc[60]	1
CTCFailedBuf_Cnt_M_lgc[61]	1
CTCFailedBuf_Cnt_M_lgc[62]	1
CTCFailedBuf_Cnt_M_lgc[63]	0
CTCFailedBuf_Cnt_M_lgc[64]	1
CTCFailedBuf_Cnt_M_lgc[65]	0
CTCFailedBuf_Cnt_M_lgc[66]	0
CTCFailedBuf_Cnt_M_Igc[67]	0
CTCFailedBuf_Cnt_M_lgc[68]	0
CTCFailedBuf_Cnt_M_lgc[69]	0
CTCFailedBuf_Cnt_M_lgc[70]	0
CTCFailedBuf_Cnt_M_lgc[71]	0
CTCFailedBuf_Cnt_M_lgc[72]	0
CTCFailedBuf_Cnt_M_lgc[73]	0
CTCFailedBuf_Cnt_M_lgc[74]	0
CTCFailedBuf_Cnt_M_lgc[75]	0
CTCFailedBuf_Cnt_M_lgc[76]	0
CTCFailed_Cnt_M_lgc	0
DTC	0
DTCKind	1
DTCStatusNew	
DTCStatusNew	148 39
Dem_DTCNumberTable[0]	181
Dom DTCNumberTeble[4]	
Dem_DTCNumberTable[1] Dem_DTCNumberTable[2]	1 41

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Demlf_DTCStatusChanged		TAZOI(AL
Name	Input Value	
Dem_DTCNumberTable[3]	22	
Dem_DTCNumberTable[4]	24	
Dem_DTCNumberTable[5]	254	
Dem_DTCNumberTable[6]	209	
Dem_DTCNumberTable[7]	209	
Dem_DTCNumberTable[8]	181	
Dem_DTCNumberTable[9]	1	
Dem_DTCNumberTable[10]	209	
Dem_DTCNumberTable[11]	128	
Dem_DTCNumberTable[12] Dem_DTCNumberTable[13]	209	
Dem_DTCNumberTable[13] Dem_DTCNumberTable[14]	181	
Dem_DTCNumberTable[15]	1	
Dem_DTCNumberTable[16]	1	
Dem_DTCNumberTable[17]	209	
Dem_DTCNumberTable[18]	33	
Dem_DTCNumberTable[19]	181	
Dem_DTCNumberTable[20]	1	
Dem_DTCNumberTable[21]	209	
Dem_DTCNumberTable[22]	181	
Dem_DTCNumberTable[23]	41	
Dem_DTCNumberTable[24]	22	
Dem_DTCNumberTable[25]	24	
Dem_DTCNumberTable[26]	254	
Dem_DTCNumberTable[27]	1	
Dem_DTCNumberTable[28]	181	
Dem_DTCNumberTable[29]	1	
Dem_DTCNumberTable[30]	181	
Dem_DTCNumberTable[31]	181	
Dem_DTCNumberTable[32]	1	
Dem_DTCNumberTable[33]	1	
Dem_DTCNumberTable[34]	181	
Dem_DTCNumberTable[35]	1 181	
Dem_DTCNumberTable[36] Dem_DTCNumberTable[37]	181	
Dem_DTCNumberTable[37]	181	
Dem_DTCNumberTable[39]	1	
Dem_DTCNumberTable[40]	1	
Dem_DTCNumberTable[41]	41	
Dem_DTCNumberTable[42]	22	
Dem_DTCNumberTable[43]	24	
Dem_DTCNumberTable[44]	254	
Dem_DTCNumberTable[45]	209	
Dem_DTCNumberTable[46]	181	
Dem_DTCNumberTable[47]	1	
Dem_DTCNumberTable[48]	22	
Dem_DTCNumberTable[49]	181	
Dem_DTCNumberTable[50]	1	
Dem_DTCNumberTable[51]	181	
Dem_DTCNumberTable[52]	181	
Dem_DTCNumberTable[53]	1	
Dem_DTCNumberTable[54]	22	
Dem_DTCNumberTable[55]	209	
Dem_DTCNumberTable[56]	181	
Dem_DTCNumberTable[57]	1	
Dem_DTCNumberTable[58] Dem_DTCNumberTable[59]	181 209	
Dem_DTCNumberTable[59] Dem_DTCNumberTable[60]	181	
Dem_DTCNumberTable[60]	1	
Dem_DTCNumberTable[62]	22	
Dem_DTCNumberTable[63]	41	
Dem_DTCNumberTable[64]	22	
Dem_DTCNumberTable[65]	24	
Dem_DTCNumberTable[66]	254	
Dem_DTCNumberTable[67]	181	
Dem_DTCNumberTable[68]	181	
Dem_DTCNumberTable[69]	1	
Dem_DTCNumberTable[70]	22	
Dem_DTCNumberTable[71]	209	
Dem_DTCNumberTable[72]	22	
Dem_DTCNumberTable[73]	41	
Dem_DTCNumberTable[74]	22	
Delli_D i Ortalibel rabie[14]	22 24	

Demlf\_DTCStatusChanged

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		(144-16-16-16-16-16-16-16-16-16-16-16-16-16-
Name	Input Value	
Dem_DTCNumberTable[76]	254	
Dem_DTC_FTB_Table[0]	245	
Dem_DTC_FTB_Table[1]	151	
Dem_DTC_FTB_Table[2]	199	
Dem_DTC_FTB_Table[3]	160	
Dem_DTC_FTB_Table[4]	30	
Dem_DTC_FTB_Table[5]	136	
Dem_DTC_FTB_Table[6]	178	
Dem_DTC_FTB_Table[7]	178	
Dem_DTC_FTB_Table[8]	245	
Dem_DTC_FTB_Table[9]	151	
Dem_DTC_FTB_Table[10]	178	
Dem_DTC_FTB_Table[11]	31	
Dem_DTC_FTB_Table[12]	151	
Dem_DTC_FTB_Table[13]	178	
Dem_DTC_FTB_Table[14]	245	
Dem_DTC_FTB_Table[15]	151	
Dem_DTC_FTB_Table[16]	151	
Dem_DTC_FTB_Table[17]	178	
Dem_DTC_FTB_Table[18]	234	
	245	
Dem_DTC_FTB_Table[19] Dem_DTC_FTB_Table[20]	151	
Dem_DTC_FTB_Table[20]	178	
Dem_DTC_FTB_Table[21]	245	
Dem_DTC_FTB_Table[22] Dem_DTC_FTB_Table[23]	199	
	160	
Dem_DTC_FTB_Table[24] Dem_DTC_FTB_Table[25]	30	
Dem_DTC_FTB_Table[26]	136	
	151	
Dem_DTC_FTB_Table[27]	245	
Dem_DTC_FTB_Table[28]	151	
Dem_DTC_FTB_Table[29]	245	
Dem_DTC_FTB_Table[30]	245	
Dem_DTC_FTB_Table[31]	151	
Dem_DTC_FTB_Table[32] Dem_DTC_FTB_Table[33]	151	
Dem_DTC_FTB_Table[33]	245	
Dem_DTC_FTB_Table[34]	151	
	245	
Dem_DTC_FTB_Table[36] Dem_DTC_FTB_Table[37]	245	
	245	
Dem_DTC_FTB_Table[38]	151	
Dem_DTC_FTB_Table[39]	151	
Dem_DTC_FTB_Table[40]	199	
Dem_DTC_FTB_Table[41]	160	
Dem_DTC_FTB_Table[42] Dem_DTC_FTB_Table[43]		
Dem_DTC_FTB_Table[44]	30 136	
Dem_DTC_FTB_Table[45]	178	
Dem_DTC_FTB_Table[46]	245	
Dem_DTC_FTB_Table[47]	151	
Dem_DTC_FTB_Table[48]	160	
Dem_DTC_FTB_Table[49]	245	
Dem_DTC_FTB_Table[50]	151	
Dem_DTC_FTB_Table[51]	245	
Dem_DTC_FTB_Table[52]	245	
Dem_DTC_FTB_Table[53]	151	
Dem_DTC_FTB_Table[54]	160	
Dem_DTC_FTB_Table[55]	178	
Dem_DTC_FTB_Table[56]	245	
Dem_DTC_FTB_Table[57]	151	
Dem_DTC_FTB_Table[58]	245	
Dem_DTC_FTB_Table[59]	178	
Dem_DTC_FTB_Table[60]	245	
Dem_DTC_FTB_Table[61]	151	
Dem_DTC_FTB_Table[62]	160	
Dem_DTC_FTB_Table[63]	199	
Dem_DTC_FTB_Table[64]	160	
Dem_DTC_FTB_Table[65]	30	
Dem_DTC_FTB_Table[66]	136	
Dem_DTC_FTB_Table[67]	245	
Dem_DTC_FTB_Table[68]	245	
Dem_DTC_FTB_Table[69]	151	
Dem_DTC_FTB_Table[70]	160	
Dem_DTC_FTB_Table[71]	178	

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Name	Input Value		
Dem_DTC_FTB_Table[72]	160		
Dem_DTC_FTB_Table[73]	199		
Dem_DTC_FTB_Table[74]	160		
Dem_DTC_FTB_Table[75]	30		
Dem_DTC_FTB_Table[76]	136		
Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[0]	1	1	~
CTCFailedBuf_Cnt_M_lgc[1]	1	1	~
CTCFailedBuf_Cnt_M_lgc[2]	1	1	~
CTCFailedBuf_Cnt_M_lgc[3]	1	1	~
CTCFailedBuf_Cnt_M_lgc[4]	1	1	~
CTCFailedBuf_Cnt_M_lgc[5]	0	0	~
CTCFailedBuf_Cnt_M_lgc[6]	1	1	~
CTCFailedBuf_Cnt_M_lgc[7]	1	1	~
CTCFailedBuf_Cnt_M_lgc[8]	1	1	~
CTCFailedBuf_Cnt_M_lgc[9]	1	1	~
CTCFailedBuf_Cnt_M_lgc[10]	1	1	~
CTCFailedBuf_Cnt_M_lgc[11]	1	1	~
CTCFailedBuf_Cnt_M_lgc[12]	1	1	~
CTCFailedBuf_Cnt_M_lgc[13]	1	1	~
CTCFailedBuf_Cnt_M_lgc[14]	1	1	~
CTCFailedBuf_Cnt_M_lgc[15]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[16]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[17]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[18]	1	1	~
CTCFailedBuf_Cnt_M_lgc[19]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[20]	0	0	<b>→</b>
CTCFailedBuf_Cnt_M_lgc[21]	0	0	
CTCFailedBuf_Cnt_M_lgc[22]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[23]	1	1	
CTCFailedBuf_Cnt_M_lgc[24]	0	0	~
CTCFailedBuf_Cnt_M_lgc[25] CTCFailedBuf_Cnt_M_lgc[26]	1	1	Ž
	1	1	~
CTCFailedBuf_Cnt_M_lgc[27]	1	1	J
CTCFailedBuf_Cnt_M_lgc[28] CTCFailedBuf_Cnt_M_lgc[29]	1	1	~
CTCFailedBuf_Cnt_M_lgc[30]	1	1	
CTCFailedBuf_Cnt_M_lgc[31]	1	1	~
CTCFailedBuf_Cnt_M_lgc[32]	1	1	
CTCFailedBuf_Cnt_M_lgc[33]	1	1	~
CTCFailedBuf_Cnt_M_lgc[34]	0	0	
CTCFailedBuf_Cnt_M_lgc[35]	0	0	~
CTCFailedBuf Cnt M lgc[36]	0	0	_
CTCFailedBuf_Cnt_M_lgc[37]	0	0	~
CTCFailedBuf_Cnt_M_lgc[38]	0	0	~
CTCFailedBuf_Cnt_M_lgc[39]	0	0	~
CTCFailedBuf_Cnt_M_lgc[40]	0	0	~
CTCFailedBuf_Cnt_M_lgc[41]	0	0	~
CTCFailedBuf_Cnt_M_lgc[42]	0	0	~
CTCFailedBuf_Cnt_M_lgc[43]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[44]	0	0	~
CTCFailedBuf_Cnt_M_lgc[45]	0	0	~
CTCFailedBuf_Cnt_M_lgc[46]	0	0	~
CTCFailedBuf_Cnt_M_lgc[47]	0	0	~
CTCFailedBuf_Cnt_M_lgc[48]	0	0	~
CTCFailedBuf_Cnt_M_lgc[49]	0	0	~
CTCFailedBuf_Cnt_M_lgc[50]	0	0	~
CTCFailedBuf_Cnt_M_lgc[51]	0	0	~
CTCFailedBuf_Cnt_M_lgc[52]	0	0	~
CTCFailedBuf_Cnt_M_lgc[53]	1	1	~
CTCFailedBuf_Cnt_M_lgc[54]	1	1	~
CTCFailedBuf_Cnt_M_lgc[55]	1	1	~
CTCFailedBuf_Cnt_M_lgc[56]	1	1	~
CTCFailedBuf_Cnt_M_lgc[57]	1	1	~
CTCFailedBuf_Cnt_M_lgc[58]	1	1	~
CTCFailedBuf_Cnt_M_lgc[59]	1	1	~
CTCFailedBuf_Cnt_M_lgc[60]	1	1	~
CTCFailedBuf_Cnt_M_lgc[61]	1	1	<b>V</b>
CTCFailedBuf_Cnt_M_lgc[62]	1	1	•
CTCFailedBuf_Cnt_M_lgc[63]	0	0	-
CTCFailedBuf_Cnt_M_lgc[64]	1	1	- 4
CTCFailedBuf_Cnt_M_lgc[65]	0	0	<b>*</b>
CTCFailedBuf_Cnt_M_lgc[66]	Į <b>v</b>	0	

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Name	Actual Value	Expected Value	Result
CTCFailedBuf_Cnt_M_lgc[67]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[68]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[69]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[70]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[71]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[72]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[73]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[74]	0	0	<b>✓</b>
CTCFailedBuf_Cnt_M_lgc[75]	0	0	✓
CTCFailedBuf_Cnt_M_lgc[76]	0	0	<b>✓</b>
CTCFailed_Cnt_M_lgc	0	0	<b>✓</b>
Demlf_DTCStatusChanged()	0	0	~
Rte Write Ap Demlf CTCFailed Cnt lgc(data)	0	0	✓

Test Step Call Trace				<b>/</b>		
A	ctual Function	Count	Expected Function	Count	Resu	ılt
Rt	e_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1	Rte_Write_Ap_Demlf_CTCFailed_Cnt_lgc	1		•

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DemIf\_VehSpdControl

Project Demlf

Module Demlf

DemIf\_VehSpdControl

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

**Test Object** 

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note 1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Demlf\_VehSpdControl

## Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 12.00 Cycles TS 1.2 12.00 Cycles

Description Vector Description:

TS 1.1 Enable\_Cnt\_T\_lgc=>Min TS 1.2 Enable\_Cnt\_T\_lgc=>Max

Test Step 1.1 (Repeat Count = 1)		<b>✓</b>	
Name	Input Value		
Enable_Cnt_T_lgc	0		
Name	Actual Value	Expected Value	Result
VehSpdControl_Cnt_M_lgc	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 1.2 (Repeat Count = 1)			✓
Name	Input Value		
Enable_Cnt_T_lgc	1		
Name	Actual Value	Expected Value	Result
VehSpdControl_Cnt_M_lgc	1	1	<b>✓</b>

7	est Step Call Trace				<b>✓</b>
Α	ctual Function	Count	Expected Function	Count	Result
*r	one*	0	*** No Call Expected ***	0	~

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Demlf\_SetOperationCycleState

Project Demlf Module Demlf

Test Object Demlf\_SetOperationCycleState

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Comments/Descrip	tion/Specification
Name	Text
Module 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):1051 Total RAM Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes	
Name	Value
Compiler Install Path	<pre>\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5</pre>
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



## Test Case 1: Range Test

Demlf\_SetOperationCycleState

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 502.00 Cycles

Description Vector Description:

TS 1.1 Check for Call Trace

Test Step 1.1 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
NxtrCycleState	*none*
NxtrOperationCycleId	*none*

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Dem_SetOperationCycleState	1	Dem_SetOperationCycleState	1	~

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Demlf\_RestartDem

 Project
 Demlf

 Module
 Demlf

 Test Object
 Demlf\_RestartDem

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_Demlf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demifsrc\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(PROJECTROOT)\Demlf\utp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Comments/Description/Specification		
Name	Text	
Module 'Demif'	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):1054 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.	

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision	9	
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl	
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4	
Time Unit	cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution		
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP	

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Demlf\_RestartDem

## Test Case 1: Range Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 500.00 Cycles

Description Vector Description:

TS1.1 Only Call trace is checked

## Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Dem_Init	1	Dem_Init	1	~

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Demlf\_CheckVoltageRange

Project	Demlf
Module	Demlf
Test Object	Demlf_CheckVoltageRange

## Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	2	
Successful	2	✓
Failed	0	
Not Executed	0	

## **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf
Configuration File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config \TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I\$(PROJECTROOT)\Demlflutp\contract -I\$(PROJECTROOT)\Demlflutp\contract\Ap_Demlf -I\$ (PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include

Name	Text
Module 'Demi <b>f</b> '	Name of Tester:Ameya Shirodkar Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:3 Module Design Document:Demlf_MDD.docx Module Design Document Version:1 Data Dictionary Version:1 Unit Test Plan Version:3 Optimization Level:Ogeneral Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:None Model Version:Nexteer EPS Unit Test Tool 1.0 Total FLASH Used (Bytes):1051 Total RAM Used (Bytes):104 Total CALS Used (Bytes):50 Special Test Requirements:NA Test Date:4/10/2018 Comments: Note1:Inline functions are not unit tested. Note2:"CBD_Sandbox_dbg.map" MAP file embedded in UTP for reference.

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision	9	
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(TESSY_SYSPATH)\compiler\ti\tms470\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl	
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4	
Time Unit	cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution	1	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	

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Demlf\_CheckVoltageRange

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\PSA_CMP_05.01.01_DemIf\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Demlf\_CheckVoltageRange

#### Test Case 1: Metrics Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

TS 1.1 76.00 Cycles TS 1.2 97.00 Cycles

Description Vector Description:

 $TS 1.1 \ Shortest \ Execution \ Path=>if ((voltage_Volt_T_f32 < min_Volt_T_f32)=>False \ || \ (max_Volt_T_f32 < voltage_Volt_T_f32)=>False) \ TS 1.2 \ Longest \ Execution \ Path=>if ((voltage_Volt_T_f32 < min_Volt_T_f32)=>True \ || \ (max_Volt_T_f32 < voltage_Volt_T_f32))$ 

Test Step 1.1 (Repeat Count = 1)			✓
Name	Input Value		
max_Volt_T_f32	0		
min_Volt_T_f32	0		
time_cnt_T_u32	0		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 1.2 (Repeat Count = 1)			✓
Name	Input Value		
max_Volt_T_f32	0.426099986		
min_Volt_T_f32	12.3562002		
time_cnt_T_u32	1452352		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1452352	1452352	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~



#### **Test Case 2: Range Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)

CPU Cycles:

TS 2.1 76.00 Cycles
TS 2.2 76.00 Cycles
TS 2.2 76.00 Cycles
TS 2.3 97.00 Cycles
TS 2.4 101.00 Cycles
TS 2.5 78.00 Cycles
TS 2.6 78.00 Cycles
TS 2.7 99.00 Cycles
TS 2.8 99.00 Cycles
TS 2.9 78.00 Cycles
TS 2.10 96.00 Cycles
TS 2.11 76.00 Cycles
TS 2.12 97.00 Cycles
TS 2.12 97.00 Cycles
TS 2.13 101.00 Cycles
TS 2.14 99.00 Cycles

#### Description

#### Vector Description:

TS 1.1All Min TS 1.2All Max

TS 1.2All Max
TS 1.3voltage\_Volt\_T\_f32=>Min
TS 1.4voltage\_Volt\_T\_f32=Max
TS 1.5voltage\_Volt\_T\_f32=>Pos
TS 1.6min\_Volt\_T\_f32=>Max
TS 1.7min\_Volt\_T\_f32=>Max
TS 1.8min\_Volt\_T\_f32=>Pos
TS 1.9max\_Volt\_T\_f32=>Min
TS 1.10max\_Volt\_T\_f32=>Pos
TS 1.11max\_Volt\_T\_f32=>Pos
TS 1.12time\_cnt\_T\_u32=>Min
TS 1.13time\_cnt\_T\_u32=>Pos

Test Step 2.1 (Repeat Count = 1)			✓
Name	Input Value		
max_Volt_T_f32	0		
min_Volt_T_f32	0		
time_cnt_T_u32	0		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	~

Test Step Call Trace						<b>✓</b>
1	ctual Function	Count	Expected Function	Count	Resu	lt
*	none*	0	*** No Call Expected ***	0		<b>✓</b>

Test Step 2.2 (Repeat Count = 1)	Test Step 2.2 (Repeat Count = 1)		
Name	Input Value		
max_Volt_T_f32	31		
min_Volt_T_f32	31		
time_cnt_T_u32	4294967295		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	31		
Name	Actual Value	Expected Value	Result
target timer cnt T u32	0	0	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.3 (Repeat Count = 1)			
Name	Input Value		
max_Volt_T_f32	0.426099986		
min_Volt_T_f32	12.3562002		
time_cnt_T_u32	1452352		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	1452352	1452352	<b>✓</b>

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Demlf\_CheckVoltageRange

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.4 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	0.125400007		
min_Volt_T_f32	8.41409969		
time_cnt_T_u32	2151351		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	31		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	2151351	2151351	<b>✓</b>

Test Step Call Trace				V	
Act	ual Function	Count	Expected Function	Count	Result
*non	ne*	0	*** No Call Expected ***	0	~

Test Step 2.5 (Repeat Count = 1)	Test Step 2.5 (Repeat Count = 1)			
Name	Input Value			
max_Volt_T_f32	9.11979961			
min_Volt_T_f32	5.12400007			
time_cnt_T_u32	1241			
timer_cnt_T_u32	target_timer_cnt_T_u32			
voltage_Volt_T_f32	12.1353998			
Name	Actual Value	Expected Value	Result	
target_timer_cnt_T_u32	1241	1241	<b>✓</b>	

Test Step Call Trace					<b>✓</b>
4	Actual Function	Count	Expected Function	Count	Result
*	none*	0	*** No Call Expected ***	0	~

Test Step 2.6 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	5.07380009		
min_Volt_T_f32	0		
time_cnt_T_u32	1151336		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	19.5648003		
Name	Actual Value	Expected Value	Result
target timer cnt T u32	1151336	1151336	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.7 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	1.73090005		
min_Volt_T_f32	31		
time_cnt_T_u32	52		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	12.3786001		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	52	52	~

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Demlf\_CheckVoltageRange

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.8 (Repeat Count = 1)				
Name	Input Value			
max_Volt_T_f32	2.5236001			
min_Volt_T_f32	8.14509964			
time_cnt_T_u32	78073			
timer_cnt_T_u32	target_timer_cnt_T_u32			
voltage_Volt_T_f32	0.0706999972			
Name	Actual Value	Expected Value	Result	
target_timer_cnt_T_u32	78073	78073	•	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.9 (Repeat Count = 1)	Test Step 2.9 (Repeat Count = 1)		
Name	Input Value		
max_Volt_T_f32	0		
min_Volt_T_f32	0.262400001		
time_cnt_T_u32	3424		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	1.22490001		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	✓

Test Step Call Trace					<b>✓</b>
4	Actual Function	Count	Expected Function	Count	Result
*	none*	0	*** No Call Expected ***	0	~

Test Step 2.10 (Repeat Count = 1)	Test Step 2.10 (Repeat Count = 1)			
Name	Input Value			
max_Volt_T_f32	31			
min_Volt_T_f32	9.23530006			
time_cnt_T_u32	857634			
timer_cnt_T_u32	target_timer_cnt_T_u32			
voltage_Volt_T_f32	12.9097004			
Name	Actual Value	Expected Value	Result	
target_timer_cnt_T_u32	3424	3424	<b>✓</b>	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.11 (Repeat Count = 1)			✓
Name	Input Value		
max_Volt_T_f32	14.2140999		
min_Volt_T_f32	1.46340001		
time_cnt_T_u32	352624		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	10.7594995		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	3424	3424	<b>✓</b>

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Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.12 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	16.8927994		
min_Volt_T_f32	26.1240997		
time_cnt_T_u32	0		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	0		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.13 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	12.0332003		
min_Volt_T_f32	12.1252003		
time_cnt_T_u32	4294967295		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	21.4778004		
Name	Actual Value	Expected Value	Result
target_timer_cnt_T_u32	4294967295	4294967295	~

Test Step Call Trace				V	
<b>Actual Function</b>		Count	Expected Function	Count	Result
*none*		0	*** No Call Expected ***	0	~

Test Step 2.14 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
max_Volt_T_f32	0.977800012		
min Volt T f32	3.65319991		
time_cnt_T_u32	1524114		
timer_cnt_T_u32	target_timer_cnt_T_u32		
voltage_Volt_T_f32	1.12510002		
Name	Actual Value	Expected Value	Result
target timer cnt T u32	1524114	1524114	~

Test Step Call Trace					V	ı
	Actual Function	Count	Expected Function	Count	Result	l
	*none*	0	*** No Call Expected ***	0	~	