Integration Manual -- Spi Nexteer

Contents

[1 Dependencies 1](#_Toc363214774)

[1.1 SWCs 1](#_Toc363214775)

[1.2 Global Functions(Non RTE) to be provided to Integration Project 2](#_Toc363214776)

[2 Configuration 2](#_Toc363214777)

[2.1 Build Time Config 2](#_Toc363214778)

[2.2 Configuration Files to be provided by Integration Project 2](#_Toc363214779)

[2.2.1 Da Vinci Parameter Configuration Changes 2](#_Toc363214780)

[2.2.2 Da Vinci Interrupt Configuration Changes 3](#_Toc363214781)

[2.2.3 Manual Configuration Changes 3](#_Toc363214782)

[3 Integration 4](#_Toc363214783)

[3.1 Required Global Data Inputs 4](#_Toc363214784)

[3.2 Required Global Data Outputs 4](#_Toc363214785)

[3.3 Specific Include Path present 4](#_Toc363214786)

[4 Runnable Scheduling 5](#_Toc363214787)

[5 Memory Mapping 5](#_Toc363214788)

[5.1 Mapping 5](#_Toc363214789)

[5.2 Usage 5](#_Toc363214790)

[5.3 Non RTE NvM Blocks 5](#_Toc363214791)

[5.4 RTE NvM Blocks 5](#_Toc363214792)

[6 Compiler Settings 5](#_Toc363214793)

[6.1 Preprocessor MACRO 5](#_Toc363214794)

[6.2 Optimization Settings 6](#_Toc363214795)

# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
| Dio | Dio\_WriteChannel() when SpiNxt used with Turns Counter |
| TMS570 MIBSPI3 and MIBSPI5 peripheral | Exclusive access to the MIBSPI3 and MIBSPI5 peripheral registers.  MIBSPI3 CS3 provided as a No Connect pin on CCA design when SpiNxt used with Turns Counter |
| Os | Category 2 ISR mapping for MIBSPI3 IRQ sources when SpiNxt used with Turns Counter |
| TurnsCounter | TurnsCounter\_TxConfirmation() when SpiNxt used with Turns Counter |
| ePWM | Must provide SPI transmit trigger on N2HET1[14] for mibspi3, and N2HET1[18] for mibspi5, when SpiNxt used with Digital MSB. |

## Global Functions(Non RTE) to be provided to Integration Project

void **SpiNxt\_Init**(void);

Std\_ReturnType **SpiNxt\_AsyncTransmit**( Spi\_SequenceType Sequence );  
NOTE that this function is hardcoded for use with the Turns Counter component and returns E\_NOT\_OK when SpiNxt not configured for use with Turns Counter (see section 2.2.1).

Spi\_SeqResultType **SpiNxt\_GetSequenceResult**( Spi\_SequenceType Sequence );

Std\_ReturnType **SpiNxt\_SetupEB**( Spi\_ChannelType Channel,  
 P2CONST(Spi\_DataType, AUTOMATIC, SPI\_APPL\_DATA) SrcDataBufferPtr,  
 P2VAR(Spi\_DataType, AUTOMATIC, SPI\_APPL\_DATA) DesDataBufferPtr,  
 Spi\_NumberOfDataType Length);  
NOTE that this function is hardcoded for use with the Turns Counter component and returns E\_NOT\_OK when SpiNxt not configured for use with Turns Counter (see section 2.2.1).

void **mibspiSetData**(const mibspiBASE\_t \*mibspi, uint32 group, const uint16 data[]);

void **mibspiSetCtrlData**(const mibspiBASE\_t \*mibspi, uint32 group, const uint32 data[]);

uint32 **mibspiGetData**(const mibspiBASE\_t \*mibspi, uint32 group, uint16 data[]);  
NOTE this function is optimized for use by the Digital MSB component when SpiNxt is configured for use with Digital MSB (see section 2.2.1). In that configuration, the mibspi argument must be equal to the base register address of mibspi3 or mibspi5, the length of all transfer groups is assumed to be the constant D\_TGSIZE\_CNT\_U16 (defined in SpiNxt.h), the function always returns zero, and the data argument must be the receive data buffer for the caller.

void **mibspiTransfer**(mibspiBASE\_t \*mibspi, uint32 group);

NOTE that this function enables the specified transfer group for the specified mibspi (with base address equal to the mibspi argument). Depending on the configuration of the transfer group, it will either enable a single transfer on the next trigger (if the transfer group is configured for oneshot) or will enable ongoing transfers as triggered ((if the transfer group is **not** configured for oneshot).

# Configuration

## Build Time Config

|  |  |
| --- | --- |
| Modules | Notes |
| None |  |

## Configuration Files to be provided by Integration Project

SpiNxt\_Cfg.h as generated by SpiNxt\_cfg.h.tt

### Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| Parameter | Notes | SWC |
| Dio Channel Name: “SPI\_TCCS” | Chip Select DIO output mapped to the turns counter chip select pin when used with Turns Counter | Dio |
| All MIBSPI3 and MIBSPI5 configuration | The third party Spi driver shall be configured such that it does not read/write any of the MIBSPI3 or MIBSPI5 control registers. | Spi |
| Port pin SPI3CLK: SPI Output |  | Port |
| Port pin SPI3NCS3: SPI Output | When used with Turns Counter | Port |
| Port pin SPI3NCS0: SPI Output | When used with Digital MSB | Port |
| Port pin SPI3SIMO: SPI Output |  | Port |
| Port pin SPI3SOMI: SPI Input |  | Port |
| Port pin SPI5CLK: SPI Output |  | Port |
| Port pin SPI5NCS0: SPI Output | When used with Digital MSB | Port |
| Port pin SPI5SIMO: SPI Output |  | Port |
| Port pin SPI5SOMI: SPI Input | When used with Digital MSB | Port |
| SPINXT\_EXCLUSIVE\_AREA\_0 | This exclusive area covers the events that need to be synchronized to minimize jitter on the CS to SCLK delay specified by the TurnsCounter FDD 20C (when used with Turns Counter) | SchM |
| SpiNxtGeneral\ SpiNxtUseWith | This parameter controls generation of D\_SPINXTUSEWITH\_CNT\_ENUM in the SpiNxt\_Cfg.h file. Set to D\_SPINXT\_USEWITHTC for use with the PIC Turns Counter, or set to D\_SPINXT\_USEWITHDIGMSB for use with the Digital MSB.  When this parameter is set to D\_SPINXT\_USEWITHTC, the SpiNxt.h file provides the following constants which previously were manually configured: SPI\_TCDATA\_CH, SPI\_TCDATA\_SEQ, D\_SPINXTNUMCHAN\_CNT\_U16, and CALL\_MIBSPI3\_NOTIFFCN(). | SpiNxt |
| SpiNxtGeneral\ SpiNxtUseDMA | This parameter controls generation of BC\_SPINXT\_USEDMA in the SpiNxt\_Cfg.h file. Set to STD\_ON when using DMA with SPI. | SpiNxt |
|  |  |  |

### Da Vinci Interrupt Configuration Changes

|  |  |  |
| --- | --- | --- |
| ISR Name | Notes | SWC |
| SpiNxt\_IrqUnit2TxRx: MIBSPI3 level 0 interrupt | Category 2 interrupt mapped to Mibspi3 RxTx interrupt source when used with Turns Counter | Os |
| SpiNxt\_IrqUnit2TxRxERR: MIBSPI3 level 1 interrupt | Category 2 interrupt mapped to Mibspi3 RxTx error interrupt source when used with Turns Counter | Os |

### Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| None |  |  |

# Integration

## Required Global Data Inputs

<None>

## Required Global Data Outputs

<None>

## Specific Include Path present

<Yes>

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Init | Scheduling Requirements | Trigger |
| SpiNxt\_Init() | Must be executed prior to using any of the module C/S API. | Init |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| SpiNxt\_MainFunction() | Dummy runnable used for assigning the SpiNxt component to an application | N/A |

# Memory Mapping

## Mapping

|  |  |
| --- | --- |
| Constant | Notes |
| SPINXT\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED |  |
| SPINXT\_START\_SEC\_CODE |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| Full driver |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| Block Name |
| <None > |

Note : Size of the NVM block if configured in developer

## RTE NvM Blocks

|  |
| --- |
| Block Name |
| <None > |

Note : Size of the NVM block if configured in developer

# Compiler Settings

## Preprocessor MACRO

<Define all the preprocessor Macros needed and conditions when needed>.

## Optimization Settings

<Define Optimization levels that are needed and conditions when needed>.

# Revision Control Log

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Item #** | **Rev #** | **Change Description** | **Date** | **Author Initials** |
| 1 | 1 | Initial version |  | JJW |
| 2 | 2 | Added exclusive area configuration and Category 2 interrupt configuration |  | JJW |
| 3 | 3 | Added ISR MIBSPI level configuration requirement |  | JJW |
| 4 | 4 | New Notification build configuration parameter |  | JJW |
| 5 | 5 | Changes and additions for configurability of SpiNxt to be used with PIC Turns Counter or with Digital MSB. | 8/2/13 | KMC |
| 6 | 6 | Updated information on Halcogen API functions and added configuration parameter for use of DMA with SPI as needed for ES-50A rev 005. | 4/1/14 | KMC |