**Integration Manual**

**For**

**Torque Reasonableness Diagnostic**

**VERSION: 4.0**

**DATE: 05-Aug-2016**

**Prepared By:**

**Software Group,**

**Nexteer Automotive,**

**Saginaw, MI, USA**

**Location:** The official version of this document is stored in the Nexteer Configuration Management System.

**Revision History**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sl. No.** | **Description** | **Author** | **Version** | **Date** |
| 1 | Initial version | Selva | 1.0 | 10-Apr-13 |
| 2 | Updated for the new torque reasonableness | Selva | 2.0 | 23-Nov-13 |
| 3 | Updated for new output (v5) of the FDD | Selva | 3.0 | 25-Mar-15 |
| 4 | Updated to version 6 of FDD and to new template | SB | 4.0 | 05-Aug-16 |

**Table of Contents**

[1 Abbrevations And Acronyms 4](#_Toc458171648)

[2 References 5](#_Toc458171649)

[3 Dependencies 6](#_Toc458171650)

[3.1 SWCs 6](#_Toc458171651)

[3.2 Global Functions(Non RTE) to be provided to Integration Project 6](#_Toc458171652)

[4 Configuration REQUIREMeNTS 7](#_Toc458171653)

[4.1 Build Time Config 7](#_Toc458171654)

[4.2 Configuration Files to be provided by Integration Project 7](#_Toc458171655)

[4.3 Da Vinci Parameter Configuration Changes 7](#_Toc458171656)

[4.4 DaVinci Interrupt Configuration Changes 7](#_Toc458171657)

[4.5 Manual Configuration Changes 7](#_Toc458171658)

[5 Integration DATAFLOW REQUIREMENTS 8](#_Toc458171659)

[5.1 Required Global Data Inputs 8](#_Toc458171660)

[5.2 Required Global Data Outputs 8](#_Toc458171661)

[5.3 Specific Include Path present 8](#_Toc458171662)

[6 Runnable Scheduling 9](#_Toc458171663)

[7 Memory Map REQUIREMENTS 10](#_Toc458171664)

[7.1 Mapping 10](#_Toc458171665)

[7.2 Usage 10](#_Toc458171666)

[7.3 NvM Blocks 10](#_Toc458171667)

[8 Compiler Settings 11](#_Toc458171668)

[8.1 Preprocessor MACRO 11](#_Toc458171669)

[8.2 Optimization Settings 11](#_Toc458171670)

[9 Appendix 12](#_Toc458171671)

# Abbrevations And Acronyms

|  |  |
| --- | --- |
| **Abbreviation** | **Description** |
| DFD | Design functional diagram |
| MDD | Module design Document |
|  | <ADD more to the table if applicable> |
|  |  |
|  |  |

# References

This section lists the title & version of all the documents that are referred for development of this document

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Title** | **Version** |
| <1> | <MDD Guidelines> | Proces release 04.02.01 |
| <2> | <Software Naming Conventions> | Proces release 04.02.01 |
| <3> | <Coding standards> | Proces release 04.02.01 |
| <4> | FDD – SF31\_CurrentReasonablenessDiagnostic | 006 |
|  | <Add if more available> |  |

# Dependencies

## SWCs

|  |  |
| --- | --- |
| **Module** | **Required Feature** |
| **None** |  |

Note : Referencing the external components should be avoided in most cases. Only in unavoidable circumstance external components should be referred. Developer should track the references.

## Global Functions(Non RTE) to be provided to Integration Project

None

# Configuration REQUIREMeNTS

## Build Time Config

|  |  |  |
| --- | --- | --- |
| **Modules** | **Notes** |  |
| **None** |  |  |

## Configuration Files to be provided by Integration Project

<Configuration file that will generated from this components that will require Da Vinci Config generation or manual generation. Describe each parameter >

## Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Notes** | **SWC** |
| **None** |  |  |

## DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| **ISR Name** | **VIM #** | **Priority Dependency** | **Notes** |
| **None** |  |  |  |

## Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Constant** | **Notes** | **SWC** |
| **None** |  |  |

# Integration DATAFLOW REQUIREMENTS

## Required Global Data Inputs

CorrMtrPosElec\_Rev\_ f32

EstKe\_VpRadpS\_ f32

EstR\_Ohm\_ f32

MRFMtrVel\_MtrRadpS\_ f32

MtrCurrDaxRef\_Amp\_ f32

MtrCurrQaxFinalRef\_Amp\_ f32

MtrVoltDax\_Volt\_ f32

MtrVoltQax\_Volt\_ f32

OutputRampMult\_Uls\_ f32

TrqLimitMin\_MtrNm\_ f32

## Required Global Data Outputs

MtrCurrIdptSig\_Cnt\_u08

## Specific Include Path present

No

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| **Init** | **Scheduling Requirements** | **Trigger** |
| **TqRsDg\_Init1** | On Init | Rte\_Init |

|  |  |  |
| --- | --- | --- |
| **Runnable** | **Scheduling Requirements** | **Trigger** |
| **TqRsDg \_Per1** | Must run after CmMtrCurr\_Per2  and before CurrCmd\_Per1 | RTE(2ms) |
|  |  |  |

**.**

# Memory Map REQUIREMENTS

## Mapping

|  |  |  |
| --- | --- | --- |
| **Memory Section** | **Contents** | **Notes** |
| TQRSDG\_START\_SEC\_VAR\_CLEARED\_32 |  |  |
| TQRSDG\_START\_SEC\_VAR\_NOINIT\_UNSPECIFIED |  |  |
| TQRSDG\_START\_SEC\_VAR\_CLEARED\_16 |  |  |
| RTE\_START\_SEC\_AP\_TQRSDG\_APPL\_CODE |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| **Feature** | **RAM** | **ROM** |
| **None** |  |  |

Table 1: ARM Cortex R4 Memory Usage

## NvM Blocks

None

# Compiler Settings

## Preprocessor MACRO

N/A

## Optimization Settings

N/A

# Appendix

*N/A*