EE301

Course Project

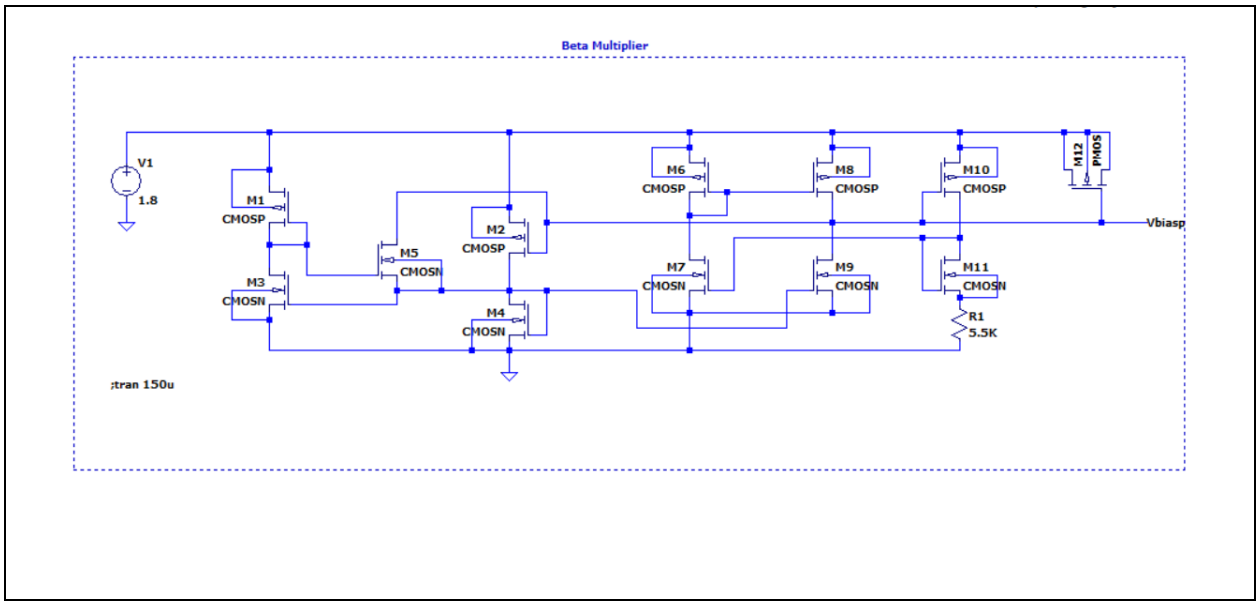
Design of cascode amplifier and cascode current mirror in schematic and layout

Manan Dangwal (2021EEB1186)

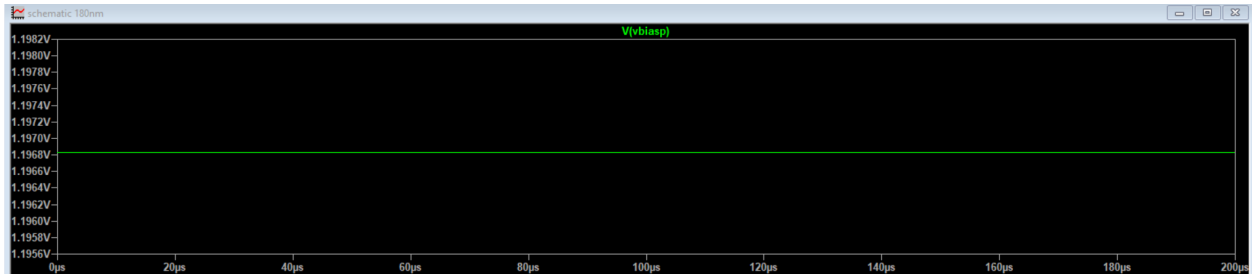
Objective: Design of cascode amplifier and cascode current mirror in schematic and layout using LTSpice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

Circuits [180nm]:

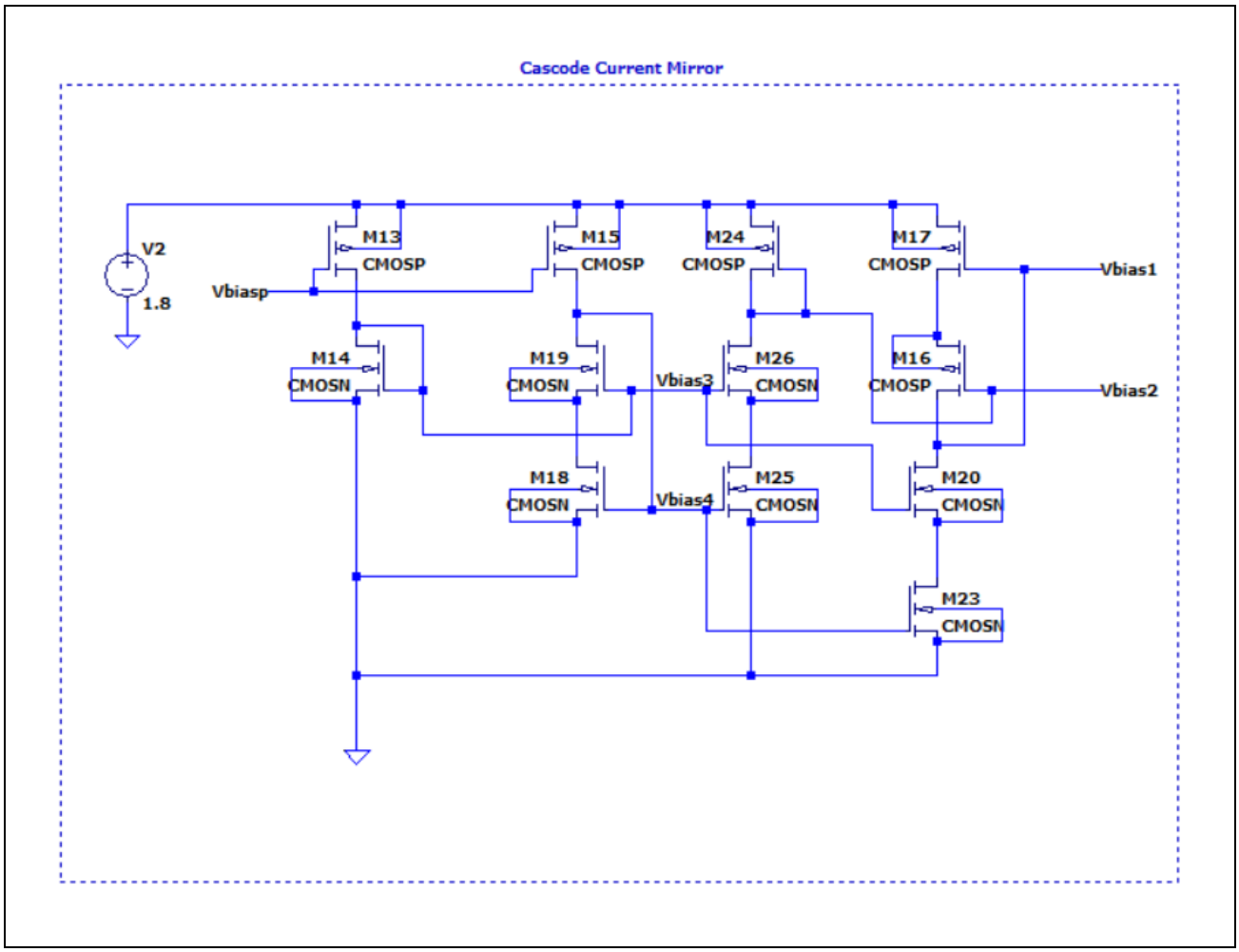
Beta Multiplier:



The Vbiasp obtained via simulation was *1.197V.*



Cascode Current Mirror:



The bias voltages obtained were:

Vbias1 = 1.16V

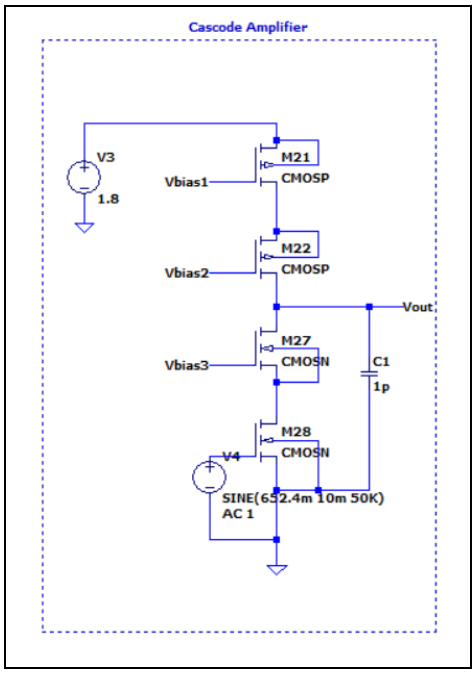
Vbias2 = 1.06V

Vbias3 = 629mV

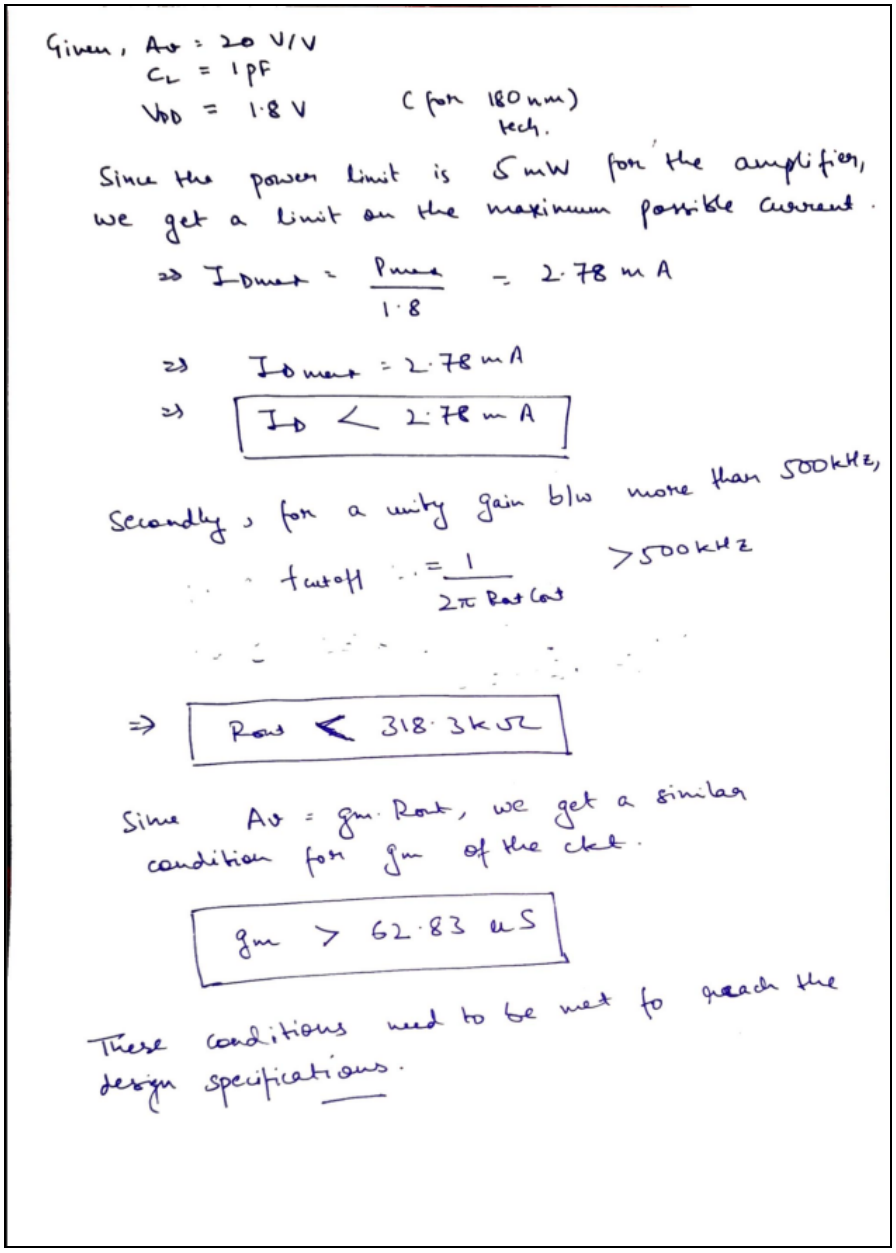
Vbias4 = 652mV

These are the voltages used to bias the transistors in the cascode amplifier.

Cascode Amplifier:



Calculations:



Given, $A_v = 20$ V/V
$C_L = 1$ pF
$V_{DD} = 1.8$ V (for 180 nm tech.)

Since the power limit is 5 mW for the amplifier, we get a limit on the maximum possible current.

$$\Rightarrow I_{Dmax} = \frac{P_{max}}{1.8} = 2.78 \text{ mA}$$

$$\Rightarrow I_{Dmax} = 2.78 \text{ mA}$$

$$\Rightarrow \boxed{I_D < 2.78 \text{ mA}}$$

Secondly, for a unity gain b/w more than 500kHz,

$$\therefore f_{cutoff} = \frac{1}{2\pi R_{out} C_{out}} > 500\text{kHz}$$

$$\Rightarrow \boxed{R_{out} < 318.3\text{k}\Omega}$$

Since $A_v = g_m \cdot R_{out}$, we get a similar condition for g_m of the ckt.

$$\boxed{g_m > 62.83 \text{ uS}}$$

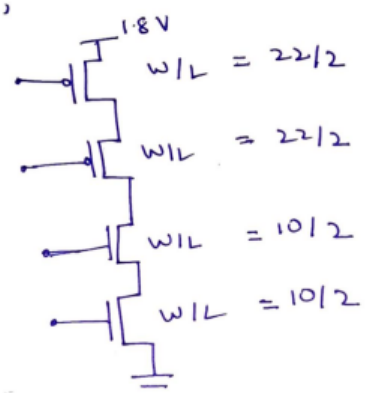
These conditions need to be met to reach the design specifications.

To operate MOSFETs in saturation,

$V_{ds} > V_{gs} - V_{thn}$ (NMOS)

$|V_{ds}| > |V_{gs}| - |V_{thp}|$ (PMOS)

By iterative tweaking of W and L for the 4 MOSFETs,



The Bode plot of this [redacted] starts at 26 dB (20 V/V), and has a unity gain b/w of 5.32 MHz

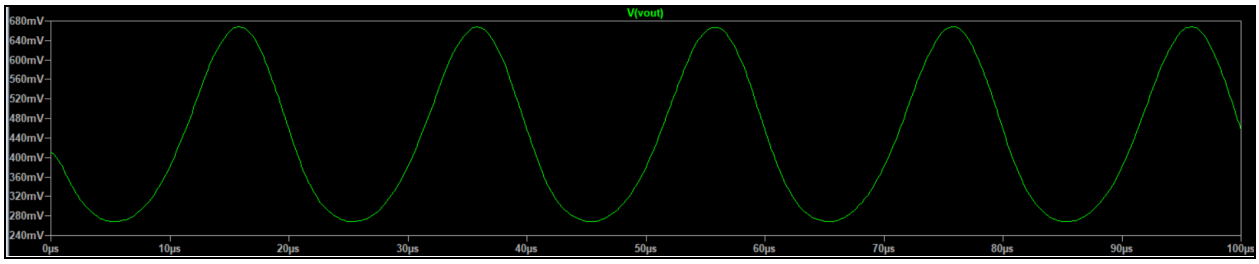
Thus all the conditions are met for the circuit.

The drain current swings around 10.7 μA.

Power Dissipation < 5 mW

Results:

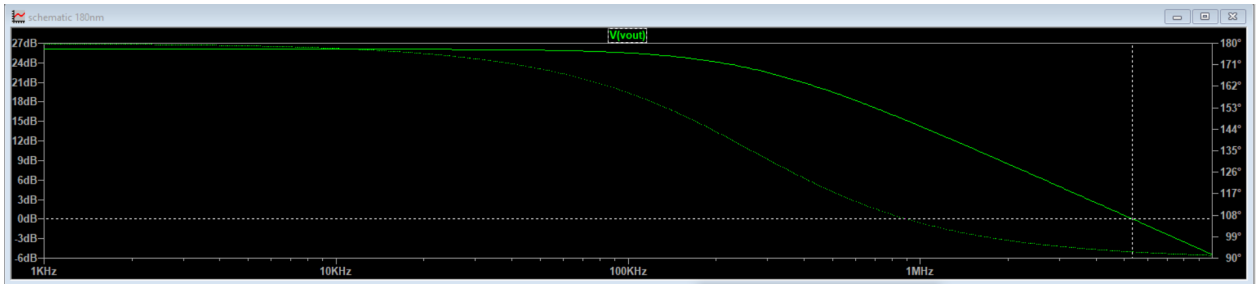
- Gain = 26 dB = 19.95 V/V
- Unity Gain Bandwidth = 5.32 MHz
- Power Dissipation = 19.4 μW

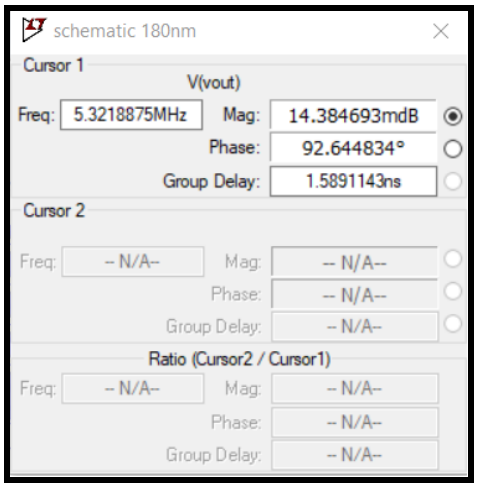


Output Voltage, sine with amplitude almost 200 mV

Input was a sine wave with amplitude 10 mV

The frequency response is shown below:

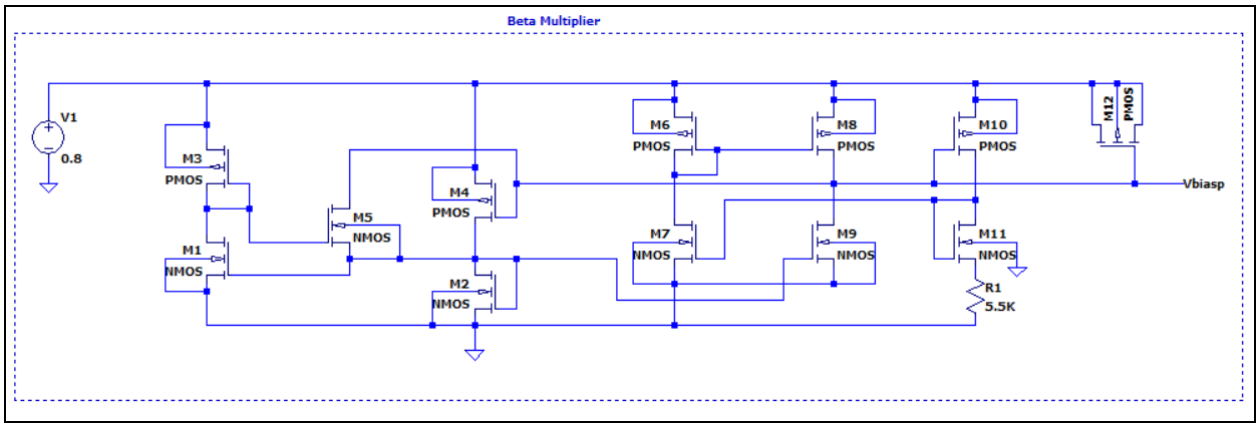




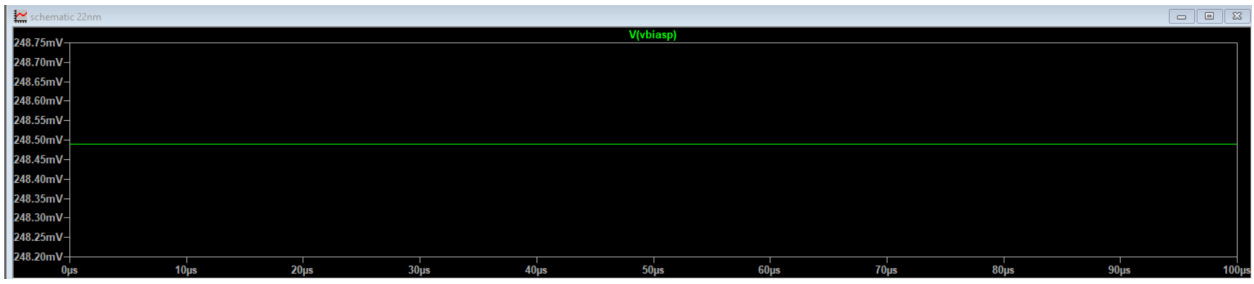
The corresponding LTSpice file is attached in the zip.

Circuits [22nm]:

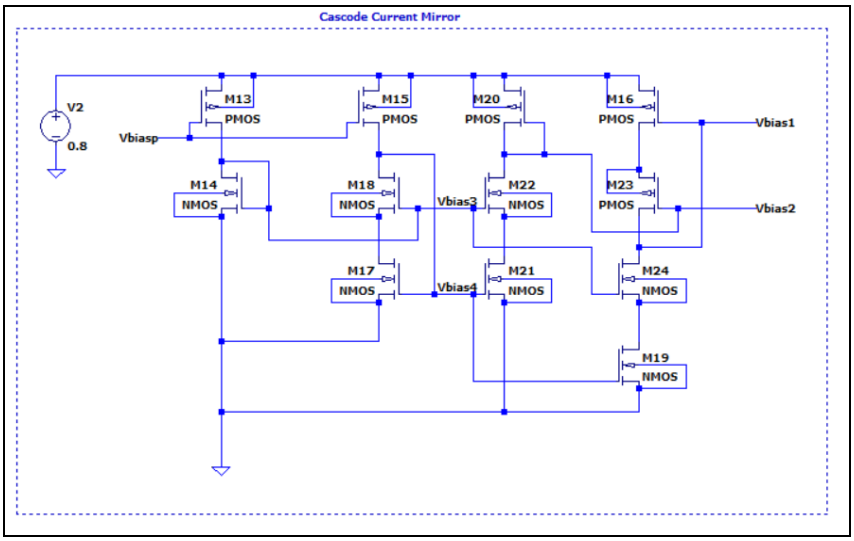
Beta Multiplier:



The Vbiasp is *248.5mV.*



Cascode Current Mirror:



The bias voltages obtained were:

Vbias1 = 244.3mV

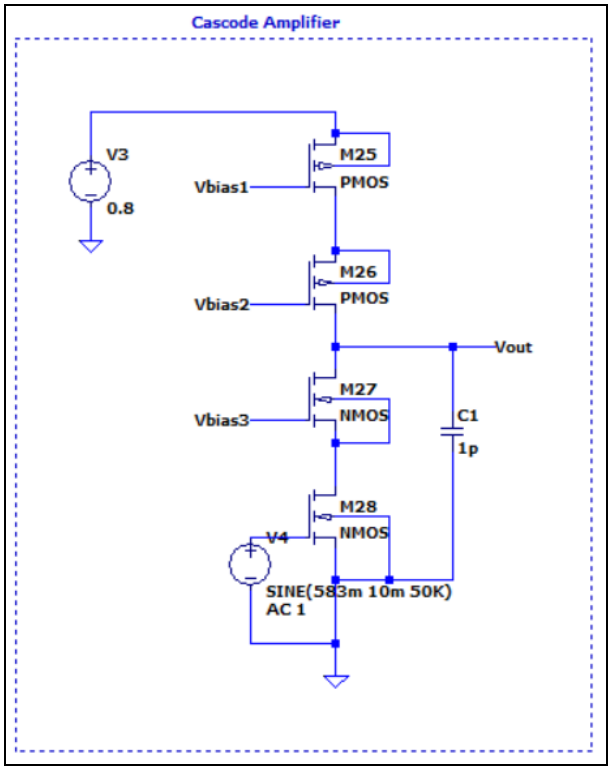
Vbias2 = 138mV

Vbias3 = 591.8mV

Vbias4 = 584.5mV

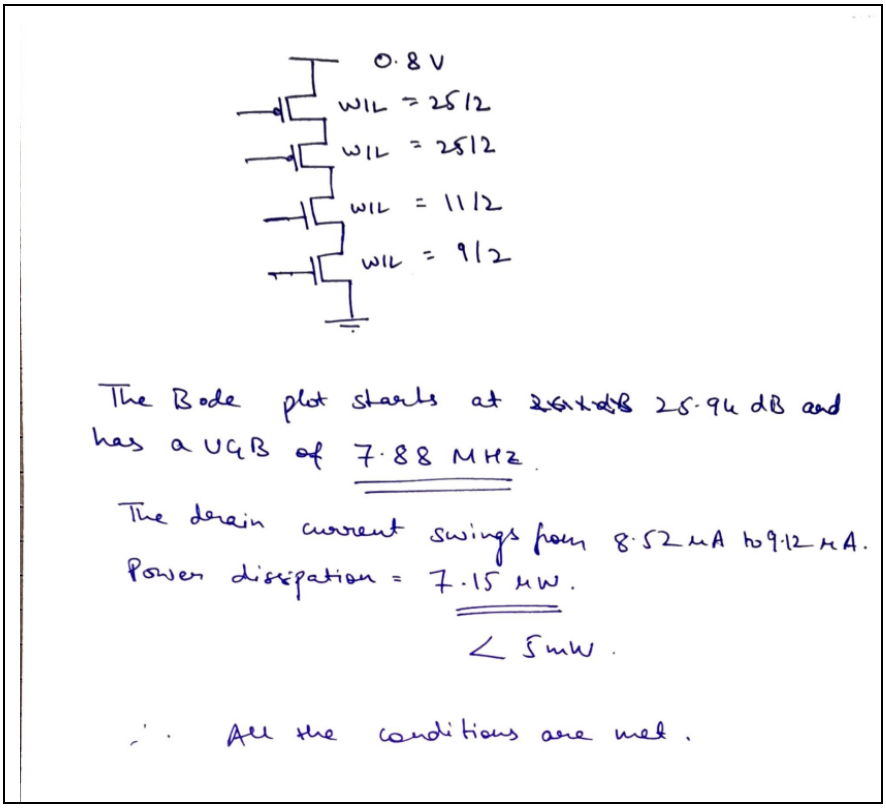
These are the voltages used to bias the transistors in the cascode amplifier.

Cascode Amplifier:



Calculations:

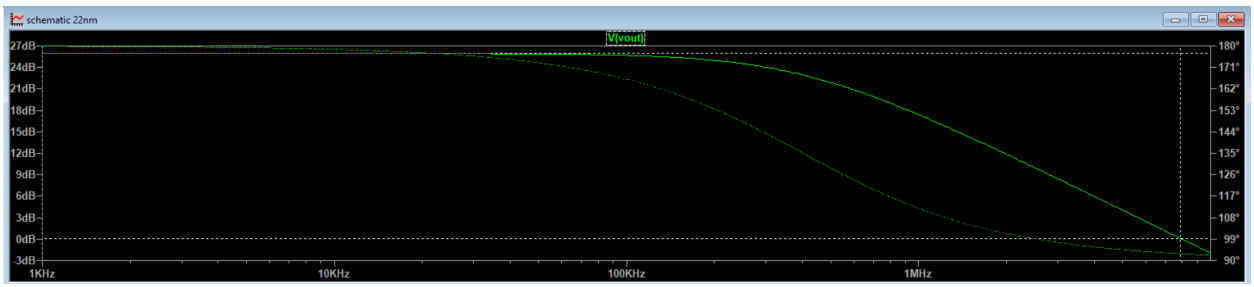
The initial set of calculations remain constant (that is, power dissipation constraint, current constraint, UGB constraint). Other calculations are given below:

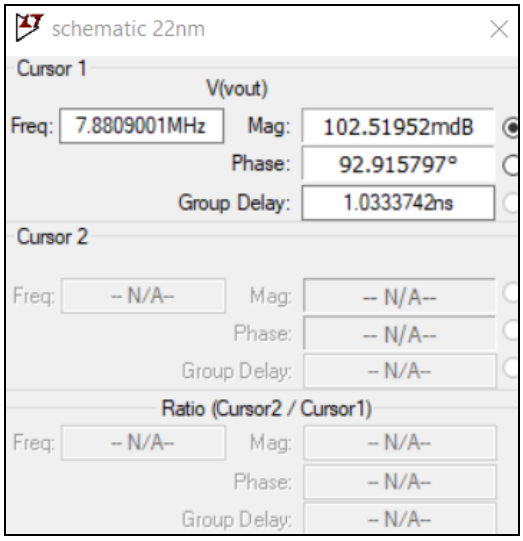


Results:

- Gain = 25.94 dB = 19.82 V/V
- Unity Gain Bandwidth = 7.88 MHz
- Power Dissipation = 7.15 µW

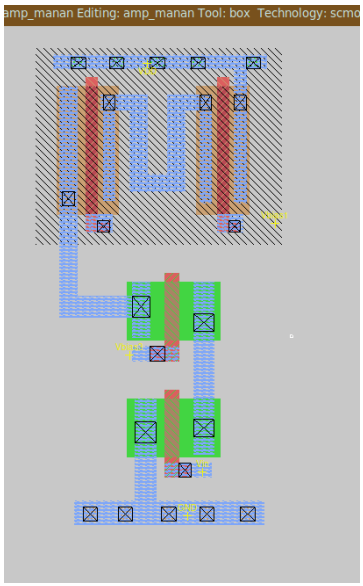
The frequency response is shown below:





Thus, both the circuits work as required within the specified parameters.

Magic Layout for 180nm:



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