Dept of Electronics and Communication Engineering,
National Institute of Technology Karnataka, Surathkal

EC280 Digital System Design

Assignment - 2

Instructions:

1. This assignment is graded and therefore should be submitted **on or before Wednesday*, 13th March 2019, 11:55PM***

2. The assignment has to be uploaded on Moodle. ***Submission by email or WhatsApp or Facebook is strictly not allowed.***

3. The assignment ***must be done in groups of 2.***

4. You must clearly mention who has done which questions and what are the contributions of each of you in this assignment.

5. You will turn in the following during your submission:
   Firstly, you must include a block diagram of what you are trying to design, clearly showing all the details including various interfaces, internal signals and wires, properly named. A paragraph or two on what you are designing and what your approach is must be included. In addition,
   a) Verilog Code in .v format . The code should contain relevant comments without which the assignment will not be evaluated.
   b) Timing Simulation waveforms. Simulation waveform after Implementation must be included. Go through the simulator help and find out how to save the waveform file. Use the instructions given there to save the waveforms. A screenshot of the same (with all signals and values clearly visible must be included as a screenshot in your PDF File.)
   c) The elaborated design schematic must be included.
   d) Post implementation report, which contains Resource utilization, timing details etc.

6. Other than the Verilog Code, everything must be included in a PDF document of size not more than 1MB. All the verilog codes must be included in your PDF and as well as kept as .v files.

7. The first page of your PDF file must clearly mention EC280 Digital System Design Assignment 1, Submitted by Name 1 (Roll No) and Name 2 (Roll No).

8. Zip the PDF and .v files, along with waveforms and upload in moodle.

9. File name should be Your_name_Your_Teammate_Name.pdf and Your_name_Your_Teammate_Name.zip or rar

Dept of Electronics and Communication Engineering,
National Institute of Technology Karnataka, Surathkal

EC280 Digital System Design

Assignment - 2

1. Construct an FSM that checks if a binary number is divisible by 3. Specifically, your FSM should take input bits sequentially starting from LSB and output REM= 1 if the number is not divisible and REM = 0 if the number is divisible. Write a ***synthesisable Verilog code*** for the same. Do a post implementation simulation using a verilog testbench. Submit the verilog code, the verilog testbench code and the FSM you have designed. You may hand draw the FSM and take a snapshot and include it in the PDF file along with the verilog code and the testbench code. Zip this PDF, verilog file and verilog test bench file. Use the naming convention as mentioned in the instructions.

2. Design a finite state machine for 8-bit ***restoring*** division. Write a synthesisable verilog code for the same. Simulate the code and show that the code you have written and the controller you have designed indeed does division. Submit the verilog code, the verilog testbench code and the FSM you have designed. You may hand draw the FSM and take a snapshot and include it in the PDF file along with the verilog code and the testbench code. Zip this PDF, verilog file and verilog test bench file. Use the naming convention as mentioned in the instructions.

3. Design a finite state machine for 8-bit ***non-restoring*** division. Write a synthesisable verilog code for the same. Simulate the code and show that the code you have written and the controller you have designed indeed does division. Submit the verilog code, the verilog testbench code and the FSM you have designed. You may hand draw the FSM and take a snapshot and include it in the PDF file along with the verilog code and the testbench code. Zip this PDF, verilog file and verilog test bench file. Use the naming convention as mentioned in the instructions.

4. Design a finite-state machine that illustrates the operation of a digital watch with two function buttons. Each successive push of button 1 causes the watch to change from displaying the time, to setting the hours, to setting the minutes and back to displaying the time again and so on. Button 2 allows the user to increment either the hours or the minutes when the watch is in the appropriate state.

5. Design an FSM for a digital hardware circuit used to control an automatic teller machine that performs three tasks: tells the user the balance of his bank account, permits the user to withdraw an amount of money not greater than the balance on his account, and permits the user to deposit money into his account.

6. The overall objective is to create a line tracking robot. The system has two digital inputs and two digital outputs. You can simulate the system with two switches and two LEDs, or build a robot with two DC motors and two optical reflectance sensors. Both sensor inputs will be on if the machine is completely on the line. One sensor input will be on and the other off if the machine is just going off the track. If the machine is totally off the line, then both sensor inputs will be off. Implement the controller using a finite state machine. Choose a Moore or Mealy format as appropriate.

7. Consider a FSM that will receive input from a keypad and lock/unlock a door:
1. The keypad has digits 0...9.
2. On power up, the door is locked.
3. As soon as the sequence 1, 1, 3, 8 is entered, the door must be unlocked.

4. Once in a not locked state, when 0 is entered, the door is immediately locked and the FSM returns to a state in which it is waiting for a code.
5. As soon as the sequence 1, 1, 3, 0 is entered, the FSM sounds an alarm and the door is permanently locked.
6. Sequences other than the two listed above are ignored.
7. The events are: 0, 1, ...9.
8. The actions are: LOCK, UNLOCK, ALARM and none (X).

Draw the diagram that describes the behaviour of this FSM.