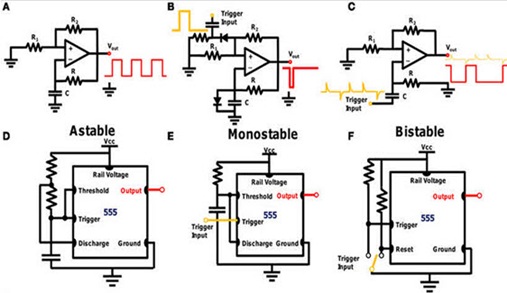
**DIGITAL CIRCUIT AND SYSTEMS**

**ASSIGNMENT - 6**

**SUBMITTED BY: MANAN (2018UIC3087)**

**Q1. Explain various types of multivibrators.**

**Answer** - Multi-vibrator circuits refer to the special type of electronic circuits used for generating pulse signals. These pulse signals can be rectangular or square wave signals. They generally produce output in two states: high or low. A specific characteristic of multi-vibrators is the use of passive elements like resistor and capacitor to determine the output state.



*Multivibrator Circuits*

## **Types of Multi-Vibrators**

a. **Monostable Multi-vibrator**: A monostable multivibrator is the type of multivibrator circuit whose output is in only one stable state. It is also known as one-shot multivibrator. In a monostable multivibrator, the output pulse duration is determined by the RC time constant and is given as: 1.11\*R\*C

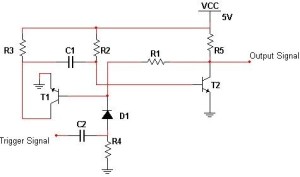
b. **Astable Multi-vibrator**: A stable vibrator is a circuit with an oscillating output. It doesn’t need any external triggering, and it has got no stable state. It is a type of regenerative oscillator.

c. **Bistable Multi-vibrator**: A bistable vibrator is a circuit with two stable states: high and low. Generally a switch is required for toggling between the high and low state of the output.

### **Three Types of Multi-vibrator Circuits**

1. **Monostable Multi-vibrator**

**a. Using Transistors**



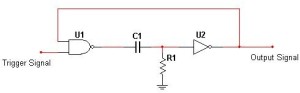
*Monostable Multi-vibrator Circuit*

In the above circuit, in absence of any external trigger signal, the base of the transistor T1 is at the ground level and the collector is at a higher potential. Therefore, the transistor is cut off. However, the base of the transistor T2 gets positive voltage supply from the VCC through a resistor, and the transistor T2 is driven to saturation. And, as the output pin is connected to the ground through the T2, it is at logic low level.

When a trigger signal is applied to the base of the transistor T1, it starts conducting as its base current increases. As the transistor conducts, its collector voltage decreases. At the same time, the capacitor C2’s voltage starts discharging through the T1. Since the output pin is now directly connected to a positive supply through resistor: Vout is at logic high level.

After sometime, when the capacitor is discharged completely, it starts charging up through the resistor. The potential at the base terminal of transistor T2 starts increasing gradually and eventually the T2 is driven to conduction. Thus, the output is again at a logic low level or the circuit is back to its stable state.

**b. Using Logic Gates**



*Mono-Stable Multi-Vibrator Circuit*

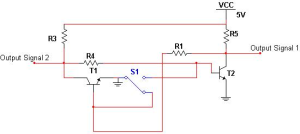
Initially the potential across the resistor is at ground level. This implies a low logic signal to the input of the NOT gate. Thus, the output is at logic high level.

As both the inputs of NAND gate are at logic high levels, the output is at logic low level, and the circuit output remains in its stable state.

Now, suppose a logic low signal is given to one of the inputs of the NAND gate, the other input being at logic high level, the output of the gate is logic 1, i.e., positive voltage. Since there is a potential difference across R, VR1 is at logic high level, and accordingly the output of the NOT gate is logic 0. As this logic low signal is fed back to the input of NAND gate, its output remains at logic 1 and the capacitor voltage starts increasing gradually. This in turn causes the potential drop across the resistor, i.e., VR1 starts decreasing gradually and at one point it goes low, such that a logic low signal is fed to the input of NOT gate, and the output is again at logic high signal. The time period for which the output remains in its stable state is determined by the RC time constant.

**2. Bistable Multivibrator**

**a. Using Transistors**



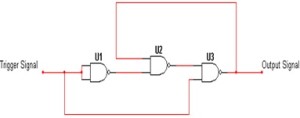
*Bistable Multivibrator Circuit*

The above circuit is a bistable multivibrator circuit with two outputs, defining the two stable states of the circuit.

Initially, when the switch is at the position A, the base of transistor T1 is at the ground potential, and therefore, it is cut off. At the same time, the base of transistor T2 is at a comparatively higher potential, it starts conducting. This causes output pin 1 to be directly connected to the ground, and the Vout1 to be at logic low level. The output pin2 at the collector of T1 is connected directly to the Vcc, and the Vout2 is at logic high level.

**b. Using Logic Gates**

The simplest form of bistable multi-vibrator is the SR latch, realized by logic gates.



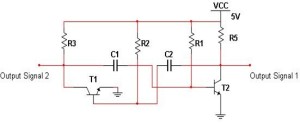
*Bistable Multi-vibrator Circuit*

Suppose the initial output is at a logic high level (Set) and the input trigger signal is at a logic low signal (Reset). This causes the output of NAND gate 1 to be at logic high level. As both the inputs of U2 are at logic high level, the output is at logic low level.

Since both the inputs of U3 are at a logic high level, the output is at logic low level, i.e., Reset. The same operation occurs for a logic high signal at the input, and the circuit changes state between 0 and 1. As seen the use of logic gates for multi-vibrators are actually examples of digital logic circuits.

**3. Astable Multivibrator**

1. **Using Transistors**



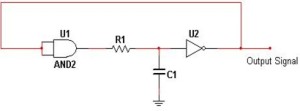
*Astable Multivibrator Circuit*

The above circuit is an oscillator circuit. Suppose, initially the transistor T1 is in conduction and T2 is in cut off. The output 2 is at logic level, and the output 1 is at logic low level. As the capacitor c2 starts charging up through R4, the potential at the base of T2 starts increasing gradually until T2 starts conducting. This decreases its collector potential and gradually the potential at the base of T1 starts decreasing until it is completely cut off.

Now, as C1 charges through R1, the potential at the base of the transistor T1 starts increasing and eventually it is driven to conduction, and the whole process repeats. Thus, the output is constantly repeating or oscillating.

Apart from using BJTs, other types of transistors are also used in multi-vibrator circuits.

**b. Using Logic Gates**



*Astable Multi-vibrator Circuit*

Initially, when the supply is given, the capacitor is uncharged and a logic low signal is fed to the input of the NOT gate. This causes the output to be at logic high level. As this logic high signal is fed back to the AND gate, its output is at logic 1. The capacitor starts charging and the input level of the NOT gate increases until it reaches the logic high threshold, and the output is at logic low.

Again, the AND gate output is at logic low (logic low input is being fed back), and the capacitor starts discharging until its potential at input of the NOT gate reaches logic low threshold, and the output is again switched back to the logic high.

This is actually a type of relaxation oscillator circuit.

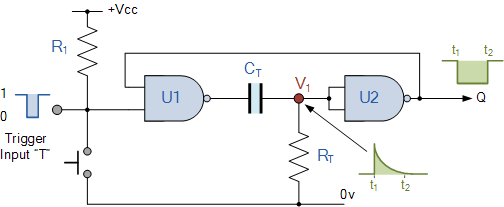
**Q2. Explain in detail the gated version of Monostable Multivibrator.**

**Answer -** Monostable Multivibrators or “one-shot” pulse generators are generally used to convert short sharp pulses into wider ones for timing applications. Monostable multivibrators generate a single output pulse, either “HIGH” or “LOW”, when a suitable external trigger signal or pulse T is applied.

This trigger pulse signal initiates a timing cycle which causes the output of the monostable to change state at the start of the timing cycle, ( t1 ) and remain in this second state until the end of the timing period, ( t2 ) which is determined by the time constant of the timing capacitor, CT and the resistor, RT.

The monostable multivibrator now stays in this second timing state until the end of the RC time constant and automatically resets or returns itself back to its original (stable) state. Then, a monostable circuit has only one stable state. A more common name for this type of circuit is simply a “Flip-Flop” as it can be made from two cross-coupled NAND gates (or NOR gates) as we have seen previously. Consider the circuit below.

### **Simple NAND Gate Monostable Circuit**



Suppose that initially the trigger input T is held HIGH at logic level “1” by the resistor R1 so that the output from the first NAND gate U1 is LOW at logic level “0”, (NAND gate principals). The timing resistor, RT is connected to a voltage level equal to logic level “0”, which will cause the capacitor, CT to be discharged. The output of U1 is LOW, timing capacitor CT is completely discharged therefore junction V1 is also equal to “0” resulting in the output from the second NAND gate U2, which is connected as an inverting NOT gate will therefore be HIGH.

The output from the second NAND gate, ( U2 ) is fed back to one input of U1 to provide the necessary positive feedback. Since the junction V1 and the output of U1 are both at logic “0” no current flows in the capacitor CT. This results in the circuit being **Stable** and it will remain in this state until the trigger input T changes.

If a negative pulse is now applied either externally or by the action of the push-button to the trigger input of the NAND gate U1, the output of U1 will go HIGH to logic “1” (NAND gate principles).

Since the voltage across the capacitor cannot change instantaneously (capacitor charging principals) this will cause the junction at V1 and also the input to U2 to also go HIGH, which in turn will make the output of the NAND gate U2 change LOW to logic “0” The circuit will now remain in this second state even if the trigger input pulse T is removed. This is known as the **Meta-stable** state.

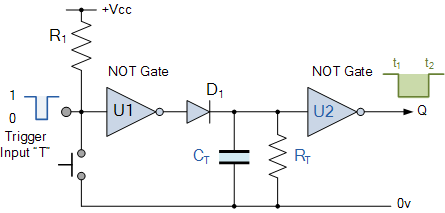
The voltage across the capacitor will now increase as the capacitor CT starts to charge up from the output of U1 at a time constant determined by the resistor/capacitor combination. This charging process continues until the charging current is unable to hold the input of U2 and therefore junction V1 HIGH.

When this happens, the output of U2 switches HIGH again, logic “1”, which in turn causes the output of U1 to go LOW and the capacitor discharges into the output of U1 under the influence of resistor RT. The circuit has now switched back to its original stable state.

Thus for each negative going trigger pulse, the monostable multivibrator circuit produces a LOW going output pulse. The length of the output time period is determined by the capacitor/resistor combination (**RC Network**) and is given as the **Time Constant** T = 0.69RC of the circuit in seconds. Since the input impedance of the NAND gates is very high, large timing periods can be achieved.

As well as the NAND gate monostable type circuit above, it is also possible to build simple monostable timing circuits that start their timing sequence from the rising-edge of the trigger pulse using NOT gates, NAND gates and NOR gates connected as inverters as shown below.

### **NOT Gate Monostable Multivibrator**



As with the NAND gate circuit above, initially the trigger input T is HIGH at a logic level “1” so that the output from the first NOT gate U1 is LOW at logic level “0”. The timing resistor, RT and the capacitor, CT are connected together in parallel and also to the input of the second NOT gate U2. As the input to U2 is LOW at logic “0” its output at Q is HIGH at logic “1”.

When a logic level “0” pulse is applied to the trigger input T of the first NOT gate it changes state and produces a logic level “1” output. The diode D1 passes this logic “1” voltage level to the RC timing network. The voltage across the capacitor, CT increases rapidly to this new voltage level, which is also connected to the input of the second NOT gate. This in turn outputs a logic “0” at Q and the circuit stays in this **Meta-stable** state as long as the trigger input T applied to the circuit remains LOW.

When the trigger signal returns HIGH, the output from the first NOT gate goes LOW to logic “0” (NOT gate principals) and the fully charged capacitor, CT starts to discharge itself through the parallel resistor, RT connected across it. When the voltage across the capacitor drops below the lower threshold value of the input to the second NOT gate, its output switches back again producing a logic level “1” at Q. The diode D1 prevents the timing capacitor from discharging itself back through the first NOT gates output.

Then, the **Time Constant** for a NOT gate **Monostable Multivibrator** is given as T = 0.8RC + Trigger in seconds.

One main disadvantage of **Monostable Multivibrators** is that the time between the application of the next trigger pulse T has to be greater than the RC time constant of the circuit.