# Name : Manan Madan

## Roll No : 2018UIC3087

# Q1

# Transistor-Transistor Logic (TTL)

Logic Gates like NAND, NOR are used in daily applications for performing logic operations. The Gates are manufactured using semiconductor devices like BJT, Diodes or FETs. Different Gate’s are constructed using Integrated circuits. Digital logic circuits are manufactured depending on the specific circuit technology or logic families.

## Tri-state Logic:

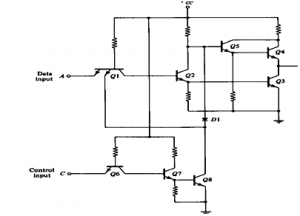
name itself implies there are 3 states of the buffer

high (1)

low (0)

High Impedance (Z)

In electronics, **high impedance** means that a point in a circuit (a node) allows a relatively small amount of current through, per unit of applied voltage at that point. **High impedance** circuits are low current, **high** voltage, whereas low **impedance**circuits are the opposite.

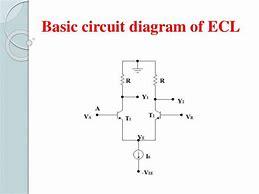


1. Low level state when lower transistor is ON and upper transistor is OFF.
2. High level state when lower transistor is OFF and upper transistor is ON.
3. Third state when both transistors are OFF. It [allows a direct wire connection](https://www.edgefxkits.com/wireless-scada) of many outputs.

# Q2

ANS: Emitter-coupled logic (ECL) is a high-speed integrated circuit bipolar transistor logic family. ECL uses an overdriven BJT differential amplifier with single-ended input and limited emitter current to avoid the saturated (fully on) region of operation and its slow turn-off behavior.As the current is steered between two legs of an emitter-coupled pair, ECL is sometimes called current-steering logic (CSL),current-mode logic (CML) or current-switch emitter-follower (CSEF) logic.

The circuit consists of a differential amplifier. a temperature- and voltage-compensated bias network. And an emitter-follower output. The emitter outputs require a pull-down resistor for current to flow. This is obtained from the input resistor Rp of another similar gate or from an ex tern al resistor connected to a negative voltage supply.



In ECL, the transistors are never in saturation, the input/output voltages have a small swing (0.8 V), the input impedance is high and the output impedance is low. As a result, the transistors change states quickly, gate delays are low, and the fanout capability is high. In addition, the essentially constant current draw of the differential amplifiers minimises delays and glitches due to supply-line inductance and capacitance, and the complementary outputs decrease the propagation time of the whole circuit by reducing inverter count.

**Noise Margin Calculation**  
Logic Noise Margin is the difference between what the driver IC outputs as a valid logic voltage and what the receiver IC expects to see as a valid logic voltage. There are two different types of noise margin, one for a logic high value and one for a logic low value . For a valid logic high, the worst case noise margin for the circuit is the minimum high level voltage which may be output from the driver, minus, the minimum high level voltage which may be seen at the receiver IC. For a valid logic low, the worst case noise margin for the circuit is the maximum low level voltage which may be output from the driver; minus, the maximum low level voltage which may be seen at the receiver IC. The equations for noise margins are provided below, use the minimum of maximum numbers as described above.  
   
Noise Margin Output high = VOH [driving device] - VIH [receiving device]  
Noise Margin Output low = VIL [receiving device] - VOL [driving device]  
The higher the numbers the better, with negative numbers indicating in-operability [no Noise Margin].  
Use Minimum numbers for output High, and maximum numbers for Output Low to calculate Noise Margin.

FOR ECL

Prop. Delay= 1.45ns

Rise/fall time= o.35ns

VIH min  = -1.165v

VIL max= -1.475v

VOH min = -1.025v

Vol **m**ax = -1.610v

NOISE MARGIN = 0.135V

POWER DISSIPATION :

