Basic computer

With Verilog

Our team

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About the project:

This is verilog module implementation of a simple computer, referred to as the "Basic Computer." It has the following components:

- A clock input (clk).
- Eight-bit registers for instruction register (IR), data register (DR), and accumulator (AC).
- A four-bit program counter (PC) and address register (AR).
- A flag for indirect addressing mode (I), as well as carry (E) and start (S) flip-flops.
- A memory array (MEM) with 16 ×8-bit words.
- in put register (as a in put for adder and logic)
- Out put register
- An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used in the arithmetic logic units.
- Before everything we do some important instructions:
  - ✓ Fetch: (The Control Unit generates the control signals that copy an instruction byte from the memory into the Instruction Register, IR. The address of this instruction is in the Program Counter, PC.), and
  - ✓ Decode: (which is a hardware component inside the CPU – decodes the binary instruction and decides how to deal with the electrical signal (the instruction) based on the instruction.)
- And finally we do “Instruction execute”

  The 8 bits in the IR are connected to the Control Unit. These 8 bits determine the sequence of control signals that the Control Unit generates. The sequence of control signals generated by the Control Unit causes the execution of the instruction. The sequence finishes by starting fetch and decode ,so fetching the next instruction into the IR.The system clock signal determines the timing of all these control signals. There are a large number of control signals. Thus there will

be a control signal that is connected to the enable input of a three-state buffer that connects a register to a bus. There will be other signals that are connected to the load input of every register so causing that register to be loaded from the bus. Yet other signals will go to the ALU_mode control signals of the ALU causing the ALU to be set to perform a particular arithmetic or logical operation. Another control signal is connected to the WriteEnable input of the memory so determining whether the memory will read or write.

Control Functions and Micro operation for the Basic Computer :

Fetch	T_0	AR ← PC
	T_1	IR ←M[AR] , PC ←Pc+1
Decode	T_2	D0,..,D3 ← IR(6-4) , AR←IR (3-0) I ← IR (7) ,
indirect	$D_7\,'I\,T_3$	AR←M[AR]

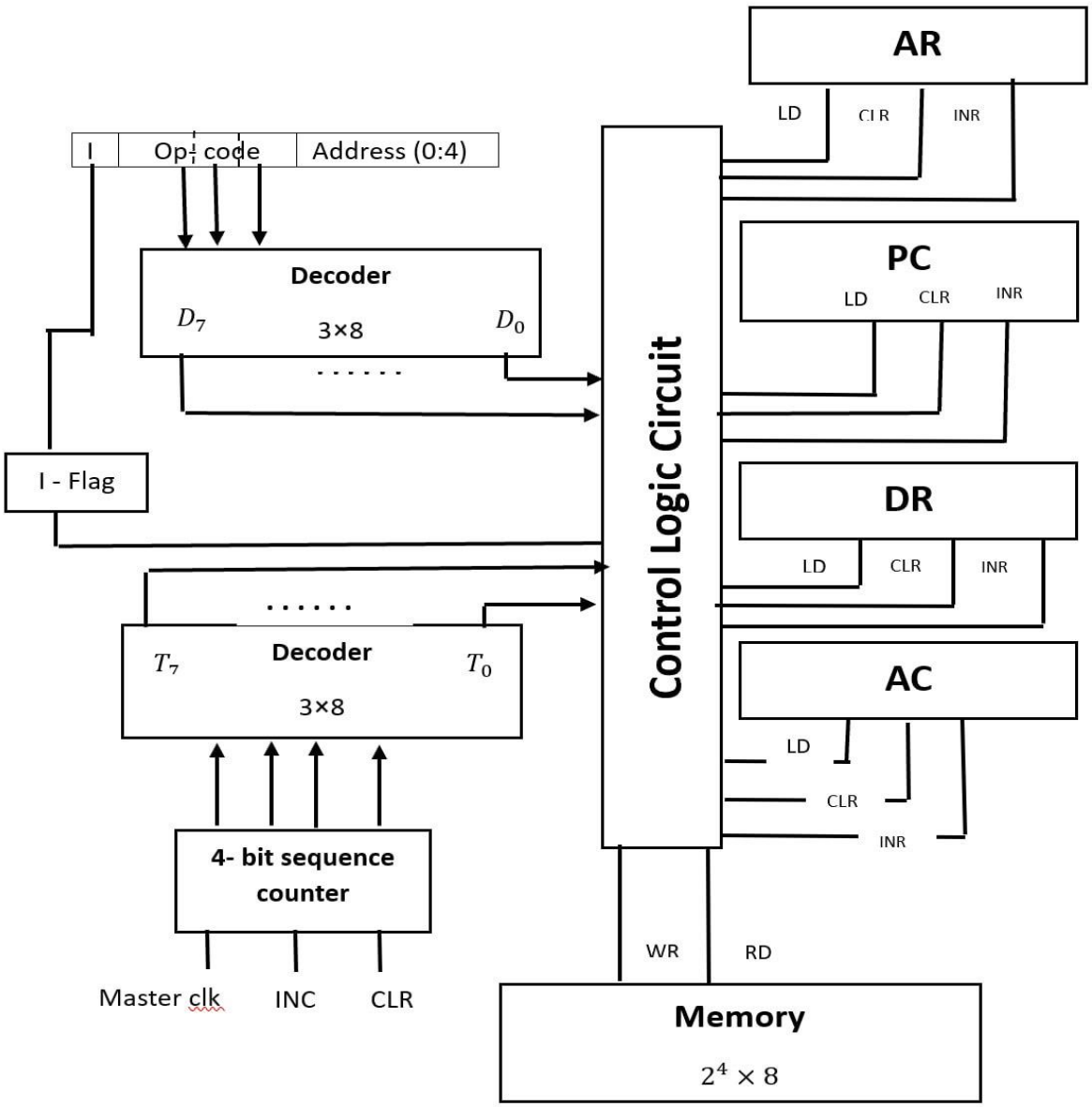
Memory Reference

AND	$D_0\,T_4$	DR← M[AR]
	$D_0\,T_5$	AC← AC&DR , SC← 0
ADD	$D_1\,T_4$	DR← M[AR]
	$D_1\,T_5$	AC← AC+DR, SC← 0
LDA	$D_5\,T_4$	DR← M[AR]
	$D_5\,T_5$	AC ← DR, SC←0
BUN	D_6T_4	PC ← AR, SC← 0

Register Reference:

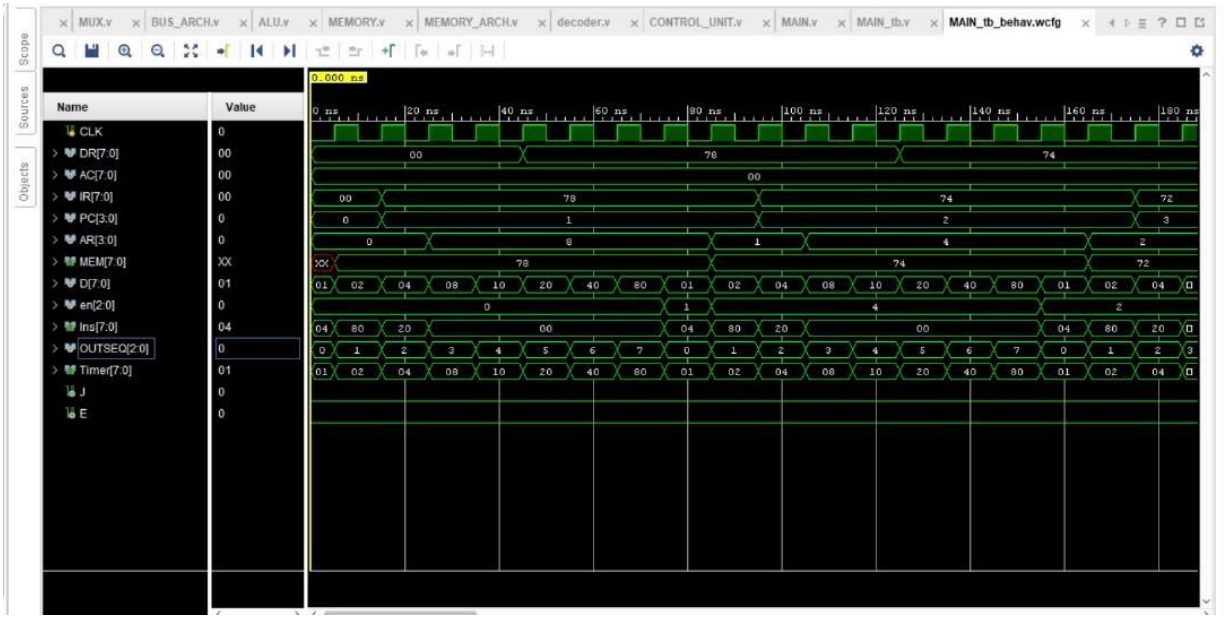
CLA	rB_3	AC← 0, SC← 0
CMA	rB_2	AC ← ~AC, SC← 0
INC	rB_1	AC ← AC + 1, SC← 0

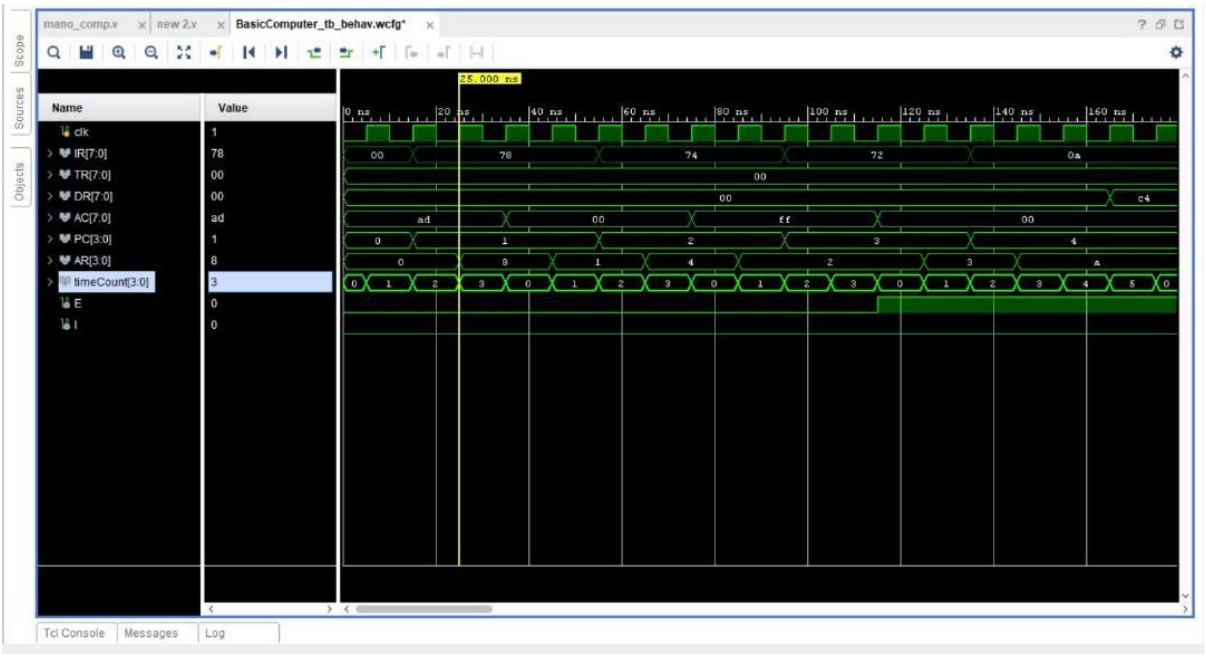
Computer design :

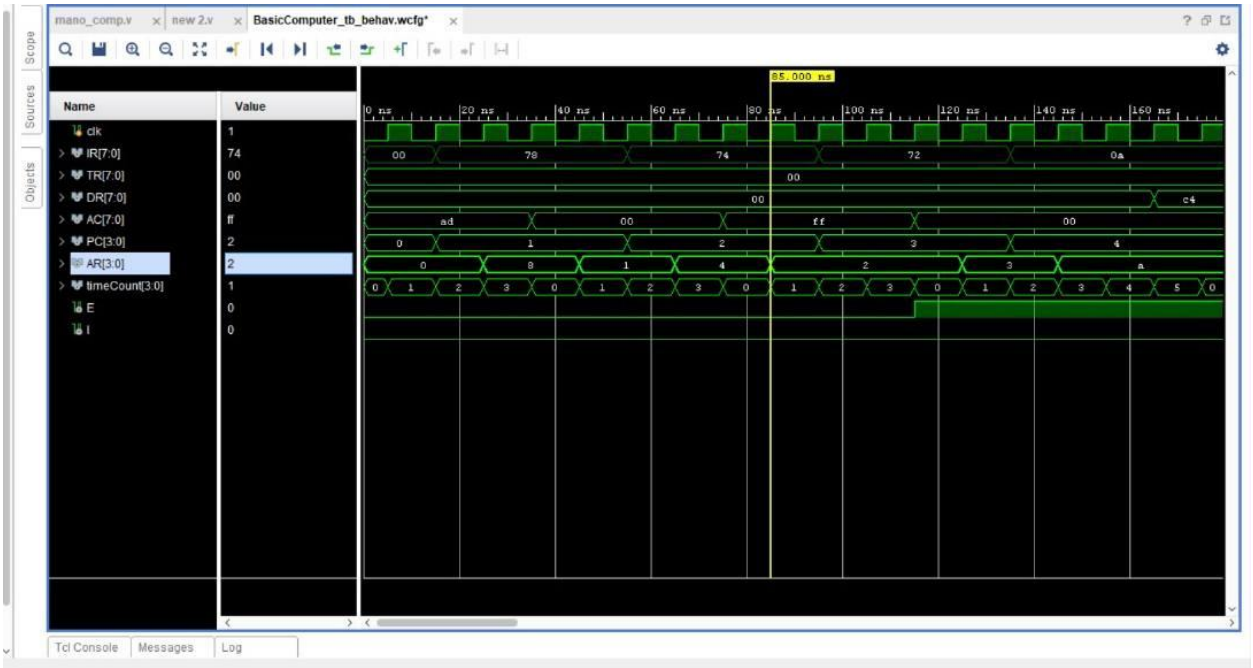


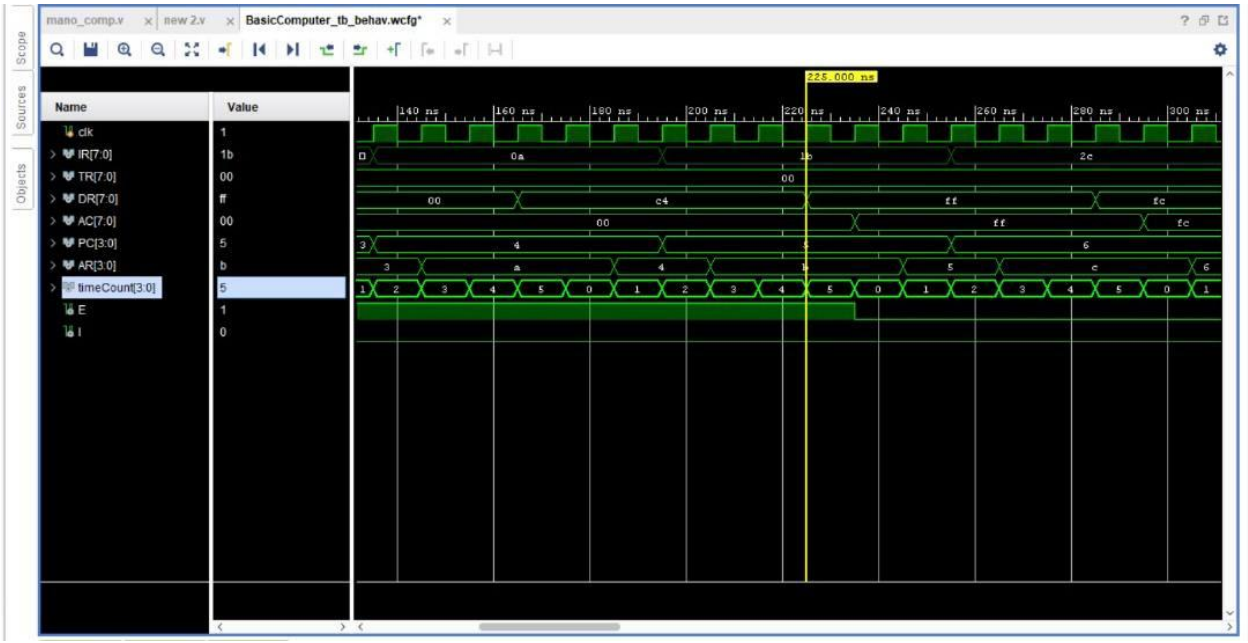
- Link to the code on github
  https://github.com/manar-mohmd/Computer_Mano.git

- Simulation



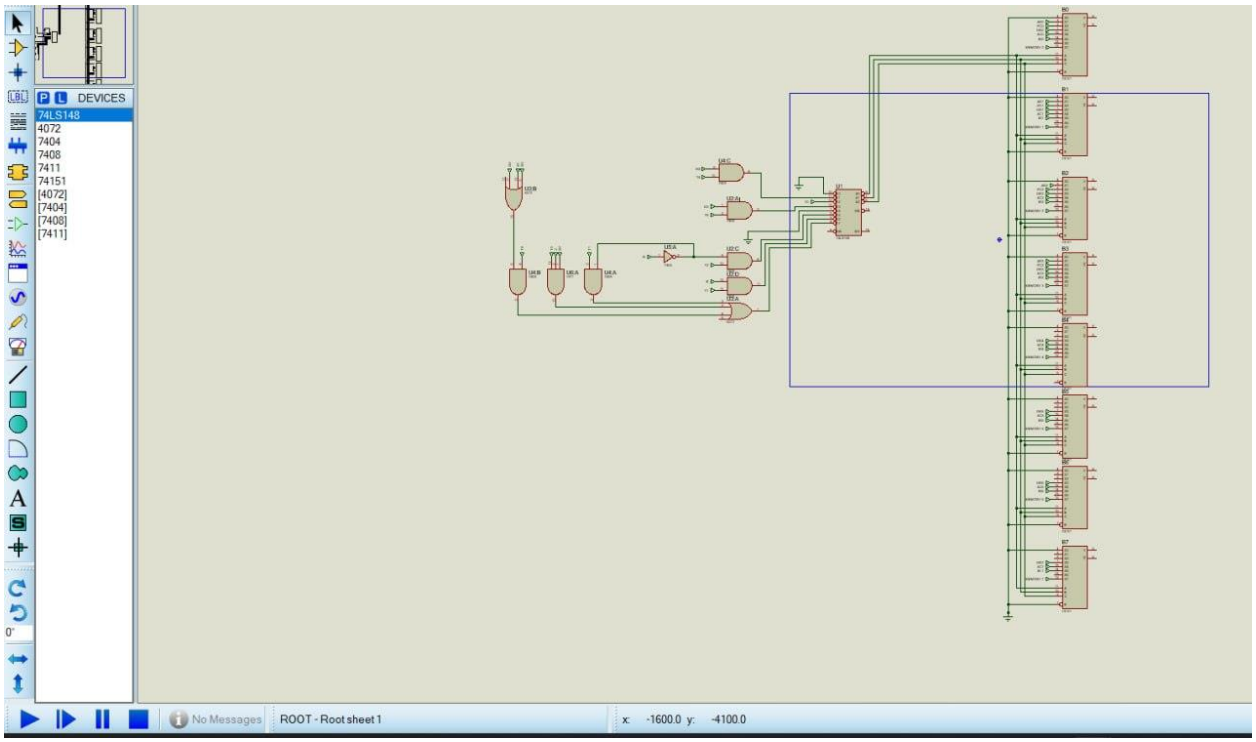

mano_comp.v
new 2.v
BasicComputer_tb_behav.wcfg*
Name
Value
clk 1
IR[7:0] 78
TR[7:0] 00
DR[7:0] 00
AC[7:0] ad
PC[3:0] 1
AR[3:0] 8
timeCount[3:0] 3
E 0
I 0
25.000 ns
Tcl Console
Messages
Log


mano_comp.v
new 2.v
BasicComputer_tb_behav.wcfg*
Name
Value
clk 1
IR[7:0] 74
TR[7:0] 00
DR[7:0] 00
AC[7:0] ff
PC[3:0] 2
AR[3:0] 2
timeCount[3:0] 1
E 0
I 0
85.000 ns
Tcl Console
Messages
Log

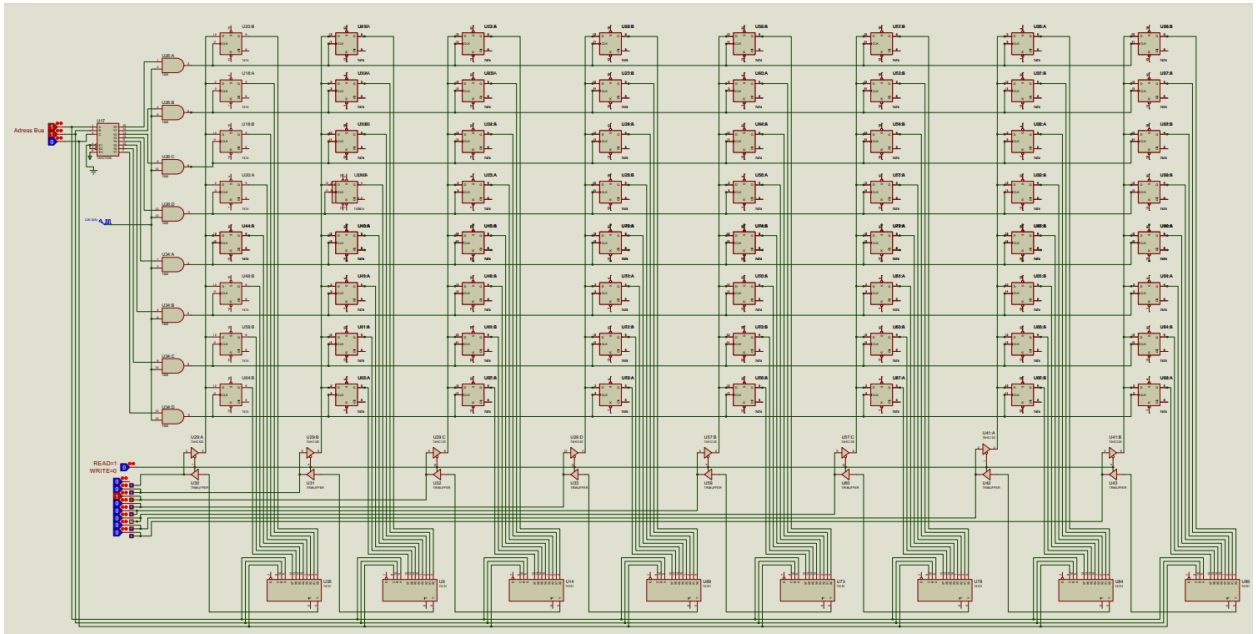

mano_comp.v
new 2.v
BasicComputer_tb_behav.wcfg*
Scope
Sources
Objects
Name
Value
clk
IR[7:0]
TR[7:0]
DR[7:0]
AC[7:0]
PC[3:0]
AR[3:0]
timeCount[3:0]
E
I
1
1b
00
ff
00
5
b
5
1
0
225.000 ns
140 ns
160 ns
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns

- Proteus simulation

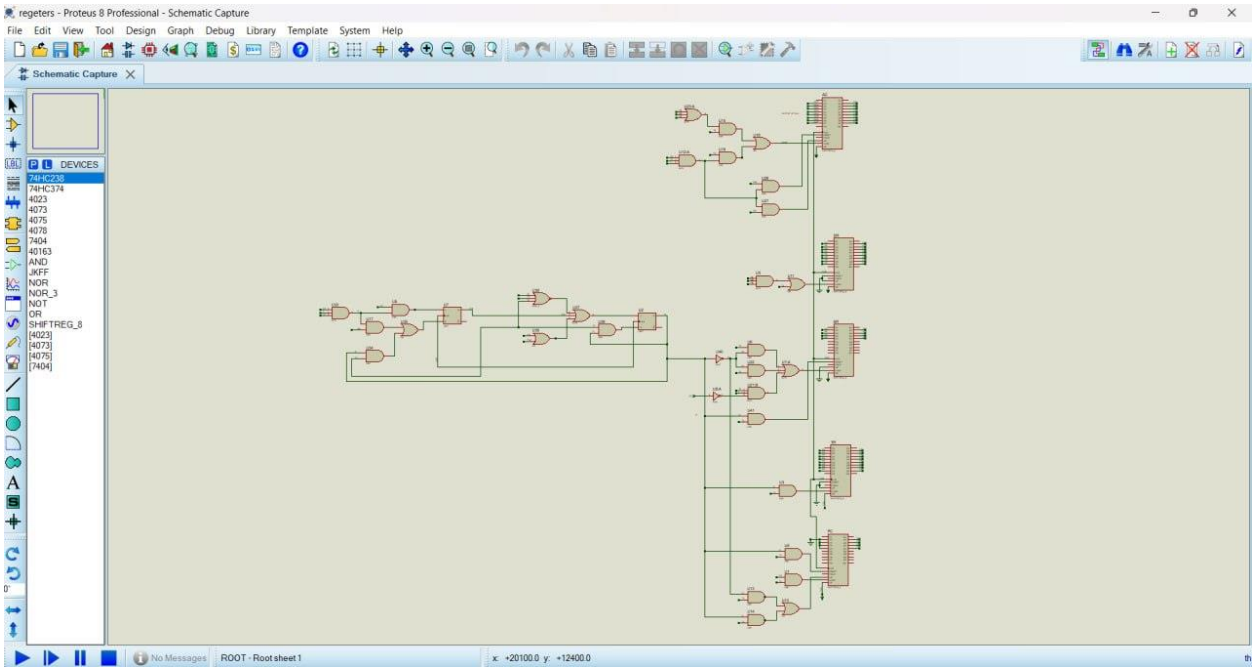
Bus



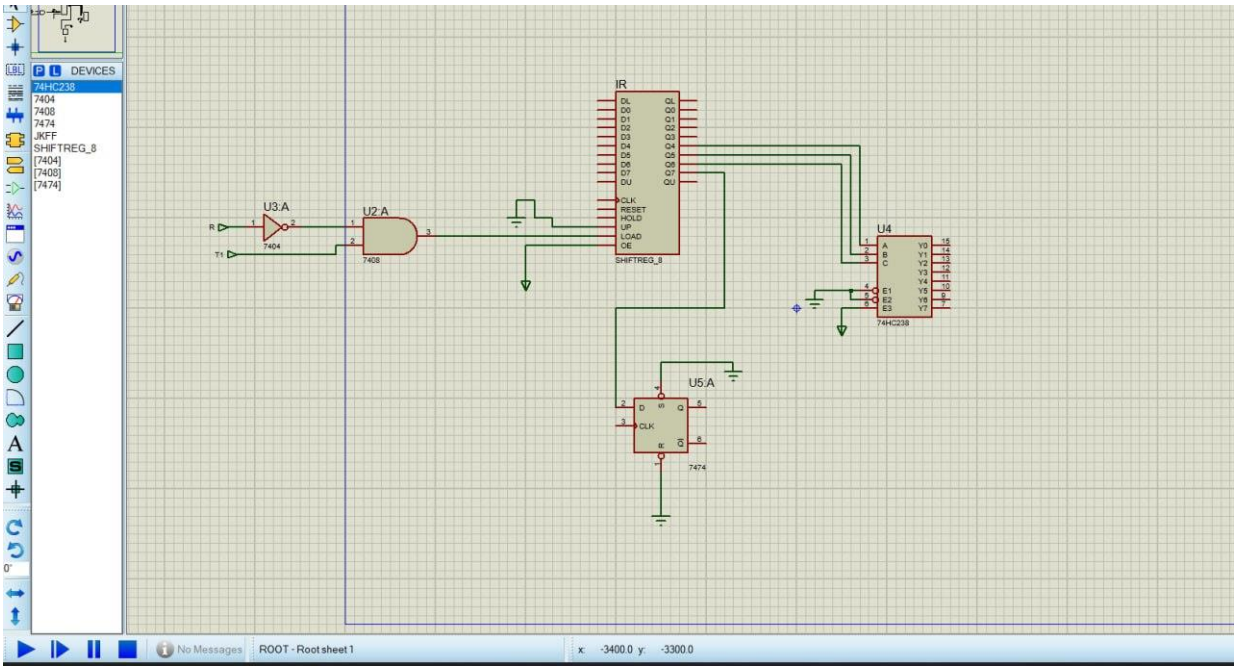
Memory



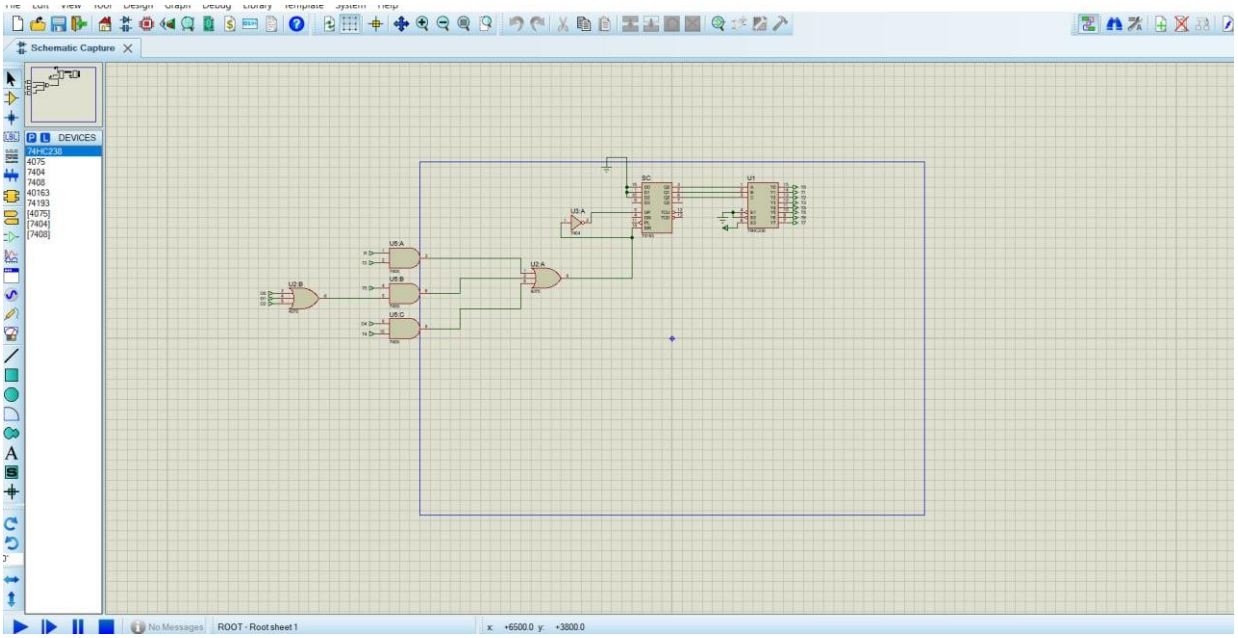
Registers



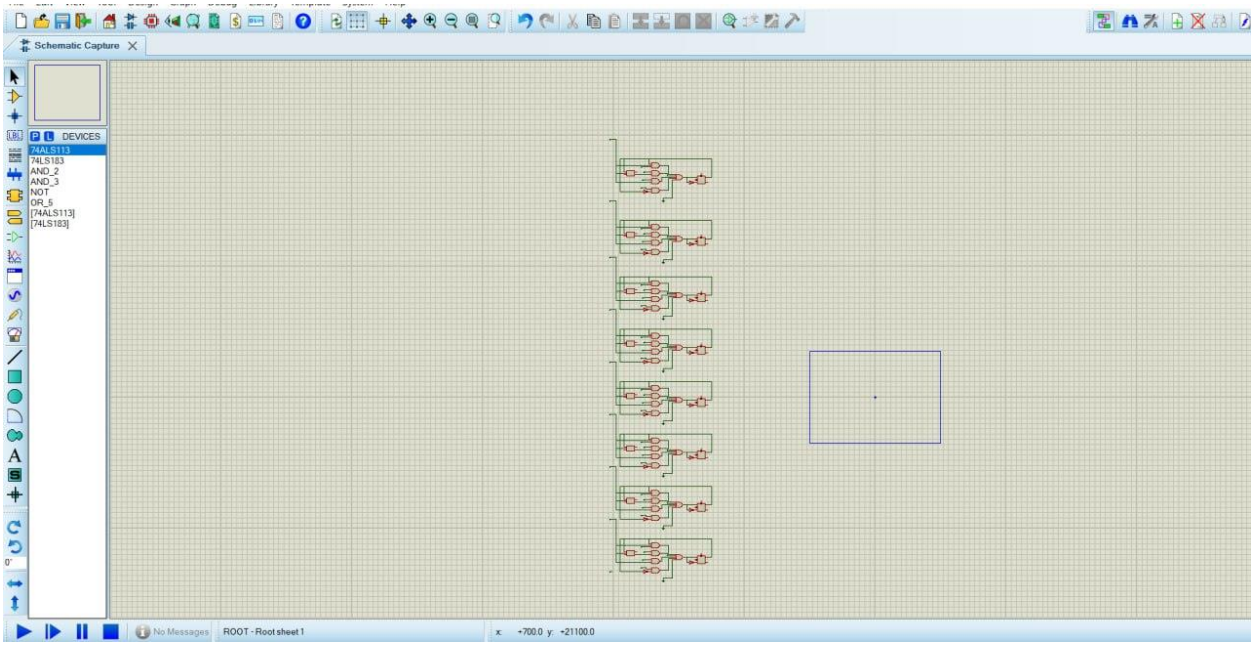
IR



SC


Schematic Capture
DEVICES
74HC238
4075
7404
7408
40163
74193
[4075]
[7404]
[7408]
No Messages
ROOT - Root sheet 1

ALU


Schematic Capture
DEVICES
74ALS113
74LS183
AND_2
AND_3
NOT
OR_5
[74ALS113]
[74LS183]
No Messages
ROOT - Root sheet 1

Basic Computer