

Implementation of RTL to GDS flow



Presented By: Manar Abdo

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1-Introduction

The design and implementation of integrated circuits (ICs) involve a complex sequence of steps that transform an abstract functional description into a physical layout ready for fabrication. Among these steps, the RTL-to-GDS flow plays a pivotal role as it bridges the gap between high-level hardware description languages (HDLs) and the final geometrical patterns that define the chip layout. This flow ensures that the design is not only functionally correct but also meets stringent performance, area, and power requirements while remaining manufacturable.

In this project, the RTL description of a digital system transmitter is taken through the full RTL-to-GDS flow. The process begins with logic synthesis, where the RTL code is translated into a gate-level netlist. Synthesis optimization techniques are applied to achieve a high-quality result (QoR), focusing on improving area utilization, timing performance, and overall efficiency of the design. The generated netlist forms the foundation for the subsequent physical implementation stages.

The next step involves floorplanning, where the physical arrangement of functional blocks is defined with careful consideration of area, aspect ratio, and utilization. A well-planned floorplan directly influences timing closure and routing efficiency, making it a critical phase of the flow. Following this, placement, clock tree synthesis (CTS), and routing are performed to create a complete physical design. Special attention is given to clock distribution to minimize skew and ensure reliable synchronization across the chip.

Throughout the place-and-route (PnR) process, detailed documentation is maintained, including snapshots of the floorplan, placement results, CTS, and routing stages. Any timing violations identified during the process are analyzed in detail, and effective strategies are applied to resolve them. This ensures that the final design not only meets functional requirements but also adheres to strict timing and performance constraints.

The goal of this project is to generate a manufacturable GDSII layout of the digital system transmitter that is fully optimized in terms of area, timing, and performance. By carefully documenting each step synthesis QoR reports, gate-level schematics, floorplan aspects, and timing closure strategies the project provides a comprehensive overview of the complete RTL-to-GDS flow. This implementation not only demonstrates practical knowledge of modern VLSI design techniques but also highlights the importance of optimization and systematic methodology in achieving high-quality digital systems.

2-Synthesis

2.1-Compile with no constraints

2.1.1-Gate-level netlist schematic

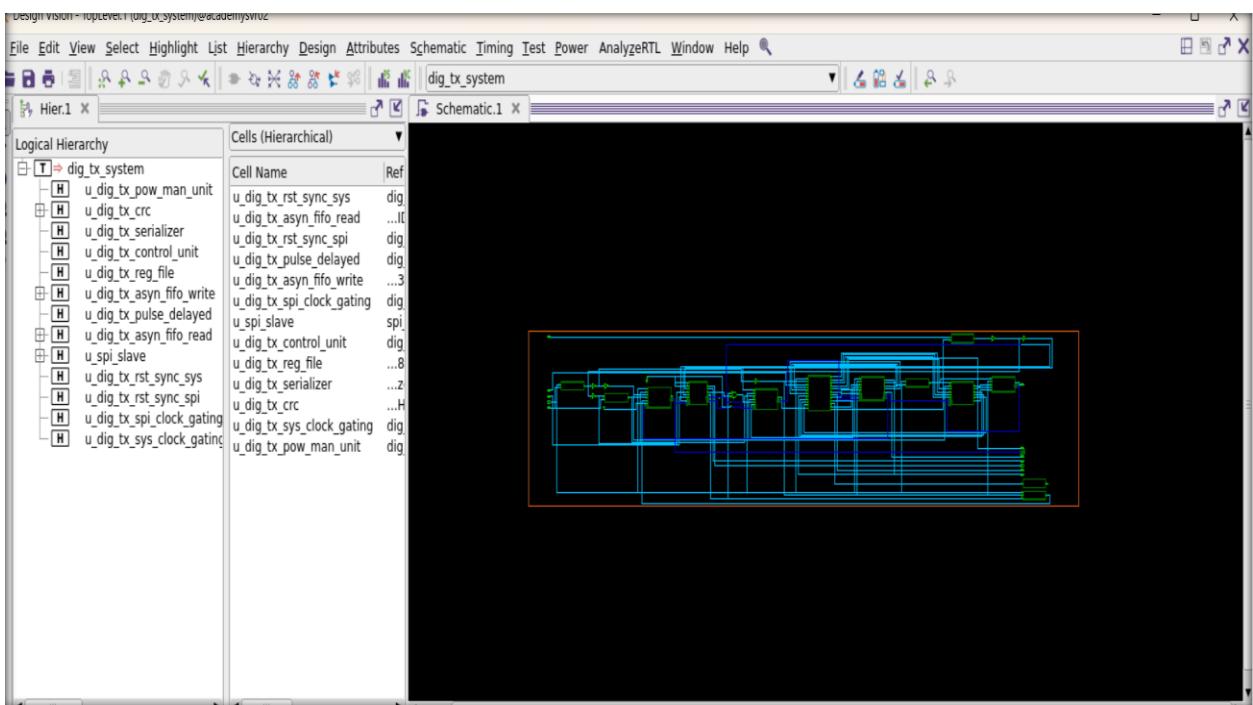


Figure 1:Gate-level netlist schematic

2.1.2-synthesis Optimization

- Optimization methods used: None

2.1.3 timing report

```
Report : timing
  -path full
  -delay max
  -max_paths 1
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date : Sun Aug 17 16:14:46 2025
*****
Operating Conditions: tt0p8v25c Library: saed14lvt_base_tt0p8v25c
Wire Load Model Mode: top
Startpoint: u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]
  (rising edge-triggered flip-flop)
```

```
Endpoint: o_dig_tx_system_miso
  (output port)
Path Group: (none)
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----  
dig_tx_system      8000                  saed14lvt_base_tt0p8v25c

Point           Incr      Path
-----  
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]/CK (SAEDLVT14_FDPRBQ_V2_1)    0.00    0.00 r  
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]/Q (SAEDLVT14_FDPRBQ_V2_1)    0.07    0.07 f  
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr[0] (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)  0.00    0.07 f  
u_dig_tx_asyn_fifo_write/fifom/i_dig_tx_fifo_mem_b_rptr[0] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2) 0.00    0.07 f  
u_dig_tx_asyn_fifo_write/fifom/U22/X (SAEDLVT14_INV_0P5)          0.27    0.34 r  
u_dig_tx_asyn_fifo_write/fifom/U21/X (SAEDLVT14_ND2_CDC_0P5)        0.31    0.65 f  
u_dig_tx_asyn_fifo_write/fifom/U6/X (SAEDLVT14_OA22_0P75)         0.04    0.69 f  
u_dig_tx_asyn_fifo_write/fifom/U5/X (SAEDLVT14_OAI21_0P5)         0.05    0.74 r  
u_dig_tx_asyn_fifo_write/fifom/o_dig_tx_fifo_mem_data_out[7] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2) 0.00    0.74 r  
u_dig_tx_asyn_fifo_write/o_dig_tx_asyn_fifo_data_out[7] (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)          0.00    0.74 r  
u_spi_slave/i_rf_din[7] (spi_slave)          0.00    0.74 r  
u_spi_slave/U46/X (SAEDLVT14_MUX12_U_0P5)       0.06    0.79 f  
u_spi_slave/U45/X (SAEDLVT14_OAI22_0P5)         0.05    0.84 r  
u_spi_slave/U44/X (SAEDLVT14_A021_1)          0.02    0.86 r  
u_spi_slave/o_miso (spi_slave)            0.00    0.86 r  
o_dig_tx_system_miso (out)                 0.00    0.86 r  
data arrival time                         0.86  
-----  
(Path is unconstrained)
```

1

Plain Text ▾ Tab Width: 8 ▾ Ln 1, C

Figure 2:timing report

2.1.4 area report

```

Report : area
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date : Sun Aug 17 16:14:46 2025
*****
Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)

Number of ports:          493
Number of nets:           2038
Number of cells:          1492
Number of combinational cells: 1089
Number of sequential cells: 378
Number of macros/black boxes: 0
Number of buf/inv:         313
Number of references:      17

Combinational area:       367.498802
Buf/Inv area:             64.957200
Noncombinational area:   389.698806
Macro/Black Box area:     0.000000
Net Interconnect area:   808.621402

Total cell area:          757.197609
Total area:                1565.819011

```

Hierarchical area distribution						
Hierarchical cell	Global cell area			Local cell area		
	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black-boxes	Design
dig_tx_system	757.1976	100.0	2.7972	0.0000	0.0000	dig_tx_system
u_dig_tx_asyn_fifo_read	225.3300	29.8	0.7992	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1
u_dig_tx_asyn_fifo_read/fifom	172.9824	22.8	83.4720	89.5104	0.0000	dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/rptr_h	17.4936	2.3	7.8588	9.6348	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/sync_rptr	8.5248	1.1	0.0000	8.5248	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_1
u_dig_tx_asyn_fifo_read/sync_wptr	8.5248	1.1	0.0000	8.5248	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_0
u_dig_tx_asyn_fifo_read/wptr_h	17.0052	2.2	7.4148	9.5904	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_write	83.0280	11.0	0.7992	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8
u_dig_tx_asyn_fifo_write/fifom	42.0024	5.5	19.6248	22.3776	0.0000	dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/rptr_h	13.2756	1.8	5.7720	7.5036	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/sync_rptr	6.9264	0.9	0.5328	6.3936	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_1
u_dig_tx_asyn_fifo_write/sync_wptr	6.6600	0.9	0.2664	6.3936	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_0
u_dig_tx_asyn_fifo_write/wptr_h	13.3644	1.8	5.9052	7.4592	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2
u_dig_tx_control_unit	26.6904	2.7	14.2968	6.3936	0.0000	dig_tx_control_unit
u_dig_tx_crc	73.7928	9.7	27.3504	42.6240	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56
u_dig_tx_crc/add_57	3.8184	0.5	3.8184	0.0000	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56_DW01_inc_0_DW01_inc_3
u_dig_tx_pow_man_unit	0.2664	0.0	0.2664	0.0000	0.0000	dig_tx_pow_man_unit
u_dig_tx_pulse_delayed	2.1312	0.3	0.0000	2.1312	0.0000	dig_tx_pulse_delayed
u_dig_tx_reg_file	139.1052	18.4	60.2508	78.8544	0.0000	dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32
u_dig_tx_rst_sync_spi	2.5752	0.3	0.3996	2.1756	0.0000	dig_tx_rst_sync_0
u_dig_tx_rst_sync_sys	2.5308	0.3	0.3996	2.1312	0.0000	dig_tx_rst_sync_1
u_dig_tx_serializer	66.1560	8.7	44.8440	21.3120	0.0000	dig_tx_serializer_32_16_24_55557a
u_dig_tx_spi_clock_gating	0.9324	0.1	0.3108	0.6216	0.0000	dig_tx_clock_gating_1
u_dig_tx_sys_clock_gating	0.9324	0.1	0.3108	0.6216	0.0000	dig_tx_clock_gating_0
u_spi_slave	136.9296	18.1	75.5244	56.9208	0.0000	spi_slave
u_spi_slave/r119	4.4844	0.6	4.4844	0.0000	0.0000	spi_slave_DW01_inc_0_DW01_inc_6
Total	367.4988	389.6988	0.0000			

Figure 3:area report

2.1.5 power report

```

Report : power
-hier
-analysis_effort low
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date  : Sun Aug 17 16:14:52 2025
*****  

Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)  

Operating Conditions: tt0p8v25c Library: saed14lvt_base_tt0p8v25c
Wire Load Model Mode: top
  

Design      Wire Load Model      Library
----- 8000      saed14lvt_base_tt0p8v25c
  

Global Operating Voltage = 0.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW   (derived from V,C,T units)
    Leakage Power Units = 1pW
  

-----  

Hierarchy          Switch  Int    Leak    Total
                  Power   Power   Power   Power   %
-----  

dig_tx_system      0.152  4.84e-02 2.07e+06  0.293 100.0
  u_dig_tx_pow_man_unit (dig_tx_pow_man_unit)
    0.000  0.000 1.26e+03 1.25e-06  0.0
  u_dig_tx_crc (dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56)
    4.82e-03 2.42e-04 1.65e+05 4.42e-03  2.2
    add 57 (dig_tx_crc REGISTER_WIDTH16_INPUT_LENGTH56_DW01_inc_0 DW01_inc_3)
  

-----  

-----  

u_dig_tx_reg_file (dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32)
  1.90e-03 8.05e-04 4.97e+04 2.76e-03  1.4
  2.91e-02 1.05e-02 3.61e+05 4.00e-02 19.7
u_dig_tx_asyn_fifo_write (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
  1.49e-02 7.45e-03 2.53e+05 2.26e-02 11.2
  fifom (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
    5.13e-03 3.71e-03 1.38e+05 8.97e-03  4.4
  rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)
    1.65e-03 9.30e-04 3.87e+04 2.62e-03  1.3
  wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2)
    2.35e-03 1.02e-03 3.70e+04 3.41e-03  1.7
  sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_1)
    1.90e-03 8.49e-04 1.88e+04 2.77e-03  1.4
  sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_0)
    1.34e-03 7.53e-04 1.72e+04 2.11e-03  1.0
u_dig_tx_pulse_delayed (dig_tx_pulse_delayed)
  0.000 1.93e-04 5.43e+03 1.99e-04  0.1
u_dig_tx_asyn_fifo_read (dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1)
  3.97e-02 2.05e-02 7.09e+05 6.09e-02 30.0
  fifom (dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3)
    2.78e-02 1.50e-02 5.65e+05 4.34e-02 21.4
  rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH3)
    3.37e-03 1.49e-03 5.08e+04 4.92e-03  2.4
  wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3)
    2.38e-03 1.44e-03 4.64e+04 3.87e-03  1.9
  sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_1)
    0.000 1.24e-03 2.13e+04 1.26e-03  0.6
  sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_0)
    0.000 1.17e-03 2.17e+04 1.19e-03  0.6
u_spi_slave (spi_slave)
  5.42e-02 7.48e-03 3.44e+05 6.20e-02 30.6
  r119 (spi_slave_DW01_inc_0 DW01_inc_6)
    0.000  0.000 1.21e+04 1.21e-05  0.0
u_dig_tx_RST_SYNC_SYS (dig_tx_RST_SYNC_1)
  1.20e-04 3.35e-04 7.63e+03 4.62e-04  0.2
u_dig_tx_RST_SYNC_SPI (dig_tx_RST_SYNC_0)
  1.76e-03 3.63e-04 8.32e+03 2.13e-03  1.0
u_dig_tx_SPI_CLOCK_GATING (dig_tx_CLOCK_GATING_1)
  1.59e-04 1.17e-04 3.57e+03 2.80e-04  0.1
u_dig_tx_SYS_CLOCK_GATING (dig_tx_CLOCK_GATING_0)
  0.000 7.50e-05 3.36e+03 7.84e-05  0.0
1

```

Figure 4:power report

2.1.6 qor report

```
*****  
Report : qor  
Design : dig_tx_system  
Version: W-2024.09-SP5-1  
Date   : Sun Aug 17 16:14:46 2025  
*****  
  
Timing Path Group (none)  
-----  
Levels of Logic:          7.00  
Critical Path Length:    0.86  
Critical Path Slack:     uninit  
Critical Path Clk Period: n/a  
Total Negative Slack:    0.00  
No. of Violating Paths:  0.00  
Worst Hold Violation:   0.00  
Total Hold Violation:   0.00  
No. of Hold Violations: 0.00  
-----  
  
Cell Count  
-----  
Hierarchical Cell Count:  25  
Hierarchical Port Count: 473  
Leaf Cell Count:         1467  
Buf/Inv Cell Count:      313  
Buf Cell Count:          104  
Inv Cell Count:          209  
CT Buf/Inv Cell Count:   0  
Combinational Cell Count: 1089  
Sequential Cell Count:   378  
Macro Count:              0  
-----
```

```
Buf/Inv Area:       64.957200  
Total Buffer Area: 27.71  
Total Inverter Area: 37.25  
Macro/Black Box Area: 0.000000  
Net Area:          808.621402  
-----  
Cell Area:          757.197609  
Design Area:        1565.819011  
  
Design Rules  
-----  
Total Number of Nets:      1579  
Nets With Violations:    0  
Max Trans Violations:    0  
Max Cap Violations:      0  
-----  
Hostname: academysvr02  
Compile CPU Statistics  
-----  
Resource Sharing:          7.07  
Logic Optimization:        1.76  
Mapping Optimization:      1.44  
-----  
Overall Compile Time:     28.55  
Overall Compile Wall Clock Time: 31.25  
-----  
Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0  
Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0  
-----  
1
```

Figure 5:qor report

2.2-Compile for area

2.2.1- Gate-level netlist schematic:

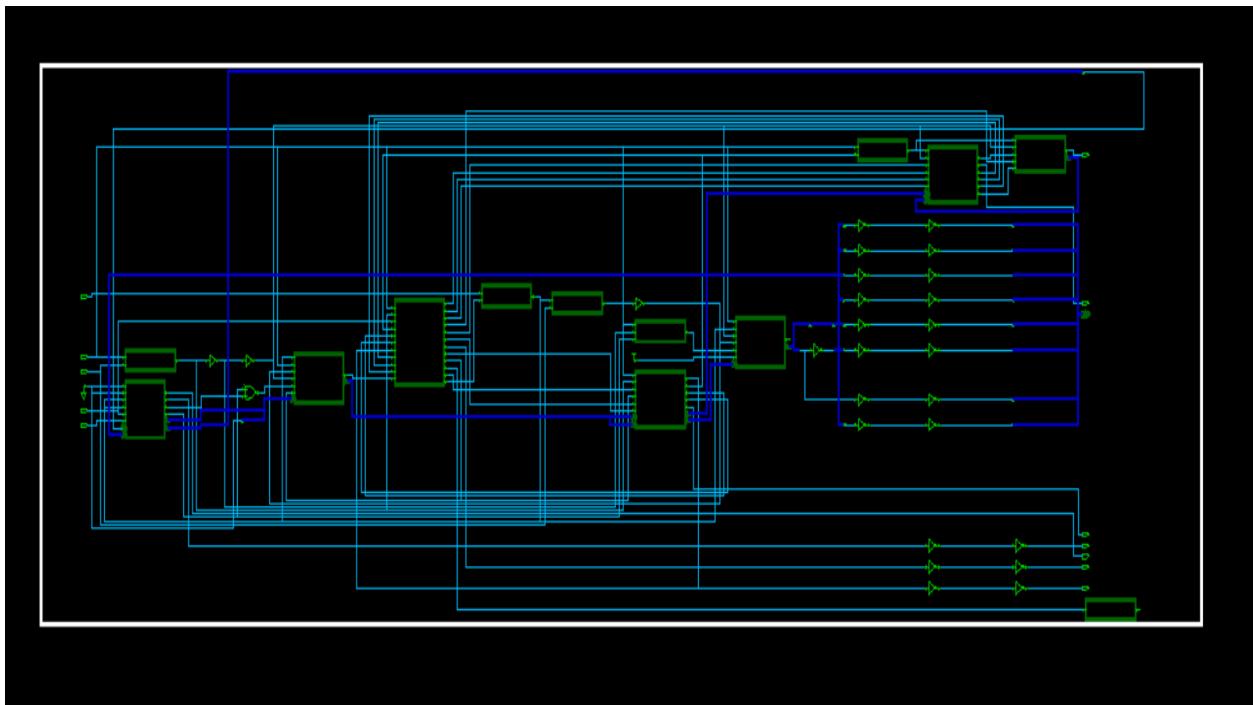


Figure 6:Gate-level netlist schematic

2.2.2-synthesis Optimization

- **Optimization methods:**

```
compile -map_effort medium -area_effort high -power_effort none
```

2.2.3- timing report

Startpoint: u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]		
(rising edge-triggered flip-flop clocked by spi_gated_clk)		
Endpoint: u_spi_slave/miso_reg_reg[7]		
(Falling edge-triggered flip-flop clocked by spi_gated_clk)		
Path Group: req2reg		
Path Type: max		
Des/Clust/Port	Wire Load Model	Library
dig_tx_system	8000	saedlvt14lvt_base_tt0p8v25c
Point	Incr	Path
clock spi_gated_clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]/CK (SAEDLVT14_FDPRBQ_V2_4)	0.00	0.00 r
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]/Q (SAEDLVT14_FDPRBQ_V2_4)	0.03	0.03 f
u_dig_tx_asyn_fifo_write/rptr_h/U3/X (SAEDLVT14_BUF_16)	0.01	0.04 f
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr[0] (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)	0.00	0.04 f
u_dig_tx_asyn_fifo_write/fifom/i_dig_tx_fifo_mem_b_rptr[0] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)	0.00	0.04 f
u_dig_tx_asyn_fifo_write/fifom/U3/X (SAEDLVT14_INV_S_16)	0.00	0.05 r
u_dig_tx_asyn_fifo_write/fifom/U2/X (SAEDLVT14_BUF_20)	0.01	0.06 r
u_dig_tx_asyn_fifo_write/fifom/U17/X (SAEDLVT14_OA22_2)	0.02	0.08 r
u_dig_tx_asyn_fifo_write/fifom/U19/X (SAEDLVT14_OAI21_0P5)	0.05	0.13 f
u_dig_tx_asyn_fifo_write/fifom/o_dig_tx_fifo_mem_data_out[6] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)	0.00	0.13 f
u_dig_tx_asyn_fifo_write/o_dig_tx_asyn_fifo_data_out[6] (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)	0.00	0.13 f
UB/X (SAEDLVT14_BUF_S_1P5)	0.02	0.15 f
u_spi_slave/i_rf_din[6] (spi_slave)	0.00	0.15 f
u_cni_slave/U94/X (SAEDLVT14_OA2BB2_V1_2)	0.02	0.17 r
u_spi_slave/miso_reg_reg[7]/D (SAEDLVT14_FDNRBSBQ_V2_1)	0.01	0.19 f

u_dig_tx_asyn_fifo_write/rptr_h/U3/X (SAEDLVT14_BUF_16)	0.01	0.04 f
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr[0] (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)	0.00	0.04 f
u_dig_tx_asyn_fifo_write/fifom/i_dig_tx_fifo_mem_b_rptr[0] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)	0.00	0.04 f
u_dig_tx_asyn_fifo_write/fifom/U3/X (SAEDLVT14_INV_S_16)	0.00	0.05 r
u_dig_tx_asyn_fifo_write/fifom/U2/X (SAEDLVT14_BUF_20)	0.01	0.06 r
u_dig_tx_asyn_fifo_write/fifom/U17/X (SAEDLVT14_OA22_2)	0.02	0.08 r
u_dig_tx_asyn_fifo_write/fifom/U19/X (SAEDLVT14_OAI21_0P5)	0.05	0.13 f
u_dig_tx_asyn_fifo_write/fifom/o_dig_tx_fifo_mem_data_out[6] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)	0.00	0.13 f
u_dig_tx_asyn_fifo_write/o_dig_tx_asyn_fifo_data_out[6] (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)	0.00	0.13 f
U8/X (SAEDLVT14_BUF_S_1P5)	0.02	0.15 f
u_spi_slave/i_rf_din[6] (spi_slave)	0.00	0.15 f
u_spi_slave/U94/X (SAEDLVT14_OA2BB2_V1_2)	0.02	0.17 r
u_spi_slave/U105/X (SAEDLVT14_OAI21_V1_4)	0.01	0.19 f
u_spi_slave/miso_reg_reg[7]/D (SAEDLVT14_FDNRBSBQ_V2_1)	0.00	0.19 f
data arrival time		0.19
clock spi_gated_clk (fall edge)	0.50	0.50
clock network delay (ideal)	0.00	0.50
clock uncertainty	-0.30	0.20
u_spi_slave/miso_reg_reg[7]/CK (SAEDLVT14_FDNRBSBQ_V2_1)	0.00	0.20 f
library setup time	-0.01	0.19
data required time		0.19

data required time		0.19
data arrival time		-0.19

slack (MET)		0.00

1

Figure 7:timing report

2.2.4- area report

```

Report : area
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date   : Sun Aug 17 16:19:19 2025
*****Library(s) Used:
saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)
Number of ports:          493
Number of nets:           2290
Number of cells:          1723
Number of combinational cells: 1320
Number of sequential cells: 378
Number of macros/black boxes: 0
Number of buf/inv:         484
Number of references:      23
Combinational area:       509.134799
Buf/Inv area:             168.808799
Noncombinational area:    392.673605
Macro/Black Box area:     0.000000
Net Interconnect area:    1051.595677
Total cell area:          901.808404
Total area:               1953.404081

```

Hierarchical area distribution						
Hierarchical cell	Global cell area			Local cell area		
	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black-boxes	Design
dig_tx_system	901.8084	100.0	17.9376	0.0000	0.0000	dig_tx_system
u_dig_tx_asyn_fifo_read	246.7752	27.4	0.5328	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1
u_dig_tx_asyn_fifo_read/fifom	193.5396	21.5	104.0292	89.5104	0.0000	dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/rptr_h	18.0798	2.0	8.3916	9.6792	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/sync_rptr	8.7912	1.0	0.2664	8.5248	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_1
u_dig_tx_asyn_fifo_read/sync_wptr	8.5248	0.9	0.0000	8.5248	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_0
u_dig_tx_asyn_fifo_read/wptr_h	17.3160	1.9	7.7256	9.5904	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_write	96.5790	10.7	0.5328	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8
u_dig_tx_asyn_fifo_write/fifom	53.1468	5.9	30.7692	22.3776	0.0000	dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/rptr_h	16.5612	1.8	8.7912	7.7700	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/sync_rptr	6.6600	0.7	0.2664	6.3936	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_1
u_dig_tx_asyn_fifo_write/sync_wptr	6.6600	0.7	0.2664	6.3936	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_0
u_dig_tx_asyn_fifo_write/wptr_h	13.0092	1.4	5.5500	7.4592	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2
u_dig_tx_control_unit	29.4816	3.3	22.6884	6.7932	0.0000	dig_tx_control_unit
u_dig_tx_crc	91.2420	10.1	44.5776	42.6684	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56
u_dig_tx_crc/add_57	3.9960	0.4	3.9960	0.0000	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56_DW01_inc_0_DW01_inc_3
u_dig_tx_pow_man_unit	0.2664	0.0	0.2664	0.0000	0.0000	dig_tx_pow_man_unit
u_dig_tx_pulse_delayed	2.1312	0.2	0.0000	2.1312	0.0000	dig_tx_pulse_delayed
u_dig_tx_reg_file	155.1336	17.2	75.7988	79.3428	0.0000	dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32
u_dig_tx_rst_sync_spi	2.5308	0.3	0.3996	2.1312	0.0000	dig_tx_rst_sync_0
u_dig_tx_rst_sync_sys	2.5308	0.3	0.3996	2.1312	0.0000	dig_tx_rst_sync_1
u_dig_tx_serializer	74.1480	8.2	52.8360	21.3120	0.0000	dig_tx_serializer_32_16_24_55557a
u_dig_tx_spi_clock_gating	1.1544	0.1	0.5328	0.6216	0.0000	dig_tx_clock_gating_1
u_dig_tx_sys_clock_gating	1.1544	0.1	0.5328	0.6216	0.0000	dig_tx_clock_gating_0
u_spi_slave	180.7524	20.0	117.5712	58.6968	0.0000	spi_slave
u_spi_slave/r101	4.4844	0.5	4.4844	0.0000	0.0000	spi_slave_DW01_inc_0_DW01_inc_6
Total		509.1348	392.6736	0.0000		

1

Figure 8: area report

2.2.5- power report

```

Report : power
  -hier
  -analysis_effort low
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date  : Sun Aug 17 16:19:24 2025
*****



Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)

Operating Conditions: tt0p8v25c Library: saed14lvt_base_tt0p8v25c
Wire Load Model Mode: top

Design      Wire Load Model      Library
-----
dig_tx_system          8000      saed14lvt_base_tt0p8v25c

Global Operating Voltage = 0.8
Power-specific unit information :
  Voltage Units = IV
  Capacitance Units = 1.000000pf
  Time Units = ns
  Dynamic Power Units = 1mW   (derived from V,C,T units)
  Leakage Power Units = 1pW

-----
Hierarchy           Switch  Int     Leak    Total
                  Power   Power   Power   %
-----  

dig_tx_system       5.836   0.715  3.27e+06  6.554 100.0  

u_dig_tx_pow_man_unit (dig_tx_pow_man_unit)  

    0.000   0.000  1.26e+03  1.25e-06  0.0  

u_dig_tx_crc (dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56)  

    1.27e-02 7.44e-02 3.21e+05  8.75e-02  1.3

```

```

          1.53e-03 1.14e-02 1.51e+05 1.31e-02  0.2
u_dig_tx_reg_file (dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32)
    2.18e-02   0.138 4.87e+05   0.160   2.4
u_dig_tx_asyn_fifo_write (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
    8.12e-03 9.23e-02 3.93e+05   0.101   1.5
fifom (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
    4.87e-04 4.35e-02 2.47e+05  4.42e-02  0.7
rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)
    1.98e-03 1.34e-02 7.73e+04  1.55e-02  0.2
wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2)
    1.95e-03 1.30e-02 3.54e+04  1.50e-02  0.2
sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_1)
    1.48e-03 1.11e-02 1.53e+04  1.26e-02  0.2
sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_0)
    1.48e-03 1.11e-02 1.53e+04  1.26e-02  0.2
u_dig_tx_pulse_delayed (dig_tx_pulse_delayed)
    8.34e-06 3.70e-03 4.69e+03  3.71e-03  0.1
u_dig_tx_asyn_fifo_read (dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1)
    1.19e-02   0.237 7.98e+05   0.250   3.8
fifom (dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3)
    1.44e-03   0.174 6.57e+05   0.176   2.7
rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH3)
    2.79e-03 1.70e-02 5.23e+04  1.98e-02  0.3
wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3)
    1.42e-03 1.68e-02 4.79e+04  1.82e-02  0.3
sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_1)
    2.19e-03 1.49e-02 2.00e+04  1.71e-02  0.3
sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_0)
    1.64e-05 1.48e-02 1.87e+04  1.48e-02  0.2
u_spi_slave (spi_slave)
    1.661    0.107 7.26e+05   1.768   27.0
r10I (spi_slave_DW01_inc_0_DW01_inc_6)
    1.05e-05 4.19e-06 1.21e+04  2.68e-05  0.0
u_dig_tx_RST_SYNC_SYS (dig_tx_RST_SYNC_1)
    3.23e-04 4.92e-03 6.86e+03  5.25e-03  0.1
u_dig_tx_RST_SYNC_SPI (dig_tx_RST_SYNC_0)
    3.23e-04 4.92e-03 6.86e+03  5.25e-03  0.1
u_dig_tx_SPI_CLOCK_GATING (dig_tx_CLOCK_GATING_1)
    3.111 7.66e-04 6.41e+03   3.112   47.5
u_dig_tx_SYS_CLOCK_GATING (dig_tx_CLOCK_GATING_0)
    0.928 2.77e-03 5.87e+03   0.931   14.2
1

```

Figure 9:power report

2.2.6-qor report

```
Timing Path Group 'reg2reg'
-----
Levels of Logic:          8.00
Critical Path Length:    0.19
Critical Path Slack:     0.00
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0.00
Worst Hold Violation:   -0.12
Total Hold Violation:   -21.64
No. of Hold Violations: 339.00
-----

Cell Count
-----
Hierarchical Cell Count: 25
Hierarchical Port Count: 473
Leaf Cell Count: 1698
Buf/Inv Cell Count: 484
Buf Cell Count: 152
Inv Cell Count: 359
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 1320
Sequential Cell Count: 378
Macro Count: 0
-----

Area
-----
Combinational Area: 509.134799
Noncombinational Area: 392.673605
Buf/Inv Area: 168.808799
Total Buffer Area: 82.14
Total Inverter Area: 120.28
Macro/Black Box Area: 0.000000
Net Area: 1051.595677
-----
Cell Area: 901.808404
Design Area: 1953.404081
```

```
Design Rules
-----
Total Number of Nets: 1830
Nets With Violations: 15
Max Trans Violations: 15
Max Cap Violations: 15
-----

Hostname: academysvr02

Compile CPU Statistics
-----
Resource Sharing: 1.14
Logic Optimization: 8.07
Mapping Optimization: 14.81
-----
Overall Compile Time: 43.07
Overall Compile Wall Clock Time: 45.17
-----

Design WNS: 6.52 TNS: 85.04 Number of Violating Paths: 15

Design (Hold) WNS: 0.12 TNS: 21.64 Number of Violating Paths: 339
-----

1
```

Figure 10:qor report

2.3-Compile for power

2.3.1- Gate-level netlist schematic

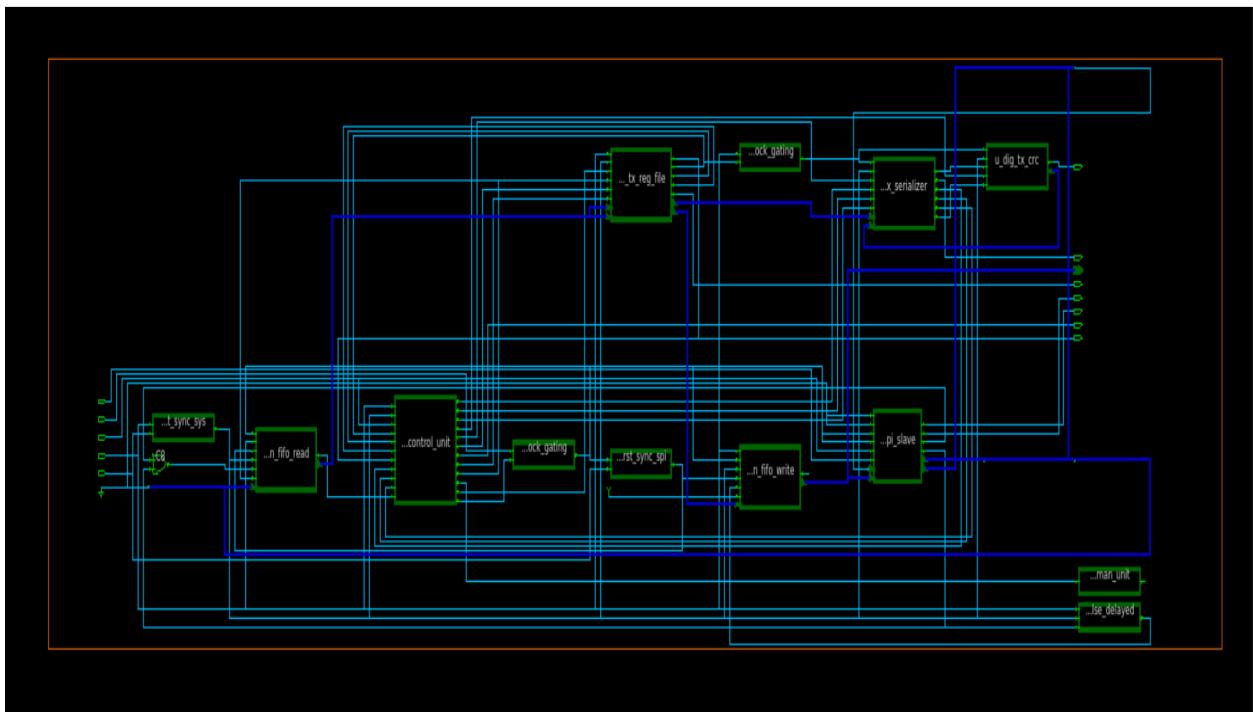


Figure 11:Gate-level netlist schematic

2.3.2-synthesis Optimization

- **Optimization methods used:**

```
compile -exact_map -map_effort high -area_effort medium -power_effort none
```

2.3.3- timing report

dig_tx_system_power_reports.log dig_tx_system_timing_reports.log power_dig_tx_system_qor_reports.log power_dig_tx_system_timing_reports.log

```

Startpoint: u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]
            (rising edge-triggered flip-flop clocked by spi_gated_clk)
Endpoint: u_spi_slave/miso_reg/reg[7]
            (falling edge-triggered flip-flop clocked by spi_gated_clk)
Path Group: reg2reg
Path Type: max

Des/Clust/Port    Wire Load Model      Library
-----          saedlvt14lvt_base_tt6p8v25c

Point           Incr     Path
-----
clock spi_gated_clk (rise edge)      0.00   0.00
clock network delay (ideal)         0.00   0.00
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]/C (SAEDLVT14_FDPRBQ_V2_4)
            0.00   0.00 r
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[0]/Q (SAEDLVT14_FDPRBQ_V2_4)
            0.04   0.04 f
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr[0] (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)
            0.00   0.04 f
u_dig_tx_asyn_fifo_write/fifom/i_dig_tx_fifo_mem_b_rptr[0] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
            0.00   0.04 f
u_dig_tx_asyn_fifo_write/fifom/U42/X (SAEDLVT14_INV_12)
            0.01   0.04 r
u_dig_tx_asyn_fifo_write/fifom/U15/X (SAEDLVT14_BUF_20)
            0.01   0.06 r
u_dig_tx_asyn_fifo_write/fifom/U7/X (SAEDLVT14_INV_S_16)
            0.00   0.06 f
u_dig_tx_asyn_fifo_write/fifom/U14/X (SAEDLVT14_INV_S_20)
            0.00   0.06 r
u_dig_tx_asyn_fifo_write/fifom/U44/X (SAEDLVT14_OA22_2)
            0.02   0.08 r
u_dig_tx_asyn_fifo_write/fifom/U20/X (SAEDLVT14_OA121_OP5)
            0.05   0.13 f
u_dig_tx_asyn_fifo_write/fifom/o_dig_tx_fifo_mem_data_out[6] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
            0.00   0.13 f
u_dig_tx_asyn_fifo_write/o_dig_tx_asyn_fifo_data_out[6] (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
            0.00   0.13 f
u_spi_slave/i_rf_din[6] (spi_slave)
            0.00   0.13 f
u_spi_slave/U62/X (SAEDLVT14_OA2BB2_V1_1)
            0.04   0.17 r
u_spi_slave/U65/X (SAEDLVT14_OA121_V1_4)
            0.01   0.19 f
u_spi_slave/miso_reg/reg[7]/D (SAEDLVT14_FDNRBSBQ_V2_1)
            0.00   0.19 f
data arrival time
            0.00   0.19
clock spi_gated_clk (fall edge)      0.50   0.50
clock network delay (ideal)         0.00   0.50
clock uncertainty                  -0.30   0.20
u_spi_slave/miso_reg/reg[7]/CK (SAEDLVT14_FDNRBSBQ_V2_1)
            0.00   0.20 f
library setup time                 -0.01   0.19
data required time                  0.19   0.19
data arrival time                  -0.19   0.19
-----
slack (MET)                         0.00   0.00

```

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```

u_dig_tx_asyn_fifo_write/fifom/i_dig_tx_fifo_mem_b_rptr[0] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
            0.00   0.04 f
u_dig_tx_asyn_fifo_write/fifom/U42/X (SAEDLVT14_INV_12)
            0.00   0.04 f
u_dig_tx_asyn_fifo_write/fifom/U15/X (SAEDLVT14_BUF_20)
            0.01   0.04 r
u_dig_tx_asyn_fifo_write/fifom/U7/X (SAEDLVT14_INV_S_16)
            0.01   0.06 r
u_dig_tx_asyn_fifo_write/fifom/U14/X (SAEDLVT14_INV_S_20)
            0.00   0.06 f
u_dig_tx_asyn_fifo_write/fifom/U44/X (SAEDLVT14_OA22_2)
            0.00   0.06 r
u_dig_tx_asyn_fifo_write/fifom/U20/X (SAEDLVT14_OA121_OP5)
            0.02   0.08 r
u_dig_tx_asyn_fifo_write/fifom/o_dig_tx_fifo_mem_data_out[6] (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
            0.05   0.13 f
u_dig_tx_asyn_fifo_write/fifom/o_dig_tx_asyn_fifo_data_out[6] (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
            0.00   0.13 f
u_dig_tx_asyn_fifo_write/o_dig_tx_asyn_fifo_data_out[6] (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
            0.00   0.13 f
u_spi_slave/i_rf_din[6] (spi_slave)
            0.00   0.13 f
u_spi_slave/U62/X (SAEDLVT14_OA2BB2_V1_1)
            0.04   0.17 r
u_spi_slave/U65/X (SAEDLVT14_OA121_V1_4)
            0.01   0.19 f
u_spi_slave/miso_reg/reg[7]/D (SAEDLVT14_FDNRBSBQ_V2_1)
            0.00   0.19 f
data arrival time
            0.00   0.19
clock spi_gated_clk (fall edge)      0.50   0.50
clock network delay (ideal)         0.00   0.50
clock uncertainty                  -0.30   0.20
u_spi_slave/miso_reg/reg[7]/CK (SAEDLVT14_FDNRBSBQ_V2_1)
            0.00   0.20 f
library setup time                 -0.01   0.19
data required time                  0.19   0.19
data arrival time                  -0.19   0.19
-----
slack (MET)                         0.00   0.00

```

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Figure 12:timing report

2.3.4- area report

```
*****
Report : area
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date  : Sun Aug 17 16:20:16 2025
*****



Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)

Number of ports:          493
Number of nets:           2347
Number of cells:          1889
Number of combinational cells: 1486
Number of sequential cells: 378
Number of macros/black boxes: 0
Number of buf/inv:         679
Number of references:      20

Combinational area:      1075.456800
Buf/Inv area:             462.426000
Noncombinational area:   400.132804
Macro/Black Box area:    0.000000
Net Interconnect area:  1061.713910

Total cell area:          1475.589604
Total area:               2537.303513
*****
```

Hierarchical area distribution						
Hierarchical cell	Global cell area			Local cell area		
	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black-boxes	Design
dig_tx_system	1475.5896	100.0	18.8700	0.0000	0.0000	dig_tx_system
u_dig_tx_asyn_fifo_read	413.5860	28.0	2.5752	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1
u_dig_tx_asyn_fifo_read/fifom	338.1584	22.9	248.6400	89.5104	0.0000	dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/rptr_h	27.0840	1.8	17.4492	9.6348	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/sync_rptr	10.3452	0.7	1.2876	9.0576	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_1
u_dig_tx_asyn_fifo_read/sync_wptr	10.3452	0.7	1.2876	9.0576	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_0
u_dig_tx_asyn_fifo_read/wptr_h	25.0860	1.7	15.4956	9.5904	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_write	138.4392	9.4	2.5752	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8
u_dig_tx_asyn_fifo_write/fifom	83.7384	5.7	61.3608	22.3776	0.0000	dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/rptr_h	19.0920	1.3	11.3220	7.7700	0.0000	dig_tx_re_ptr_handler_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/sync_rptr	8.0000	0.5	1.2876	6.7932	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_1
u_dig_tx_asyn_fifo_write/sync_wptr	8.0000	0.5	1.2876	6.7932	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_0
u_dig_tx_asyn_fifo_write/wptr_h	16.8720	1.1	9.4128	7.4592	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2
u_dig_tx_control_unit	40.3596	2.7	33.8328	6.5268	0.0000	dig_tx_control_unit
u_dig_tx_crc	140.1780	9.5	92.2188	42.6248	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56
u_dig_tx_crc/add_57	5.3280	0.4	5.3280	0.0000	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56_DW01_inc_0_DW01_inc_3
u_dig_tx_pow_man_unit	1.2876	0.1	1.2876	0.0000	0.0000	dig_tx_pow_man_unit
u_dig_tx_pulse_delayed	2.2644	0.2	0.0000	2.2644	0.0000	dig_tx_pulse_delayed
u_dig_tx_req_file	282.2064	19.1	203.1300	79.0764	0.0000	dig_tx_req_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32
u_dig_tx_rst_sync_spi	2.6640	0.2	0.3996	2.2644	0.0000	dig_tx_rst_sync_0
u_dig_tx_rst_sync_sys	2.6640	0.2	0.3996	2.2644	0.0000	dig_tx_rst_sync_1
u_dig_tx_serializer	119.3472	8.1	98.0352	21.3120	0.0000	dig_tx_serializer_32_16_24_55557a
u_dig_tx_spi_clock_gating	1.5096	0.1	0.5328	0.9768	0.0000	dig_tx_clock_gating_1
u_dig_tx_sys_clock_gating	1.1544	0.1	0.5328	0.6216	0.0000	dig_tx_clock_gating_0
u_spi_slave	311.0664	21.1	240.8256	64.1580	0.0000	spi_slave
u_spi_slave/r101	6.0828	0.4	6.0828	0.0000	0.0000	spi_slave_DW01_inc_0_DW01_inc_6
Total	1075.4568	400.1328	0.0000			
1						

Figure 13: area report

2.3.5- power report

```

Report : power
-hier
-analysis_effort low
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date   : Sun Aug 17 16:26:21 2025
*****



Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)

Operating Conditions: tt0p8v25c Library: saed14lvt_base_tt0p8v25c
Wire Load Model: top

Design      Wire Load Model          Library
-----      -----      -----
dig_tx_system     8000      saed14lvt_base_tt0p8v25c

Global Operating Voltage = 0.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW (derived from V,C,T units)
    Leakage Power Units = 1pw

-----      Switch      Int      Leak      Total      -
Hierarchy      Power      Power      Power      Power      %
-----      -----
dig_tx_system      5.840      0.757 8.71e+06      6.606 100.0
u_dig_tx_pow_man_unit (dig_tx_pow_man_unit)
    0.000      0.000 1.71e+04 1.71e-05      0.0
u_dig_tx_crc (dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56)
    1.23e-02 7.97e-02 7.67e+05 9.27e-02      1.4
add_57 (dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56 DW01_inc_0 DW01_inc_3)

```

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```

1.57e-05 1.10e-02 2.54e+03 1.52e-02 0.2
u_dig_tx_reg_file (dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32)
    2.29e-02      0.147 1.78e+06      0.172      2.6
u_dig_tx_asyn_fifo_write (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
    7.60e-03 9.57e-02 7.92e+05      0.104      1.6
fifo (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
    4.83e-04 4.35e-02 5.11e+05 4.45e-02      0.7
rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)
    1.72e-03 1.38e-02 9.75e+04 1.57e-02      0.2
wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2)
    1.73e-03 1.35e-02 7.50e+04 1.53e-02      0.2
sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_1)
    1.32e-03 1.19e-02 3.80e+04 1.32e-02      0.2
sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_0)
    1.32e-03 1.19e-02 3.80e+04 1.32e-02      0.2
u_dig_tx_pulse_delayed (dig_tx_pulse_delayed)
    7.58e-06 3.79e-03 7.20e+03 3.80e-03      0.1
u_dig_tx_asyn_fifo_read (dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1)
    1.22e-02      0.242 2.36e+06      0.257      3.9
fifo (dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3)
    1.59e-03      0.173 1.96e+06      0.177      2.7
rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH3)
    2.82e-03 1.85e-02 1.45e+05 2.14e-02      0.3
wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3)
    2.89e-03 1.83e-02 1.29e+05 2.13e-02      0.3
sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_1)
    1.96e-03 1.56e-02 4.52e+04 1.77e-02      0.3
sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_0)
    1.96e-03 1.57e-02 4.52e+04 1.77e-02      0.3
u_spi_slave (spi_slave)
    r101 (spi_slave_DW01_inc_0_DW01_inc_6)
        1.674      0.121 1.99e+06      1.797      27.2
        1.39e-05 6.97e-06 2.74e+04 4.82e-05      0.0
u_dig_tx_RST_SYNC_SYS (dig_tx_RST_SYNC_1)
    3.95e-04 5.16e-03 9.28e+03 5.57e-03      0.1
u_dig_tx_RST_SYNC_SPI (dig_tx_RST_SYNC_0)
    3.95e-04 5.16e-03 9.28e+03 5.57e-03      0.1
u_dig_tx_SPI_CLOCK_GATING (dig_tx_CLOCK_GATING_1)
    3.111 7.27e-04 1.00e+04      3.112      47.1
u_dig_tx_SYS_CLOCK_GATING (dig_tx_CLOCK_GATING_0)
    0.928 2.77e-03 5.87e+03      0.931      14.1
1

```

Figure 14:power report

2.3.6- qor report

```
Timing Path Group 'reg2reg'
-----
Levels of Logic:          8.00
Critical Path Length:    0.19
Critical Path Slack:     0.00
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0.00
Worst Hold Violation:   -0.12
Total Hold Violation:   -26.69
No. of Hold Violations: 353.00
-----

Cell Count
-----
Hierarchical Cell Count: 25
Hierarchical Port Count: 473
Leaf Cell Count: 1864
Buf/Inv Cell Count: 679
Buf Cell Count: 179
Inv Cell Count: 500
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 1486
Sequential Cell Count: 378
Macro Count: 0
-----

Area
-----
Combinational Area: 1075.456800
Noncombinational Area: 400.132804
Buf/Inv Area: 462.426000
Total Buffer Area: 205.22
Total Inverter Area: 257.21
Macro/Black Box Area: 0.000000
Net Area: 1061.713910
-----
```

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```
Cell Area:           1475.589604
Design Area:         2537.303513

Design Rules
-----
Total Number of Nets:      1887
Nets With Violations:    15
Max Trans Violations:    15
Max Cap Violations:     15
-----

Hostname: academysvr02

Compile CPU Statistics
-----
Resource Sharing:          0.99
Logic Optimization:        6.65
Mapping Optimization:      7.16
-----
Overall Compile Time:     32.83
Overall Compile Wall Clock Time: 34.12
-----

Design  WNS: 6.25  TNS: 84.81  Number of Violating Paths: 15

Design (Hold)  WNS: 0.12  TNS: 26.69  Number of Violating Paths: 353
-----
```

1

Figure 15:qor report

2.4-Compile for timing

2.4.1- Gate-level netlist schematic

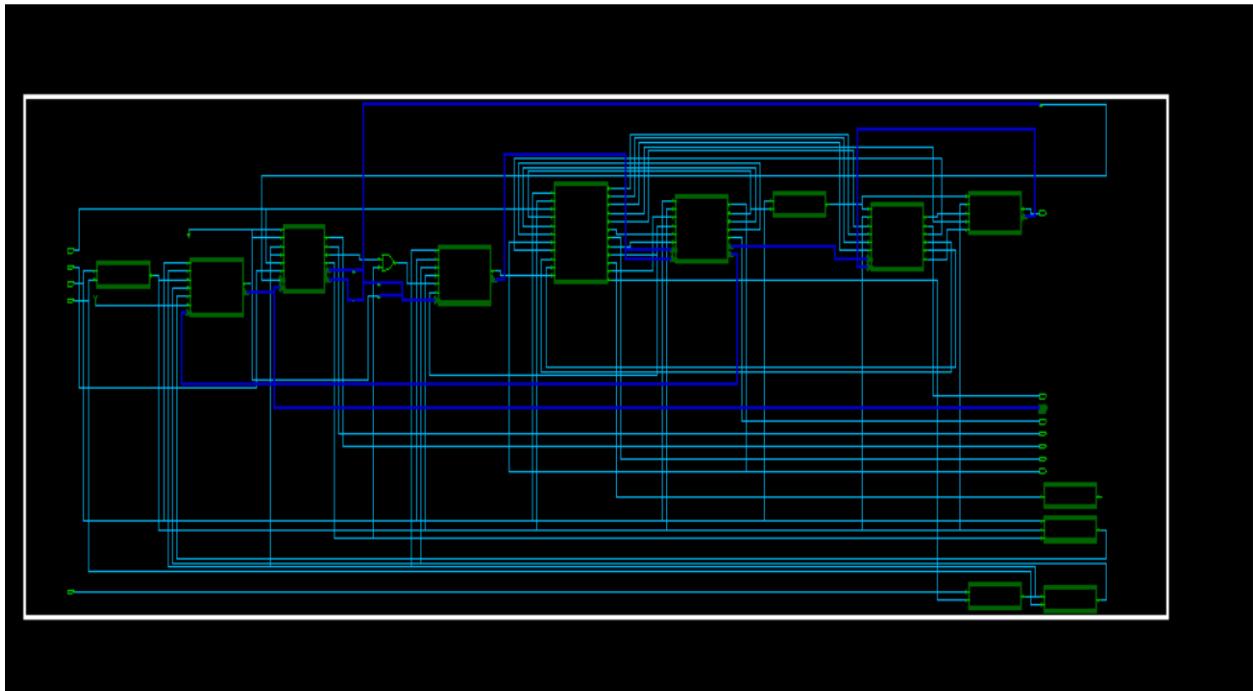


Figure 16:Gate-level netlist schematic

2.4.2-synthesis Optimization

Optimization methods:

```
compile -exact_map -map_effort high -area_effort medium -power_effort none
```

2.4.3- timing report

Path Group: reg2reg			
Path Type: max			
Des/Clust/Port	Wire Load Model	Library	
dig_tx_system	8000	saed14lvt_base_tt0p8v25c	
Point	Incr	Path	
clock spi_gated_clk (fall edge)	0.50	0.50	
clock network delay (ideal)	0.00	0.50	
u_spi_slave/state_tx_reg[2]/CK (SAEDLVT14_FDNRBSBQ_V2_1)	0.00	0.50 f	
u_spi_slave/state_tx_reg[2]/Q (SAEDLVT14_FDNRBSBQ_V2_1)	0.07	0.57 r	
u_spi_slave/U164/X (SAEDLVT14_NR2_MM_0P5)	0.08	0.65 f	
u_spi_slave/U145/X (SAEDLVT14_INV_S_1)	0.05	0.70 r	
u_spi_slave/U24/X (SAEDLVT14_A0221_0P5)	0.12	0.82 r	
u_spi_slave/U99/X (SAEDLVT14_INV_S_8)	0.04	0.86 f	
u_spi_slave/U117/X (SAEDLVT14_BUF_S_1)	0.16	1.02 f	
u_spi_slave/U109/X (SAEDLVT14_ND2_MM_12)	0.02	1.05 r	
u_spi_slave/U166/X (SAEDLVT14_BUF_S_1)	0.07	1.11 r	
u_spi_slave/U246/X (SAEDLVT14_OA2BB2_V1_1)	0.04	1.15 r	
u_spi_slave/U245/X (SAEDLVT14_OAI21_0P5)	0.03	1.18 f	
u_spi_slave/status_reg_reg[2]/D (SAEDLVT14_FDNRBSBQ_V2_1)	0.00	1.18 f	
data arrival time		1.18	
clock spi_gated_clk (fall edge)	1.50	1.50	
clock network delay (ideal)	0.00	1.50	
clock uncertainty	-0.30	1.20	
u_spi_slave/status_reg_reg[2]/CK (SAEDLVT14_FDNRBSBQ_V2_1)	0.00	1.20 f	
library setup time	-0.02	1.18	
data required time		1.18	

data required time		1.18	
data arrival time		-1.18	

slack (MET)	0.00		

Figure 17:timing report

2.4.4- area report

```

Report : area
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date   : Sun Aug 17 16:16:17 2025
*****



Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)

Number of ports:          493
Number of nets:           2313
Number of cells:          1754
Number of combinational cells: 1351
Number of sequential cells: 378
Number of macros/black boxes: 0
Number of buf/inv:         514
Number of references:      20

Combinational area:       511.887598
Buf/Inv area:             178.177198
Noncombinational area:    392.940005
Macro/Black Box area:     0.000000
Net Interconnect area:    1046.152349

Total cell area:          904.827603
Total area:                1950.979952

```

Hierarchical area distribution						
Hierarchical cell	Global cell area			Local cell area		
	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black-boxes	Design
dig_tx_system	904.8276	100.0	15.7620	0.0000	0.0000	dig_tx_system
u_dig_tx_asyn_fifo_read	245.5320	27.1	0.5328	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1
u_dig_tx_asyn_fifo_read/fifom	192.4296	21.3	102.9192	89.5104	0.0000	dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/rptr_h	17.9376	2.0	8.1696	9.7680	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_read/sync_rptr	8.7912	1.0	0.2664	8.5248	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_1
u_dig_tx_asyn_fifo_read/sync_wptr	8.5248	0.9	0.0000	8.5248	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH3_0
u_dig_tx_asyn_fifo_read/wptr_h	17.3160	1.9	7.7256	9.5904	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3
u_dig_tx_asyn_fifo_write	91.5084	10.1	1.1544	0.0000	0.0000	dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH8
u_dig_tx_asyn_fifo_write/fifom	48.3960	5.3	26.0184	22.3776	0.0000	dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/rptr_h	15.6288	1.7	7.8588	7.7700	0.0000	dig_tx_fifo_re_ptr_handler_PTR_WIDTH2
u_dig_tx_asyn_fifo_write/sync_rptr	6.6600	0.7	0.2664	6.3936	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_1
u_dig_tx_asyn_fifo_write/sync_wptr	6.6600	0.7	0.2664	6.3936	0.0000	dig_tx_fifo_synchronizer_PTR_WIDTH2_0
u_dig_tx_asyn_fifo_write/wptr_h	13.0092	1.4	5.5500	7.4592	0.0000	dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2
u_dig_tx_control_unit	32.5008	3.6	25.7076	6.7932	0.0000	dig_tx_control_unit
u_dig_tx_crc	89.2440	9.9	42.6240	42.6240	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56
u_dig_tx_crc/add_57	3.9960	0.4	3.9960	0.0000	0.0000	dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56_DW01_inc_0_DW01_inc_3
u_dig_tx_pow_man_unit	0.2664	0.0	0.2664	0.0000	0.0000	dig_tx_pow_man_unit
u_dig_tx_pulse_delayed	2.1312	0.2	0.0000	2.1312	0.0000	dig_tx_pulse_delayed
u_dig_tx_reg_file	165.7896	18.3	86.3580	79.4316	0.0000	dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32
u_dig_tx_rst_sync_spi	2.5308	0.3	0.3996	2.1312	0.0000	dig_tx_rst_sync_0
u_dig_tx_rst_sync_sys	2.5308	0.3	0.3996	2.1312	0.0000	dig_tx_rst_sync_1
u_dig_tx_serializer	71.2620	7.9	49.9500	21.3120	0.0000	dig_tx_serializer_32_16_24_55557a
u_dig_tx_spi_clock_gating	1.1544	0.1	0.5328	0.6216	0.0000	dig_tx_clock_gating_1
u_dig_tx_sys_clock_gating	1.1544	0.1	0.5328	0.6216	0.0000	dig_tx_clock_gating_0
u_spi_slave	183.4688	20.3	120.1464	58.8300	0.0000	spi_slave
u_spi_slave/r101	4.4844	0.5	4.4844	0.0000	0.0000	spi_slave_DW01_inc_0_DW01_inc_6
Total		511.8876	392.9400	0.0000		
1						

Figure 18: area report

2.4.5- power report

```

Report : power
-hier
-analysis_effort low
Design : dig_tx_system
Version: W-2024.09-SP5-1
Date   : Sun Aug 17 16:16:27 2025
*****  

Library(s) Used:
    saed14lvt_base_tt0p8v25c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db)  

Operating Conditions: tt0p8v25c Library: saed14lvt_base_tt0p8v25c
Wire Load Model Mode: top
  

Design      Wire Load Model      Library
-----  

dig_tx_system      8000      saed14lvt_base_tt0p8v25c  

Global Operating Voltage = 0.8
Power-specific unit information :
    Voltage Units = IV
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW (derived from V,C,T units)
    Leakage Power Units = 1pW  

-----  

Hierarchy          Switch  Int     Leak    Total
                  Power   Power   Power   Power   %
-----  

dig_tx_system      5.837   0.717   3.32e+06   6.557 100.0
    u_dig_tx_pow_man_unit (dig_tx_pow_man_unit)
        0.000   0.000   1.26e+03   1.25e-06   0.0
    u_dig_tx_crc (dig_tx_crc_REGISTER_WIDTH16_INPUT_LENGTH56)
        1.27e-02 7.44e-02   3.03e+05   8.75e-02   1.3

```

```

1.54e-03 1.14e-02 1.74e+05 1.31e-02   0.2
u_dig_tx_reg_file (dig_tx_reg_file_REGISTER_DEPTH5_REGISTER_WIDTH8_PAYLOAD_WIDTH32)
    2.18e-02   0.138   5.40e+05   0.161   2.4
u_dig_tx_asyn_fifo_write (dig_tx_asyn_fifo_FIFO_DEPTH3_REGISTER_WIDTH8)
    8.08e-03 9.22e-02 3.45e+05   0.101   1.5
    fifom (dig_tx_fifo_mem_FIFO_DEPTH3_REGISTER_WIDTH8_PTR_WIDTH2)
        4.72e-04 4.35e-02 2.06e+05 4.41e-02   0.7
    rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH2)
        1.96e-03 1.33e-02 6.44e+04 1.54e-02   0.2
    wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH2)
        1.95e-03 1.30e-02 3.54e+04 1.50e-02   0.2
    sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_1)
        1.48e-03 1.11e-02 1.53e+04 1.26e-02   0.2
    sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH2_0)
        1.48e-03 1.11e-02 1.53e+04 1.26e-02   0.2
u_dig_tx_pulse_delayed (dig_tx_pulse_delayed)
    8.34e-06 3.70e-03 4.69e+03 3.71e-03   0.1
u_dig_tx_asyn_fifo_read (dig_tx_asyn_fifo_FIFO_DEPTH8_REGISTER_WIDTH8_ADDRESS_WIDTH3_VALID_WIDTH1)
    1.19e-02   0.237   8.54e+05   0.250   3.8
    fifom (dig_tx_fifo_mem_FIFO_DEPTH8_REGISTER_WIDTH12_PTR_WIDTH3)
        1.44e-03   0.174   7.12e+05   0.176   2.7
    rptr_h (dig_tx_fifo_re_ptr_handler_PTR_WIDTH3)
        2.88e-03 1.70e-02 5.27e+04 1.98e-02   0.3
    wptr_h (dig_tx_fifo_wr_ptr_handler_PTR_WIDTH3)
        1.42e-03 1.68e-02 4.79e+04 1.82e-02   0.3
    sync_rptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_1)
        2.19e-03 1.49e-02 2.00e+04 1.71e-02   0.3
    sync_wptr (dig_tx_fifo_synchronizer_PTR_WIDTH3_0)
        1.64e-05 1.48e-02 1.87e+04 1.48e-02   0.2
u_spi_slave (spi_slave)
    1.662   0.109   7.42e+05   1.771   27.0
    r101 (spi_slave_DW01_inc_0_DW01_inc_6)
        1.05e-05 4.19e-06 1.21e+04 2.68e-05   0.0
u_dig_tx_RST_SYNC_SYS (dig_tx_RST_SYNC_1)
    3.23e-04 4.92e-03 6.86e+03 5.25e-03   0.1
u_dig_tx_RST_SYNC_SPI (dig_tx_RST_SYNC_0)
    3.23e-04 4.92e-03 6.86e+03 5.25e-03   0.1
u_dig_tx_SPI_CLOCK_GATING (dig_tx_CLOCK_GATING_1)
    3.111 7.66e-04 6.41e+03   3.112   47.5
u_dig_tx_SYS_CLOCK_GATING (dig_tx_CLOCK_GATING_0)
    0.928 2.77e-03 5.87e+03   0.931   14.2
1

```

Plain Text ▾ Tab Width:

Figure 19:power report

2.4.6- qor report

```
Timing Path Group 'reg2reg'
-----
Levels of Logic:          9.00
Critical Path Length:    0.68
Critical Path Slack:     0.00
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0.00
Worst Hold Violation:   -0.12
Total Hold Violation:   -21.00
No. of Hold Violations: 338.00
-----

Cell Count
-----
Hierarchical Cell Count: 25
Hierarchical Port Count: 473
Leaf Cell Count:         1729
Buf/Inv Cell Count:      514
Buf Cell Count:          164
Inv Cell Count:          367
CT Buf/Inv Cell Count:   0
Combinational Cell Count: 1351
Sequential Cell Count:   378
Macro Count:              0
-----

Area
-----
Combinational Area:      511.887598
Noncombinational Area:   392.940005
Buf/Inv Area:            178.177198
Total Buffer Area:       77.30
Total Inverter Area:    126.36
Macro/Black Box Area:   0.000000
Net Area:                1046.152349
-----
Cell Area:               904.827603
Design Area:             1950.979952
```

```
Design Rules
-----
Total Number of Nets:      1853
Nets With Violations:    15
Max Trans Violations:    15
Max Cap Violations:      15
-----

Hostname: academysvr02
Compile CPU Statistics
-----
Resource Sharing:          1.03
Logic Optimization:        6.99
Mapping Optimization:      15.75
-----
Overall Compile Time:     43.49
Overall Compile Wall Clock Time: 61.34
-----

Design  WNS: 6.41  TNS: 85.02  Number of Violating Paths: 15
Design (Hold)  WNS: 0.12  TNS: 21.00  Number of Violating Paths: 338
-----
1
```

Figure 20: qor report

3-synthesis comparison:

	Compile	Compile for area	Compile for power	Compile for time
Total area	1565.8	1950.98	2537.3	1953.5
Total power	.203	6.554	6.606	6.557
setup	unconstrained	0	0	0
hold	unconstrained	-0.12	-0.12	-0.12

Comment:

- **Smallest Area:** 1950.98 (Compile for area): Expected
- **Smallest Power:** 6.554 (Compile for area): Unexpected - should be "Compile for power"
- **Best Timing:**
- **Setup:** 0 (all three are equal)
- **Hold:** -0.12 (all three are equal)
- **Key Insight:** "Compile for area" achieves the best results across both area and power metrics, while all three optimization strategies achieve identical timing constraints. This suggests that area optimization provides the most efficient overall solution when timing requirements are met.

3-Backend Implementation with Timing Constraints

3.1-setup



Figure 21:setup

3.2-floorplanning

- **Create_Floorplan & port placement**

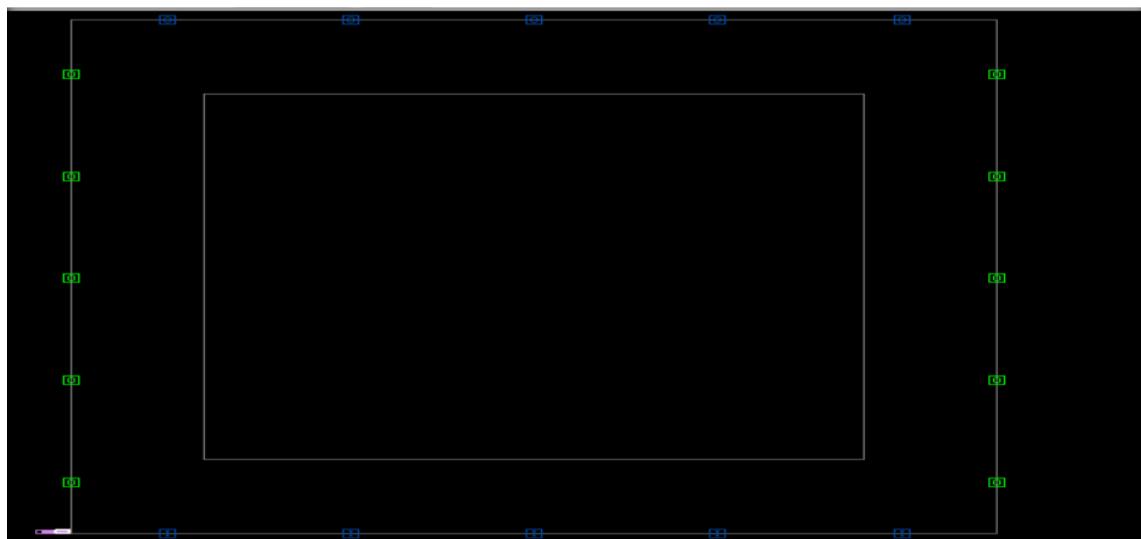


Figure 22:Creating Floorplan

➤ Create_Floorplane_Placement

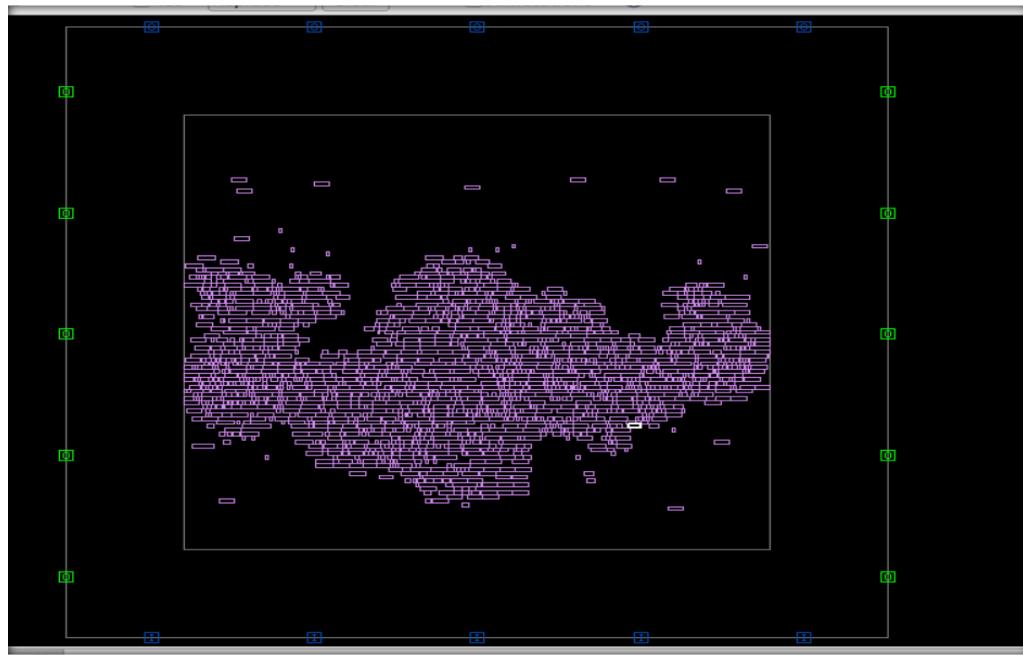


Figure 23:Create_Floorplane_Placement

3.3-powerplanning

➤ Create_STD_Cells_Rail

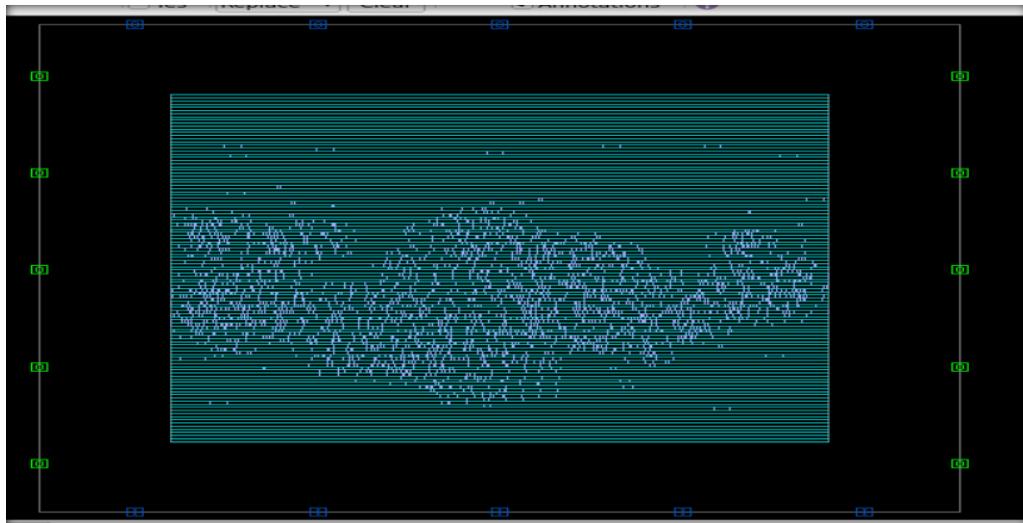


Figure 24:Cells_Rail

➤ Create_middle_Vertical_Mesh

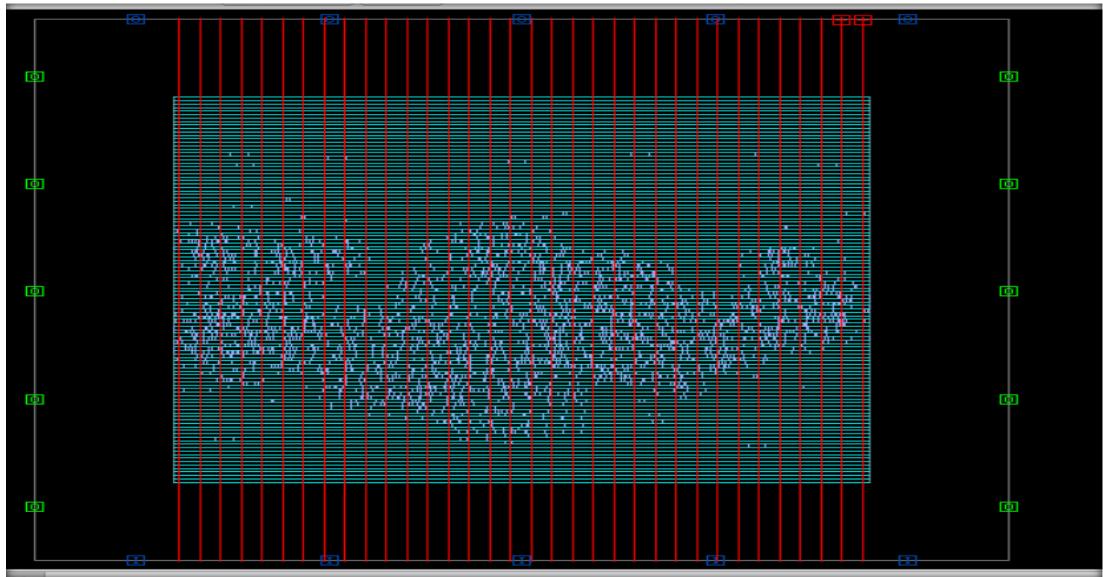


Figure 25:middle_Vertical_Mesh

➤ Create_Top_Horizontal_Mesh

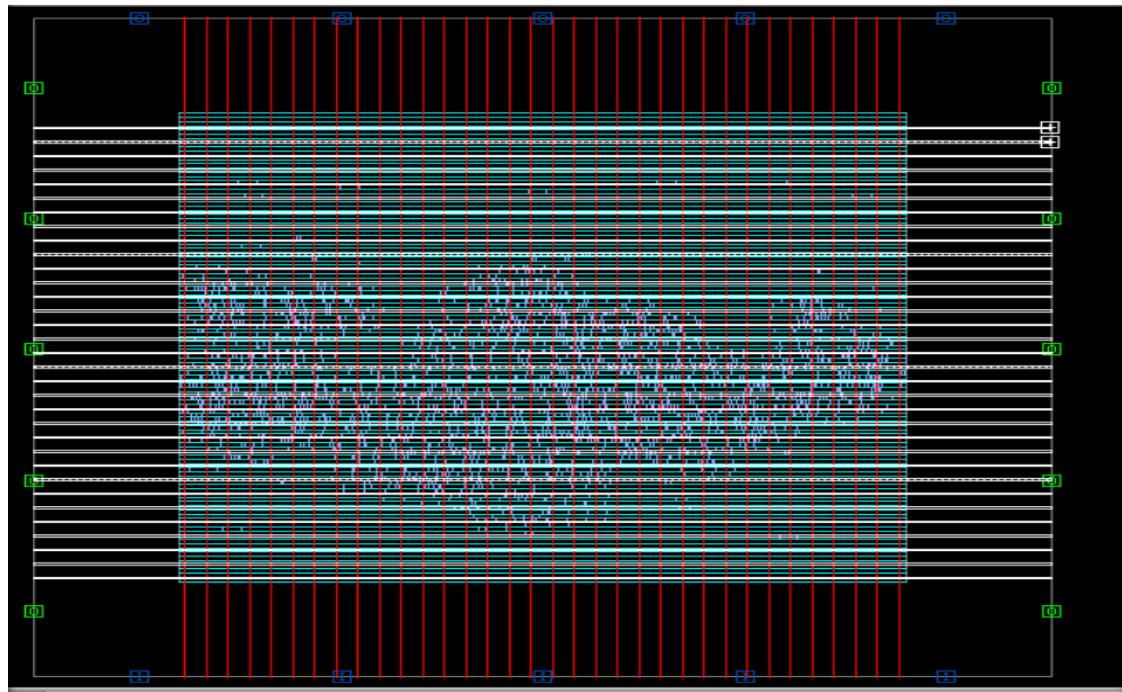


Figure 26:Top_Horizontal_Mesh

➤ Create_Top_Vertical_Mesh

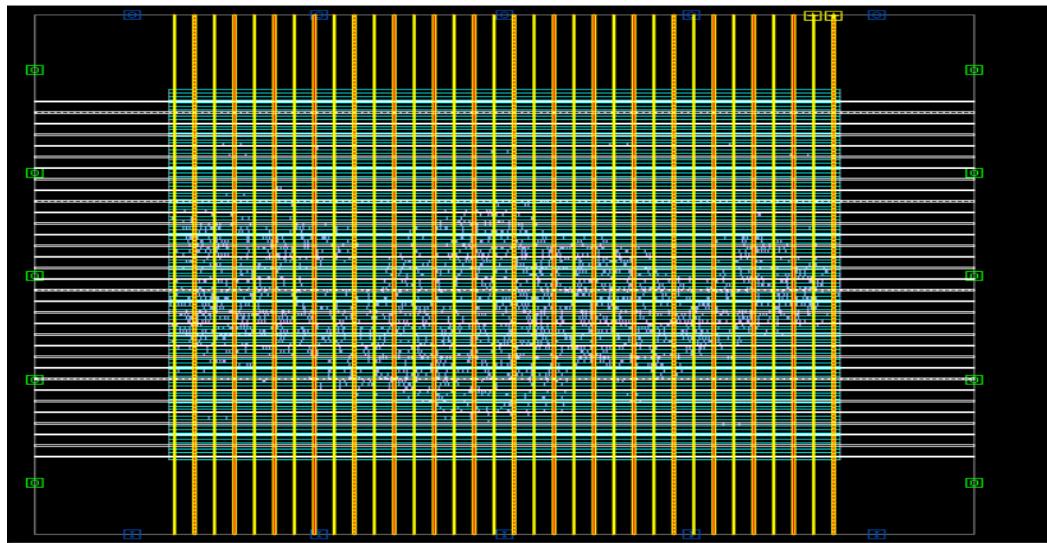


Figure 27:Top_Vertical_Mesh

➤ 3.5-Create_Rectangular_Rings

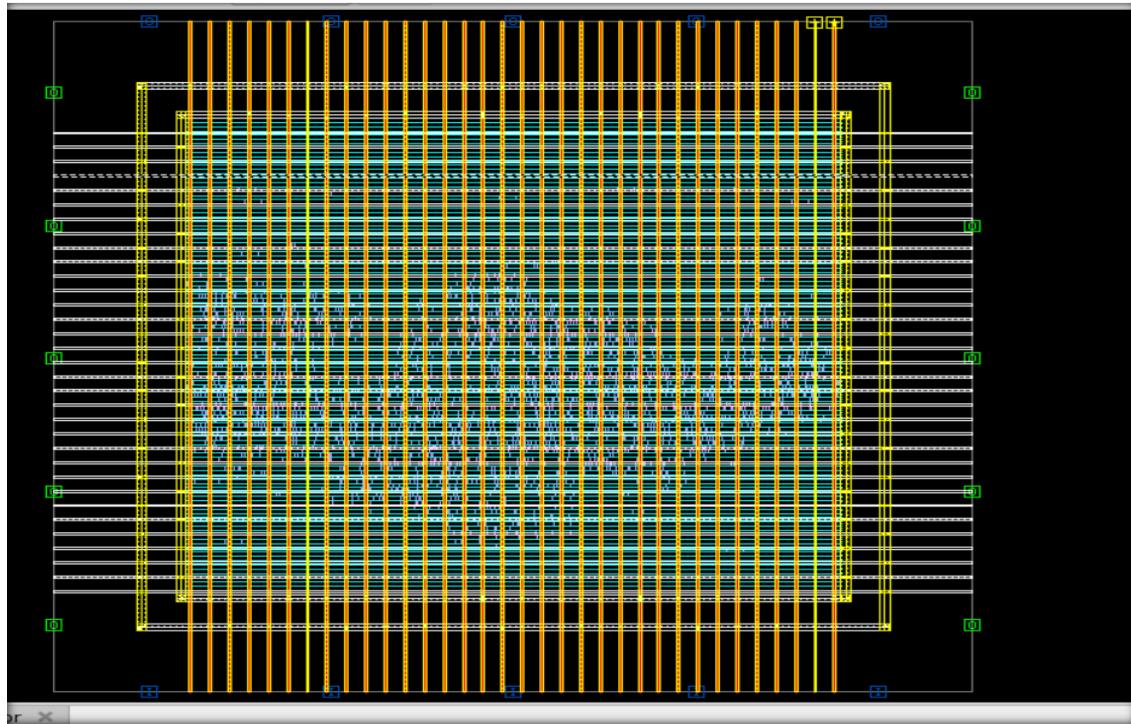


Figure 28:Rectangular_Rings

➤ Congestion

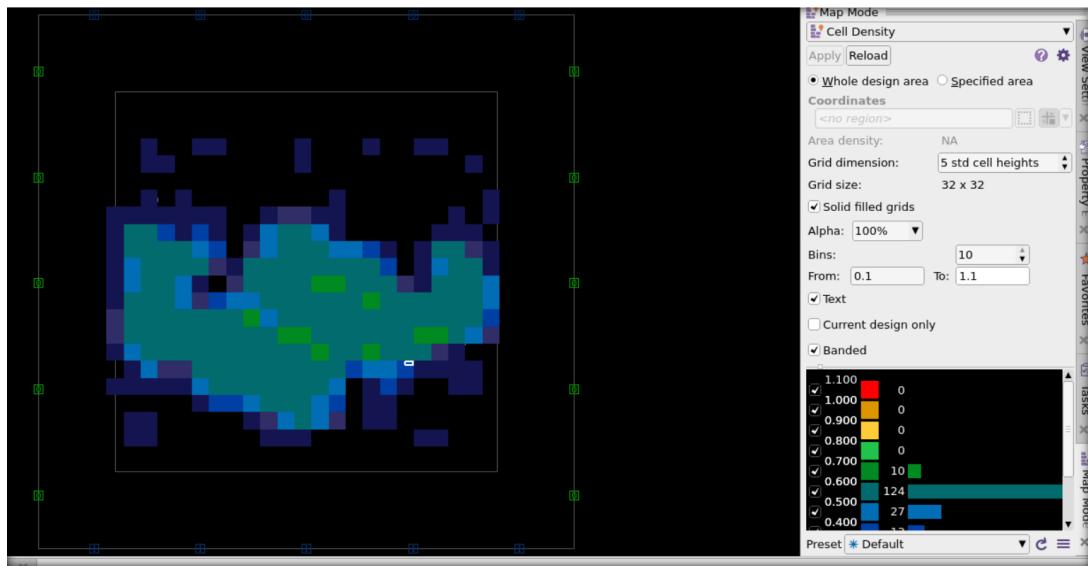


Figure 29:Congestion

3.4-placement

➤ place-opt

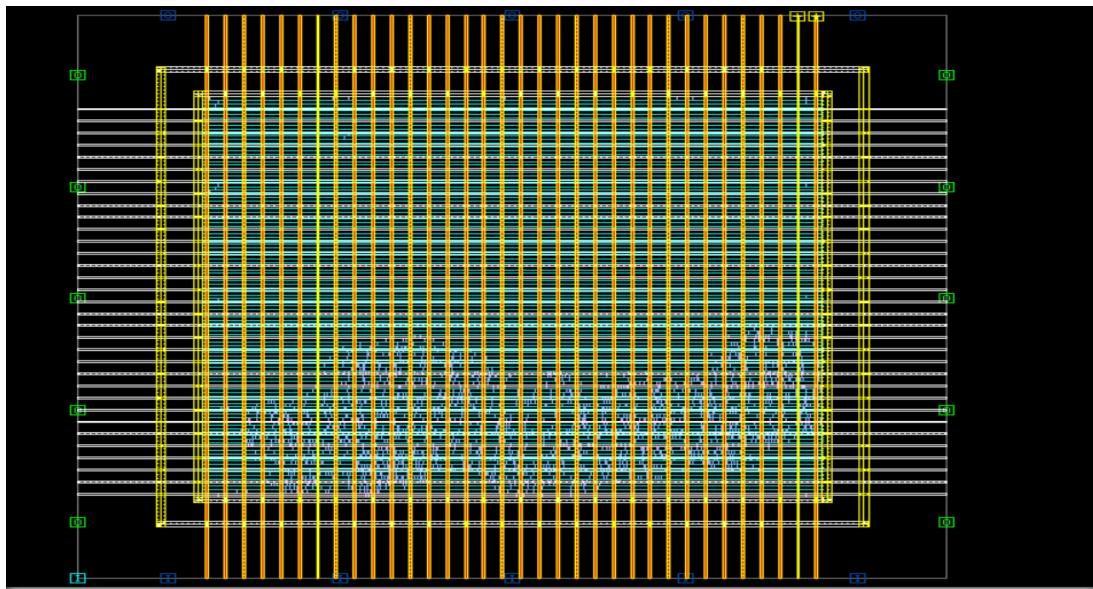


Figure 30:place-opt

➤ legalize placement

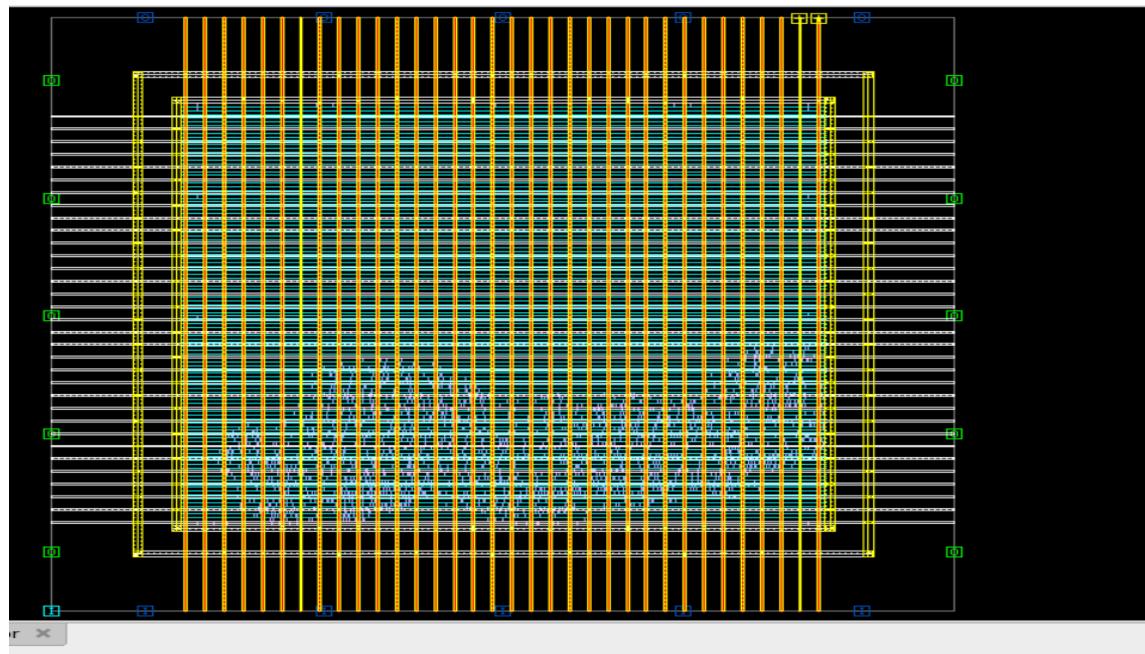


Figure 31:legalize placement

3.5- Clock Tree Synthesis (CTS)

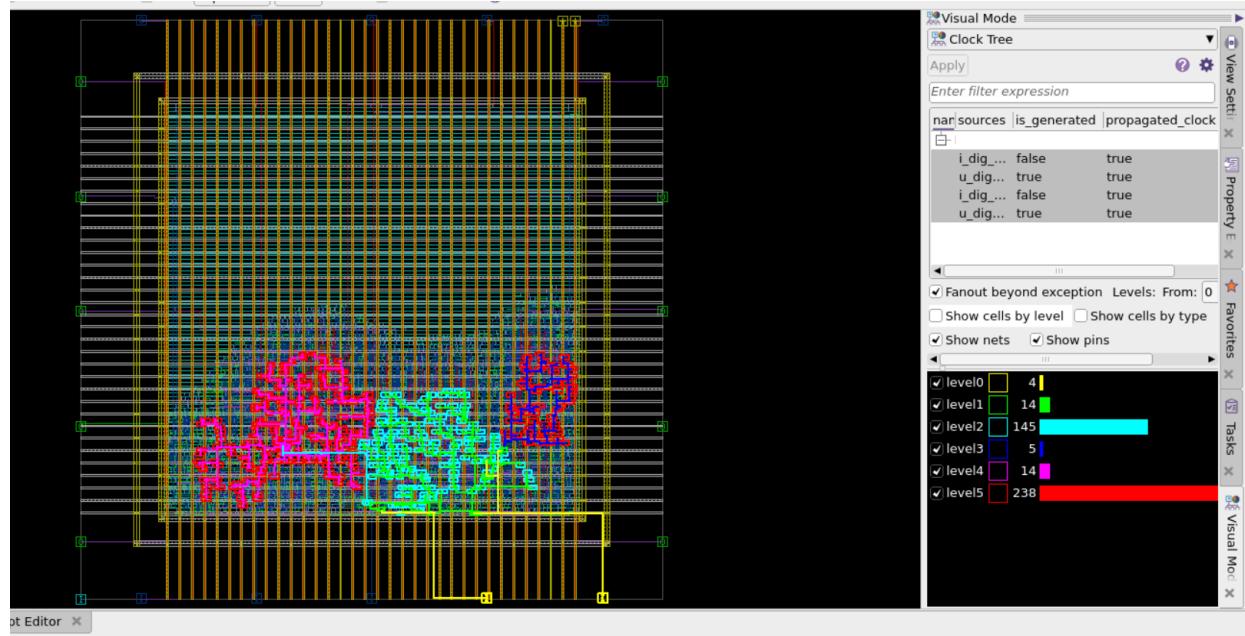


Figure 32:CTS

3.6-route

➤ Route_auto

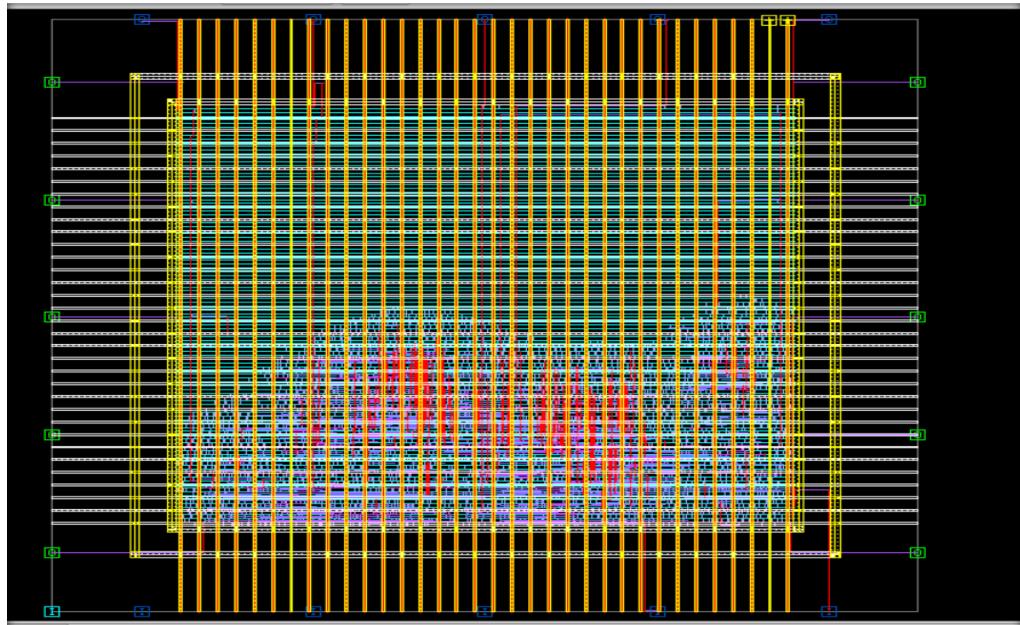


Figure 33:Route_auto

➤ route_opt

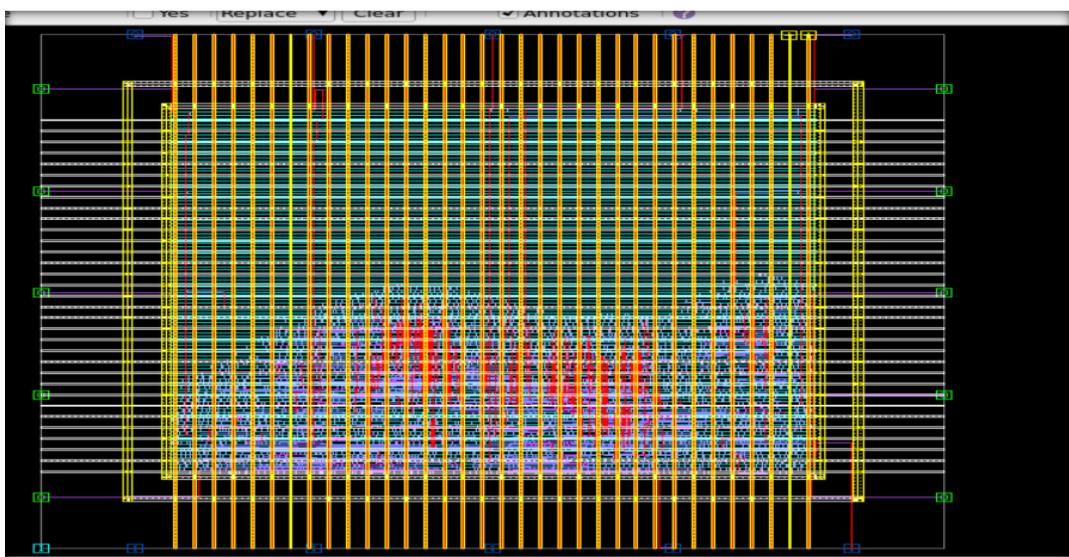


Figure 34:route_opt

3.7-Finshing

➤ Insert_Filler

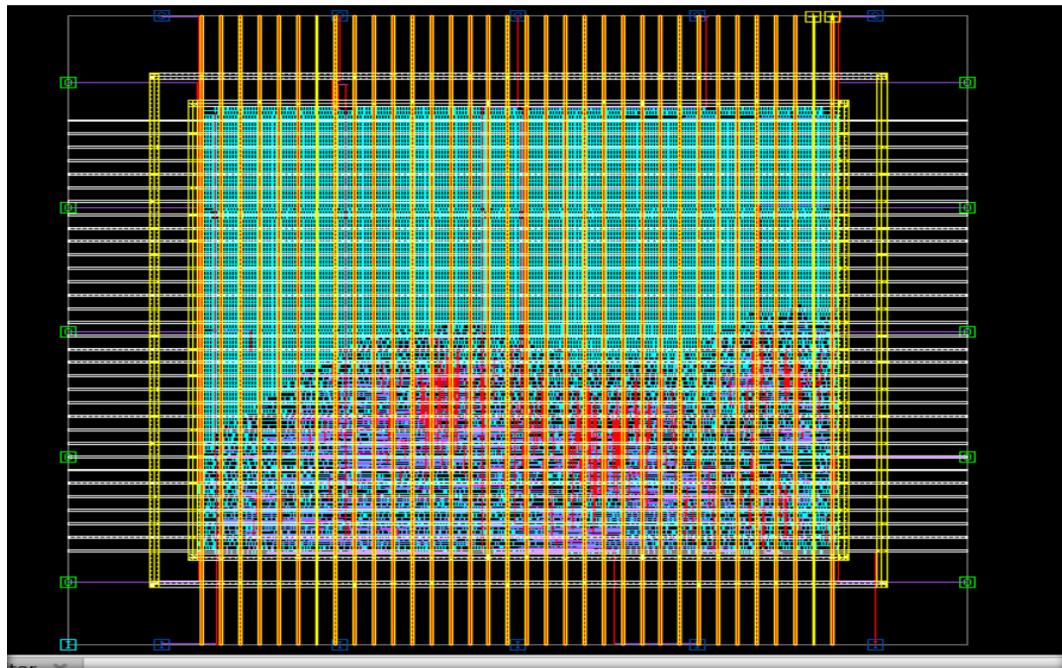


Figure 35:Insert_Filler

4-Backend Implementation with area Constraints

4.1-setup

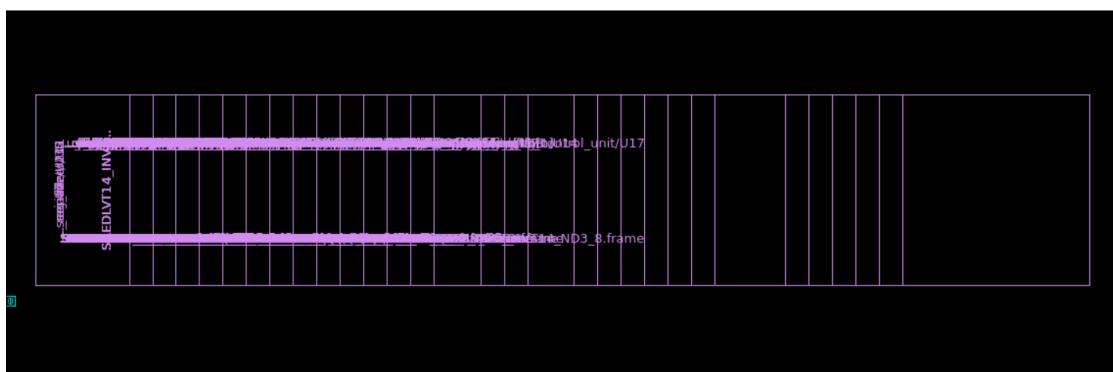


Figure 36:setup

4.2-floorplanning

- **Create_Floorplan & port placement**

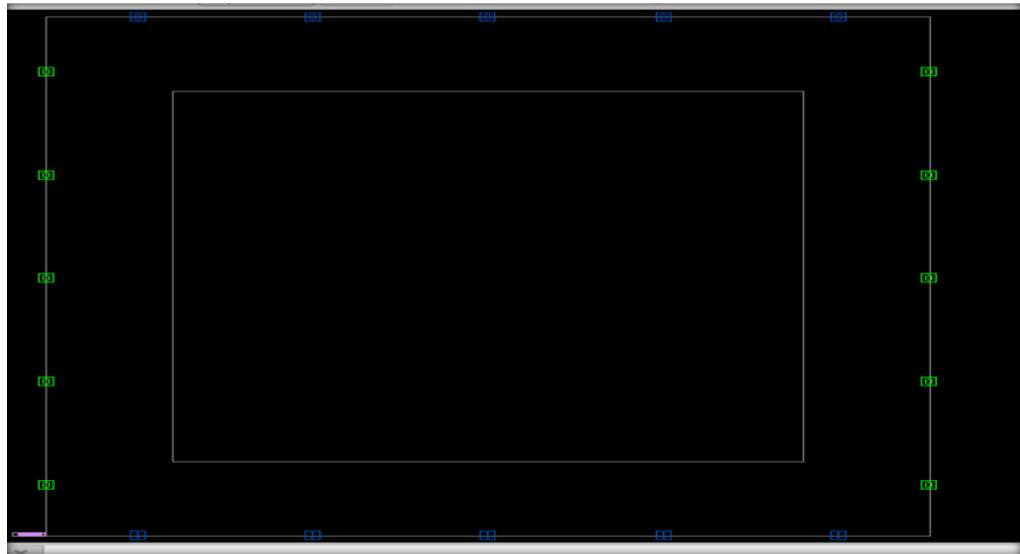


Figure 37:Create Floorplan & port placement

- **Create_Floorplane_Placement**

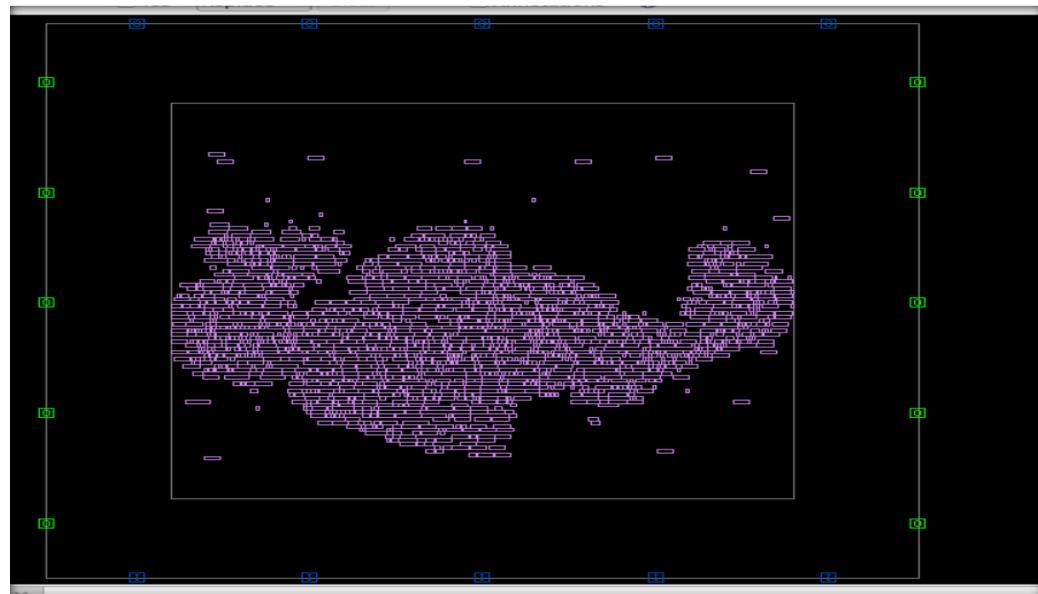


Figure 38:Floorplane_Placement

4.3-powerplanning

➤ Create_STD_Cells_Rail

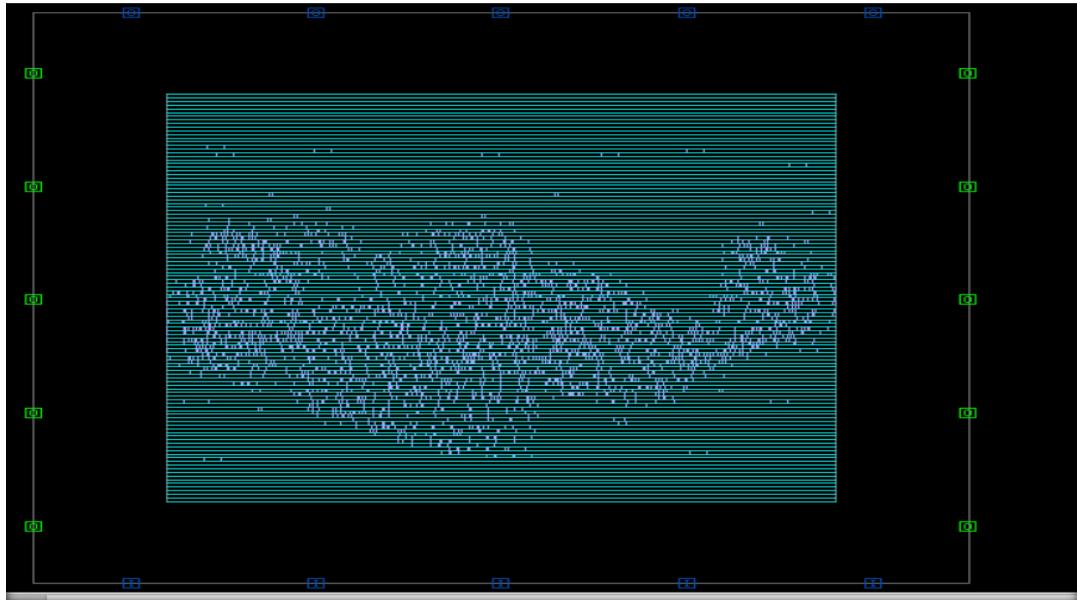


Figure 39:Cells_Rail

➤ Create_middle_Vertical_Mesh

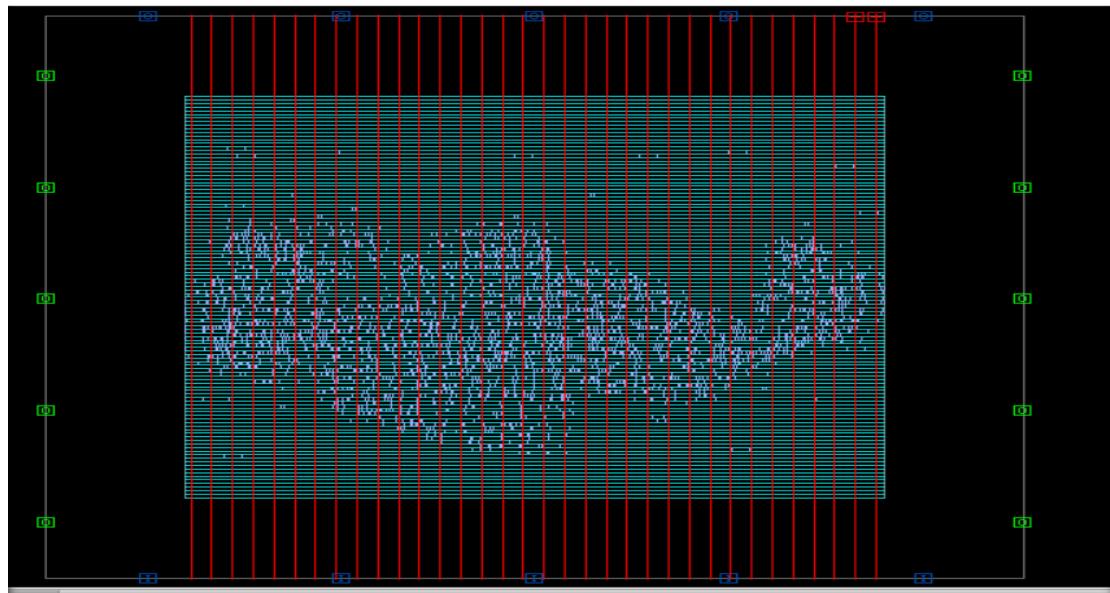


Figure 40:middle_Vertical_Mesh

➤ **Create_Top_Horizontal_Mesh**

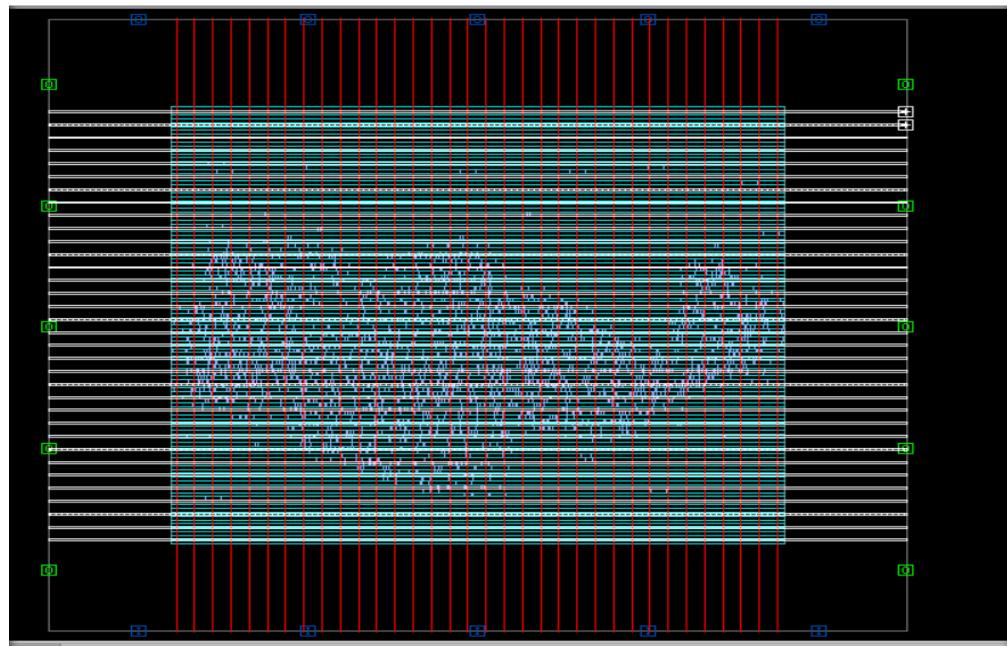


Figure 41:Top_Horizontal_Mesh

➤ **Create_Top_Vertical_Mesh**

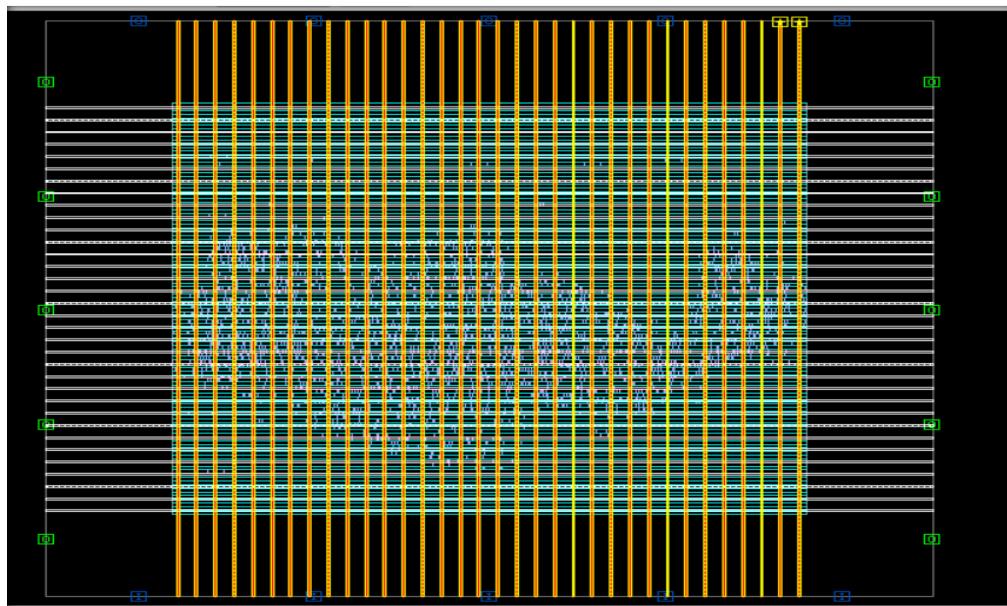


Figure 42:Top_Vertical_Mesh

➤ **Create_Rectangular_Rings**

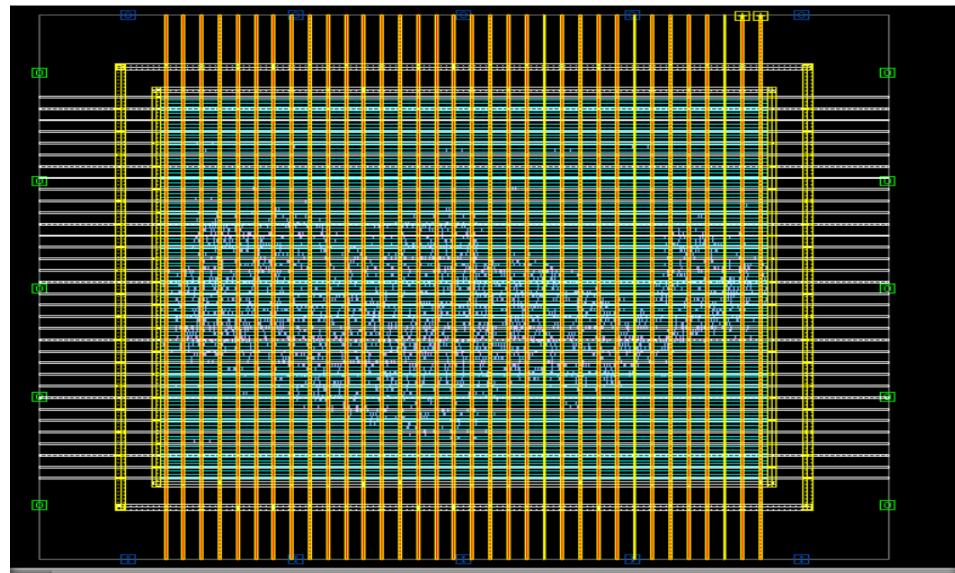


Figure 43:Rectangular_Rings

4.4-placement

➤ **place_opt**

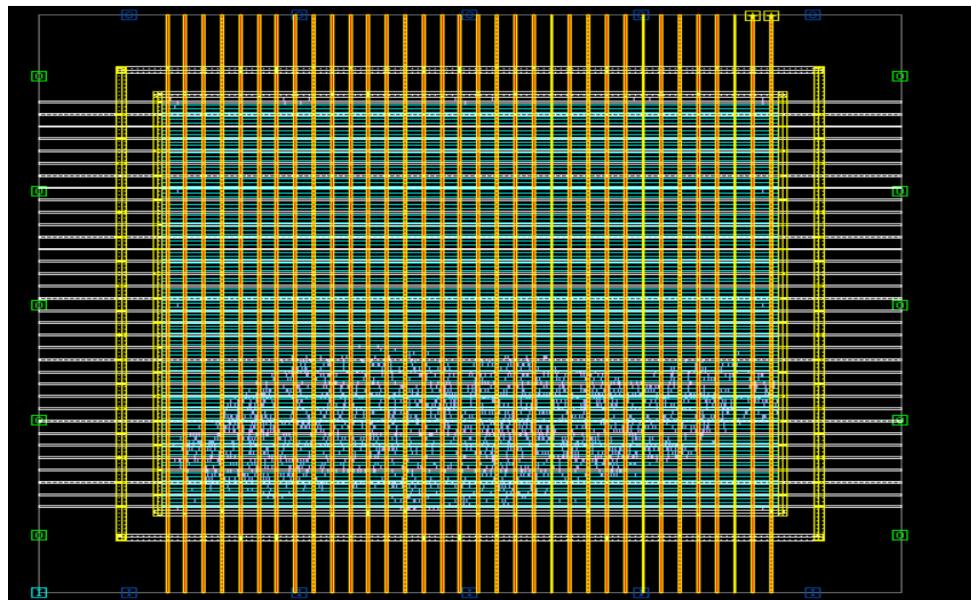


Figure 44:place_opt

➤ **legalize_placement**

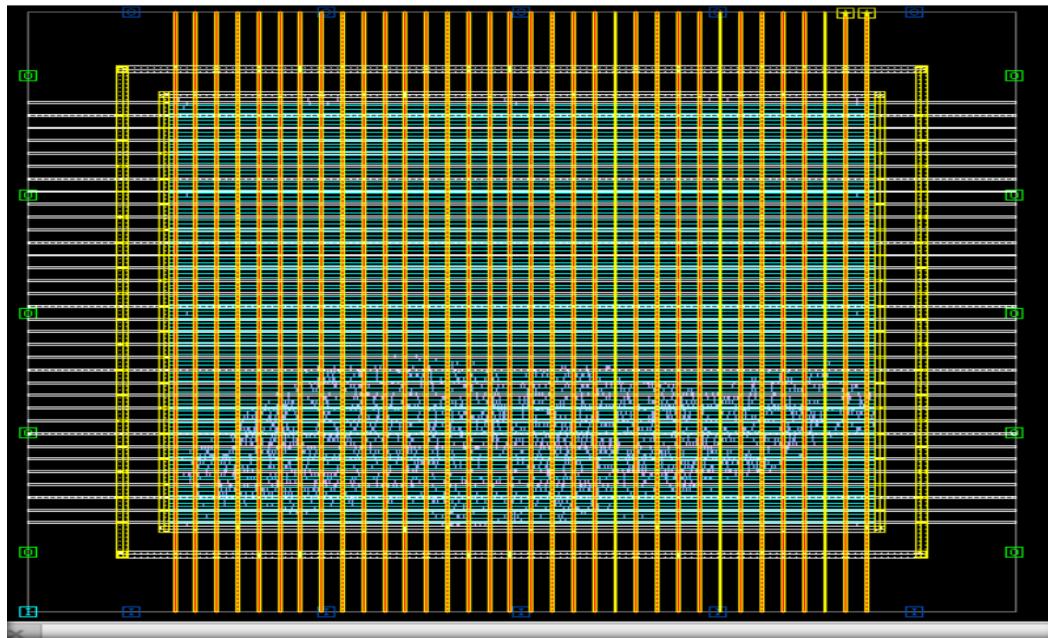


Figure 45:*legalize_placement*

4.5-Clock Tree Synthesis (CTS)

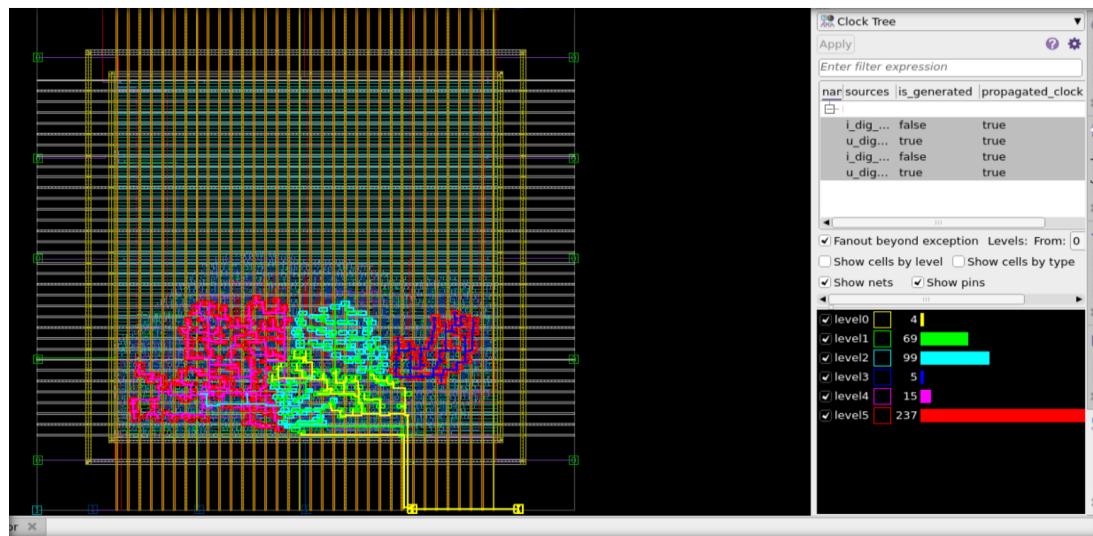


Figure 46:*CTS*

4.6-route

➤ route_auto

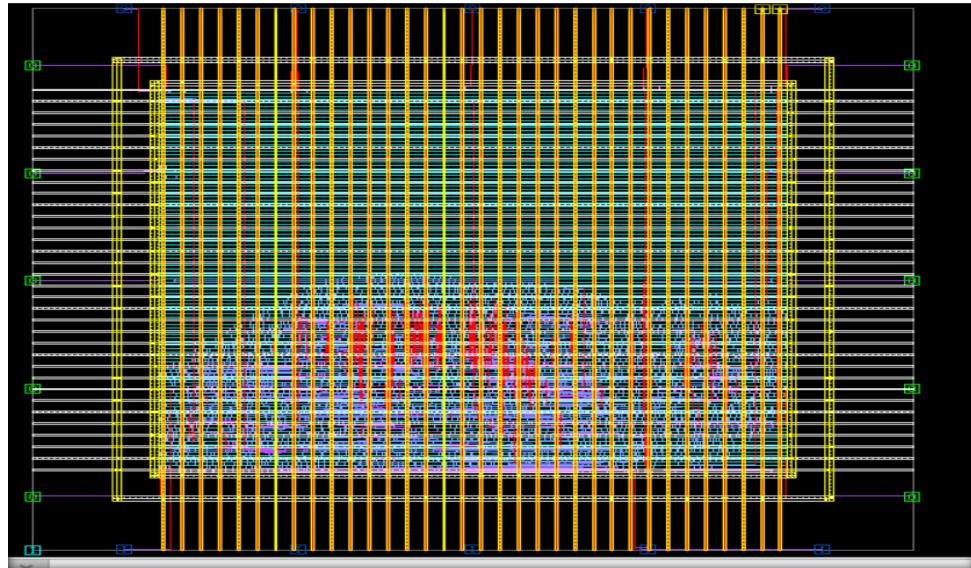


Figure 47:route auto

➤ route_opt

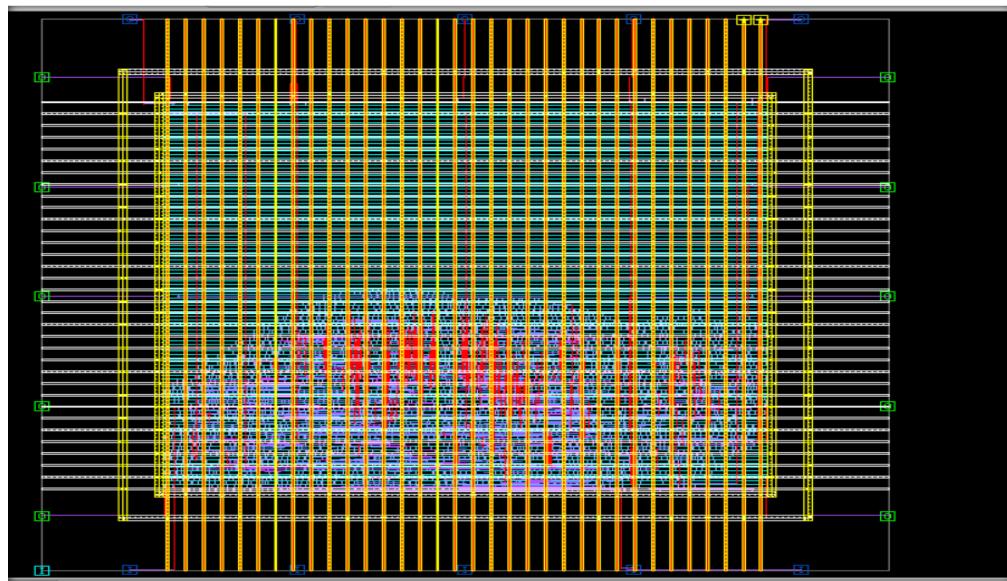


Figure 48:route_opt

4.7-finishing

➤ **insert filler**

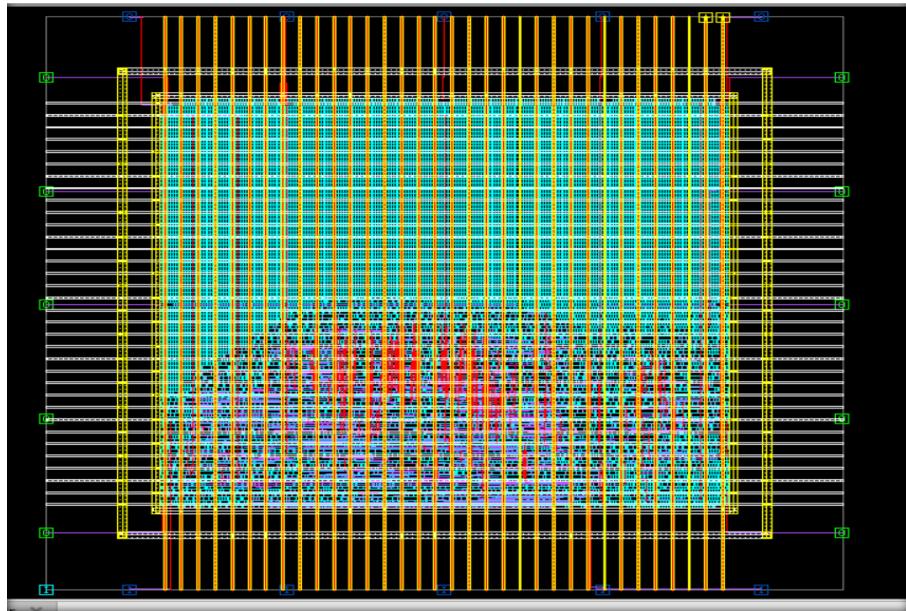


Figure 49:insert filler

5-Backend Implementation with power Constraints

5.1-setup

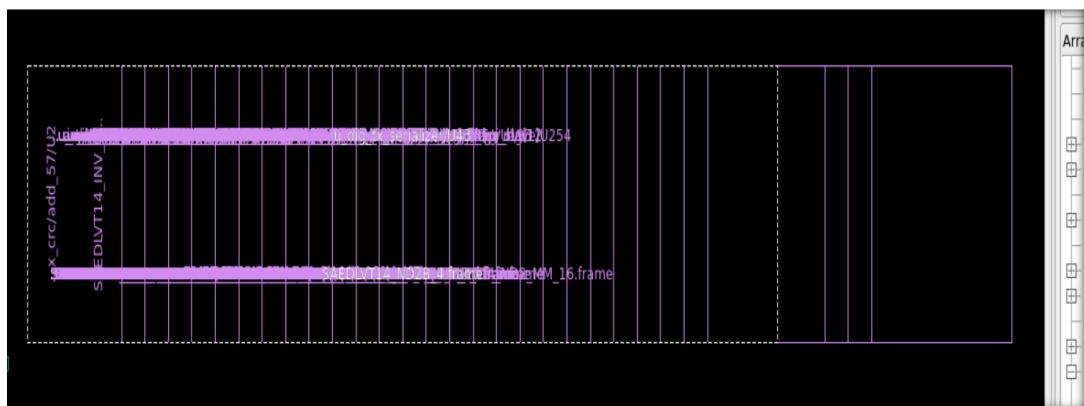


Figure 50:setup

5.2-floorplanning

- **Create_Floorplan & port placement**

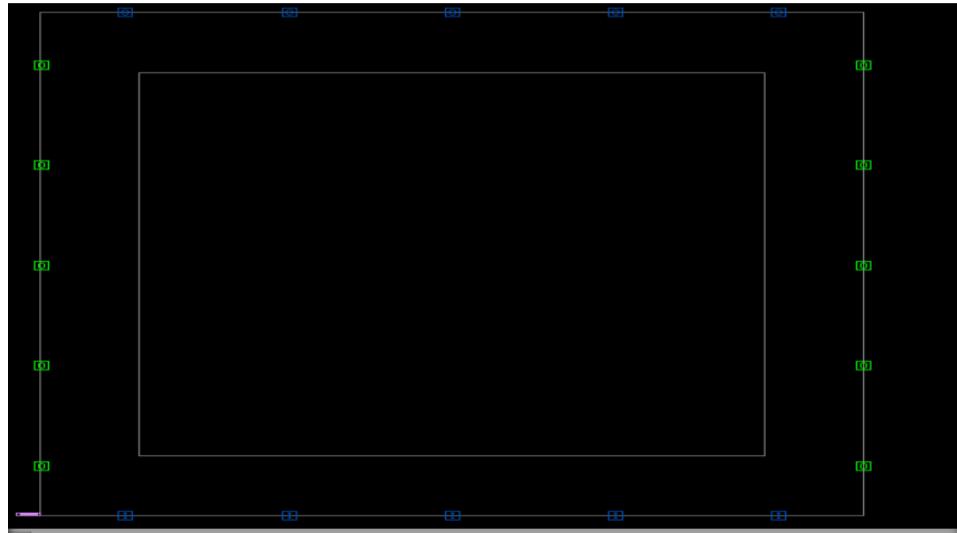


Figure 51:Create_Floorplan & port placement

- **Create_Floorplane_Placement**

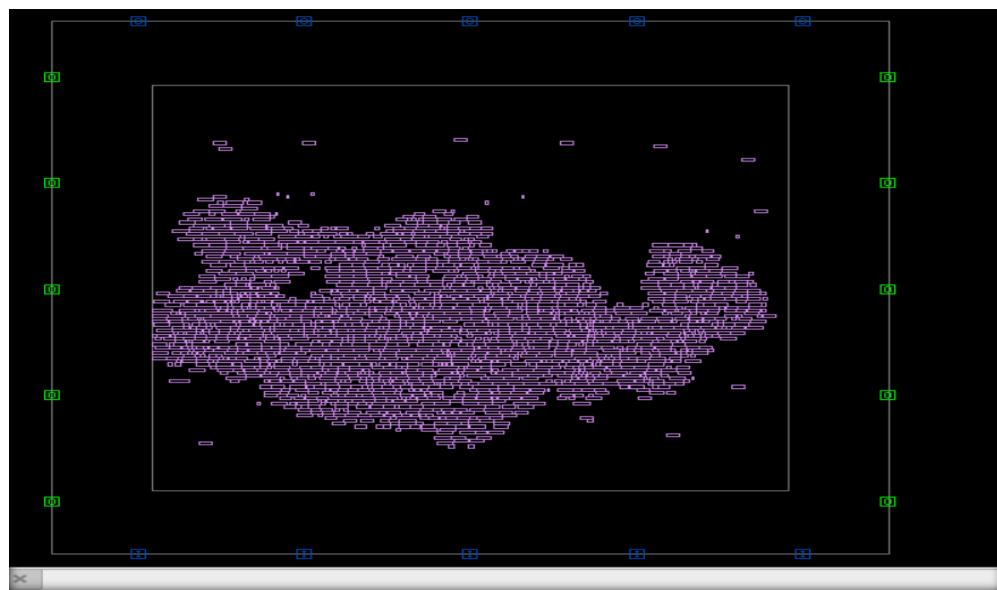


Figure 52:Floorplane_Placement

➤ Congestion

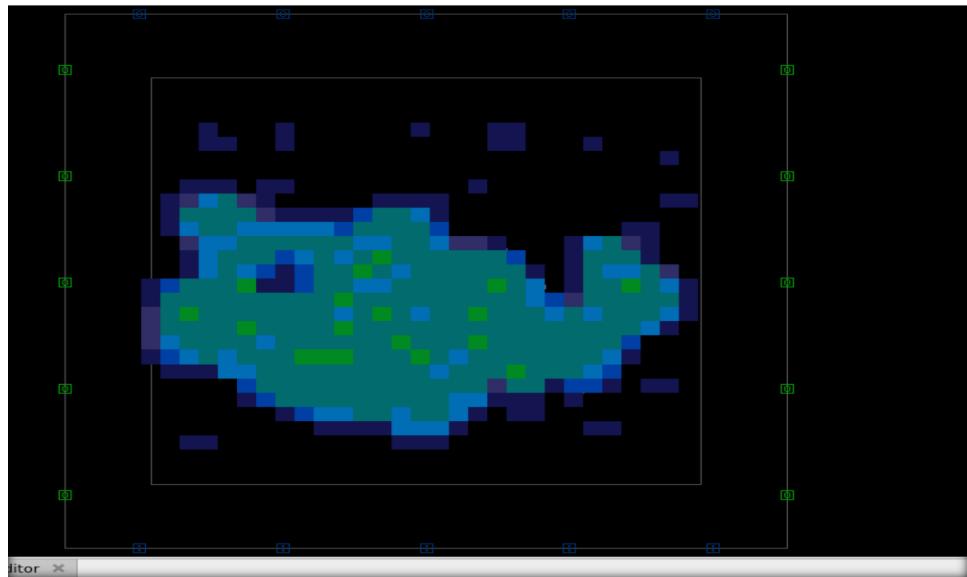


Figure 53:Congestion

5.3-powerplanning

➤ Create_STD_Cells_Rail

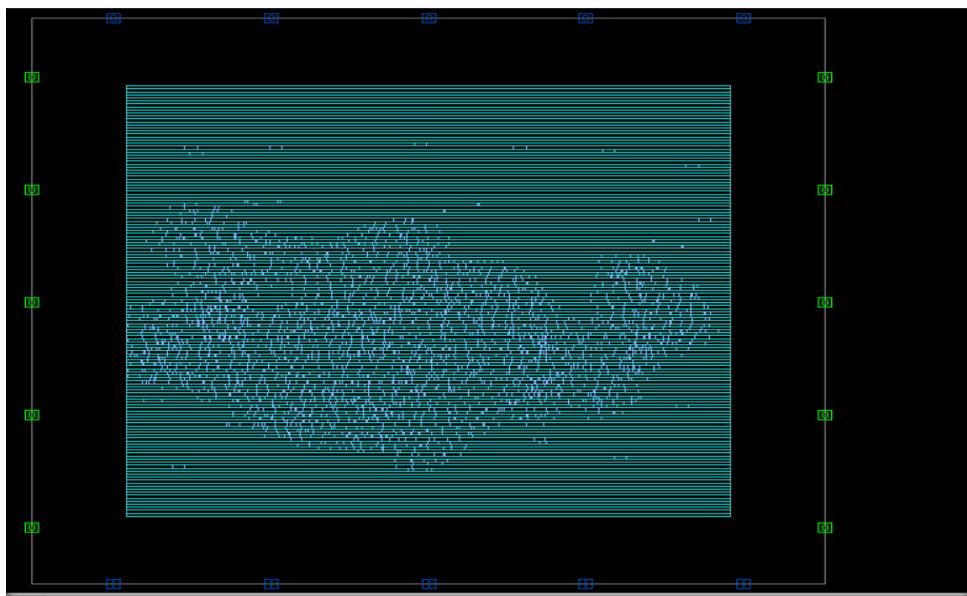


Figure 54:Cells_Rail

➤ **Create_middle_Vertical_Mesh**

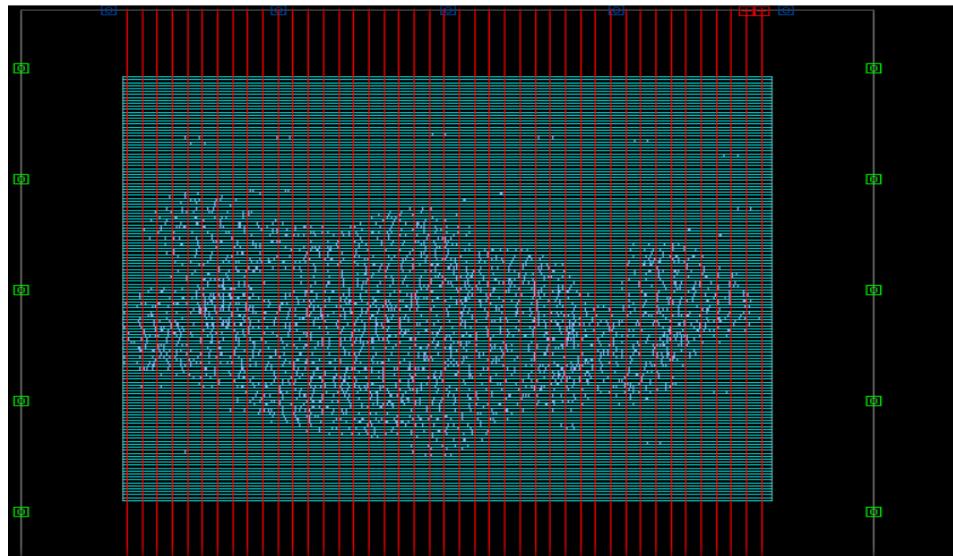


Figure 55:middle_Vertical_Mesh

➤ **Create_Top_Horizontal_Mesh**

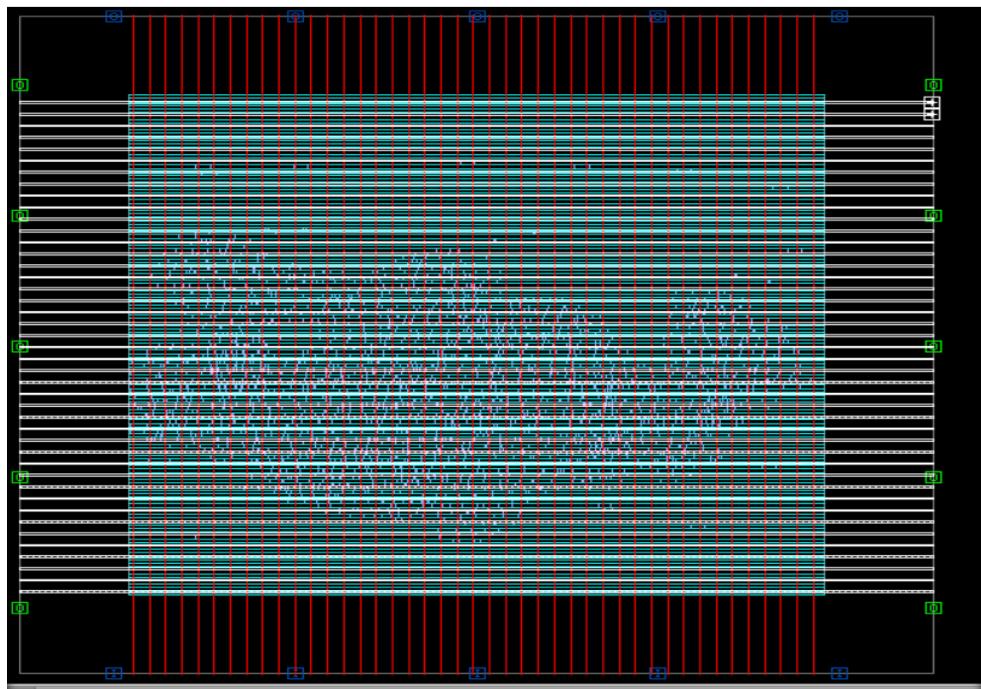


Figure 56:Top_Horizontal_Mesh

➤ **Create_Top_Vertical_Mesh**

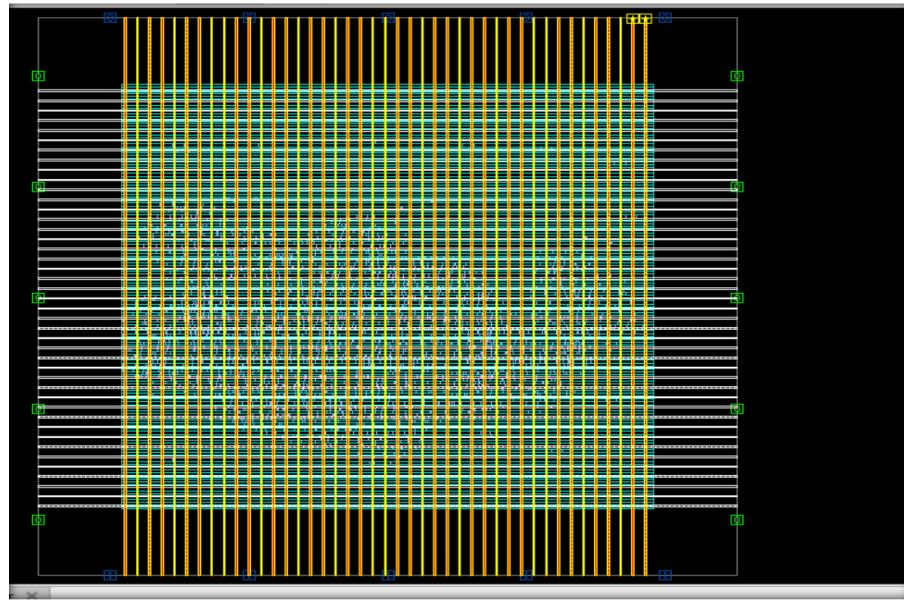


Figure 57:Top_Vertical_Mesh

➤ **Create_Rectangular_Rings**

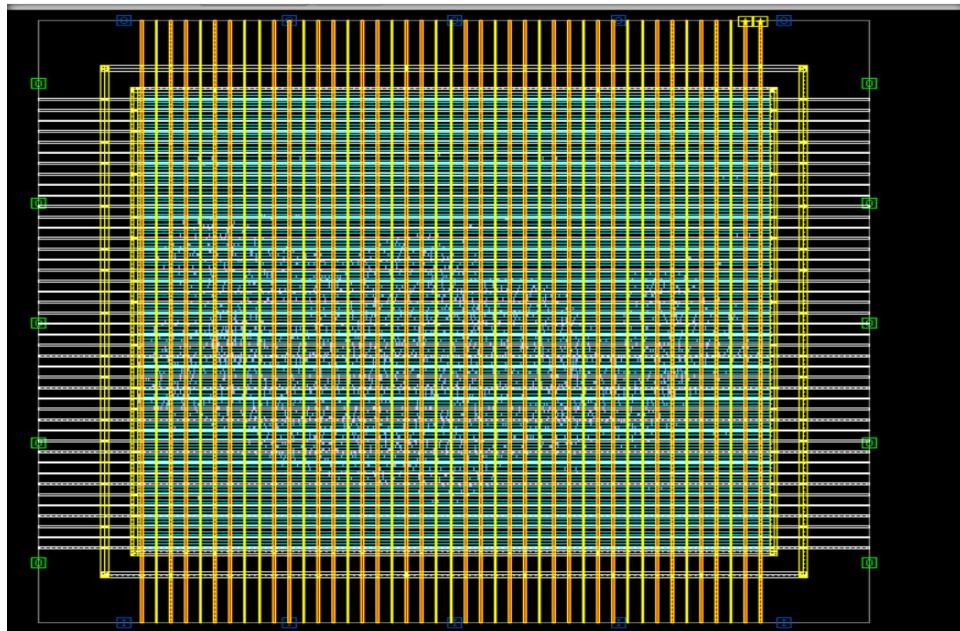


Figure 58:Rectangular_Rings

5.4-place

➤ **place_opt**

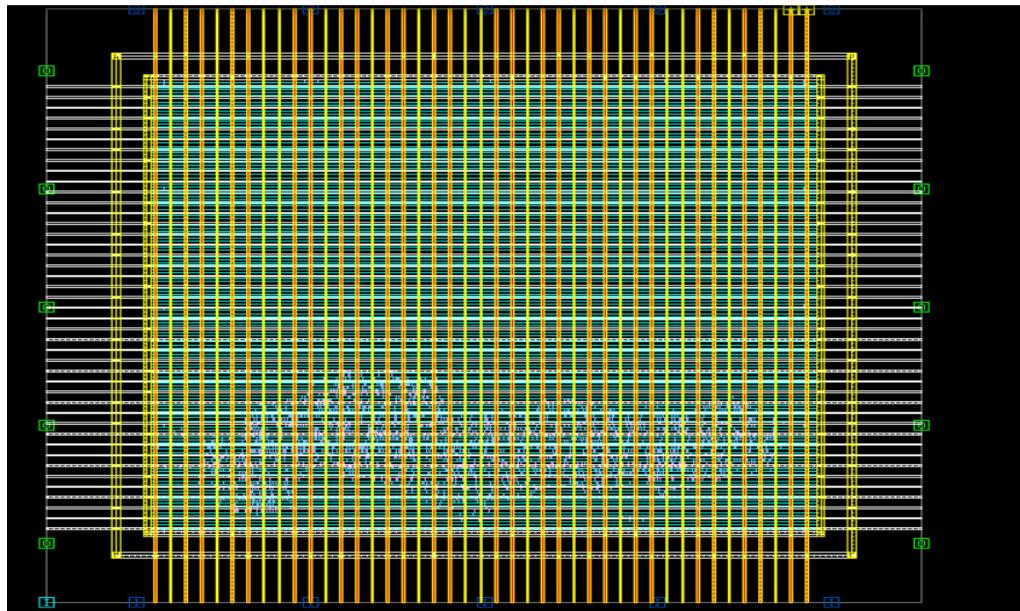


Figure 59:place_opt

➤ **legalize_placement**

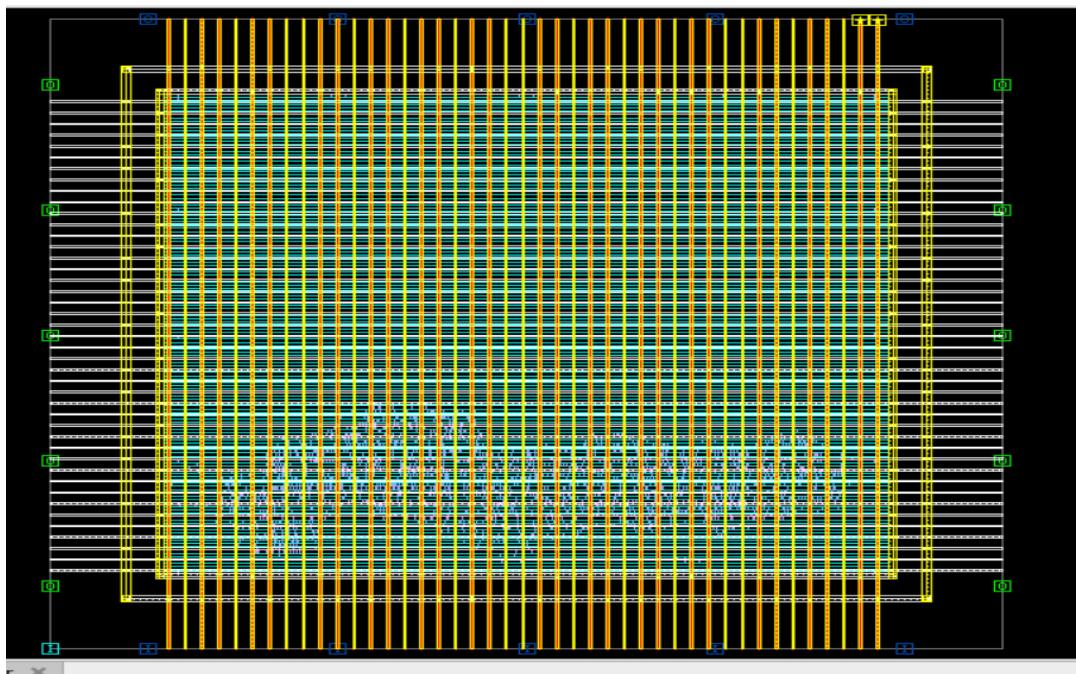


Figure 60:legalize_placement

5.5- Clock Tree Synthesis (CTS)

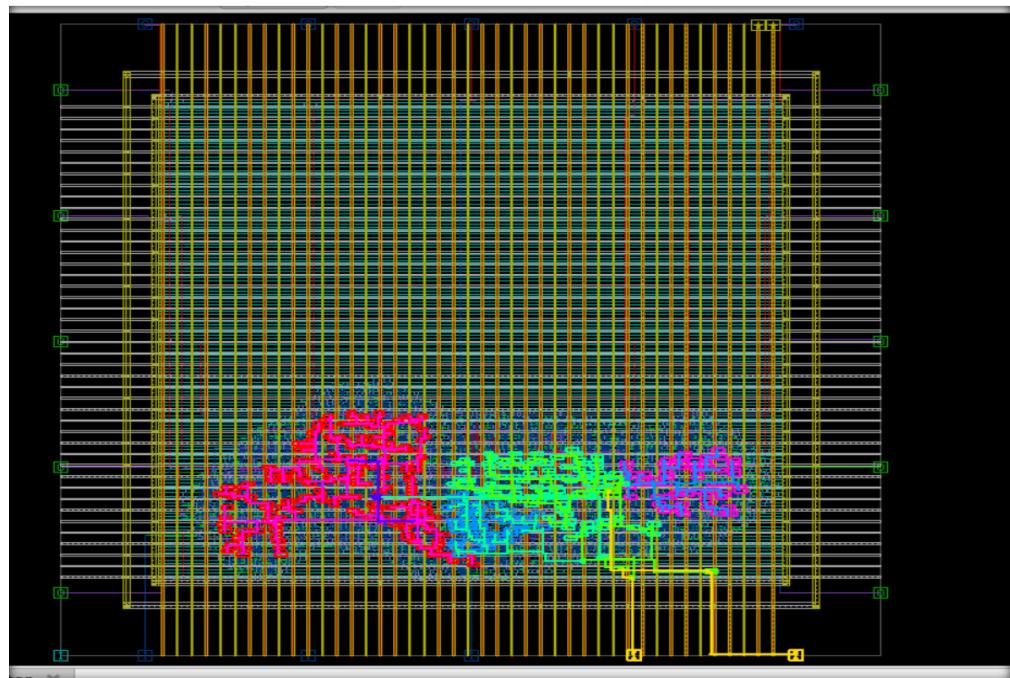


Figure 61:CTS

5.6-route

➤ **route_auto**

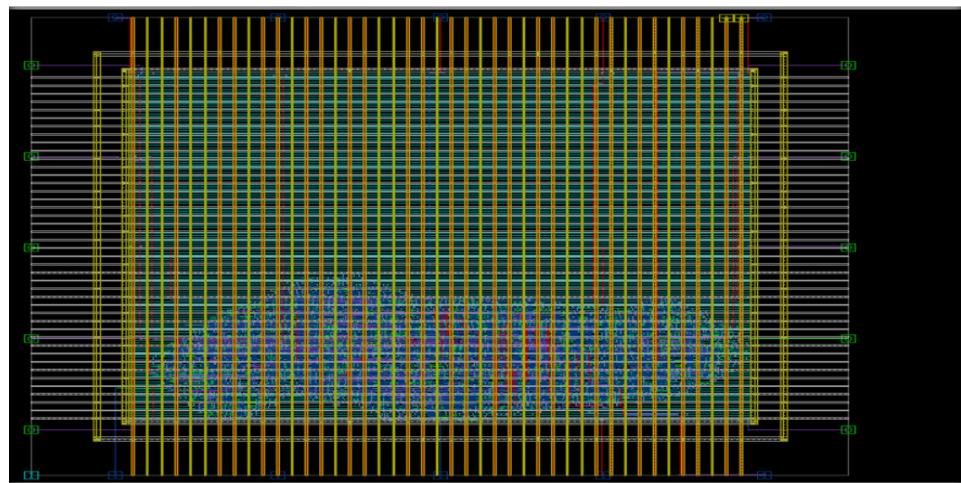


Figure 62: route auto

➤ route_opt

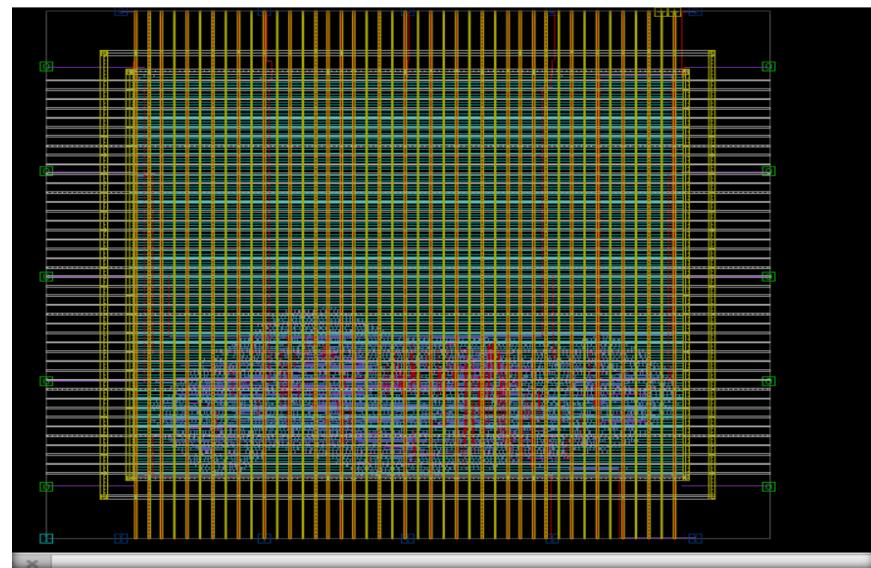


Figure 63:route opt

5.7-Finishing

➤ insert filler

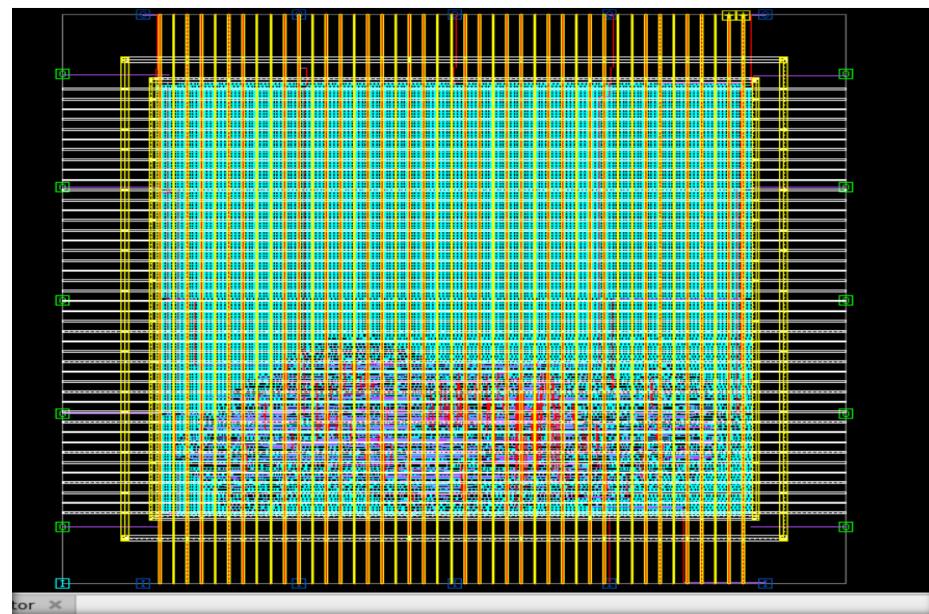


Figure 64:insert filler

6-Reports

6.1-area report

- Place global time

```
Report : global timing
      -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 13:35:06 2025
*****
Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -7.193      0.000     -0.057     -7.193     -6.670
TNS     -93.695     0.000     -0.866    -86.158     -6.670
NUM       42          0          27         14          1
-----
Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -0.180     -0.180      0.000      0.000      0.000
TNS     -39.412    -39.412      0.000      0.000      0.000
NUM      390        390          0          0          0
-----
1
```

Figure 65:Place global time

➤ Place qor

```

Scenario          'func_slow'
Timing Path Group 'reg2reg'
-----
Levels of Logic:          6
Critical Path Length:    0.15
Critical Path Slack:     0.14
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:   0
Worst Hold Violation:    -0.18
Total Hold Violation:    -38.73
No. of Hold Violations:   368
-----

Cell Count
-----
Hierarchical Cell Count:      25
Hierarchical Port Count:      552
Leaf Cell Count:              1564
Buf/Inv Cell Count:           391
Buf Cell Count:               57
Inv Cell Count:               334
Combinational Cell Count:     1186
Single-bit Isolation Cell Count: 0
Multi-bit Isolation Cell Count: 0
Isolation Cell Banking Ratio: 0.00%
Single-bit Level Shifter Cell Count: 0
Multi-bit Level Shifter Cell Count: 0
Level Shifter Cell Banking Ratio: 0.00%
Single-bit ELS Cell Count:     0
Multi-bit ELS Cell Count:      0
ELS Cell Banking Ratio:       0.00%
Sequential Cell Count:        378
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count:    0
Single-bit Sequential Cell Count: 378
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflop:                  1.00
Macro Count:                  0
-----

Level Shifter Cell Banking Ratio:      0.00%
Single-bit ELS Cell Count:             0
Multi-bit ELS Cell Count:             0
ELS Cell Banking Ratio:              0.00%
Sequential Cell Count:                378
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count:         0
Single-bit Sequential Cell Count:    378
Multi-bit Sequential Cell Count:     0
Sequential Cell Banking Ratio:       0.00%
BitsPerflop:                        1.00
Macro Count:                       0
-----

Area
-----
Combinational Area:           406.62
Noncombinational Area:        391.08
Buf/Inv Area:                 114.24
Total Buffer Area:            32.68
Total Inverter Area:          81.56
Macro/Black Box Area:         0.00
Net Area:                     0
Net XLength:                  4217.57
Net YLength:                  4194.51
-----
Cell Area (netlist):          797.69
Cell Area (netlist and physical only): 797.69
Net Length:                   8412.08
-----

Design Rules
-----
Total Number of Nets:          1689
Nets with Violations:         875
Max Trans Violations:          15
Max Cap Violations:           15
-----
1

```

Figure 66:Place qor

➤ Clock tree

```
=====
==== Summary Reporting for Corner fast ====
=====

===== Summary Table for Corner fast =====
Clock / Skew Group          Attrs   Sinks Levels    Clock Repeater Clock Stdcell Max Global Trans DRC Cap DRC Wire
Skew Group                  Count   Area       Count  Area     Area Latency Skew Count Count Count Length
=====
### Mode: func, Scenario: func_fast
sys_clock                   M,D    197   4      5    1.86   4.08   0.09   0.08   0   0   0   383.16
sys_gated_clk               G      60    1      0    0.00   0.00   0.00   0.00   0   0   0   0.00
spi_clock                   M,D    178   4      5    2.75   4.22   0.06   0.03   0   0   0   388.55
spi_gated_clk               G      178   2      4    2.49   2.49   0.02   0.02   0   0   0   296.93
All Clocks                  375   4      10   4.62   8.30   0.09   0.08   0   0   0   763.71

Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)
=====
==== Summary Reporting for Corner slow ====
=====

===== Summary Table for Corner slow =====
Clock / Skew Group          Attrs   Sinks Levels    Clock Repeater Clock Stdcell Max Global Trans DRC Cap DRC Wire
Skew Group                  Count   Area       Count  Area     Area Latency Skew Count Count Count Length
=====
### Mode: func, Scenario: func_slow
sys_clock                   M,D    197   4      5    1.86   4.08   0.09   0.08   0   0   0   383.16
sys_gated_clk               G      60    1      0    0.00   0.00   0.00   0.00   0   0   0   0.00
spi_clock                   M,D    178   4      5    2.75   4.22   0.06   0.03   0   0   0   388.55
spi_gated_clk               G      178   2      4    2.49   2.49   0.02   0.02   0   0   0   296.93
All Clocks                  375   4      10   4.62   8.30   0.09   0.08   0   0   0   763.71

Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)
1
```

Figure 67: clk tree(area)

➤ Route global time

```
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Wed Aug 20 13:39:21 2025
*****
***** Setup violations *****
-----  

Total reg->reg in->reg reg->out in->out  

-----  

WNS -7.198 0.000 -0.208 -7.198 -6.670  

TNS -98.531 0.000 -5.166 -86.695 -6.670  

NUM 42 0 27 14 1  

-----  

***** Hold violations *****
-----  

Total reg->reg in->reg reg->out in->out  

-----  

WNS -0.162 -0.162 0.000 0.000 0.000  

TNS -46.045 -46.045 0.000 0.000 0.000  

NUM 456 456 0 0 0  

-----  

1
```

Figure 68:Clk-pre-route

```
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Wed Aug 20 13:42:42 2025
*****
***** Setup violations *****
-----  

Total reg->reg in->reg reg->out in->out  

-----  

WNS -6.874 0.000 -0.203 -6.874 -6.496  

TNS -97.720 0.000 -5.106 -86.119 -6.496  

NUM 42 0 27 14 1  

-----  

***** Hold violations *****
-----  

Total reg->reg in->reg reg->out in->out  

-----  

WNS -0.141 -0.141 0.000 0.000 0.000  

TNS -0.390 -0.390 0.000 0.000 0.000  

NUM 10 10 0 0 0  

-----  

1
```

Figure 69:Clk-route

➤ Route qor

```

Scenario          'func_slow'
Timing Path Group 'reg2reg'
-----
Levels of Logic:           11
Critical Path Length:      0.19
Critical Path Slack:       0.00
Critical Path Clk Period:  1.00
Total Negative Slack:      0.00
No. of Violating Paths:    0
Worst Hold Violation:     -0.12
Total Hold Violation:      -0.12
No. of Hold Violations:    1
-----

Cell Count
-----
Hierarchical Cell Count:   25
Hierarchical Port Count:   575
Leaf Cell Count:           3622
Buf/Inv Cell Count:        2448
Buf Cell Count:             2119
Inv Cell Count:             329
Combinational Cell Count:  3244
  Single-bit Isolation Cell Count: 0
  Multi-bit Isolation Cell Count: 0
  Isolation Cell Banking Ratio:   0.00%
  Single-bit Level Shifter Cell Count: 0
  Multi-bit Level Shifter Cell Count: 0
  Level Shifter Cell Banking Ratio:  0.00%
  Single-bit ELS Cell Count: 0
  Multi-bit ELS Cell Count: 0
  ELS Cell Banking Ratio:   0.00%
  Sequential Cell Count:    378
  Integrated Clock-Gating Cell Count: 0
  Sequential Macro Cell Count: 0
  Single-bit Sequential Cell Count: 378
  Multi-bit Sequential Cell Count: 0
  Sequential Cell Banking Ratio:  0.00%
  BitsPerflop:               1.00
  Macro Count:                0

```

```

Scenario          'func_fast'
Timing Path Group 'in2out'
-----
Levels of Logic:           1
Critical Path Length:      6.92
Critical Path Slack:       -6.62
Critical Path Clk Period:  1.00
Total Negative Slack:      -6.62
No. of Violating Paths:    1
Worst Hold Violation:     0.00
Total Hold Violation:      0.00
No. of Hold Violations:    0
-----

Scenario          'func_fast'
Timing Path Group 'in2reg'
-----
Levels of Logic:           3
Critical Path Length:      0.43
Critical Path Slack:       -0.21
Critical Path Clk Period:  1.00
Total Negative Slack:      -5.59
No. of Violating Paths:    27
Worst Hold Violation:     0.00
Total Hold Violation:      0.00
No. of Hold Violations:    0
-----

Scenario          'func_fast'
Timing Path Group 'reg2out'
-----
Levels of Logic:           10
Critical Path Length:      6.57
Critical Path Slack:       -6.77
Critical Path Clk Period:  1.00
Total Negative Slack:      -85.57
No. of Violating Paths:    14
Worst Hold Violation:     0.00
Total Hold Violation:      0.00
No. of Hold Violations:    0

```

Area	
-----	-----
Combinational Area:	1144.23
Noncombinational Area:	391.56
Buf/Inv Area:	844.62
Total Buffer Area:	767.50
Total Inverter Area:	77.12
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	7780.57
Net YLength:	9585.23
-----	-----
Cell Area (netlist):	1535.80
Cell Area (netlist and physical only):	1535.80
Net Length:	17365.80

Design Rules

-----	-----
Total Number of Nets:	3755
Nets with Violations:	2089
Max Trans Violations:	15
Max Cap Violations:	15
-----	-----

1

Figure 70:Route qor

➤ finish global time

```

Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Wed Aug 20 14:17:05 2025
*****
***** Setup violations *****
-----
      Total   reg->reg   in->reg   reg->out   in->out
-----
WNS    -6.716    -0.001    -0.212    -6.716    -6.556
TNS    -97.055   -0.001    -5.600   -84.899   -6.556
NUM     43          1         27        14          1
-----
***** Hold violations *****
-----
      Total   reg->reg   in->reg   reg->out   in->out
-----
WNS    -0.133    -0.133    0.000    0.000    0.000
TNS    -0.383    -0.383    0.000    0.000    0.000
NUM      5          5         0         0         0
-----
1

```

Figure 71:finish global time

Comment:

The global timing diagnostic revealed minimal violations in regression-to-regression (reg->reg) transitions. Setup violations were negligible (0.001 for both WNS and TNS categories, 1 for NUM), while hold violations during model execution were slightly higher but still modest (0.133 WNS, 0.383 TNS, 5 NUM). These reg->reg violations indicate minor timing inconsistencies in sequential regression operations during model execution rather than specification issues.

➤ LVS

```

Information: Using 1 threads for LVS
[Check Short] Stage 1 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 1-2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2-2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 3 Elapsed = 0:00:01, CPU = 0:00:01
[Check Short] End Elapsed = 0:00:01, CPU = 0:00:01
[Check Net] Init Elapsed = 0:00:01, CPU = 0:00:01
Warning: Port VDD have no valid pin shapes. Skip this port. (RT-203)
Warning: Port VSS have no valid pin shapes. Skip this port. (RT-203)
[Check Net] 10% Elapsed = 0:00:01, CPU = 0:00:01
[Check Net] 20% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 30% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 40% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 50% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 60% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 70% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 80% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 90% Elapsed = 0:00:02, CPU = 0:00:02
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[0][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[1][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[2][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[3][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[4][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[5][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
Warning: Net u_dig_tx_asyn_fifo.read/fifom/fifo[6][1][1] has less than 2 valid port. Skip open checking for this net. (RT-284)
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:02, CPU = 0:00:02
Information: Detected open violation for Net VDD. Bbox: (0.0000 0.0000)(94.1920 94.2000). (RT-585)

=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
=====

Total number of input nets is 3755.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD.
Total number of floating route violations is 0.

```

Figure 72:LVS

Comment:

The LVS (Layout vs. Schematic) check was performed to validate the consistency between the schematic netlist and the physical layout. The report shows a total of 3755 input nets with no short or floating route violations. Only one open net was detected, which needs to be addressed to achieve a clean LVS sign-off. The absence of shorts and floating nets indicates that the layout connectivity is largely correct, and fixing the single open net will ensure complete correspondence between the schematic and layout.

➤ DRC

```
No via matrices found in the design.

FINAL DRC STATISTICS

DRC-SUMMARY:
    @@@@TOTAL VIOLATIONS =      2
    Same net via-cut spacing : 2
Total number of nets = 3745
0 open nets, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                0 ports without pins of 0 cells connected to 0 nets
                                0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 2
Total number of antenna violations = antenna checking not active
1
```

Figure 73:DRC

Comment

DRC report shows 2 violations, specifically related to *same-net via-cut spacing*. No open nets, excluded ports, or antenna violations were reported, and the overall connectivity of the design is intact. Although the violation count is small, these spacing issues must be resolved to ensure a clean sign-off before tape-out. Such violations can be addressed during the final optimization and verification stage. Tools like PrimeTime and physical verification fixes can be applied to eliminate these issues and achieve a fully DRC-clean layout.

6.2-Timing report

- Place global time

```
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 15:51:15 2025
*****
Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
WNS     -7.189     0.000     -0.056     -7.189     -6.725
TNS     -95.754    0.000     -0.832    -88.197     -6.725
NUM       42          0         27         14          1
-----
Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
WNS     -0.196     -0.196     0.000     0.000     0.000
TNS     -39.070    -39.070     0.000     0.000     0.000
NUM      367        367         0         0         0
-----
1
```

Figure 74:Place global time

- Place qor

```

Report      : create_qor_snapshot (place_qor_snp)
Design      : dig tx system
Version     : V-2023.12-SP5
Date        : Wed Aug 20 15:51:13 2025
Time unit   : 1.00ns
Resistance unit : 1.00kOhm
Capacitance unit: 1.00pF
Voltage unit  : 1.00V
Current unit   : 1.00uA
Power unit    : 1.00pW
Location      : /home/svasicint25maabdo/labs_modified/GP/WORK/./
*****
No. of scenario = 2
s1 = func_fast
s2 = func_slow
-----
WNS of each timing group:          s1      s2
-----
sys_clock           0.1677  0.1676
in2reg              -0.0561 -0.0454
reg2reg              0.1068  0.1097
reg2out             -7.1765 -7.1890
spi_clock            0.1522  0.1509
in2out              -6.7248 -6.7250
-----
Setup WNS:                 -7.1765 -7.1890 -7.1890
Setup TNS:                -95.7272 -95.4012 -95.7539
Number of setup violations:    42      42      42
Hold WNS:                  -0.1885 -0.1959 -0.1959
Hold TNS:                 -39.0426 -38.7405 -39.0703
Number of hold violations:   367     367     367
Number of max trans violations: 15      15      15
Number of max cap violations: 15      15      15
Number of min pulse width violations: 0       0       0
-----
Area:                      808.435
Cell count:                1563
Buf/inv cell count:         379
Std cell utilization:      0.1809
CPU(s):                    1899
CPU(s):                    1899

```

```

Setup WNS:                 -7.1765 -7.1890 -7.1890
Setup TNS:                -95.7272 -95.4012 -95.7539
Number of setup violations: 42      42      42
Hold WNS:                  -0.1885 -0.1959 -0.1959
Hold TNS:                 -39.0426 -38.7405 -39.0703
Number of hold violations: 367     367     367
Number of max trans violations: 15      15      15
Number of max cap violations: 15      15      15
Number of min pulse width violations: 0       0       0
-----
Area:                      808.435
Cell count:                1563
Buf/inv cell count:         379
Std cell utilization:      0.1809
CPU(s):                    1899
Mem(Mb):                  2493
Host name:                academysvr02
-----
Histogram:          s1      s2
-----
Max violations:    42      42
  above ~ -0.7 --- 15      15
  -0.6 ~ -0.7 --- 0       0
  -0.5 ~ -0.6 --- 0       0
  -0.4 ~ -0.5 --- 0       0
  -0.3 ~ -0.4 --- 0       0
  -0.2 ~ -0.3 --- 0       0
  -0.1 ~ -0.2 --- 0       0
  0 ~ -0.1 --- 27     27
-----
Min violations:    367     367
  -0.06 ~ above --- 4       2
  -0.05 ~ -0.06 --- 0       2
  -0.04 ~ -0.05 --- 2       2
  -0.03 ~ -0.04 --- 2       1
  -0.02 ~ -0.03 --- 5       2
  -0.01 ~ -0.02 --- 0       4
  0 ~ -0.01 --- 0       0

```

Figure 75:Place qor

➤ Clock tree

Summary Table for Corner fast											
Clock / Skew Group	Attrs	Sinks	Levels	Clock Repeater Count	Clock Repeater Area	Clock Stdcell Area	Max Latency	Global Skew	Trans Count	Cap DRC Count	Wire Length
## Mode: func, Scenario: func_fast											
sys_clock	M,D	197	4	2	1.47	3.69	0.08	0.05	0	0	395.11
sys_gated_clk	G	60	1	0	0.00	0.00	0.00	0.00	0	0	0.00
spi_clock	M,D	178	4	5	2.97	4.44	0.05	0.02	0	0	337.38
spi_gated_clk	G	178	2	4	2.71	2.71	0.02	0.01	0	0	268.92
All Clocks		375	4	7	4.44	8.13	0.08	0.05	0	0	732.41
Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)											
==== Summary Reporting for Corner slow ====											
Clock / Skew Group	Attrs	Sinks	Levels	Clock Repeater Count	Clock Repeater Area	Clock Stdcell Area	Max Latency	Global Skew	Trans Count	Cap DRC Count	Wire Length
## Mode: func, Scenario: func_slow											
sys_clock	M,D	197	4	2	1.47	3.69	0.08	0.05	0	0	395.11
sys_gated_clk	G	60	1	0	0.00	0.00	0.00	0.00	0	0	0.00
spi_clock	M,D	178	4	5	2.97	4.44	0.06	0.02	0	0	337.38
spi_gated_clk	G	178	2	4	2.71	2.71	0.02	0.01	0	0	268.92
All Clocks		375	4	7	4.44	8.13	0.08	0.05	0	0	732.41
Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)											

Figure 76: clk tree(timing)

➤ CTS

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Wed Aug 20 16:00:29 2025
*****  
  

Setup violations
-----
  Total reg->reg  in->reg  reg->out  in->out
WNS   -7.192    0.000   -0.194   -7.192   -6.725
TNS   -100.371   0.000   -5.176  -88.470   -6.725
NUM      42        0       27        14        1  
  

Hold violations
-----
  Total reg->reg  in->reg  reg->out  in->out
WNS   -0.164   -0.164    0.000    0.000    0.000
TNS   -47.993  -47.993    0.000    0.000    0.000
NUM     458      458        0        0        0
-----  
1|
```

Figure 77:clock_pre_route

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Wed Aug 20 16:03:57 2025
*****  
  

Setup violations
-----
  Total reg->reg  in->reg  reg->out  in->out
WNS   -6.825    0.000   -0.195   -6.825   -6.501
TNS   -97.223   0.000   -5.145  -85.577   -6.501
NUM      42        0       27        14        1  
  

Hold violations
-----
  Total reg->reg  in->reg  reg->out  in->out
WNS   -0.139   -0.139    0.000    0.000    0.000
TNS   -0.389   -0.389    0.000    0.000    0.000
NUM      7         7        0        0        0
-----  
1|
```

Figure 78:clock_route

➤ Route global time

```

Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Thu Aug 21 16:20:02 2025
*****  

Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----  

WNS     -6.747     -0.002     -0.211     -6.747     -6.646
TNS     -97.331    -0.002     -5.572    -85.111     -6.646
NUM       43          1         27         14          1  

-----  

Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----  

WNS     -0.133     -0.133     0.000      0.000     0.000
TNS     -0.400     -0.400     0.000      0.000     0.000
NUM       19          19          0          0          0  

-----  

1

```

Figure 79:Route global time

➤ Route qor

```

Scenario      'func_fast'
Timing Path Group  'reg2reg'
-----
Levels of Logic:          9
Critical Path Length:    0.19
Critical Path Slack:     0.00
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0
Worst Hold Violation:   -0.12
Total Hold Violation:   -0.14
No. of Hold Violations: 17  

-----  

Scenario      'func_slow'
Timing Path Group  'sys_clock'
-----
Levels of Logic:          0
Critical Path Length:    0.02
Critical Path Slack:     0.18
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0
Worst Hold Violation:   -0.13
Total Hold Violation:   -0.13
No. of Hold Violations: 1  

-----  

Scenario      'func_slow'
Timing Path Group  'spi_clock'
-----
Levels of Logic:          0
Critical Path Length:    0.03
Critical Path Slack:     0.17
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0
Worst Hold Violation:   -0.13
Total Hold Violation:   -0.13
No. of Hold Violations: 1

```

```

Scenario      'func_slow'
Timing Path Group  'reg2reg'
-----
Levels of Logic:          9
Critical Path Length:    0.19
Critical Path Slack:     -0.00
Critical Path Clk Period: 1.00
Total Negative Slack:    -0.00
No. of Violating Paths:   1
Worst Hold Violation:    -0.12
Total Hold Violation:    -0.12
No. of Hold Violations:   4
-----

Cell Count
-----
Hierarchical Cell Count:    25
Hierarchical Port Count:    572
Leaf Cell Count:            3657
Buf/Inv Cell Count:         2477
Buf Cell Count:             2153
Inv Cell Count:             324
Combinational Cell Count:   3279
    Single-bit Isolation Cell Count: 0
    Multi-bit Isolation Cell Count: 0
    Isolation Cell Banking Ratio:   0.00%
    Single-bit Level Shifter Cell Count: 0
    Multi-bit Level Shifter Cell Count: 0
    Level Shifter Cell Banking Ratio: 0.00%
    Single-bit ELS Cell Count: 0
    Multi-bit ELS Cell Count: 0
    ELS Cell Banking Ratio: 0.00%
Sequential Cell Count:      378
    Integrated Clock-Gating Cell Count: 0
    Sequential Macro Cell Count: 0
    Single-bit Sequential Cell Count: 378
    Multi-bit Sequential Cell Count: 0
    Sequential Cell Banking Ratio: 0.00%
    BitsPerflop: 1.00
Macro Count:                0

```

```

Area
-----
Combinational Area:        1170.38
Noncombinational Area:     390.81
Buf/Inv Area:              865.71
Total Buffer Area:         787.61
Total Inverter Area:       78.10
Macro/Black Box Area:      0.00
Net Area:                  0
Net XLength:               8415.83
Net YLength:               10265.62
-----
Cell Area (netlist):        1561.19
Cell Area (netlist and physical only): 1561.19
Net Length:                 18681.45

```

```

Design Rules
-----
Total Number of Nets:       3793
Nets with Violations:      1960
Max Trans Violations:       15
Max Cap Violations:        15
-----
```

1

Figure 80:Route qor

➤ finish global time

```
Report : global timing
          -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Thu Aug 21 16:28:44 2025
*****
Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -6.683     -0.003     -0.211     -6.683     -6.582
TNS     -96.472    -0.003     -5.573    -84.313     -6.582
NUM       43           1           27           14           1
-----
Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -0.133     -0.133      0.000      0.000      0.000
TNS     -0.391     -0.391      0.000      0.000      0.000
NUM       13          13           0           0           0
-----
1
```

Figure 81:finish global time

Comment:

The reg->reg timing shows minor setup violations but more concerning hold violations. The setup timing is nearly clean with just 3ps of negative slack affecting one path. However, the hold violations are more significant with 13 failing paths and 391ps of total negative slack.

Hold violations in reg->reg transitions typically indicate insufficient delay between sequential register stages. These hold violations need to be addressed through buffer insertion, delay cells, or routing adjustments to ensure reliable operation across all process-voltage-temperature (PVT) conditions.

➤ LVS

```
=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
=====
Total number of input nets is 3793.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD
Total number of floating route violations is 0.

Elapsed = 0:00:02, CPU = 0:00:02
1
```

Figure 82:LVS

Comment:

The results indicate high-quality layout implementation connectivity accuracy (3,792 of 3,793 nets correct). The single open net is likely a minor routing oversight or missing via connection. Once this open net is identified and corrected, the design should achieve full LVS clean status, confirming complete correspondence between the schematic intent and physical layout implementation.

➤ DRC

```
DRC-SUMMARY:
    @@@@ @@@@ TOTAL VIOLATIONS =      0
Total number of nets = 3789
0 open nets, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                0 ports without pins of 0 cells connected to 0 nets
                                0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = antenna checking not active
1
```

Figure 83:DRC

Comment:

This represents a perfect DRC result with full compliance to all manufacturing design rules. The layout is ready for fabrication from a geometric and spacing perspective. The clean DRC status, combined with the near-clean LVS result, indicates a high-quality physical implementation that should yield good manufacturing outcomes.

6.3-power report

- Place global time

```
Report : global timing
      -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 15:51:15 2025
*****
Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -7.189      0.000     -0.056     -7.189     -6.725
TNS     -95.754     0.000     -0.832    -88.197     -6.725
NUM       42          0         27         14          1
-----
Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -0.196     -0.196      0.000      0.000      0.000
TNS     -39.070    -39.070      0.000      0.000      0.000
NUM      367        367         0          0          0
-----
1
```

Figure 84:Place global time

➤ Place qor

```
Scenario          'func_fast'
Timing Path Group 'reg2reg'
-----
Levels of Logic:          8
Critical Path Length:    0.14
Critical Path Slack:     0.18
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:   0
Worst Hold Violation:    -0.18
Total Hold Violation:    -37.26
No. of Hold Violations:  368
-----

Scenario          'func_slow'
Timing Path Group 'sys_clock'
-----
Levels of Logic:          0
Critical Path Length:    0.02
Critical Path Slack:     0.17
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:   0
Worst Hold Violation:    -0.12
Total Hold Violation:    -0.12
No. of Hold Violations:  1
-----

Scenario          'func_slow'
Timing Path Group 'spi_clock'
-----
Levels of Logic:          0
Critical Path Length:    0.02
Critical Path Slack:     0.15
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:   0
Worst Hold Violation:    -0.10
Total Hold Violation:    -0.10
No. of Hold Violations:  1
```

```
Sequential Cell Count:      378
Integrated Clock-Gating Cell Count: 0
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 378
Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPer flop:               1.00
Macro Count:                0
-----

Area
-----
Combinational Area:        418.25
Noncombinational Area:    391.70
Buf/Inv Area:              120.95
Total Buffer Area:         16.34
Total Inverter Area:       104.61
Macro/Black Box Area:      0.00
Net Area:                  0
Net XLength:               4406.43
Net YLength:               4277.94
Cell Area (netlist):        809.94
Cell Area (netlist and physical only): 809.95
Net Length:                8684.37
-----

Design Rules
-----
Total Number of Nets:      1680
Nets with Violations:     793
Max Trans Violations:     15
Max Cap Violations:       15
-----
```

Figure 85:Place qor

➤ Clock tree

```
=====
==== Summary Reporting for Corner fast ====
=====

===== Summary Table for Corner fast =====
Clock / Skew Group          Attrs   Sinks Levels    Clock Repeater Repeater Stdcell Max Global Trans DRC Cap DRC Wire
Skew Group                  Count   Area       Count Area     Area Latency Skew   Count Count Length
=====
### Mode: func, Scenario: func_fast
sys_clock                   M,D    197   4      3    1.73   3.95   0.87   0.06   0   0   0   429.67
sys_gated_clk               G      60    1      0    0.00   0.00   0.00   0.00   0   0   0   0.00
spi_clock                   M,D    178   5      7    3.69   5.11   0.06   0.02   0   0   0   374.96
spi_gated_clk               G      178   3      6    3.42   3.42   0.02   0.01   0   0   0   385.64
All Clocks                  375   5      10   5.42   9.06   0.87   0.06   0   0   0   884.63
Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)
===== Summary Reporting for Corner slow ====
=====

===== Summary Table for Corner slow =====
Clock / Skew Group          Attrs   Sinks Levels    Clock Repeater Repeater Stdcell Max Global Trans DRC Cap DRC Wire
Skew Group                  Count   Area       Count Area     Area Latency Skew   Count Count Length
=====
### Mode: func, Scenario: func_slow
sys_clock                   M,D    197   4      3    1.73   3.95   0.88   0.06   0   0   0   429.67
sys_gated_clk               G      60    1      0    0.00   0.00   0.00   0.00   0   0   0   0.00
spi_clock                   M,D    178   5      7    3.69   5.11   0.06   0.02   0   0   0   374.96
spi_gated_clk               G      178   3      6    3.42   3.42   0.02   0.01   0   0   0   385.64
All Clocks                  375   5      10   5.42   9.06   0.88   0.06   0   0   0   884.63
Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)
```

Figure 86: clk tree(power)

➤ CTS

Report : global timing -format { narrow }						Report : global timing -format { narrow }					
Design : dig_tx_system Version: V-2023.12-SP5 Date : Wed Aug 20 15:03:51 2025						Design : dig_tx_system Version: V-2023.12-SP5 Date : Wed Aug 20 15:07:17 2025					
Setup violations						Setup violations					
Total	reg->reg	in->reg	reg->out	in->out	Total	reg->reg	in->reg	reg->out	in->out		
WNS	-6.914	0.000	-0.194	-6.914	-6.245	WNS	-6.779	-0.000	-0.185	-6.779	-6.202
TNS	-97.048	0.000	-5.133	-85.670	-6.245	TNS	-96.320	-0.000	-4.977	-85.141	-6.202
NUM	42	0	27	14	1	NUM	43	1	27	14	1
Hold violations						Hold violations					
Total	reg->reg	in->reg	reg->out	in->out	Total	reg->reg	in->reg	reg->out	in->out		
WNS	-0.172	-0.172	0.000	0.000	0.000	WNS	-0.142	-0.142	0.000	0.000	0.000
TNS	-44.416	-44.416	0.000	0.000	0.000	TNS	-0.419	-0.419	0.000	0.000	0.000
NUM	423	423	0	0	0	NUM	10	10	0	0	0
1											

Figure 87:clock_pre_route

Figure 88:clock_route

➤ Route global time

```

Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 15:13:24 2025
*****  

Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -6.699      0.000     -0.206     -6.699     -6.144
TNS     -96.344      0.000     -5.541    -84.660     -6.144
NUM        42          0         27         14          1  

-----
Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS     -0.133      -0.133      0.000      0.000      0.000
TNS     -0.866      -0.866      0.000      0.000      0.000
NUM       182          182          0          0          0  

-----
1

```

Figure 89:Route global time

➤ Route qor

```

Scenario           'func_fast'
Timing Path Group 'reg2reg'
-----
Levels of Logic:          10
Critical Path Length:    0.18
Critical Path Slack:     0.01
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0
Worst Hold Violation:   -0.12
Total Hold Violation:   -0.60
No. of Hold Violations: 180
-----

Scenario           'func_slow'
Timing Path Group 'sys_clock'
-----
Levels of Logic:          0
Critical Path Length:    0.02
Critical Path Slack:     0.18
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0
Worst Hold Violation:   -0.13
Total Hold Violation:   -0.13
No. of Hold Violations: 1
-----

Scenario           'func_slow'
Timing Path Group 'spi_clock'
-----
Levels of Logic:          0
Critical Path Length:    0.02
Critical Path Slack:     0.18
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0
Worst Hold Violation:   -0.13
Total Hold Violation:   -0.13
No. of Hold Violations: 1

```

```

Scenario          'func_slow'
Timing Path Group 'reg2Reg'
-----
Levels of Logic:           11
Critical Path Length:     0.18
Critical Path Slack:      0.01
Critical Path Clk Period: 1.00
Total Negative Slack:     0.00
No. of Violating Paths:   0
Worst Hold Violation:    -0.12
Total Hold Violation:    -0.30
No. of Hold Violations:  90
-----

Cell Count
-----
Hierarchical Cell Count: 25
Hierarchical Port Count: 574
Leaf Cell Count: 3760
Buf/Inv Cell Count: 2592
Buf Cell Count: 2148
Inv Cell Count: 444
Combinational Cell Count: 3382
    Single-bit Isolation Cell Count: 0
    Multi-bit Isolation Cell Count: 0
    Isolation Cell Banking Ratio: 0.00%
    Single-bit Level Shifter Cell Count: 0
    Multi-bit Level Shifter Cell Count: 0
    Level Shifter Cell Banking Ratio: 0.00%
    Single-bit ELS Cell Count: 0
    Multi-bit ELS Cell Count: 0
    ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 378
    Integrated Clock-Gating Cell Count: 0
    Sequential Macro Cell Count: 0
    Single-bit Sequential Cell Count: 378
    Multi-bit Sequential Cell Count: 0
    Sequential Cell Banking Ratio: 0.00%
    BitsPer flop: 1.00

```

Area	
Combinational Area:	1159.24
Noncombinational Area:	391.70
Buf/Inv Area:	857.10
Total Buffer Area:	753.20
Total Inverter Area:	103.90
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	7459.44
Net YLength:	9018.68

Cell Area (netlist):	1550.94
Cell Area (netlist and physical only):	1550.94
Net Length:	16478.12

Design Rules

Total Number of Nets:	3791
Nets with Violations:	2427
Max Trans Violations:	15
Max Cap Violations:	15

Figure 90:Route qor

➤ finish global time

```
Report : global timing
         -format { narrow }
Design  : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 15:20:13 2025
*****
Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
WNS     -6.650     0.000     -0.206     -6.650     -6.083
TNS     -95.712     0.000     -5.542    -84.087     -6.083
NUM       42          0          27          14          1
-----
Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
WNS     -0.133     -0.133     0.000     0.000     0.000
TNS     -0.727     -0.727     0.000     0.000     0.000
NUM      149        149          0          0          0
-----
1
```

Figure 91:finish global time

Comment:

The reg->reg timing shows significant improvement in setup timing - all setup violations have been resolved with zero negative slack. However, the hold violations have actually worsened, increasing from 13 to 17 failing paths and total negative slack growing from 391ps to 727ps.

➤ LVS

```
=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
=====
Total number of input nets is 3791.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD
Total number of floating route violations is 0.

Elapsed = 0:00:03, CPU = 0:00:03
1
```

Figure 92:LVS

Comment:

This consistent result confirms the open net is a real connectivity discrepancy between schematic and layout that requires specific debugging attention. The stability of other metrics (zero shorts, zero floating routes) demonstrates the core design integrity remains intact, making this a focused fix rather than a broad connectivity problem. The open net should be identified and resolved to achieve full LVS sign-off.

➤ DRC

```
DRC-SUMMARY:  
    @@@@@@@ TOTAL VIOLATIONS =      0  
Total number of nets = 3785  
0 open nets, of which 0 are frozen  
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets  
                                0 ports without pins of 0 cells connected to 0 nets  
                                0 ports of 0 cover cells connected to 0 non-pg nets  
Total number of DRCs = 0  
Total number of antenna violations = antenna checking not active  
1
```

Figure 93:DRC

Comment:

This represents another perfect DRC result, confirming the layout maintains excellent manufacturing compliance despite design changes. The clean physical connectivity (0 open nets in DRC) versus the persistent open net in LVS further supports that the connectivity issue is in the netlist comparison logic rather than actual routing problems.

7-Prime time

- We applied PrimeTime analysis to validate the design under timing and area constraints. Initially, the design exhibited golden violations in both area and setup timing. After running PrimeTime with proper constraint optimization, the violations were resolved, and the design successfully reached 0 violations for area and

7.1-fix setup

```
#setup  
fix_eco_timing -type setup -cell_type {combinational sequential}
```

Figure 94:fix setup

7.2-fix hold

```
insert_buffer -new_cell_names "clk_buf19" -new_net_names "clk_net19" [get_pins u_dig_tx_spi_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf20" -new_net_names "clk_net20" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf21" -new_net_names "clk_net21" [get_pins u_dig_tx_spi_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]

insert_buffer -new_cell_names "clk_buf17" -new_net_names "clk_net17" [get_pins u_dig_tx_spi_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf18" -new_net_names "clk_net18" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf16" -new_net_names "clk_net16" [get_pins u_dig_tx_spi_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf15" -new_net_names "clk_net15" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf13" -new_net_names "clk_net13" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf14" -new_net_names "clk_net14" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf11" -new_net_names "clk_net11" [get_pins -8.127 pin u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf12" -new_net_names "clk_net12" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf10" -new_net_names "clk_net10" [get_pins u_dig_tx_sys_clock_gating/U2/A1] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf8" -new_net_names "clk_net8" [get_pins u_spi_slave_clockctrl_h_inst 7413/X] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf7" -new_net_names "clk_net7" [get_pins u_spi_slave/miso_reg_reg[2]/CK] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf6" -new_net_names "clk_net6" [get_pins u_dig_tx_sys_clock_gating/clk_buf_capture/X] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf5" -new_net_names "clk_net5" [get_pins u_dig_tx_sys_clock_gating/clk_buf_capture/X] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf4" -new_net_names "clk_net4" [get_pins u_dig_tx_sys_clock_gating/enable_latch_reg/D] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf3" -new_net_names "clk_net3" [get_pins u_dig_tx_reg_file/reg_file/reg[0][0]/0] [get_lib_cells "/SAEDLVT14_BUF_1"]
insert_buffer -new_cell_names "clk_buf2" -new_net_names "clk_net2" [get_pins u_dig_tx_sys_clock_gating/enable_latch_reg/D] [get_lib_cells "/SAEDLVT14_BUF_8"]
insert_buffer -new_cell_names "clk_buf_capture" -new_net_names "clk_net_delayed" [get_pins u_dig_tx_reg_file/reg_file/reg[0][0]/CK] [get_lib_cells "/SAEDLVT14_BUF_8"]
#save outputs
write_changes -format icctcl -output eco_changes.tcl
save_session dig_tx_system
```

Figure 95:fix hold

7.3 Global timing after fixing

```
Information: Inferring 1 clock-gating checks. (PTE-017)
*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Thu Aug 21 14:33:25 2025
*****
```

Setup violations

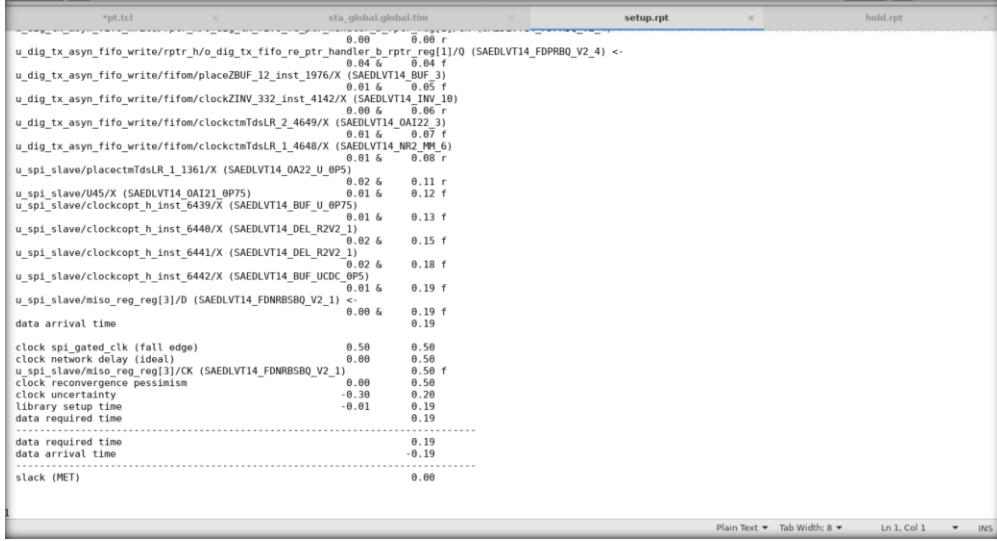
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.500	0.000	-0.215	-6.500	-6.069
TNS	-94.933	0.000	-5.635	-83.229	-6.069
NUM	42	0	27	14	1

No hold violations found.

1

Figure 96:Global timing after fixing

7.3-setup after fixing:



```

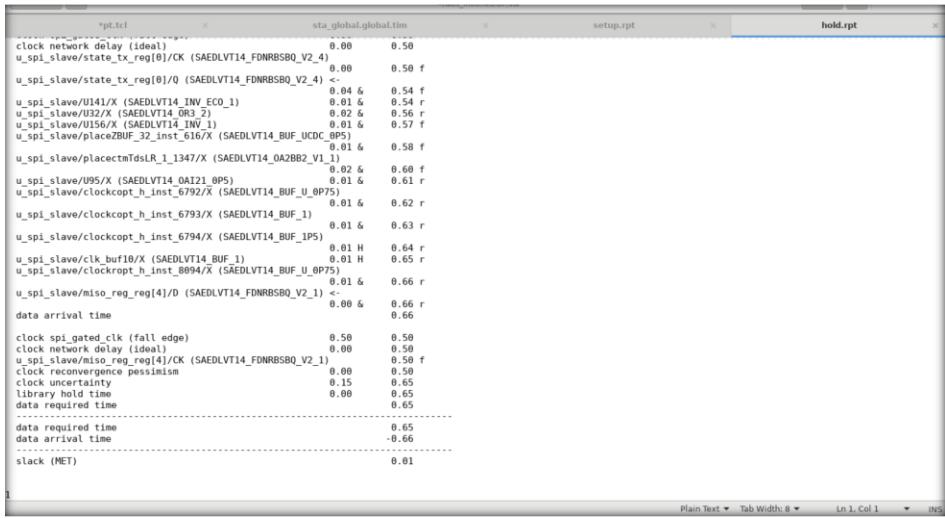
*pt.tcl          sta_global.global.tim      setup.rpt          hold.rpt
                0.00   0.00 r
u_dig_tx_asyn_fifo_write/rptr_h/o_dig_tx_fifo_re_ptr_handler_b_rptr_reg[1]/Q (SAEDLVT14_FDPRBQ_V2_4) <-
                0.04 &  0.04 f
u_dig_tx_asyn_fifo_write/fifom/placeZBUF_12_inst_1976/X (SAEDLVT14_BUF_3)
                0.01 &  0.05 f
u_dig_tx_asyn_fifo_write/fifom/clockZINV_332_inst_4142/X (SAEDLVT14_BUF_U_0018)
                0.01 &  0.06 f
u_dig_tx_asyn_fifo_write/fifom/clockcktmdsLR_2_4649/X (SAEDLVT14_0A122_3)
                0.01 &  0.07 f
u_dig_tx_asyn_fifo_write/fifom/clockcktmdsLR_1_4648/X (SAEDLVT14_NR2_MM_6)
                0.01 &  0.08 f
u_spi_slave/placecktmdsLR_1_1361/X (SAEDLVT14_0A22_U_005)
                0.02 &  0.11 r
u_spi_slave/U45/X (SAEDLVT14_0A121_0P75)
                0.01 &  0.12 f
u_spi_slave/clockcpt_h_inst_6439/X (SAEDLVT14_BUF_U_0P75)
                0.01 &  0.13 f
u_spi_slave/clockcpt_h_inst_6440/X (SAEDLVT14_DEL_R2V2_1)
                0.02 &  0.15 f
u_spi_slave/clockcpt_h_inst_6441/X (SAEDLVT14_DEL_R2V2_2)
                0.02 &  0.18 f
u_spi_slave/clockcpt_h_inst_6442/X (SAEDLVT14_BUF_UCDC_0P5)
                0.01 &  0.19 f
u_spi_slave/miso_reg_reg[3]/D (SAEDLVT14_FDNRBSBQ_V2_1) <-
                0.00 &  0.19 f
data arrival time                                0.19
clock spi_gated_clk (fall edge)                  0.50
clock network delay (ideal)                      0.00   0.50
u_spi_slave/miso_reg_reg[3]/CK (SAEDLVT14_FDNRBSBQ_V2_1) 0.00 f
clock reconvergence pessimism                   0.00
clock uncertainty                                -0.30   0.20
library setup time                               -0.61   0.19
data required time                             0.19
data arrival time                                0.19
slack (MET)                                     0.00

```

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Figure 97:setup after fixing

7.3-hold after fixing:



```

*pt.tcl          sta_global.global.tim      setup.rpt          hold.rpt
                0.00   0.00
clock network delay (ideal)                      0.00   0.50
u_spi_slave/state_tx_reg[0]/Q (SAEDLVT14_FDNRBSBQ_V2_4)
                0.00   0.50 f
u_spi_slave/placecktmdsLR_1_1347/X (SAEDLVT14_0A2B82_V1_1)
                0.04 &  0.54 f
u_spi_slave/U141/X (SAEDLVT14_INV_ECO_1)
                0.01 &  0.54 r
u_spi_slave/U32/X (SAEDLVT14_0R3_2)
                0.02 &  0.56 r
u_spi_slave/U156/X (SAEDLVT14_INV_1)
                0.01 &  0.57 f
u_spi_slave/placeZBUF_32_inst_616/X (SAEDLVT14_BUF_UCDC_0P5)
                0.01 &  0.58 f
u_spi_slave/placecktmdsLR_1_1347/X (SAEDLVT14_0A2B82_V1_1)
                0.02 &  0.66 f
u_spi_slave/U95/X (SAEDLVT14_0A121_0P5)
                0.01 &  0.61 r
u_spi_slave/clockcpt_h_inst_6792/X (SAEDLVT14_BUF_U_0P75)
                0.01 &  0.62 r
u_spi_slave/clockcpt_h_inst_6793/X (SAEDLVT14_BUF_1P5)
                0.01 &  0.63 r
u_spi_slave/clockcpt_h_inst_6794/X (SAEDLVT14_BUF_1P5)
                0.01 H  0.64 r
u_spi_slave/clk_buf10/X (SAEDLVT14_BUF_1)
                0.01 H  0.65 r
u_spi_slave/clockcpt_h_inst_8994/X (SAEDLVT14_BUF_U_0P75)
                0.01 &  0.66 r
u_spi_slave/miso_reg_reg[4]/D (SAEDLVT14_FDNRBSBQ_V2_1) <-
                0.00 &  0.66 r
data arrival time                                0.66
clock spi_gated_clk (fall edge)                  0.50
clock network delay (ideal)                      0.00   0.50
u_spi_slave/miso_reg_reg[4]/CK (SAEDLVT14_FDNRBSBQ_V2_1) 0.00 f
clock reconvergence pessimism                   0.00   0.50 f
clock uncertainty                                0.15   0.65
library hold time                               0.00   0.65
data required time                             0.65
data arrival time                                0.66
slack (MET)                                     0.01

```

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Figure 98:hold after fixing

8-Conclusions:

This project successfully demonstrates the complete RTL-to-GDSII flow for a digital system transmitter, covering synthesis, floorplanning, placement, clock tree synthesis, and routing. Each stage was carefully optimized and documented, ensuring that the design meets stringent requirements for area, power, and timing. Timing violations encountered during the flow were systematically analyzed and resolved, resulting in a functionally correct and manufacturable GDSII layout. The work highlights the importance of constraint-driven optimization and structured methodology in modern VLSI design, showcasing how high-level RTL descriptions can be efficiently transformed into optimized physical implementations ready for fabrication.

9-Appendix:

- GP path: /home/svasicint25maabdo/labs_modified/GP
- WORK path: /home/svasicint25maabdo/labs_modified/GP/WORK
- Results path: /home/svasicint25maabdo/labs_modified/GP/result
- Reports path: /home/svasicint25maabdo/labs_modified/GP/report
- Scripts: /home/svasicint25maabdo/labs_modified/GP/scripts
- Constraints: /home/svasicint25maabdo/labs_modified/GP/cons
- starrc : /home/svasicint25maabdo/labs_modified/GP/starrc
- STA: /home/svasicint25maabdo/labs_modified/GP/sta