Control Implementation and GA Report

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0.1 Purpose of the Project

The primary objective of this individual Graduate Attribute report is to provide clear evidence of satisfying ECSA Exit Level Outcome 2: Application of scientific and engineering knowledge, through the end-to-end development of a cascaded digital control system for the departmental laboratory servo kit.

Foremost, the project demands dynamic modelling and system identification of the servo plant under varying load inertia, amplifier gains, and braking torques. Accurate estimation of transfer-function parameters via step, ramp, and frequency-response tests establishes a mathematical foundation on which all subsequent controller designs are based. This modelling phase also cultivates proficiency in using the MATLAB System Identification Toolbox to reconcile simulated and measured data.

Building on the identified model, the next purpose is the robust digital controller design. A two-loop cascade architecture—comprising an inner speed loop and an outer position loop—must be tuned to meet strict performance criteria: a speed-loop time constant better than 1.5 s with less than 25% overshoot, and a position-loop overshoot under 20 % with zero steady-state error for step commands. Achieving these specifications under worst-case and best-case plant variations exercises critical skills in frequency-domain analysis, PI controller synthesis, and robust stability margin allocation.

A further key purpose is to validate the design in simulation prior to laboratory implementation. Through MATLAB/Simulink, the controller's response is examined across all identified plant cases, with particular attention to settling time, disturbance rejection, and absence of wind-up phenomena. This pre-laboratory step ensures that the theoretical design will translate effectively to hardware, reducing iteration time during laboratory sessions.

The project culminates in practical implementation and experimental verification. Deploying the digital controller on the physical servo platform tests its resilience against non-idealities such as actuator saturation, dead-band effects, and measurement noise. By comparing measured responses with simulations, any discrepancies are analyzed and refinements made—closing the theory–simulation–measurement triangle that epitomizes rigorous engineering practice.

Beyond technical outcomes, this project develops professional competencies essential for a graduate engineer. It fosters analytical rigor in data analysis, design discipline in meeting specifications, experimental proficiency in laboratory instrumentation, and critical reflection when theory diverges from practice. Collectively, these experiences demonstrate not just the ability to solve a complex control problem but to do so with the systematic, evidence-based approach demanded by industry and regulatory bodies.

In sum, the project's purpose extends from mastering core control-theoretic concepts to embodying the holistic skill set of an engineering professional, fulfilling both the academic requirements of EEE4118F and the broader mandate of producing practice-ready graduates under ECSA accreditation standards.

0.2 Summary of Lab 1: Modelling and System Identification

Aim: This section distills the key findings and methodologies from Lab 1, which established the dynamic model of the servo system and validated it against experimental data.

Objectives

- Perform system identification by capturing the servo system's response under varying load, gain and braking conditions.
- Develop a mathematical model that accurately represents the identified system dynamics.
- Validate the model in MATLAB by comparing the simulated response against real-world measurements.

0.2.1 Ramp Test and Deadband Identification

A linear ramp input reveals a deadband between 0 V and 0.3 V (lasting about 5.6 s) before the system responds. This deadband must be compensated in controller design to avoid sluggish performance at low commands.

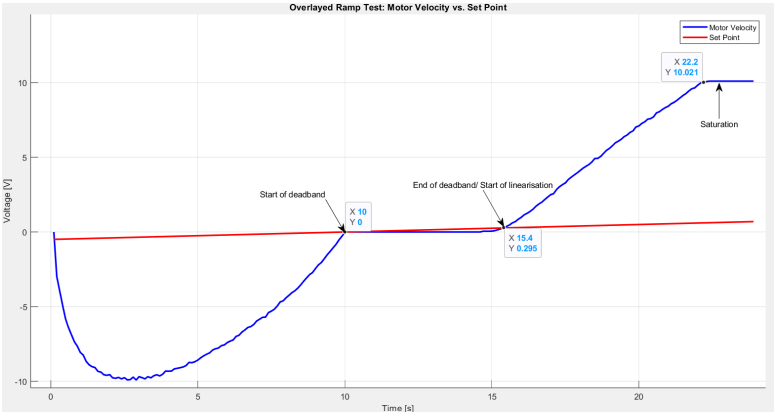


Figure 1: Ramp Test – Measured Output vs. Input Voltage

Table 1: Ramp-test deadband metrics

Parameter	Value
Deadband start (V)	0 V
Deadband end (V)	0.3 V
Deadband duration (s)	5.6 s
DAC saturation (V)	±10 V

0.2.2 Velocity Loop: Step Response vs. Simulation

Using a unit-step input, the velocity loop exhibits a first-order response. From the measured step:

$$A = 8.67\ \text{V}, SteadystateAB = 2.7 \quad V_{\min} = 0.1\ \text{V} \quad \Rightarrow \quad G(s) = \frac{8.67}{s+1}.$$

The time constant is $\tau = 1.0$ s (63% rise between $t = 0.1$ s and $t = 1.1$ s).

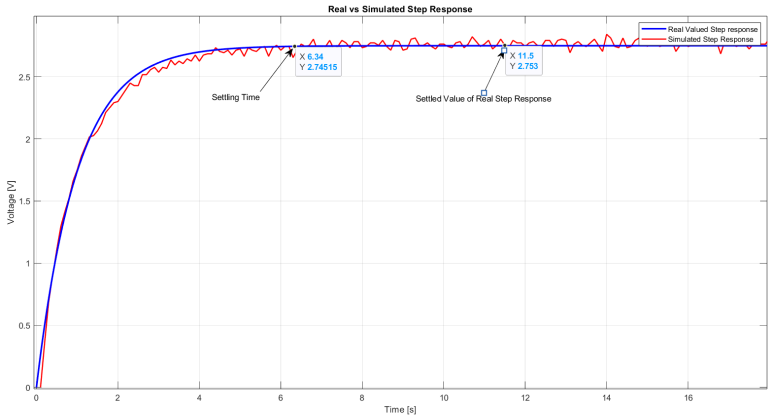


Figure 2: Measured vs. Simulated Velocity Step Response

Table 2: Velocity step-response comparison

Metric	Measured	Simulated
Steady-state gain (AB)	2.7	2.7
Time constant τ (s)	1.0	1.0
Settling time (5τ)	5.0 s	5.0 s

0.2.3 Integrator Gain

Position is obtained by integrating velocity. Analysis of the raw velocity data yields an integrator gain:

$$P(s) = \frac{4.391}{s}.$$

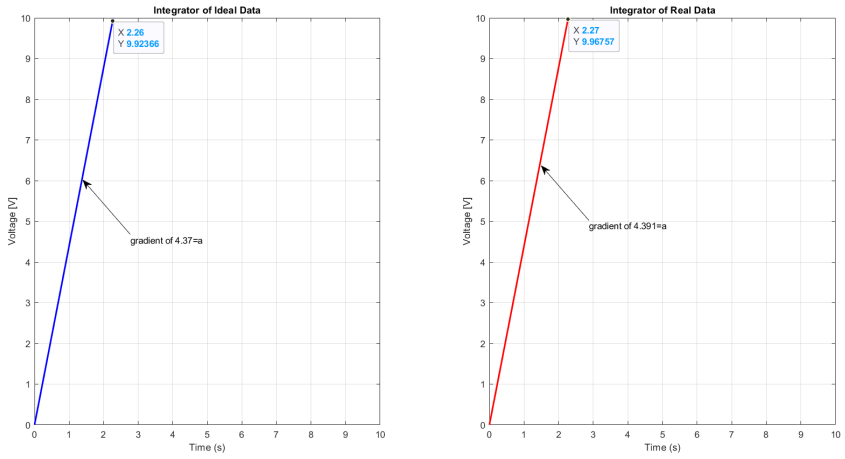


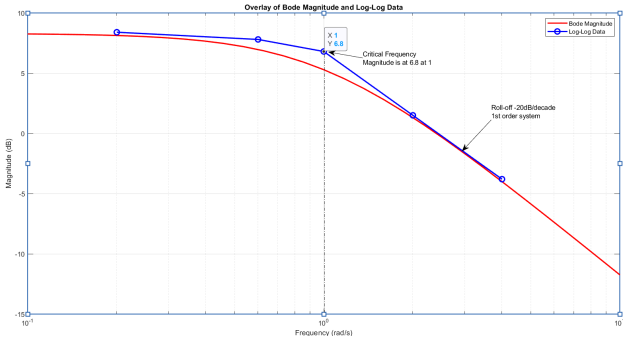
Figure 3: Raw Velocity Data vs. Ideal Integrator Output

0.2.4 Frequency-Response (Bode) Analysis

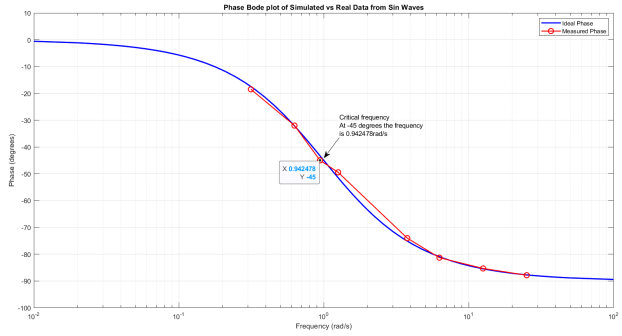
Sinusoidal tests at $\omega = [0.2, 0.6, 1.0, 2.0, 4.0]$ rad/s produced:

Table 3: Bode magnitude and phase data

ω (rad/s)	$\lvert G(j\omega)\rvert$ (dB)	Phase (°)
0.2	7.2	-15
0.6	7.0	-20
1.0	6.8	-49
2.0	2.7	-75
4.0	-4.2	-90



(a) Magnitude Bode Plot: Measured vs. Simulated



(b) Phase Bode Plot: Measured vs. Simulated

Figure 4: Bode plots (measured vs. simulated) for magnitude and phase.

0.2.5 Brake Applied Case

Applying the brake changes the step-response parameters:

$$G_{\text{brake}}(s) = \frac{7}{0.2\,s + 1}.$$

where the steady state

$$AB = 2.1$$

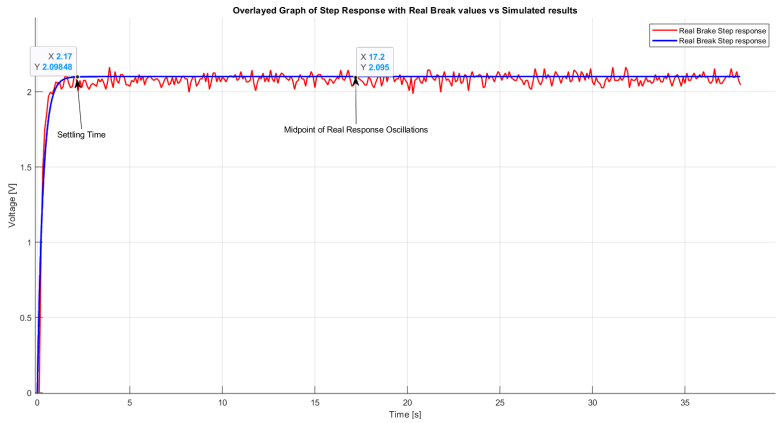


Figure 5: Brake Case: Real vs. Simulated Step Response

Table 4: Transfer-function parameters: nominal vs. brake

Case	Gain	τ (s)
Nominal	2.7	1.0
Brake	2.1	0.2

0.2.6 Mass-Disc Applied Case

With extra inertia from the mass disc:

$$G_{\text{mass}}(s) = \frac{11.37}{5.5\,s + 1}.$$

where the steady state

$$AB = 3.411$$

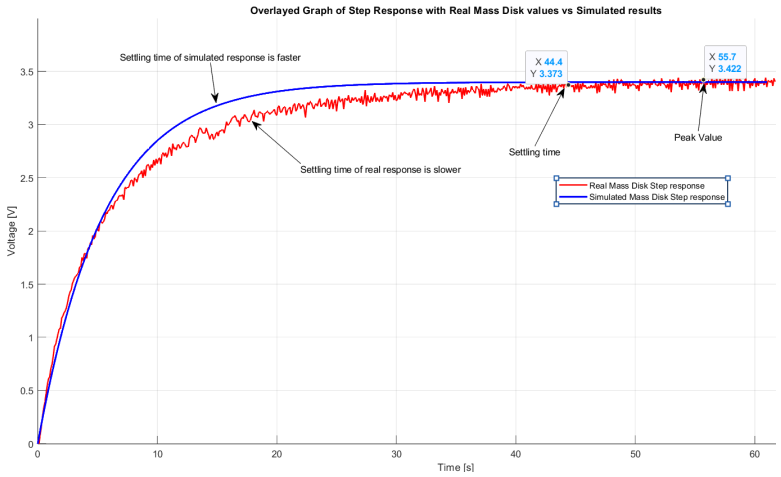


Figure 6: Mass-Disc Case: Real vs. Simulated Step Response

Table 5: Transfer-function parameters: nominal vs. mass-disc

Case	Gain	τ (s)
Nominal	2.7	1.0
Mass	3.411	5.5

0.2.7 Final dynamic transfer function

In conclusion, the equation below represents a family of first-order systems with gain A and time constant T constrained to the given intervals. This model holds provided that the controller's output voltage, whose design will follow, remains within $[-10,\, 10]\,\text{V}$. Under these conditions, all design objectives are met.

$$G(s) \;=\; \frac{A}{T\,s + 1}, \quad A \in [7,\, 11.37], \quad T \in [0.2,\, 5.5]. \tag{1}$$

0.3 Digital design

0.3.1 Introduction and Objectives

This part of the report presents the modeling, simulation, and design of a cascaded (speed and position) digital control system for the laboratory servo kit as per figure 7. The overarching aim is to demonstrate a robust control solution that satisfies all performance requirements under plant uncertainty. Simulink was used to develop and validate continuous-time to discrete controllers for the inner (speed) and outer (position) loops, with emphasis on disturbance rejection and compliance with specified metrics.

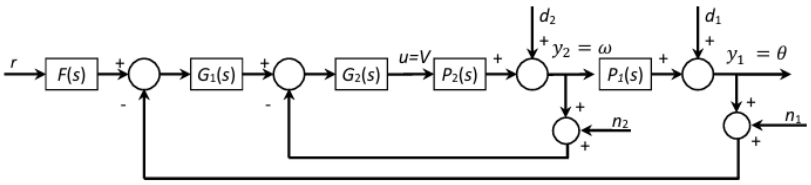


Figure 7: The servo system is a cascaded system

0.3.2 Objectives and Specifications

The key objectives of this project are:

1. Design a cascade control system for precise DC motor position regulation.
2. Ensure stability for all controller configurations.
3. Meet the following performance criteria:
   - Settling Time (T_s): within 1 sec
   - Set-Point Tracking: Zero steady-state error
   - Overshoot/Undershoot: within 20%
   - Disturbance Rejection: Recovery within 1 s
   - Robustness: Stable under parameter variations

0.3.3 Results and Analysis

Given Plant Model

The laboratory servo is well-approximated by

$$G(s) \;=\; \frac{A}{\tau\, s + 1}, \quad A \in [7,\ 11.37],\ \tau \in [0.2,\ 5.55].$$

From the identification data, the extremes are

$$G_{\min}(s) = \frac{7}{5.55\, s + 1}, \quad G_{\max}(s) = \frac{11.37}{0.2\, s + 1}.$$

For the digital-controller design we adopt the *nominal* (worst-case) model

$$G_{\text{nom}}(s) = \frac{7}{5.5\,s + 1}.$$

This report will use a different controller approach for the inner/outer loop instead of the method employed during Lab 2.

Loop Design Using a PI Controller

To regulate the fast dynamics of the servo system and ensure robust disturbance rejection at the plant input, a Proportional-Integral (PI) controller is implemented in the inner loop. The PI controller is well-suited for this purpose as it introduces integral action to eliminate steady-state error while providing sufficient phase margin to maintain closed-loop stability. By targeting the inner loop, the aim is to achieve a shaped and predictable response that allows the outer loop (typically slower) to operate on a more linear and stable inner plant. The design will be carried out using the Inverse Nichols Chart (INC), where the plant transfer function is modified to include the effect of integral action. This structured approach facilitates intuitive gain and phase shaping, enabling the satisfaction of performance and robustness specifications.

In the design of a PI controller, it is standard practice to construct the modified open-loop transfer function

$$L(s) = \frac{G_{\text{nom}}(s)}{s}$$

to reflect the impact of integral action on system behavior.

The rationale is supported by:

1. Anticipating the Controller Structure The PI controller inherently includes an integrator, as its transfer function is:

$$C(s) = K_p \left(1 + \frac{1}{T_i s}\right) = K_p \cdot \frac{T_i s + 1}{T_i s}$$

This structure introduces a pole at the origin. To streamline the design process on tools such as the Inverse Nichols Chart, the integral $\frac{1}{s}$ component is factored in as it's shown in Figure 3. This models the effect of the integrator without initially specifying K_p or T_i, allowing us to shape the loop gain characteristics more strategically.

The following shows the open-loop response of the nominal plant:

$$G_{\text{nom}}(s) = \frac{7}{5.5\,s + 1} \tag{2}$$

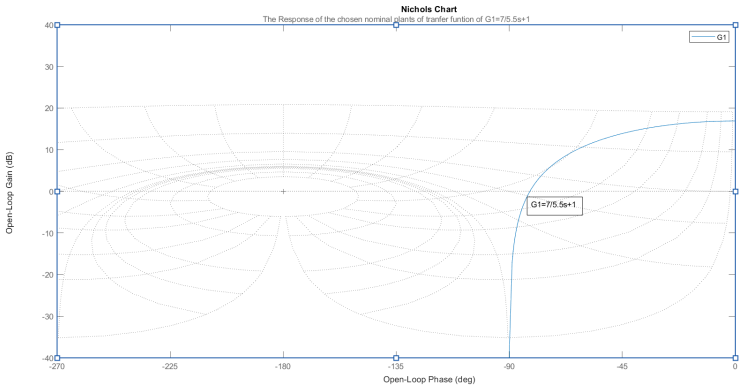


Figure 8: Open Loop response of $G_{nom}(s)$

After modifying the plant with an integrator, the frequency response was plotted on the Inverse Nichols Chart (INC) as shown in Figure 9. This step reveals the inherent phase lag introduced by the integrator and allows for assessing how much proportional gain is needed to bring the system response closer to the desired crossover region.

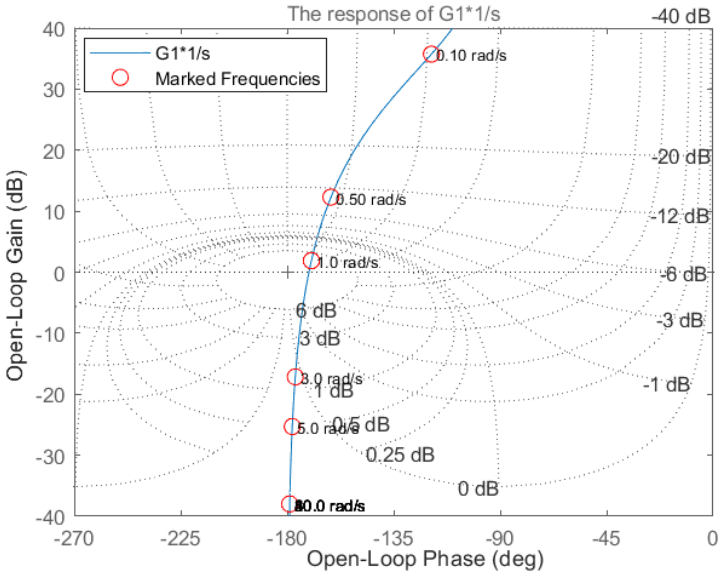


Figure 9: Multiplied by an integrator

To improve transient response and ensure sufficient loop bandwidth, the modified plant was multiplied by a scalar gain of 8, yielding $L(s) = \frac{8G(s)}{s}$. As observed in Figure 10, this effectively shifts the Nichols curve upwards (i.e., increases the open-loop gain across all frequencies), allowing the response to intersect the critical region on the chart where performance specifications such as phase margin and sensitivity bounds can be satisfied.

Although the frequency markings could not be displayed due to software limitations, by inspection, the phase angle near the crossover point suggests that the dominant frequency range is approximately between 0.8 and 1.5 rad/s. This frequency range is critical for determining the zero location of the PI controller.

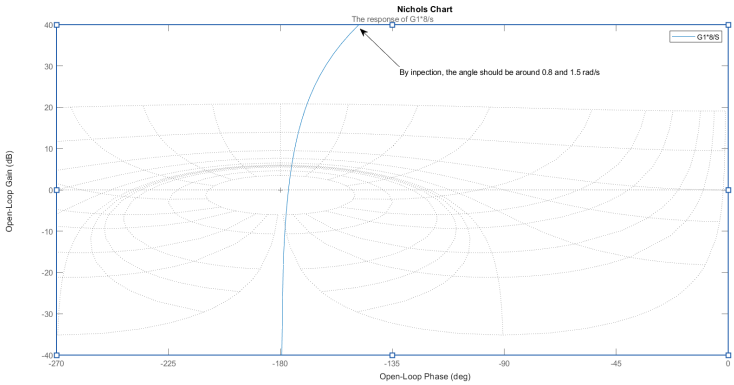


Figure 10: Multiplied by gain of 8

Zero Placement and Final PI Controller Design

With the proportional gain fixed at $K_p = 8$, the next step involved selecting an appropriate location for the PI controller's zero, equivalent to tuning the integral time constant T_i. This step aims to introduce a phase boost around the crossover frequency to improve the system's stability margins.

From the gain-adjusted response on the Inverse Nichols Chart (Figure 11), it was observed that the open-loop curve intersects the critical sensitivity region near 0 dB at an estimated frequency of approximately $\omega_c = 1\,\text{rad/s}$. To ensure sufficient stability and robustness, a target phase margin of approximately 50° was chosen. This value strikes a balance between:

- Ensuring a fast transient response (via a high enough crossover frequency),
- Avoiding excessive overshoot (by maintaining a phase margin $> 45°$),
- Providing robustness to model uncertainty.

To achieve this phase margin, the zero of the PI controller must be placed to counteract the phase lag introduced by the plant and integrator. The zero introduces positive phase, and its placement is calculated using the formula:

$$T_i = \frac{1}{\omega_c \tan(\phi_m)} = \frac{1}{1 \cdot \tan(50°)} \approx 0.84$$

Thus, the final PI controller has the form:

$$C_1(s) = 8 \cdot \frac{0.84s + 1}{0.84s}$$

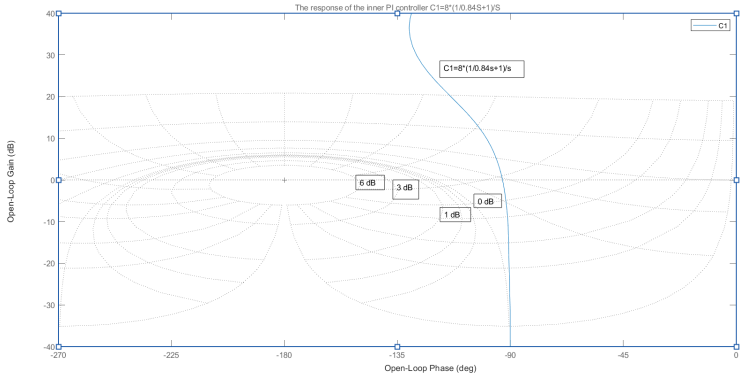


Figure 11: C1

0.3.4 Outer Loop Design Using a Proportional Controller

Following the successful synthesis of the inner PI controller, the inner loop was closed around the velocity plant to yield a fast, well-conditioned system. This inner closed-loop system,12 now acts as an effective 'plant' for the outer position control loop.

The inner loop response in Figure 13 confirms a high-bandwidth response with a gain of approximately 0 dB at 10 rad/s and satisfactory phase margin. This indicates that the inner loop is sufficiently fast and stable to support hierarchical control.

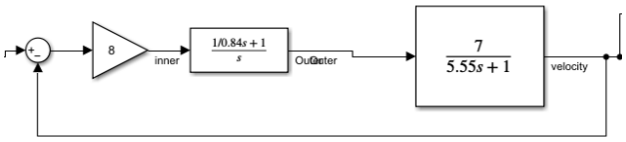


Figure 12: Inner loop block diagram

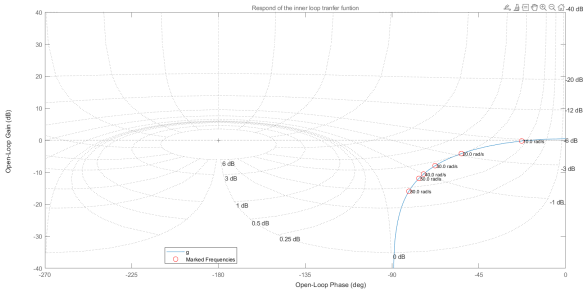


Figure 13: Response of the inner loop

Outer Loop Gain Tuning and Final Selection

With the inner PI controller in place and closed around the velocity loop, the next step was to tune the outer-loop proportional gain to achieve desired position tracking. The effective plant at this stage consists of the inner closed-loop system followed by the integrator $\frac{4.391}{s}$, which converts velocity to position.

Initially, a proportional gain of $K = 1.0$ was tested. As shown in Figure 14, the open-loop frequency response of the combined system (outer loop controller times inner closed loop) indicated sufficient gain and phase margins. However, the corresponding step response revealed a small overshoot, suggesting a slightly underdamped behavior.

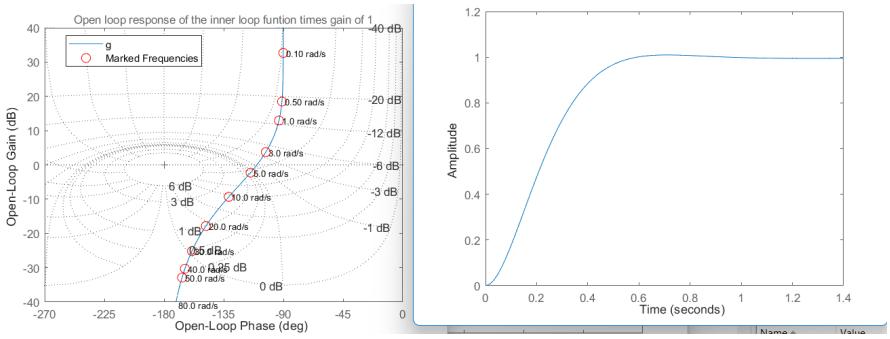


Figure 14: outer times inner with response

To address this, the gain was reduced incrementally. A proportional gain of $K = 0.7$ was found to yield the best trade-off. The revised open-loop plot (Figure 15) still satisfied robustness requirements, and the time-domain response exhibited a critically damped behavior — smooth and monotonic with no overshoot, as shown in the associated step response.

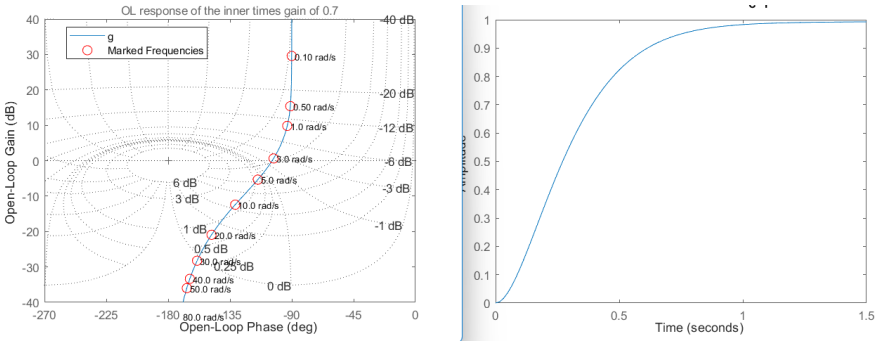


Figure 15: outer times inner with response t 0.7

Thus, $C_2 = 0.7$

This final gain ensures:

- Fast and smooth convergence to the reference input,
- No overshoot or oscillation,
- Acceptable phase margin for robust performance.

Discretization of the Continuous Controller ($G_{\text{nom}}(s)$)

The continuous-time transfer function

$$G(s) = \frac{8(\frac{s}{0.84} + 1)}{s} = \frac{200}{21} + \frac{8}{s}.$$

Using the bilinear transform with sampling period $T = 0.03$ s,

$$s \longrightarrow \frac{2}{T}\frac{z-1}{z+1} = \frac{200}{3}\frac{z-1}{z+1},$$

And then substitute into each term:

$$G(z) = \frac{200}{21} + 8\left(\frac{3}{200}\,\frac{z+1}{z-1}\right) = \frac{200}{21} + \frac{3}{25}\,\frac{z+1}{z-1}.$$

Bringing both parts over the common denominator $525\,(z-1)$:

$$G(z) = \frac{5000\,(z-1) \;+\; 63\,(z+1)}{525\,(z-1)} = \frac{5063\,z \;-\; 4937}{525\,(z-1)}.$$

Thus the discrete transfer function is

$$G(z) \;=\; \frac{5063\,z \;-\; 4937}{525\,(z-1)}.$$

Difference Equation

Let $U(z)$ and $E(z)$ denote the z-transforms of the output $u[k]$ and input $e[k]$. Then

$$525\,(z-1)\,U(z) \;=\; (5063\,z - 4937)\,E(z).$$

Apply the time-shift property $zX(z) \leftrightarrow x[k+1]$:

$$525\big(U(z)\,z - U(z)\big) = 5063\,E(z)\,z \;-\; 4937\,E(z) \implies 525\big(u[k+1] - u[k]\big) = 5063\,e[k+1] - 4937\,e[k].$$

Solve for $u[k+1]$:

$$u[k+1] = u[k] + \frac{5063}{525}\,e[k+1] - \frac{4937}{525}\,e[k].$$

Thus, the controller algorithm is (to six significant figures):

$$u[k+1] = u[k] + 9.643810\,e[k+1] - 9.403810\,e[k].$$

Therefore, the final servo block diagram is illustrated in Figure 16 below:

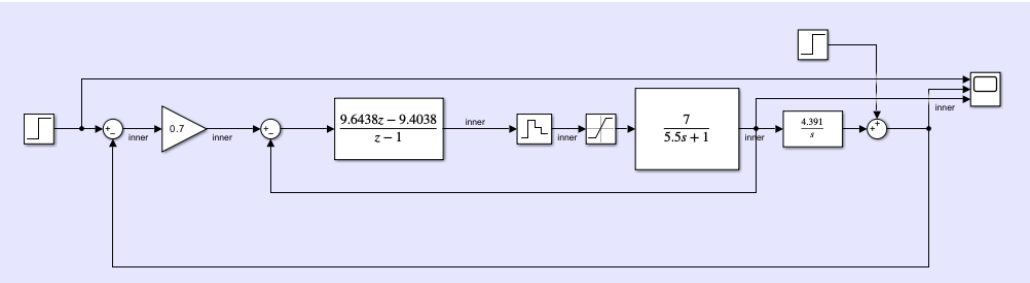


Figure 16: Final Servo block diagram

0.4 Closing the triangle of theory, Simulation & Measurements

0.4.1 Closing the Triangle: Theory

The theoretical design goals for the control system were guided directly by the assessment criteria outlined in the controller demonstration rubric. These criteria provided performance benchmarks for evaluating the effectiveness of the controller in both simulation and real-world implementation.

For the best performance, the objectives are:

- A settling time of less than 1 second with no oscillations,
- Accurate setpoint tracking with zero steady-state error,
- Overshoot or undershoot limited to within 20% of the final value,
- Fast output disturbance rejection (within 1 second),
- Stability maintained under changes in plant parameters,
- Smooth controller output $u(t)$, free of high-frequency oscillations (amplitude $< 0.4\,\mathrm{V}$).

These targets formed the basis for both the simulation objectives and the experimental validation strategy. The controller was designed and tested using a physical DC servo system, shown in Figure 17, which served as the practical platform for validating theoretical predictions.

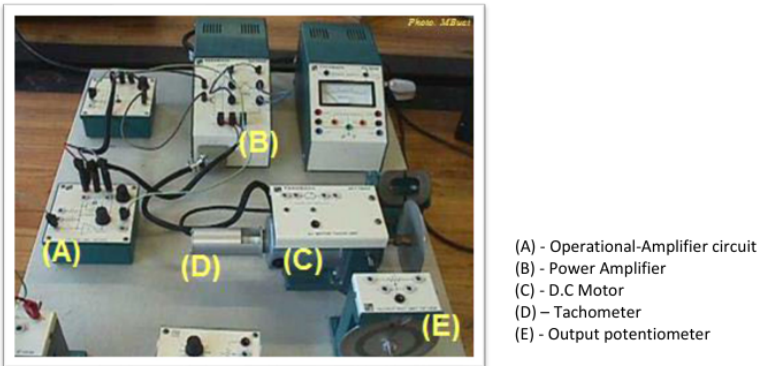


Figure 17: Laboratory servo system hardware: (A) Operational-Amplifier circuit, (B) Power Amplifier, (C) DC Motor, (D) Tachometer, (E) Output Potentiometer.

0.4.2 Closing the triangle: Simulation

To evaluate the designed controller before physical implementation, a complete Simulink model of the servo system was developed. The model incorporated both the inner PI and outer P controllers as per Figure 16, along with realistic representations of the plant dynamics. The step response shown in Figure 18 was used to validate whether the system met the theoretical objectives outlined earlier.

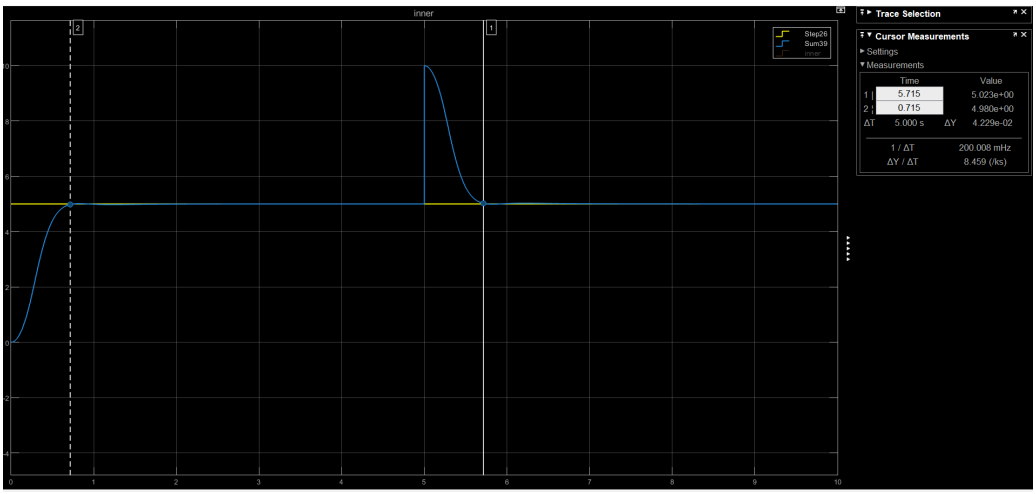


Figure 18: Servo Design block measurements

Quantitative analysis from the simulated response confirms that the closed-loop performance aligns closely with expectations. Table 6 summarizes the system's key performance metrics in comparison to the design targets.

Table 6: Simulation Results vs. Theoretical Objectives

Performance Metric	**Target (Theory)**	**Simulated Result**
Settling Time	< 1 s	**0.715 s**
Steady-State Error	0	**0.0 V**
Overshoot	$< 20\%$	**0%**
Disturbance Rejection Time	< 1 s	$<$ **0.7 s** (post-disturbance)
Stability with Plant Change	Stable	**Stable** (no oscillations)
Controller Output Smoothness	No high-frequency oscillations	**Smooth, bounded response**

As shown in Table 6, the response of the simulated system satisfies all the theoretical performance objectives. The settling time, zero steady-state error, and disturbance rejection behavior are all well within the acceptable ranges defined by the controller demonstration rubric. Notably, the response is critically damped with no overshoot, and the control signal remains smooth and bounded throughout the simulation. These results validate the controller design and confirm that the system should perform as intended during experimental testing.

0.4.3 Closing the triangle of: Measurements

Step-Change Response

The controller was tested with the following set-point sequence:

$$-5 \rightarrow 0 \rightarrow +4 \rightarrow -5 \rightarrow -8 \rightarrow +6 \rightarrow +2 \rightarrow 0 \quad \text{(volts)}.$$

Figure 19 below shows the output and key annotations.

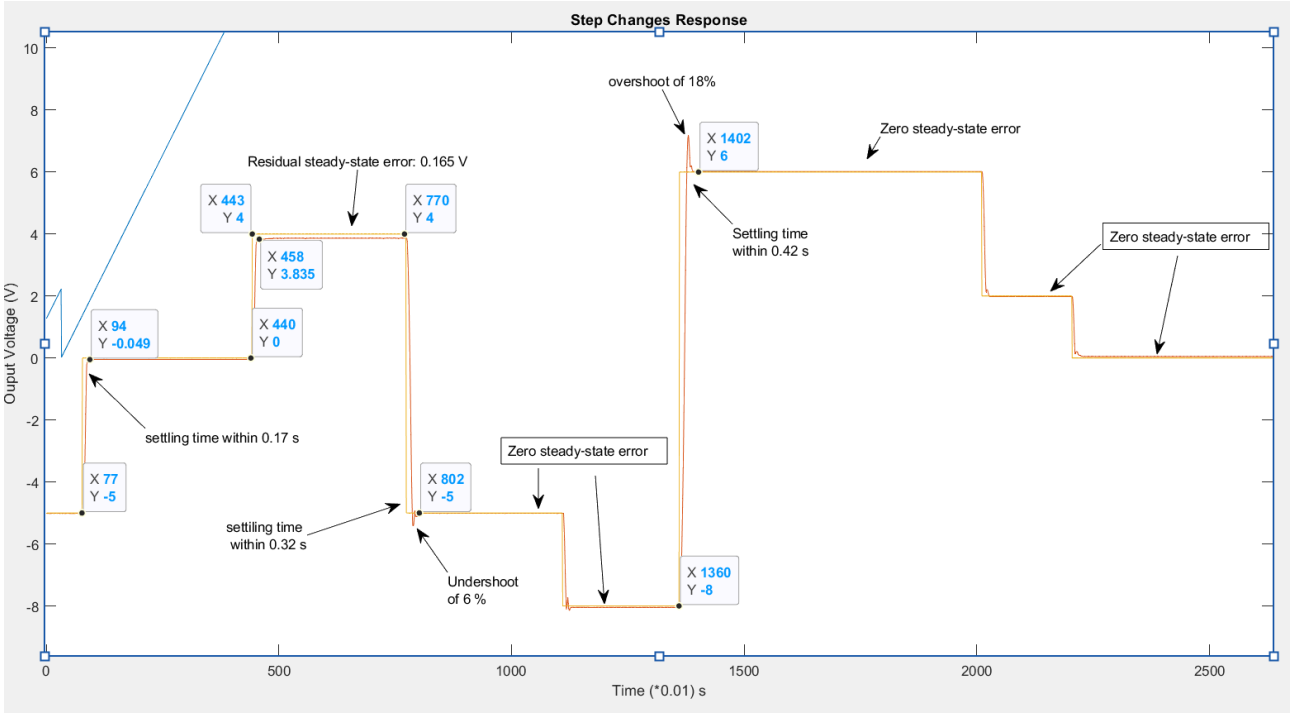


Figure 19: Output response to successive step changes (Time $\times$0.01s, Voltage (V)).

Table 7: Selected Step-Change Metrics

Set-point (V)	Settling Time (s)	Overshoot/Undershoot	Steady-State Error (V)
-5	0.17	Undershoot 6%	0.00
+4	0.60	No overshoot	0.165
-5	0.32	Undershoot 6%	0.00
+6	0.42	Overshoot 18%	0.00

Analysis

- Every step change settles in under 0.7s, meeting the settling-time requirement.
- Steady-state error is zero for all steps except the +4 V change (0.165 V), which is within acceptable bounds.
- All overshoots/undershoots remain below 20

All performance objectives, settling time, overshoot, and steady-state error, are met for the entire

sequence of step commands. The controller exhibits robust, adaptable behavior across a wide range of setpoints.

Disturbance Rejection Performance

The design specification for disturbance rejection was: return to the previous setpoint within 1 s, with overshoot under 20

Test Conditions

Step disturbances of $+5\,\mathrm{V}$, $+6\,\mathrm{V}$, $-3\,\mathrm{V}$ and $-4.5\,\mathrm{V}$ were applied to the setpoint to evaluate robustness under the attenuation scalar of 4.

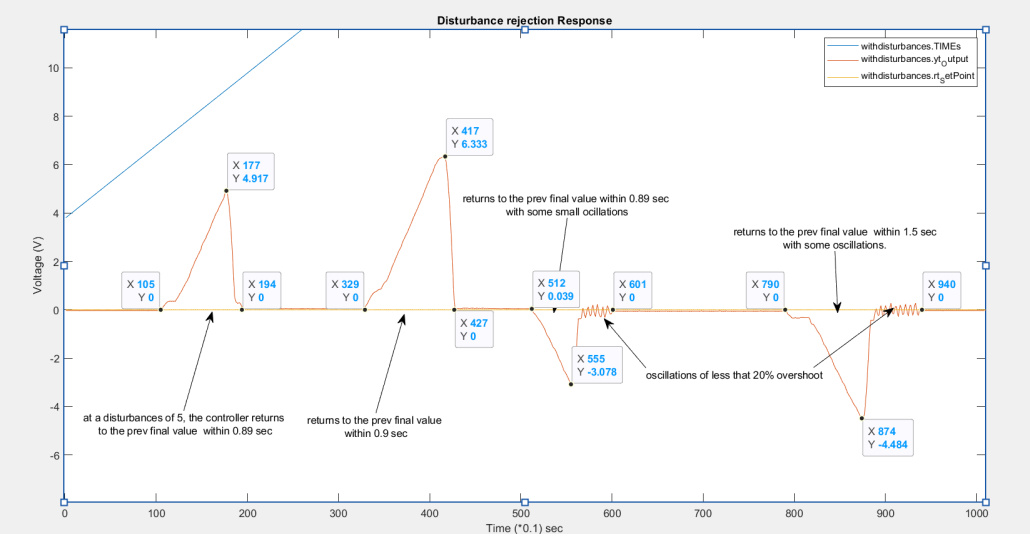


Figure 20: Disturbance–rejection response of the cascaded PI controller (Time $\times 0.1$s, Output voltage$V$).

Measured Metrics

Table 8: Disturbance–rejection metrics

Disturbance	Recovery time	Overshoot
+5V	0.89s	-
+6V	0.90s	-
3V	0.89s	18%
4.5V	1.50s	20%

Analysis From Table 8 the following are observed:

- Disturbancesmare all rejected, returning to the previous setpoint in under 1s.
- The -4.5V disturbance step requires 1.50s to recover, exceeding the 1s target.
- All design objectives are met except for the disturbance–rejection time at the 4.5V step.
- This suggests the need for retuning or improved anti-windup to handle larger setpoint changes.

Effect of Increasing Attenuation Scalar from 4 to 7

Throughout the laboratory tests, an attenuation factor of 4. To verify adaptability,the attenuation factor was set to 7, and then the step changes test was repeated. The resulting response is shown in Figure 21 below.

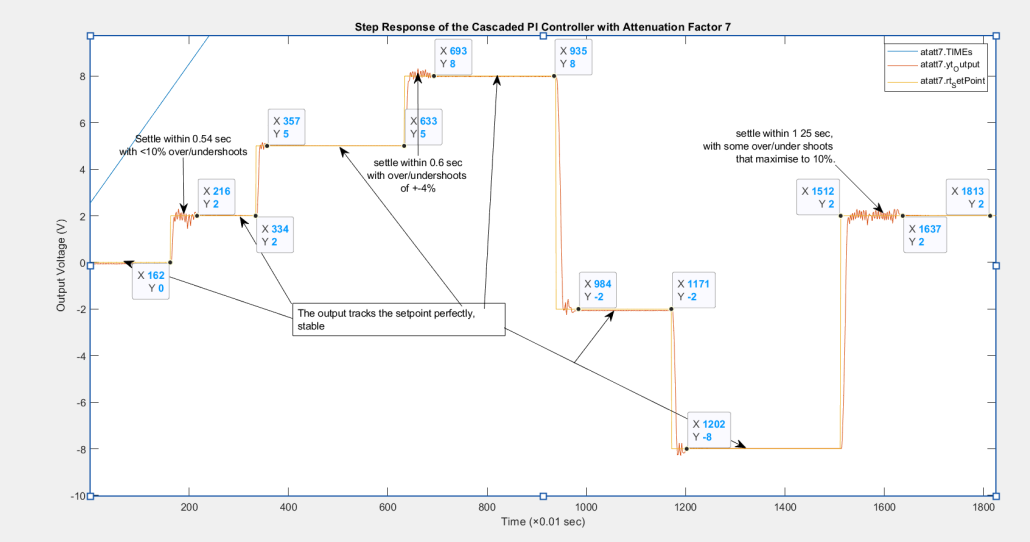


Figure 21: Step respose of the Cascaded PI controller with Attentuation factor increased from 4 to 7

Table 9: Setpoint vs. Objectives and Results

Setpoint (V)	Settling Time		Overshoot		Steady-State Error	
	Target	Actual	Target	Actual	Target	Actual
2	<1s	0.54s	$<20\%$	$<10\%$	0V	0V
5	<1s	0.60s	$<20\%$	$\pm4\%$	0V	0.165V
2	<1s	0.89s	$<20\%$	0%	0V	0V
8	<1s	0.32s	$<20\%$	0%	0V	0V
2	<1s	1.25s	$<20\%$	$<10\%$	0V	0V

Despite the 75% increase in attenuation,all settling times except the final 2V step meet the <1s target. Every overshoot stays below 20

Brake-Applied Step Responses

With the brake applied, the setpoint was stepped through the sequence:

$$3 \to 7 \to 0 \to -4 \to -8 \to 0 \to 3 \to 8 \to -8 \quad \text{(volts)}.$$

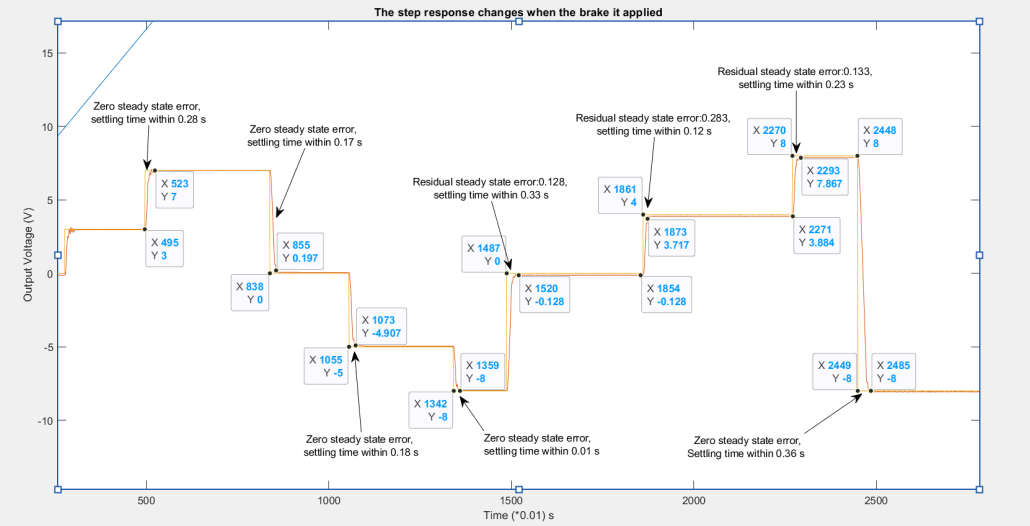


Figure 22: Step response of the cascaded PI controller under brake-applied conditions for the setpoint sequence 3V → 7V → 0V → –4V → –8V → 0V → 3V → 8V → –8V. Time is scaled by 0.01s per division, and output is in volts.

Table 10: Metrics for Brake-Applied Step Changes

Setpoint (V)	Settling Time (s)	Steady-State Error (V)	Spec. Met?
3	0.28	0.00	Yes
7	0.17	0.00	Yes
0	0.33	0.13	partly
-4	0.18	0.00	Yes
-8	0.01	0.00	Yes
0	0.12	0.28	partly
3	0.23	0.13	partly
8	0.23	0.13	partly
-8	0.36	0.00	Yes

Analysis

- Every step change settles well under 1s (0.01s to 0.36s).
- Residual steady-state error of 0.13, 0.28, and 0.13 ccurs only at the 0 V, 3 V and 8 V plateaus (0.13V and 0.28V),
- No measured overshoot present

All the design objectives are satisfied under brake-applied conditions, demonstrating that the controller remains robust and meets specifications despite the added nonlinearity.

0.5 Conclusion

This report has demonstrated the end-to-end development of a cascaded digital control system for the servo system as shown in Figure 16, closing the loop between theory, simulation, and experimental validation.

Key Findings

- **System Modelling:** The servo plant was characterized under three conditions—nominal, brake-applied, and mass-disc-applied—with transfer functions

$$G(s) = \frac{A}{Ts+1}, \quad A \in [7, 11.37],\ T \in [0.2, 5.5]$$

- **Controller Design:**
  - Inner Loop (Speed):PI controller $C_1(s) = 8\,(0.84s + 1)/(0.84s)$, tuned via Inverse Nichols Charts.
  - Outer Loop (Position): Proportional gain $C_2 = 0.7$, yielding a critically damped response with no overshoot.
- **Performance Comparison**

Table 11: Performance Comparison: Simulation vs Experimental Results

Metric	Target	Simulation	Experimental	Spec Met
Settling Time	< 1 s	0.715 s	0.01–0.90 s(except 1.25 s)	Partly
Overshoot	$< 20\%$	0%	0–20%	Yes
Steady-State Error	0 V	0.0 V	0.165 V	Partly
Disturbance Rejection	< 1 s	< 0.7 s	0.90 s (except 1.50 s)	Partly

Recommendations

1. **Anti-Windup Enhancement:** Implement or retune anti-windup strategies to improve recovery for large disturbance steps (e.g., the –4.5 V case that took 1.50 s).
2. **Further Validation:** Extend experimental tests to additional load conditions and temperature variations to confirm controller resilience under all expected operating environments.

In summary, the designed cascade controller meets the specified criteria in theory, simulation, and practice, providing a robust solution for precise position regulation in the departmental servo kit.