Sheet 3

Exercise 3-1:

A MIPS datapath has latencies of 250 ps, 350 ps, 150 ps, 300 ps, and 200 ps for the IF, ID, EX, MEM, and WB stages respectively. Its instructions are broken down as 45% ALU operations, 20% BEQ operations, 20% LW operations, and 15% SW operations. Answer the following questions:

a. What is the clock cycle time in a pipelined and non-pipelined (single cycle) processor?
b. What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
c. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?
d. Assuming there are no stalls or hazards, what is the utilization of the data memory?
e. Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?
f. Instead of a single-cycle organization, we can use a multi-cycle organization where each instruction takes multiple cycles but one instruction finishes before another is fetched. In this organization, an Instruction only goes through stages it actually needs (e.g., SW only takes four cycles because It does not need the WB stage). Compare clock cycle times and execution times with single cycle, multi-cycle, and pipelined organization.

Exercise 3-2:

The clock cycle of a pipelined MIPS that does not support forwarding is 250 ps. If full forwarding is added, the clock cycle is increased to 300 ps. If instead only ALU-ALU forwarding is added (i.e., no forwarding from the MEM to EX stage), the clock cycle is increased to 290 ps only. Answer the following questions, considering the code sequence below:

```
LW    R3, 0(R6)
OR    R1, R2, R3
OR    R2, R1, R4
AND   R1, R1, R2
```

a. Indicate data dependences and their type (i.e., Read-after-write (RAW), write-after-read (WAR), or write-after-write (WAW)).
b. Assume there is no forwarding in this pipelined processor, indicate hazards and add No-operation (**NOP**) instructions to eliminate them. Note **NOP** is a MIPS instruction.
c. Assume there is full forwarding, indicate hazards and add **NOP** instructions to eliminate them.
d. Assume there is ALU-ALU forwarding only, indicate hazards and add **NOP** instructions to eliminate them.
e. What is the total execution time of this instruction sequence without forwarding, with full forwarding, and with ALU-ALU forwarding only? What is the speedup achieved by forwarding (both cases) with respect to the no-forwarding case?

Exercise 3-3:

Based on the MIPS pipeline implementation you studied, what are the control signals that have to be stored in the ID/EX pipeline register? Group them based on the stage they are needed in.

Exercise 3-4:

Based on the MIPS pipeline implementation you studied, what are the sizes of the pipeline registers? Justify your answer.

Exercise 3-5:

Assuming the MIPS ALU inputs are named A and B, what is the condition for forwarding data from the MEM/WB register to input A?

Exercise 3-6:

Assuming the MIPS ALU input sources are controlled using the ForwardA and ForwardB signals as studied, what are the values of ForwardA and ForwardB at each clock cycle during the execution of the following program? How many clock cycles are needed for executing this entire program?

```
ADD $3, $1, $2
ADD $3, $3, $4
SUB $1, $5, $3
ADD $0, $3, $1
ADD $1, $5, $0
```