**Additional work done which was pending…**

Last time due to some problem with Pex simulation and netlist extraction, I couldn’t submit it.

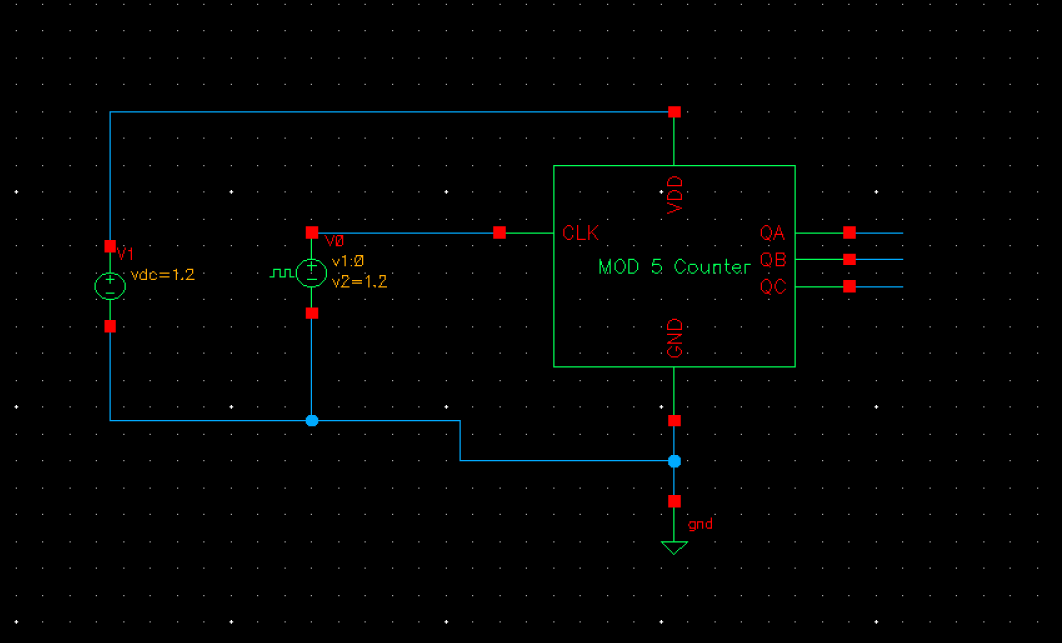
But now its done ,and ready!

**Brief overview of what was done till last submission:**

* All the scpecifications of the design were met.
* Was made of acceptable width (layout).
* Modulo 5 (Synchronous) counter with 1400nm with was successfully made using umc 65nm technology
* DRC errors (except the density ones) were cleared!
* Not only for counter but rest of the components were also free from any error.

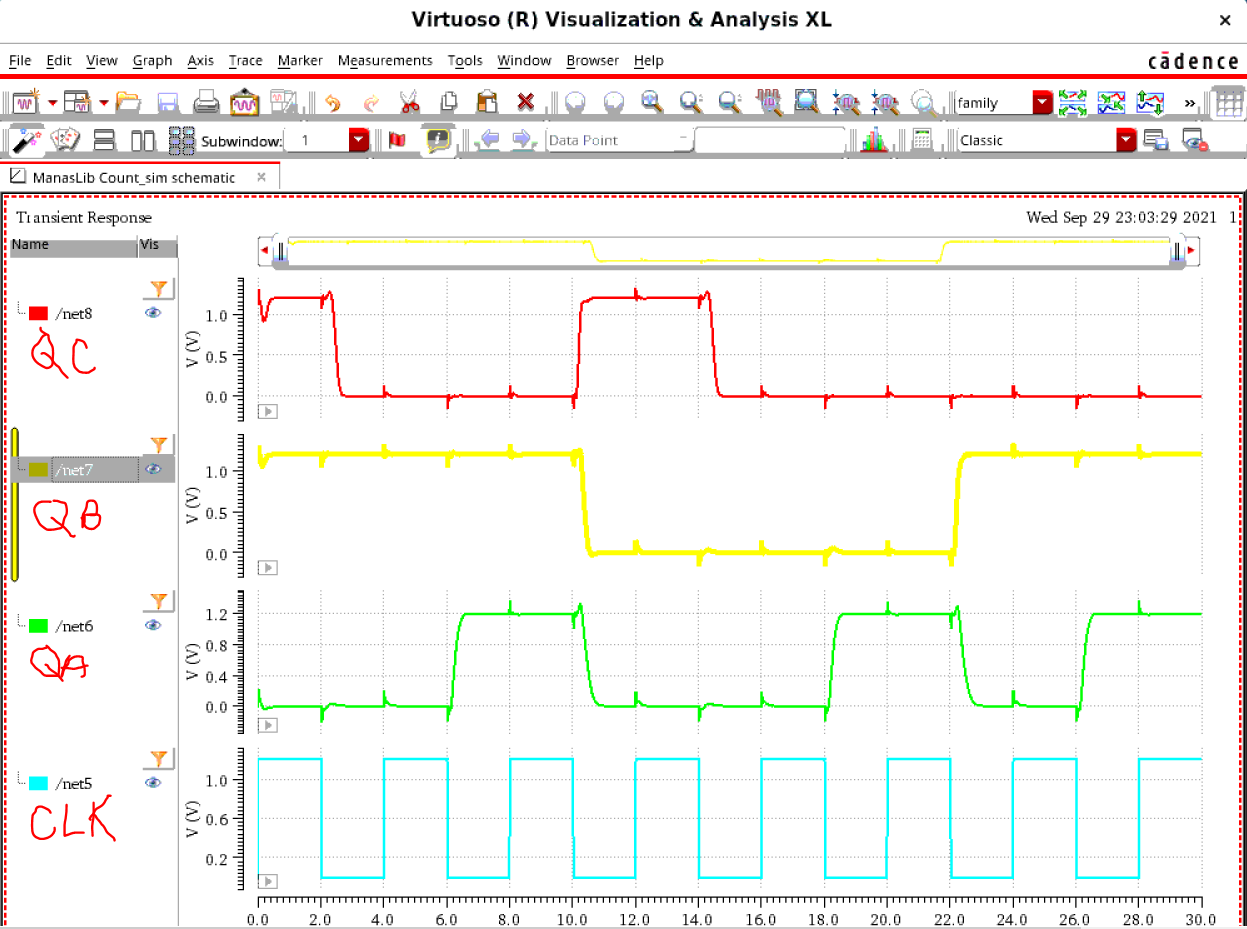
**The Parasitic Extraction and simulation of Counter:**

Here is the picture showing the schematic of the simulation:



The symbol of the mod 5 counter was placed in the Calibre environment, and simulated.

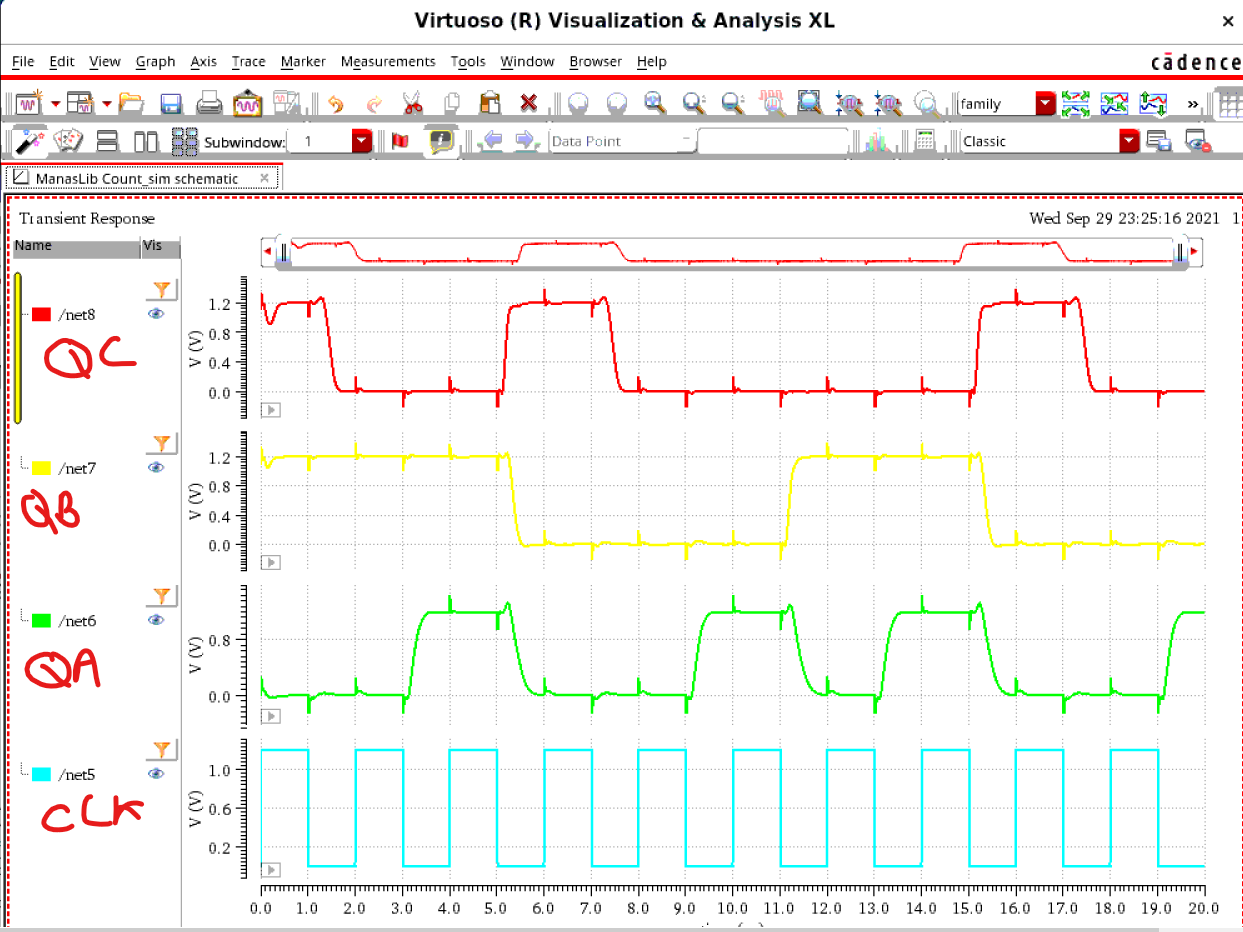
Here are the results of the simulation, when triggered with a 250MHz clock, as per the requirement :



As we can see it clearly shows the states of the counter at that frequency! (The time scale below is in nsec)

This proves that the counter satisfies the criteria

Results when the frequency was doubled :



Hence, the Counter is still working great at even double the frequency specified.

**Maximum frequency:**

It is an iterative process, and on random testing, the Maxm. Frerq. Seems to be around 2GHz, since the outputs started messing.