BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani
Pilani Campus
AUGS/ AGSR Division

SECOND SEMESTER 2020-21
COURSE HANDOUT

Date: 04.01.2020

In addition to part I (General Handout for all courses appended to the Time table) this portion gives further specific details regarding the course.

Course No : **EEE F477**
Course Title : **Modeling of Field-Effect Nano Devices**
Instructor-in-Charge : **Dr. Satyendra Kumar Mourya**

1. Course Description: Physical principles and MOS transistor phenomena, developing models including effective mobility, temperatures effects, and source/drain resistances. small-dimensional effects, impact ionization, velocity saturation drain-induced barrier lowering (DIBL), ballistic operation, polysilicon depletion, quantum effects, gate-tunneling currents, gate-induced drain leakage (GIDL) , fundamentals of low-power (low-voltage) CMOS design issues; the threshold voltage shift (due to SCE) , increased leakage power, sources of power , SOI MOS, (PDSOI, FDSOI) , multigate (MG) MOSFET, electrostatic integrity and short channel control, quantum mechanical origin, basics of BSIM CMG, compact models for multigate MOSFETs , mobility in multiple gate devices, improvement of the mobility ,crystallographic orientations, strained Si channels.

2. Scope and Objective of the Course:

This course is designed specifically for undergraduate students who have done an 'Electronic Devices' course earlier. This course will enable them to pursue modelling techniques of MOS structures, beginning with MOSFETs. This will be very helpful for those who would like to do further studies or want to work in the area of semiconductor devices and VLSI. As added perks, practical research-oriented case studies shall be taken up with special emphasis on article writing for journals and conferences. This course is organized in five modules which covers various aspects of device modelling of long channel and short channel MOSFETs and advanced field effect devices. First module includes basics of field-effect devices: physics and technology and is followed by the second module i.e. metal-insulator semiconductor capacitor. The third module is about MOSFET models and short channel effects while the fourth module addresses SOI and multigate devices. The fifth and final module consist of basic physics and applications of TFETs and memristors.

3. Text Books:

(1) Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices, *2nd ed.*, Cambridge University Press.

4. Reference Books:

R1. Jean-Pierre Colinge ,FinFETs and other multi-gate transistors, Springer.

R2. James D. Plummer, Silicon VLSI Technology, Pearson Education India, 2009

R3. R. S. Muller and T. I. Kamins, Device Electronics for Integrated Circuits, 3rd ed.,Wiley, New York.

R4. Paolo Antognetti and Giuseppe Massobrio, Semiconductor device modelling with SPICE, McGraw – Hill

R5. Yannis Tsividis & Colin McAndrew, Operation and Modeling of the MOS Transistors, 3rd ed, Oxford University Press.

5. Course Plan:

Module	No. of lectures	Topic	References	Learning Outcome
Basics of Field-effect devices: Physics and Technology	1-3	Introduction to the Field Effect Nano Devices, Evolution and Projections, Fabrication, CMOS Processes, Isolation techniques: STI, LOCOS, Tip or extension (Lightly Doped Drain) Formation, Interconnects	T.B. 1.1-1.3, (R2 2.1-2.4)	Technology process flow and foundry status, quick recap of semiconductors basic (to provide a connect with prerequisite course), Expertise in Metal-Semiconductor contacts
	4-7	Metal – semiconductor Junction, Schottky and Ohmic contacts, Band Diagrams, Schottky Barrier Diodes with surface states, Thermionic emission	T. B. 2.4 (R3)	
Metal-Insulator Semiconductor	8-9	MOS capacitors: Surface potential, Accumulation, Depletion and Inversion, Band Diagram, Modelling of surface potential and charge distribution in Silicon	T.B. 2.3.1-2.3.2 (R5)	Understanding of MOS systems in flat band, threshold voltage and subthreshold slope. Effect of interface state density, mobile ions and interface charges on the performance of MOS Devices.
	10-11	Capacitances in MOS Structure: Accumulation, Depletion and Inversion; LF, HF, Deep Depletion mode. Polysilicon-Gate Work Function and Depletion Effects. MOS under non-equilibrium and Gated Diodes	T.B. 2.3.3-2.3.5 (R5)	
	12-14	Oxide charges, C-V characteristic of the MOS Capacitor, Interface states and trap density.	TB: 2.3.6-2.3.7 (R5)	

MOSFET Models and Short channel effects	14-19	Long Channel MOSFETs, gradual channel approximation, MOSFET Level-1 model, Bulk Charge Models (Level-2), source/drain resistances	T.B. 3.1, (R4 4.2-4.5)	Effect of scaling on MOSFET performance, Importance of high-*k* dielectrics, Physical and Empirical device models and its applications
	20-23	SCE (Short Channel Effects), Drain Induced Barrier Lowering (DBE), Constant Voltage and Constant Field scaling	T.B. 3.2.1	
	24-27	High-*k* dielectrics, High Field effects: Velocity Saturation, Impact Ionization and Avalanche breakdown, Tunneling: band to band tunneling, Fowler-Nordheim Tunneling, Direct Tunneling, Trap assisted Tunneling, CMOS leakage current, leakage power	T.B. 2.5, 3.2 R.P. [3]	
SOI and Multigate Devices	28-30	Partially depleted and fully depleted SOI CMOS. Strained Silicon Channel, source drain engineered MOSFET	T.B. 10.1	Students will learn about device physics of, State of art MOS Devices including SOI, Fin-FET, CNTFET and TFT and also will be able to use SPICE empirical models for circuit simulations
	31 - 36	Introduction to Electrostatic Integrity, FinFETs and other Multi Gate Transistors, Introduction to BSIM CMG model	T.B. 10.3 (R1)	
Device Physics of TFETs, SET, and Memristors	37-40	Tunnel Field Effect Transistors, Memristors	Research Papers*	

6. Evaluation Scheme:

Component	Duration	Weightage (%)	Date & Time	Nature of component (Close Book/ Open Book)
Mid-Semester Test	90 Min.	30	<TEST_1>	Closed Book and/or Open Book
Comprehensive Examination	2 h	40	<TEST_C>	Closed Book and/or Open Book
Assignments/Seminars		15	TBA	Open Book
Quizzes		15	Surprised quizzes	Closed Book and/or Open Book

7. Chamber Consultation Hour: Will be announced in the class.

8. Notices: Notices will be put up on the EEE Department Notice Board and/or Nalanda.

9. Make-up Policy: Make-up will be allowed for genuine cases. Prior application should be sent for seeking the same. For surprise quizzes and assignments, make up will not be permitted.

10. Note (if any):

Instructor-in-charge
Course No. EEE F477