BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani
Pilani Campus
AUGS/ AGSR Division

SECOND SEMESTER 2020-21
COURSE HANDOUT

Date: 15.01.2021

Course No : **CS F342**

Course Title : **Computer Architecture**

Instructors incharge : S Gurunarayanan

Instructor (Lab) : K Ravi Teja

1. Scope and Objective:

This course aims at introducing the concept of computer architecture and organization. It involves design aspects, and deals with the current trends in computing architecture. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will also be discussed.

2. **Learning outcomes:**

- Understand various architectural techniques used in implementation of complex logic functions
- Apply these techniques in building different computing architectures
- Analyze different performance metrics of different computing architectures
- Design associated systems resources to achieve proportional increase in performance.

3. Text Book:

(T1) Patterson, David A & J L Hennessy, *Computer Organization& Design*, Elsevier, 5th Ed., 2017.

(T2) Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson Education Asia, 2nd Ed. 2006.

4. Reference Books:

(i) J.L. Hennessy & D.A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kauffmann, 6th Ed, 2019.

5. Course Plan:

Lecture No.	Topics to be covered	Reference to T1
01	Introduction	Ch. 1.1-1.3.
02	Introduction to Performance metrics of computing architectures	Ch. 1.5-1.10
03, 04	MIPS Architecture & Instruction Set	Ch. 2

	Overview of different classes and formats of MIPS instruction set	
05	Computer Arithmetic: Building hardware structures	Ch. 3.1 – 3.5
06,07,08	Data path Design: Building using functional blocks	Ch. 4.1 – 4.4
09,10	Control Hardware: FSM based Design	Appendix – D
11,12,13	Exceptions & Microprogramming	Ch. 4.9
14,15	Floating Point Arithmetic: Hardware Architectures	Ch 3.6 – 3.10
16,17	Role of Performance	Ch. 1.4
18	Memory organization- Introduction	Ch5.1
19, 20	Cache Memory Organization: Mapping Schemes	Ch.5.2
21, 22, 23	Cache Performance	Ch. 5.3
24, 25	Pipelining – Design Issues	Ch. 4.5 – 4.6
26, 27	Data Hazards	Ch. 4.7
28,29	Control Hazards	Ch. 4.8
30,31	Static Branch Prediction	Class notes
32,33,34	Dynamic Branch Prediction	Class notes
35,36	I/O Organization	Ch. 6
37-40	Advanced Concepts in pipelining	Ch. 4.12

6. Evaluation Scheme:

EC No.	Evaluation Component	Duration (Min)	Maximum marks	Date & Time	Remarks
1	Mid Semester Test	90	60	Will Be announced through LMS	Open Book
2	Lab/Assignments **	-----	60	Will be announced	Open Book
3	Comprehensive examination	180	80	6/5 FN	Open Book/Closed Book

** Details will be announced in the class & on course web page.

Text book **T2** will be used for Lab Assignments.

7. Chamber Consultation Hours: Mon: 4PM to 5 PM

8. Notices: Notices regarding the course will be put up on the LMS.

Instructor - in - charge

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