BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, Pilani
Pilani Campus
AUGS/ AGSR Division

SECOND SEMESTER 2020-21
COURSE HANDOUT

Date: 16.01.2021

In addition to part I (General Handout for all courses appended to the Time table) this portion gives further specific details regarding the course.

Course No : **CS/EEE/INSTR F241**

Course Title : **Microprocessors Programming and Interfacing**
Instructor-in-Charge : **Dr. Nitin Chaturvedi**
Instructor(s) : **Dr. GSS Chalapathi**
Tutorial Instructors : **Devesh, Vinay, Pawan, Satendra, Chalapathi, Nitin, Rahul**
Practical Instructors : **Puneet, Ziyaur, Ritesh, Suraj, Radha, Abheek, Kanika, Poonam,**
: **Prannay, Praveen, Sankalp, Nishant**

1. Course Description: Programmers model of processor, processor architecture; Instruction set, modular assembly programming using subroutines, macros etc.; Timing diagrams; Concept of interrupts: hardware & software interrupts, Interrupt handling techniques, Interrupt controllers; Types of Memory & memory interfacing; Programmable Peripheral devices and I/O Interfacing; DMA controller and its interfacing: Design of processor based system. This course will have laboratory component.

2. Scope and Objective of the Course: This course is a basic introduction to processor ISA, Assembly programming, Computer & Embedded Architecture. Intel 80x86 is used as a platform through the course. 8086 - 80486 Programmers model of processor, processor architecture; Instruction set, modular assembly programming using subroutines, macros etc.; Timing diagrams; Concept of interrupts: hardware & software interrupts, Interrupt handling techniques, Interrupt controllers. Types of Memory & memory interfacing. Programmable Peripheral devices and I/O Interfacing, DMA controller and its interfacing. Design of processor based system.

3. Text Books: Barry B Brey, The Intel Microprocessors .Pearson, Eight Ed. 2009.

4. Reference Books: Douglas V Hall, Microprocessor and Interfacing, TMH, Second Edition.

5. Course Plan:

Module No.	Lecture Session	Lecture Session	Reference (Text book)	Learning outcomes
1	1	Compute Architecture, Memory & I/O organization, CISC/RISC processors	Chapter 1	**Learn:** Introduction to Microprocessor and Microcomputers
1	2-3	Programmer's Model	Chapter 2	**Learn:**Microprocessor & its architecture
1	4-6	Addressing Modes	Chapter 3	**Learn:**Assembly Programming
1	7-16	Instruction Set & ALP	Chapter 4-6, 8	**Learn:**Assembly Programming

1	17-19	Pin Out, Modes of operation, Clocking, Buses	Chapter 9	**Learn:**8086/8088 Hardware Specifications
1	20-23	Memory Devices, Address Decoding- Memory Interface 8086- 80386	Chapter -10	**Learn:**Memory Interface
2	24	Basic I/O interfacing (I/O mapped I/O and Memory mapped I/O) I/O port address decoding, Protected Mode	Chapter 11.1, 11.2	**Learn:**I/O Interfacing
2	25-27	8255	Chapter 11.3	**Learn:**Programmable Peripheral Devices
2	28-29	Types of interrupts, Vector tables, Priority Schemes	Chapter 12.1, 12.2,	**Learn:**Interrupts
3	30-31	8259	Chapter 12.4	**Learn:**Interrupt Controller
3	32-34	8253/8254	Chapter 11.4	**Learn:**Programmable Timer
3	35-36	ADC, DAC, DMA	Chapter 11.6	**Learn:**Converters
4	37-39	Basic Operation, 8237, Shared Bus, Disk Memory Systems, Video Displays	Chapter -13	**Learn:**DMA controller
4	40-41	Processor based system design	Chapter 15	**Learn:**System Design

6. Evaluation Scheme:

Component	Duration	Weightage (%)	Date & Time	Nature of component (Close Book/ Open Book)
Mid-Semester Test	90 min.	105 (35%)	March, 2021	CB/OB
Lab (Regular)	120 min.	75 (25%)	Regular	Open Book
Comprehensive Examination	120 min.	120 (40%)	May, 2021	CB/OB
Total		300 (100%)		

7. Chamber Consultation Hour: To be announced in the class

8. Notices: Will be displayed on Nalanda Notice board

9. Make-up Policy: Make up will be allowed for genuine cases. No make up for Lab.

10. Note (if any): A student who scores less than 20% marks will be awarded NC.

Instructor-in-charge
Course No. CS/EEE/INSTR F241