# DESIGN ASSIGNMENT

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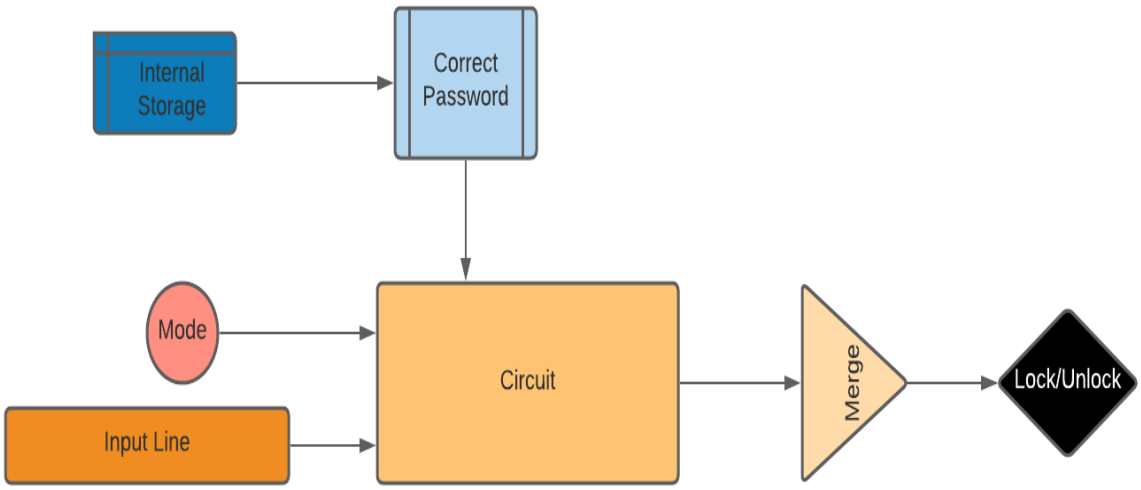
**Problem Statement:** *Design a key operated gate locking system. Only those people who have the password can unlock the gate. The password must at least be 4 BCD digits long.*

# CONTENTS

# TOP LEVEL BLOCK DIAGRAM




Circuit contain of a main logic block, a mode input, input line providing user input password for verification, a merge block which takes result from password verification and mode and make a decision to lock or unlock the block. As a design choice we are loading the correct password stored in internal memory in separate memory elements which will be used for operations. Reason for such design choices will be evident in further sections.

# DESIGN PRINCIPLES AND ASSUMPTIONS

While designing the circuit main motive was to prepare a design which during any fault in circuit can provide user the functionality to disengage the circuit to keep the system locked. Major objective was to ensure that during error or improper working circuit should not allow wrong password.

Design Assumptions are listed below:

- Inputs to our circuit is 28-bit (7-bit for each character or digit) sequence coming after operations in Sensors and ACD.
  Eg. If the entered password is 9#$1 then:
  9 will get converted as 0001001
  # will get converted as 0100011 (Binary value of 35)
  $ will get converted as 0100100 (Binary value of 36)
  1 will get converted as 0000001
  And input sequence will be in following order from right to left
  0001001 0100011 0100100 0000001
- Circuit will always remain in LOCKED state ie; output 1 until the working signal is sent(**MODE = 1**) and correct password is provided.
- Circuit will continue to remain in LOCKED state ie; output 1 irrespective of input password.
- If any user who entered the correct password unlocks the signal that after completion of job a sensory input will be sent as feedback to MODE which will set it to 0.
- No password whether correct or incorrect can send unlock signal of output 0.
- Input signal carrying the user input password must be synced with system clock ie, each bit comes at the active edge of system, in simulation that is positive edge.

# REASONS FOR ASSUMPTIONS

- For input 7-bit for is selected for one character or digit as it gives additional feature of decimal 32-126 ASCII characters.
- MODE is kept to server following functions:
    - ✓ Ensuring that circuit remains LOCKED and all components within this design block get reset and disable signal.
    - ✓ Ensure each that each user gets sufficient time to complete task after unlock.
    - ✓ Can be used as kill switch which when set to 0 system is on complete lockdown with no password whether correct or incorrect can unlock it. (During malfunction this can cutoff the input from output keeping circuit locked).

# WORKING LOGIC

Input of each character is converted into 7-bit binary and compared to binary codes of correct characters in bitwise manner. We use the fact that XOR gate can be used to find different bits.

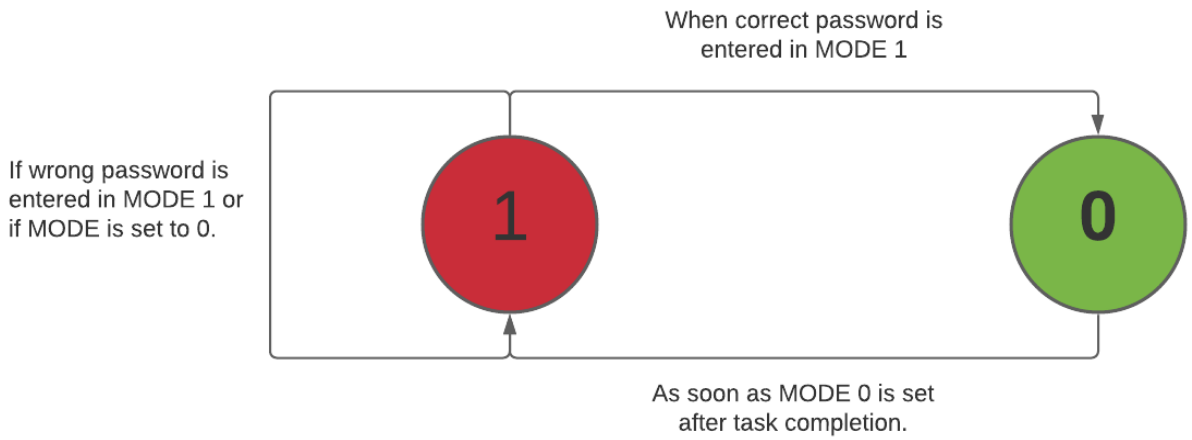
## LOGIC:

$A \oplus B$

| Inputs | | Outputs |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

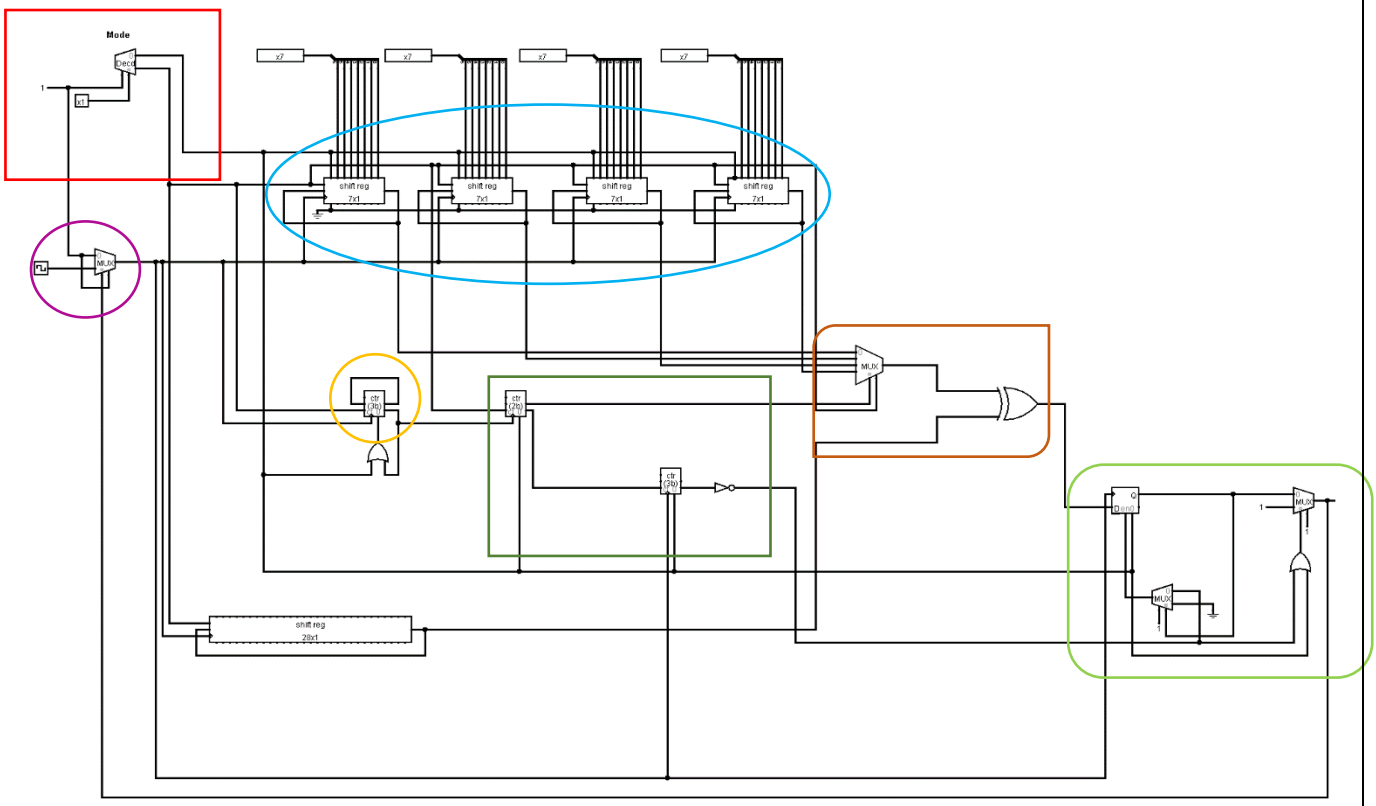
It is 1 when A and B are different.

If output is 1 it means LOCK and output 0 means unlock.



# CIRCUIT IMAGE

This image is attached for reference while analysing pin-out diagrams. There are some changes in connections in hardware implementation due to difference between simulation tools and ICs available in market.




For clarity we are splitting the block diagrams with color codes and components required for each block are written in next section.

Datasheets of each IC are attached with the project.

In the main figure we can see a 28-bit shift register in bottom left but that is not part of our logic, it was a tool which we used from Logisim to represent input line and show how our circuit will work with user input, that is representation of an input line which provides us the user entered password according to our design assumptions.

Similarly, above registers we can see some Logisim input pins also, they are representing the memory where correct password is being stored, our 7-bit registers can be used to store them but we added those connections to provide convenience for other features such as password reset which need changes in the storage. Main objective was to protect our circuit from other circuit in case of any malfunction in those blocks.

# LIST OF COMPONENTS

- Block 1
  - 1:2 Decoder [SN74LVC1G19] (Quantity: 1)
- Block 2
  - 2:1 Multiplexer [SN74LVC2G157] (Quantity: 1)
- Block 3
  - D-Flip Flop [SN74LVC1G74] (Quantity: 28)
  - 2-Input Nand Gate [SN74LVC1G00] (Quantity: 28)
- Block 4
  - 4-Bit Counter [SN74F163A] (Quantity: 1)
  - 2-Input And gate [SN74LVC1G08-Q1] (Quantity: 2)
  - 2-Input Or gate [SN74LVC1G32-EP] (Quantity: 1)
  - 1-Input Not gate [SN74LVC1G04] (Quantity: 1)
- Block 5
  - 4-Bit Counter [SN74F163A] (Quantity: 2)
  - 2-Input And gate [SN74LVC1G08-Q1] (Quantity: 2)
  - 2-Input Or gate [SN74LVC1G32-EP] (Quantity: 1)
  - 1-Input Not gate [SN74LVC1G04] (Quantity: 2)
- Block 6
  - 4:1 Multiplexer [SN74S153] (Quantity: 1)
  - 2-Input XOR gate [SN74LVC1G86] (Quantity: 1)
- Block 7
  - D-Flip Flop [SN74LVC1G74] (Quantity: 1)
  - 2:1 Multiplexer [SN74LVC2G157] (Quantity: 2)
  - 1-Input Not gate [SN74LVC1G74] (Quantity: 1)

# BILL

Given below is tentative bill of components from online sites in dollars, taxes and other import/export charges are not accounted for.

| IC | **Rate ($)** | **Quantity** | **Cost ($)** |
|---|---|---|---|
| **SN74LVC1G19** | 0.080 | 1 | 0.080 |
| **SN74LVC2G157** | 0.350 | 2 | 0.700 |
| **SN74LVC1G74** | 0.200 | 29 | 5.800 |
| **SN74LVC1G00** | 0.030 | 28 | 0.840 |
| **SN74F163A** | 0.160 | 3 | 0.480 |
| **SN74LVC1G08-Q1** | 0.030 | 4 | 0.120 |
| **SN74LVC1G32-EP** | 0.028 | 2 | 0.056 |
| **SN74LVC1G04** | 0.023 | 3 | 0.046 |
| **SN74S153** | 0.400 | 1 | 0.400 |
| **SN74LVC1G86** | 0.029 | 1 | 0.029 |
| | | **Total Cost =** | 8.551 |

When converted to INR it comes out to be 634.16 (excluding all the taxes).

# ADDITIONAL FEATURES

*This section do not discuss about the extension of logic but what is there in our present design.*

- Requirement was for just 4-digit BCD numbers but we displayed our logic can be used with large bit encodings like ASCII.
- 2 modes in logic can be used to provide user additional flexibility like, asynchronous disable where no one can unlock the circuit, and a fail-safe for malfunction to cutoff the blocks ahead to our block from sensory and ADC block.
- Our circuit provide the leverage of utilising the main output feedback and sensory feedback to give user with correct password to keep locking system open for desirable amount of time.
- If a wrong password is entered we are able to disable our main unlocking system which is Block 6 as soon as first wrong bit reaches us. This was the main reason behind selecting bitwise comparison instead of a whole comparison as it gives us option to save power in out operations by disabling some components not in use.

# KEY TAKEAWAYS

- Adding more functionality means more complex logic and more hardware meaning more power consumption.
- Simulating and Hardware design are equally difficult as hardware limits our capabilities of how we realise our simulation in real world. There it depends on expertise of designer, how he/she can modify or find a way around their simulated logic.
- Real world design is not about getting things done fast but also about getting what user might desire or look for. Logic is the major player in digital design but other factors need to be taken in account no matter if more complex logic is required.

# APPENDIX

- 1:2 Decoder [SN74LVC1G19]
  https://www.ti.com/lit/gpn/sn74lvc1g19
- 2:1 Multiplexer [SN74LVC2G157]
  https://www.ti.com/lit/gpn/sn74lvc2g157
- D-Flip Flop [SN74LVC1G74]
  https://www.ti.com/lit/gpn/SN74LVC1G74
- 2-Input Nand Gate [SN74LVC1G00]
  https://www.ti.com/lit/gpn/sn74lvc1g00
- 4-Bit Counter [SN74F163A]
  https://www.ti.com/lit/ds/sdfs088a/sdfs088a.pdf?ts=1605801297793&ref_url=https%253A%252F%252Fwww.google.com%252F
- 2-Input And gate [SN74LVC1G08-Q1]
  https://www.ti.com/product/SN74LVC1G08-Q1
- 2-Input Or gate [SN74LVC1G32-EP]
  https://www.ti.com/product/SN74LVC1G32-EP
- 1-Input Not gate [SN74LVC1G04]
  https://www.ti.com/lit/gpn/sn74lvc1g04
- 4:1 Multiplexer [SN74S153]
  https://www.alldatasheet.com/datasheet-pdf/pdf/27371/TI/SN74S153.html
- 2-Input XOR gate [SN74LVC1G86]
  https://www.ti.com/lit/gpn/SN74LVC1G86-Q1