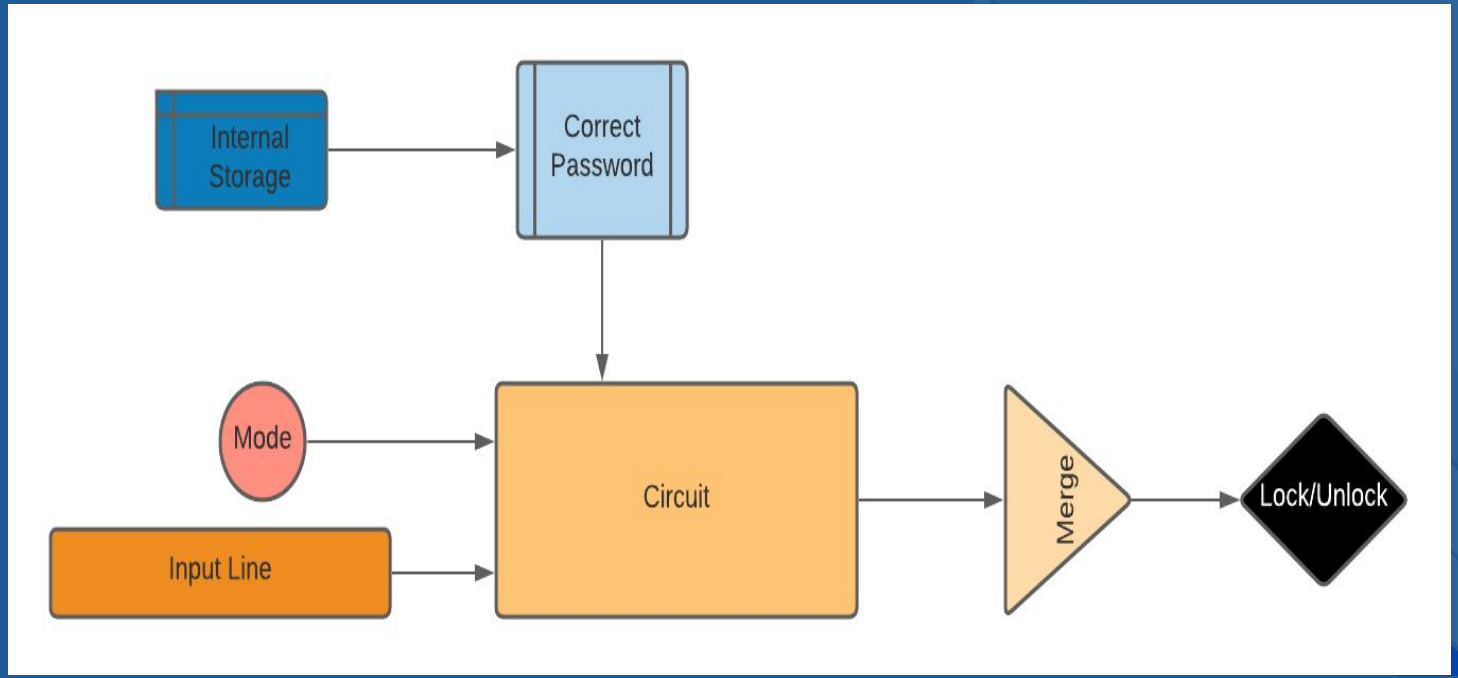
Digital Locking System

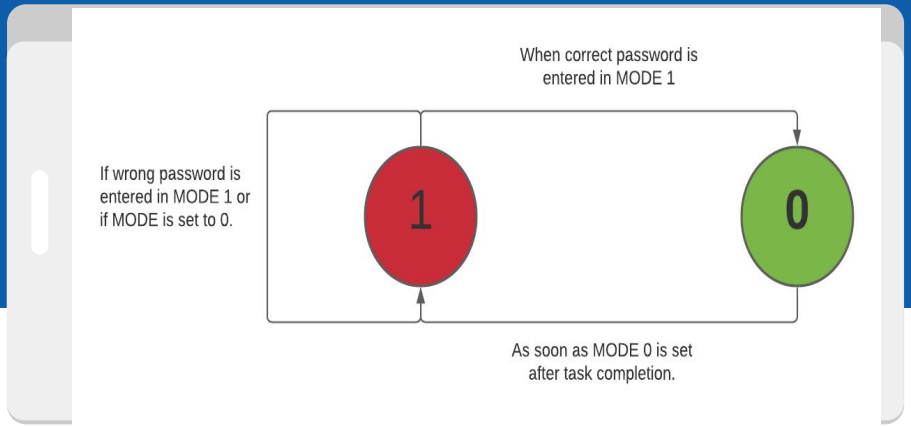
Design Assignment (**G**roup = **80**, Problem no. = 2)

Top Level Block Diagram



Working Logic

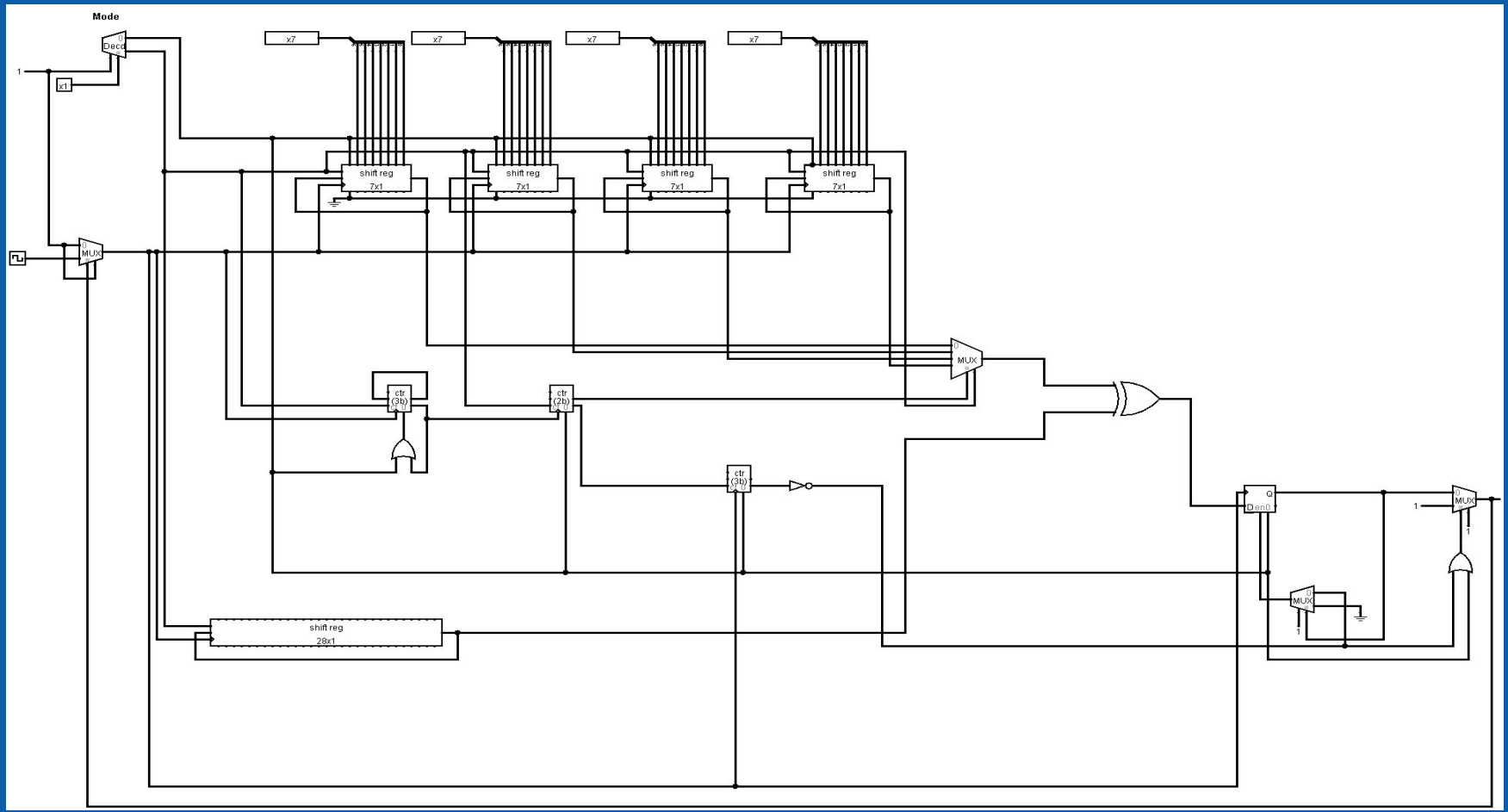
Main logic used in circuit is that XOR gate is used to detect different bits.



Output 1 means **LOCK**

Output 0 means **UNLOCK**

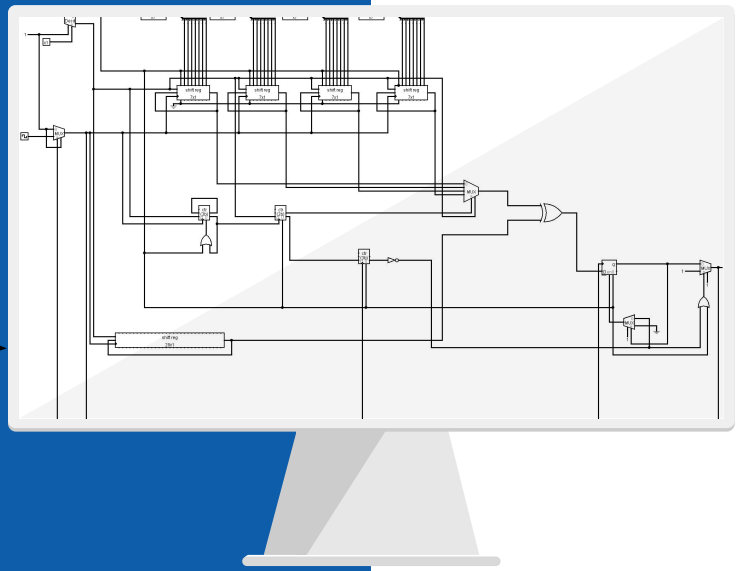
Outputs are explained in figure attached.


Mode
Dec
x1
x7
x7
x7
x7
shift reg
7x1
shift reg
7x1
shift reg
7x1
shift reg
7x1
MUX
ctr
(3b)
ctr
(2b)
ctr
(3b)
MUX
shift reg
28x1
Q
Den
MUX
MUX
1
1
1
1

Sample input and output

User input

Password: 9#$1

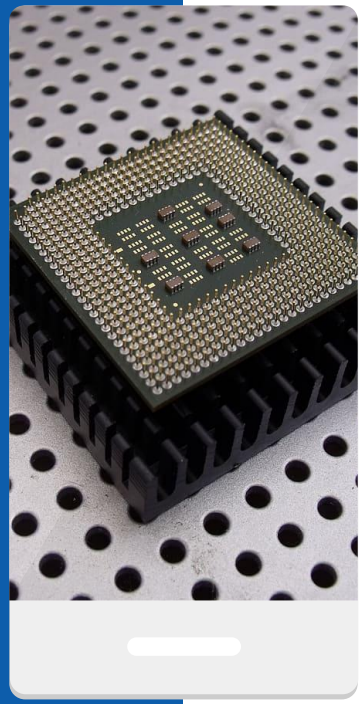


If correct: 0

If incorrect: 1

Additional Functionalities

- BCD + ASCII characters input.
- Mode:
  - 0: Asynchronous Disable
  - 1: Operation Mode
- Automatic disable of unlock system as soon as wrong bit arrives.
- Automatic disconnect from clock input as soon as unlock till next sensory input.



- Connections done for separate memory for password reset, keep our circuit memory separate.

Thank you!