CONTENTS

8086 MICROPROCESSOR: It is a 16-bit microprocessor with 20 address lines and 16 data lines that provides up to 1MB storage. The address and data bus are multiplexed in 8086 to reduce the number of pins required for 8086 IC, before8086 can be used with memory or I/O interfaces, their multiplexed bus must be demultiplexed.

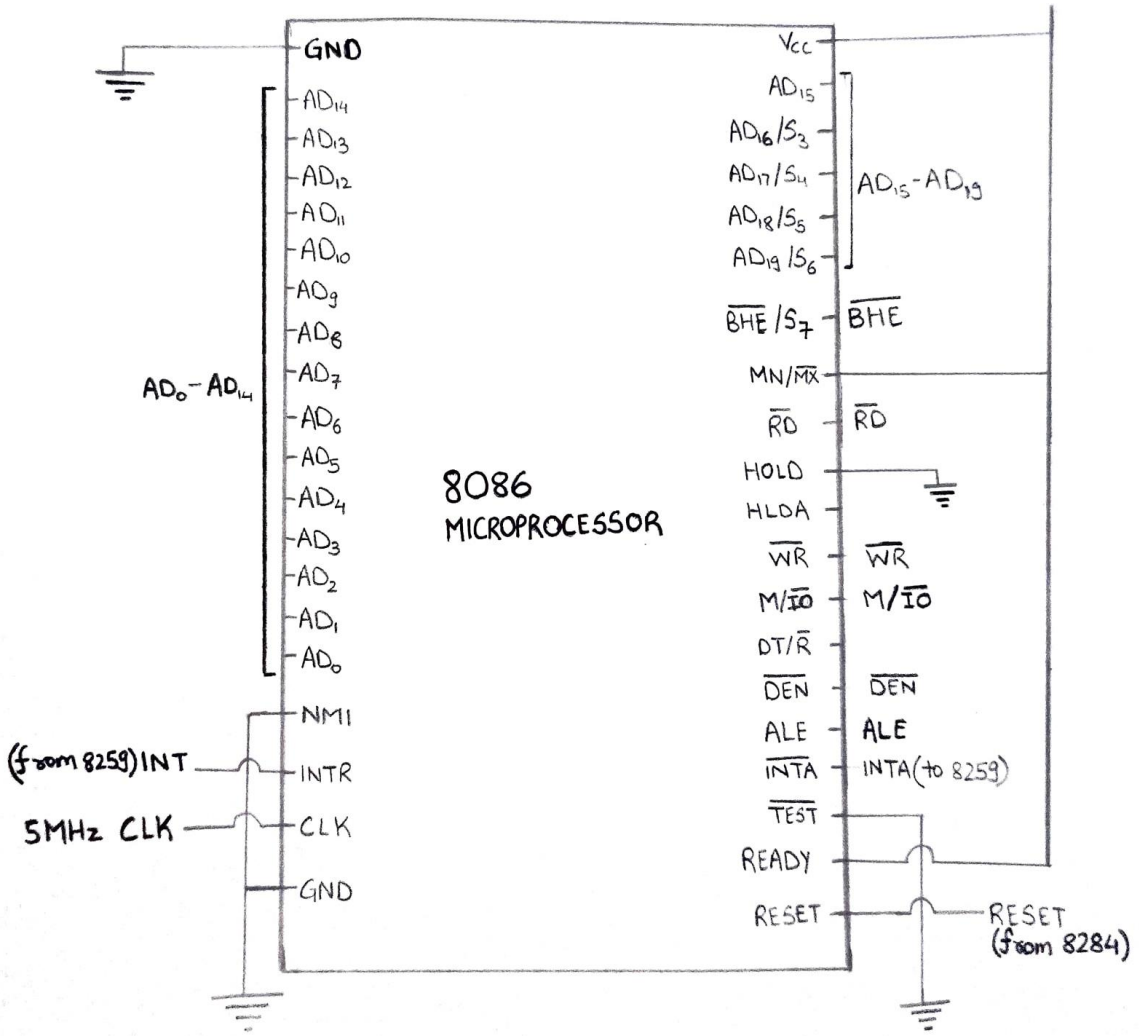


Fig 19.10

8284A: Crystals are very unstable so, vibrate at very high frequency which cannot be directly given to our ICs. So, we use 8284 which reduces frequency to desired levels (2.5MHz, and 5MHz). It provides following basic functions or signals: clock generation, RESET synchronization, READY synchronization, and a TTL level peripheral clock signal which are very important essential signal to microprocessors.

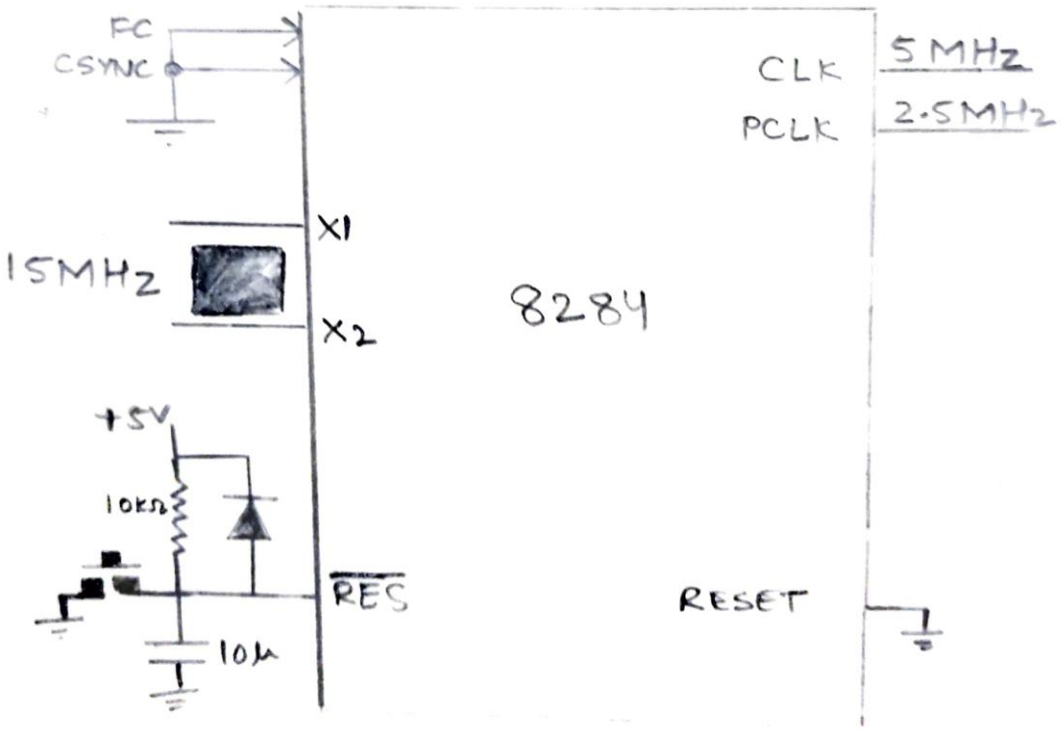


Fig 19.11

ADDRESS BUS of 8086: provides memory and I/O with memory address or the I/O port.
LS373: Octal D-type Transparent Latches AND Edge-triggered Flip-flops. For demultiplexing the busses 74LS373 demultiplexer is used.

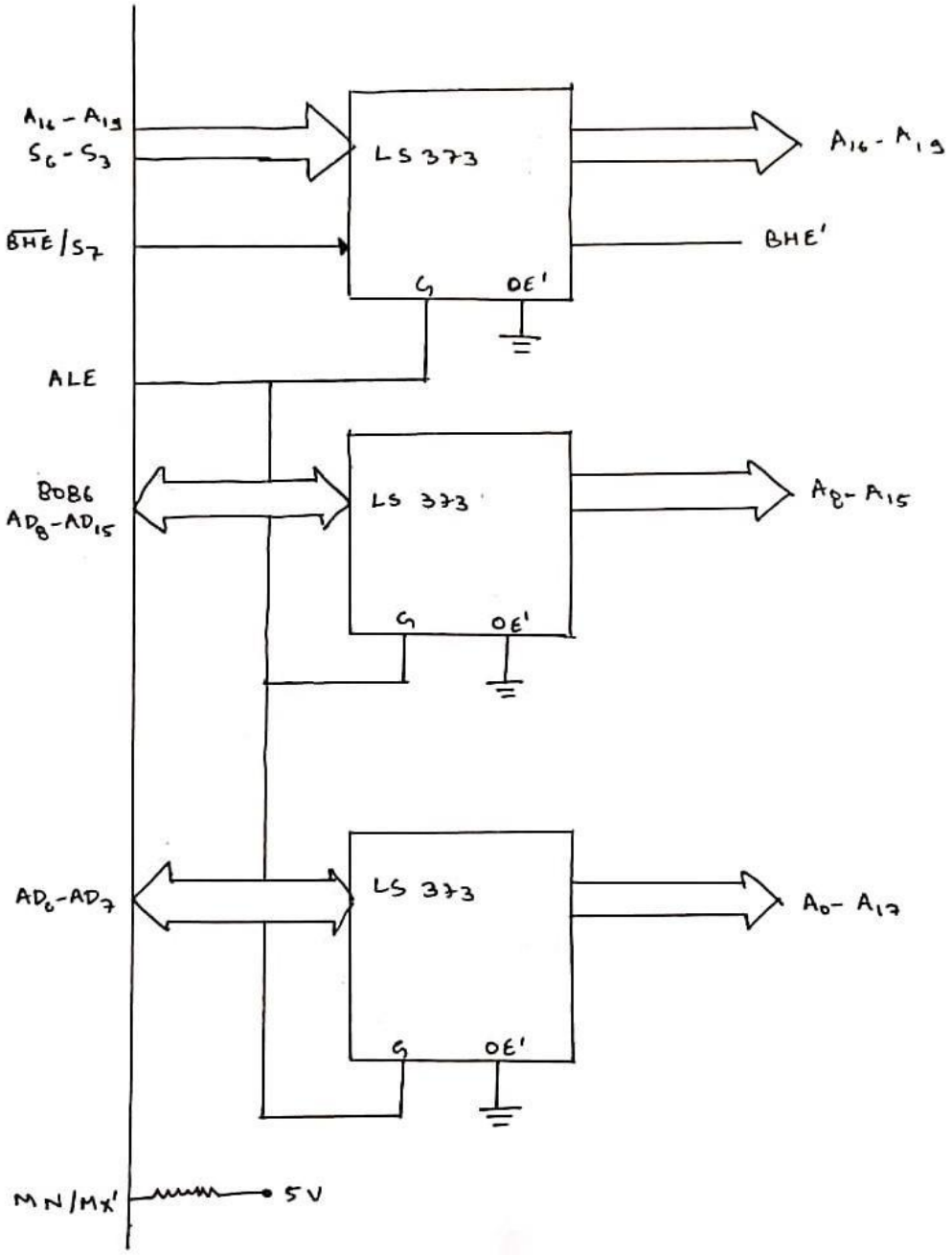


Fig 19.12

DATA BUS OF 8086: Transfers data between microprocessor, memory and I/O in the system.
LS245: Octal BUS Transceivers WITH 3-state Outputs.
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.
The output-enable (OE) input can disable the device so that the buses are effectively isolated.

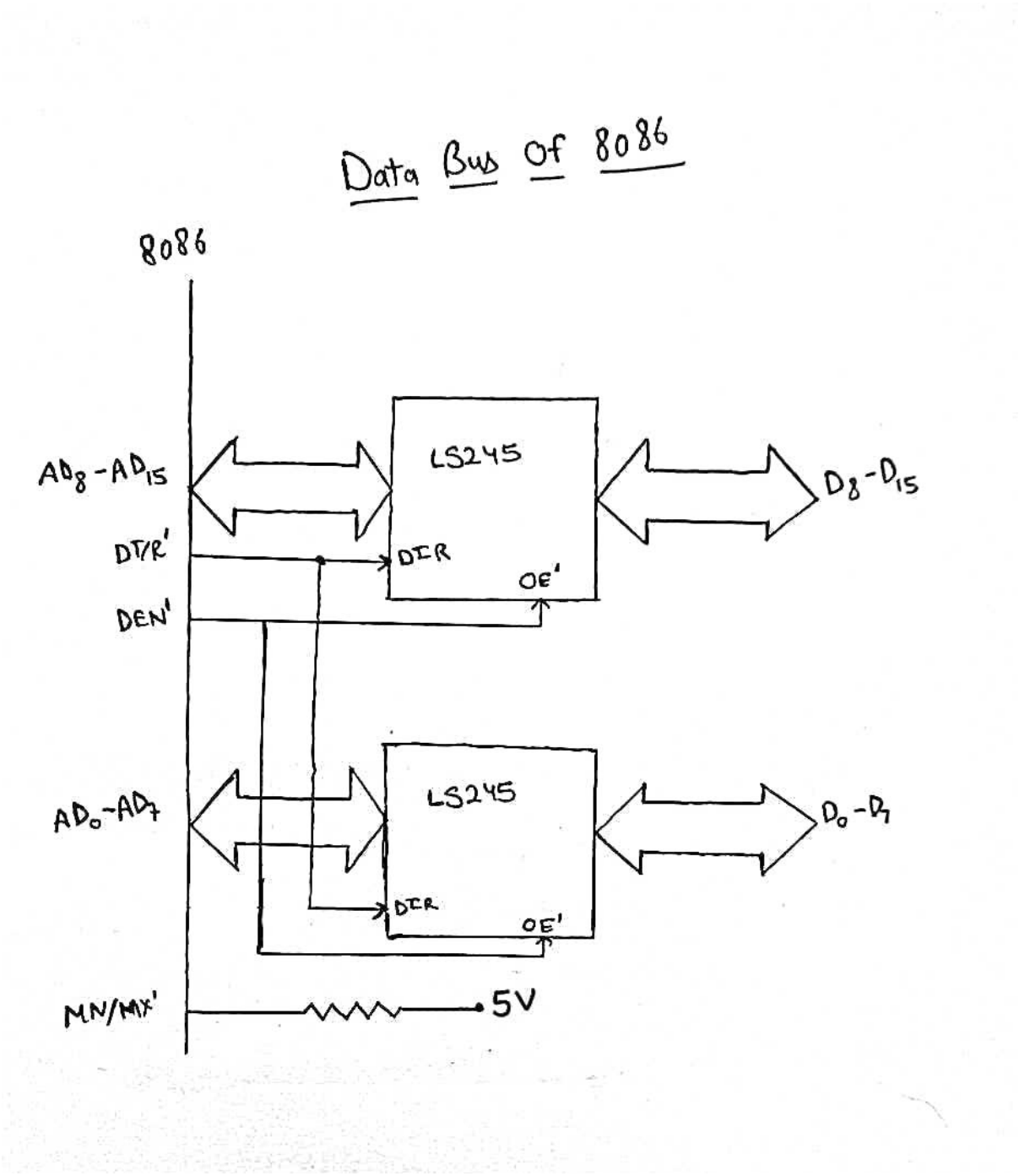


Fig 19.13

CONTROL BUS OF 8086: Provides control signal to the memory and I/O
LS244: Octal Buffers AND LINE Drivers WITH 3-state Outputs.

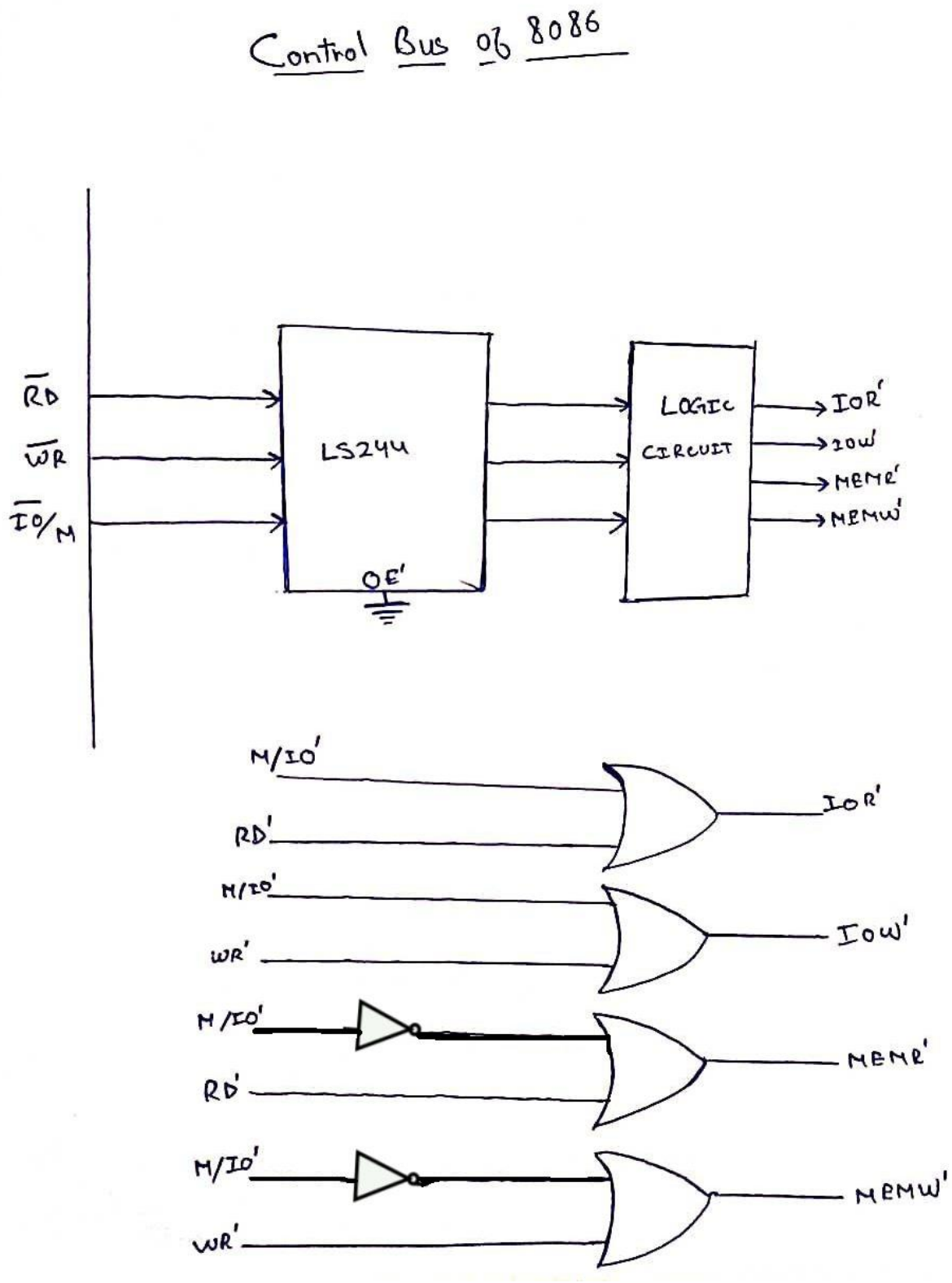


Fig 19.14

MEMORY MAP

MEMORY MAP

ROM 1-E-00000 - 00FFE
ROM 1-O-00001 - 00FFF
RAM 1 -E- 01000 - 01FFE
RAM 1 - O - 01001 - 01FFF
ROM2 - E - FF000 - FFFFE
ROM2 - O - FF001 - FFFFF

ROM1

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM1

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

ROM2

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Fig 19.15

MEMORY DECODING CIRCUIT: LS138 is used to select amongst ROM1, RAM1 and ROM2 using address lines (A14, A13, A12) and *M / IO.*
LS138: 3-to-8-line Decoder/demultiplexer.

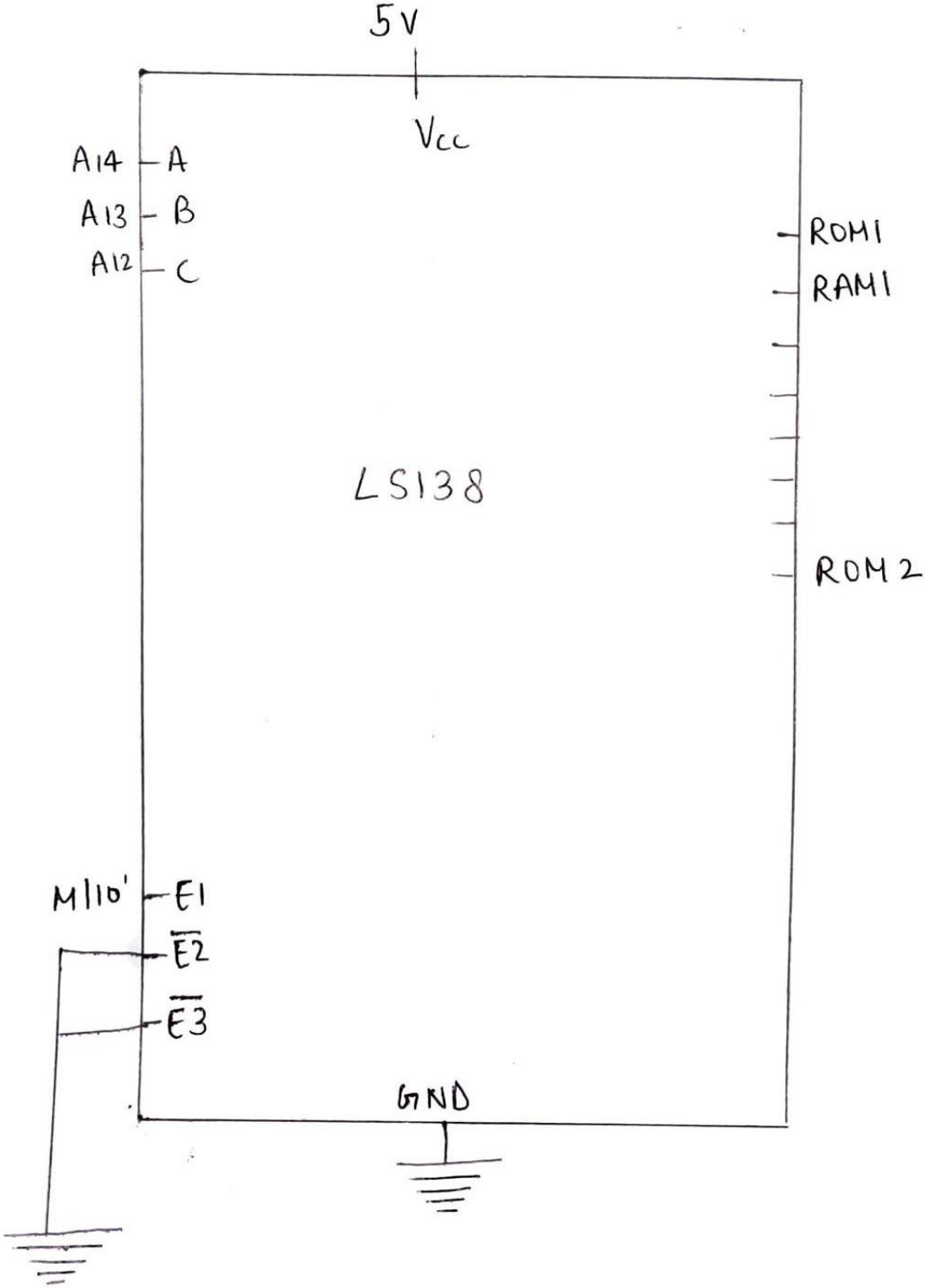


Fig 19.16

MEMORY INTERFACING CIRCUIT: When we are executing any instruction, the address of memory location is sent out by the microprocessor. The corresponding memory chip is selected by a decoding circuit.

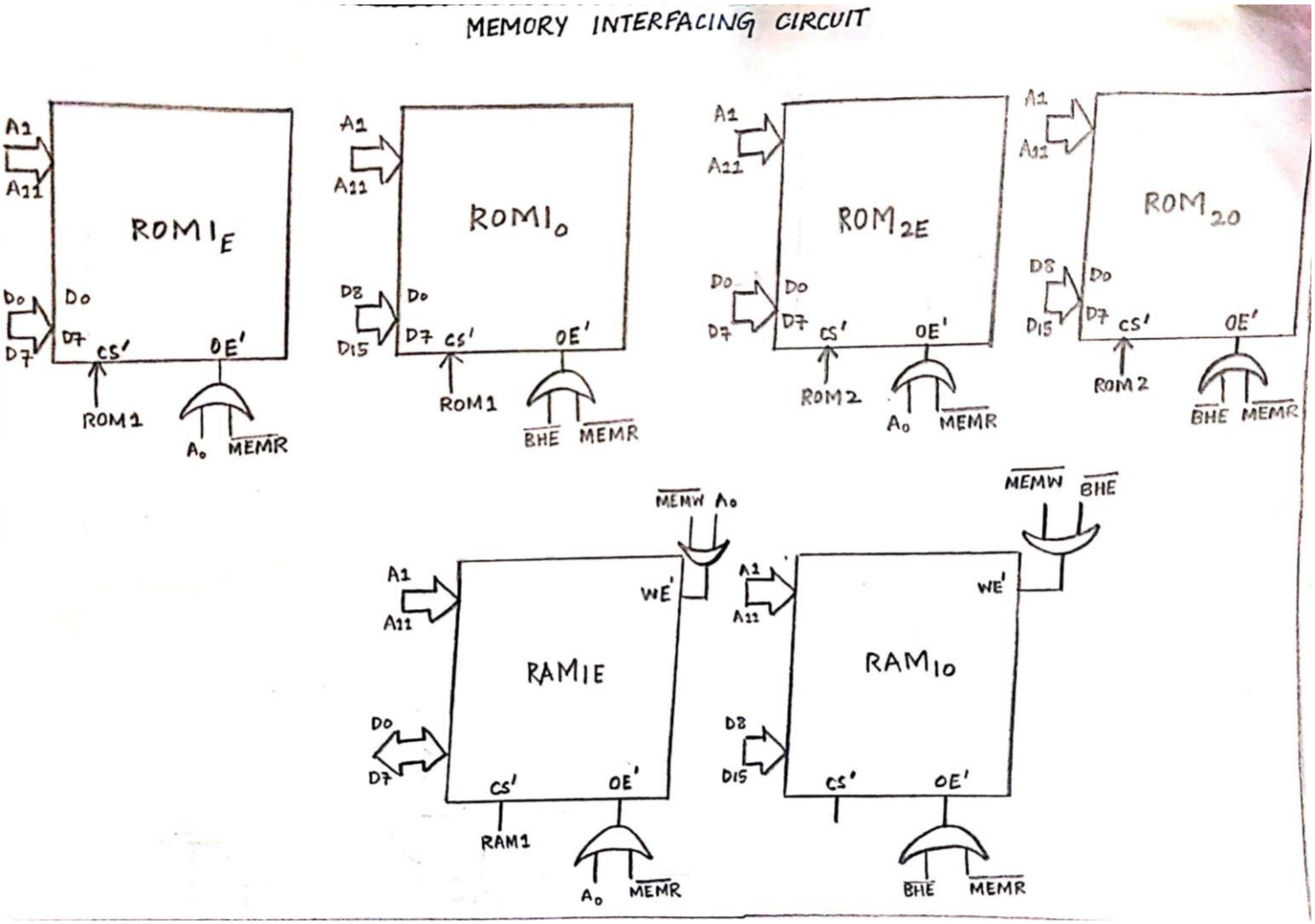
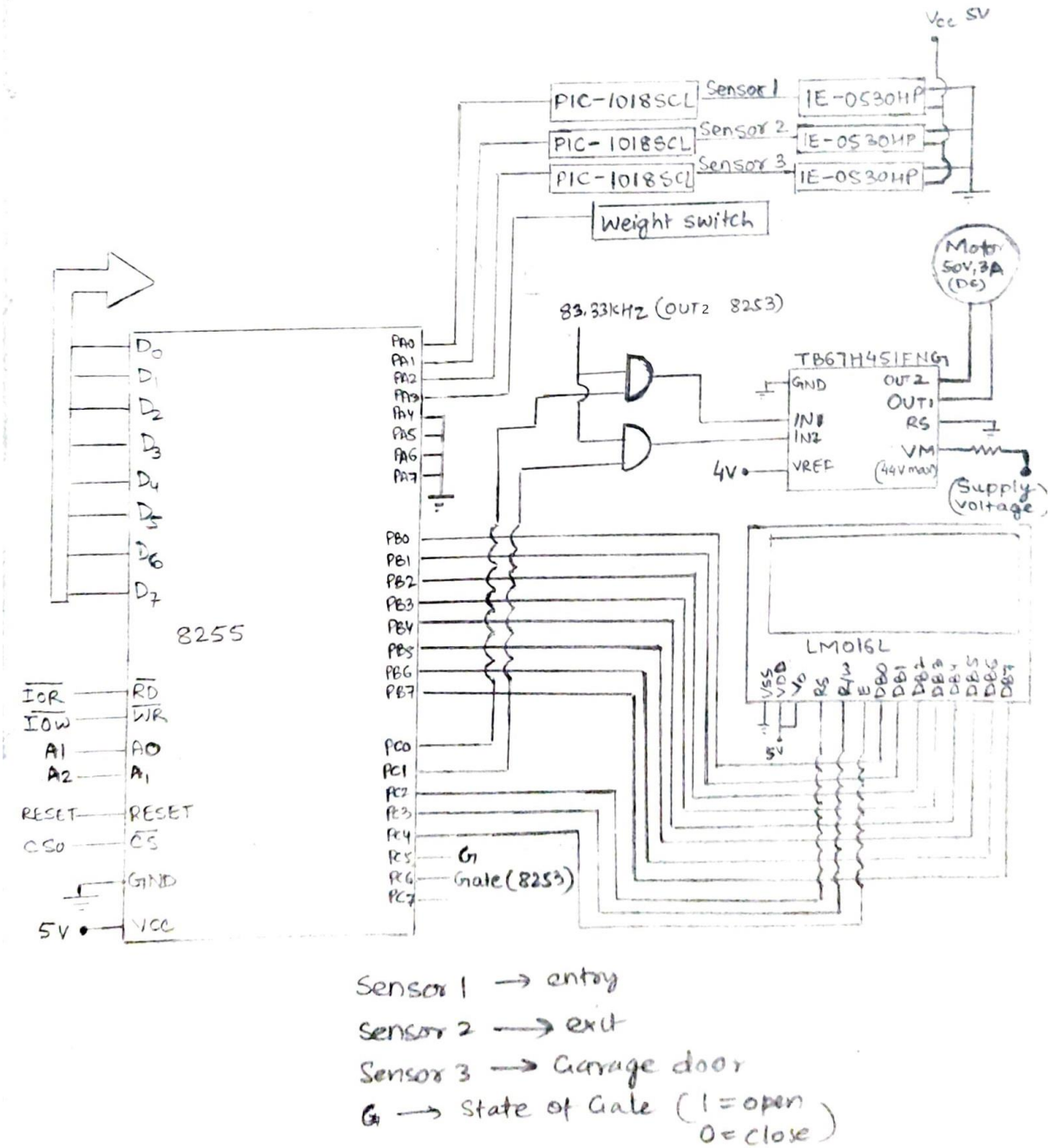


Fig 19.17

I/O DEVICES

8255: 8255 is a general purpose programmable I/O device designed to interface the CPU with its outside world such as ADC, DAC, keyboard etc. It can be used with almost any microprocessor. It consists of three 8-bit bidirectional I/O ports. We are interfacing motor driver, sensors and weight switch with 8086 via 8255.



Sensor 1 → entry
Sensor 2 → exit
Sensor 3 → Garage door
G → State of Gate (1 = open, 0 = close)

Fig 19.18

I/O DEVICES DECODING CIRCUIT

LS138 is used to select between 8255, 8259A and 8253 using address lines.

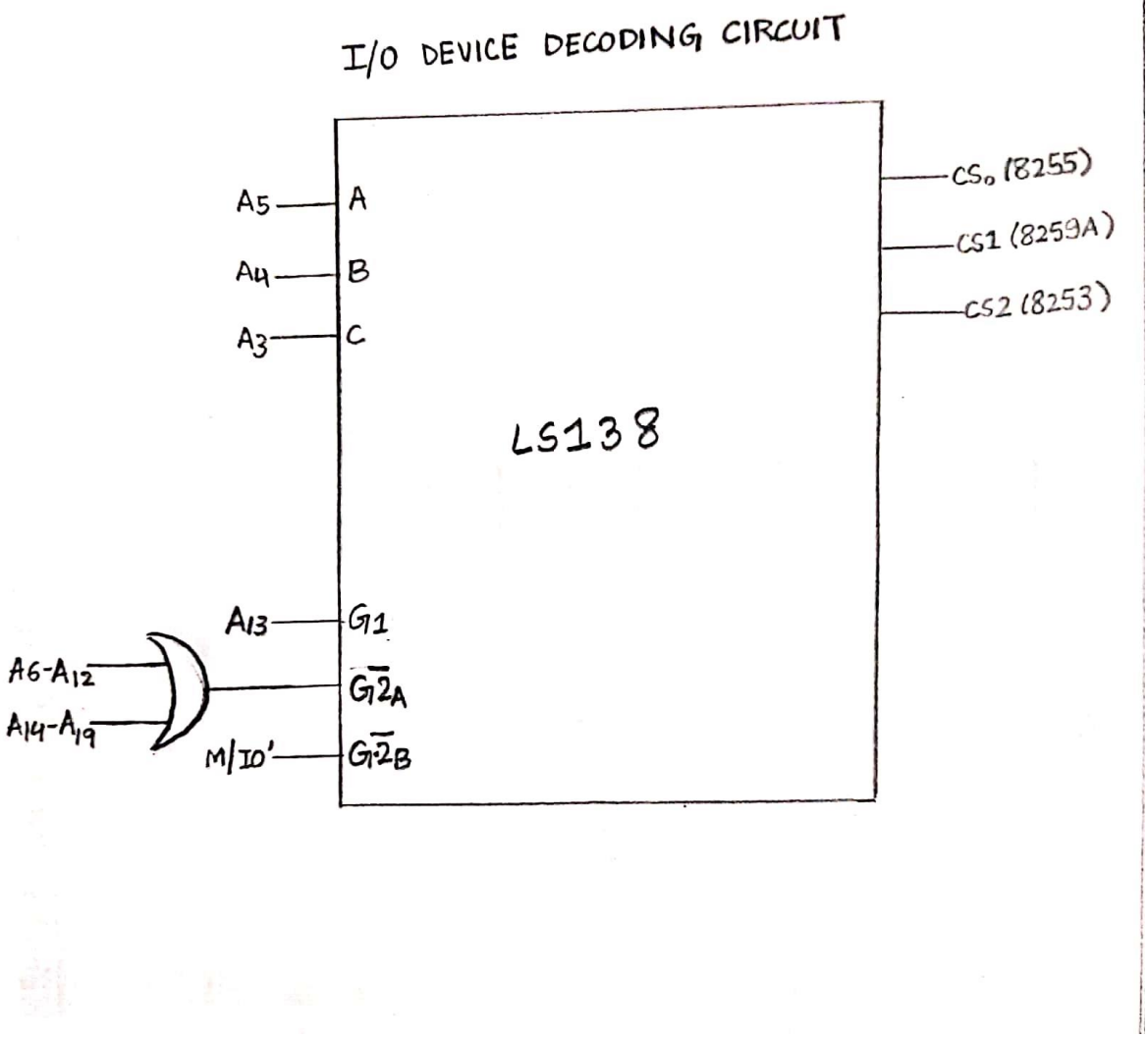


Fig 19.19

CLOCK USING 8253

8253: Counter 0, Counter 1 in mode 2 with count value of 27500 and 1000 respectively. Counter 2 in mode 3 with count value 30.
Counter 1 output gives 10 sec interrupt to gate open and close procedures, and 30 of these interrupts are counted for 5 min interrupt.
Counter 2 generates square wave of frequency less than 100KHz for maintaining DC motor input frequency.

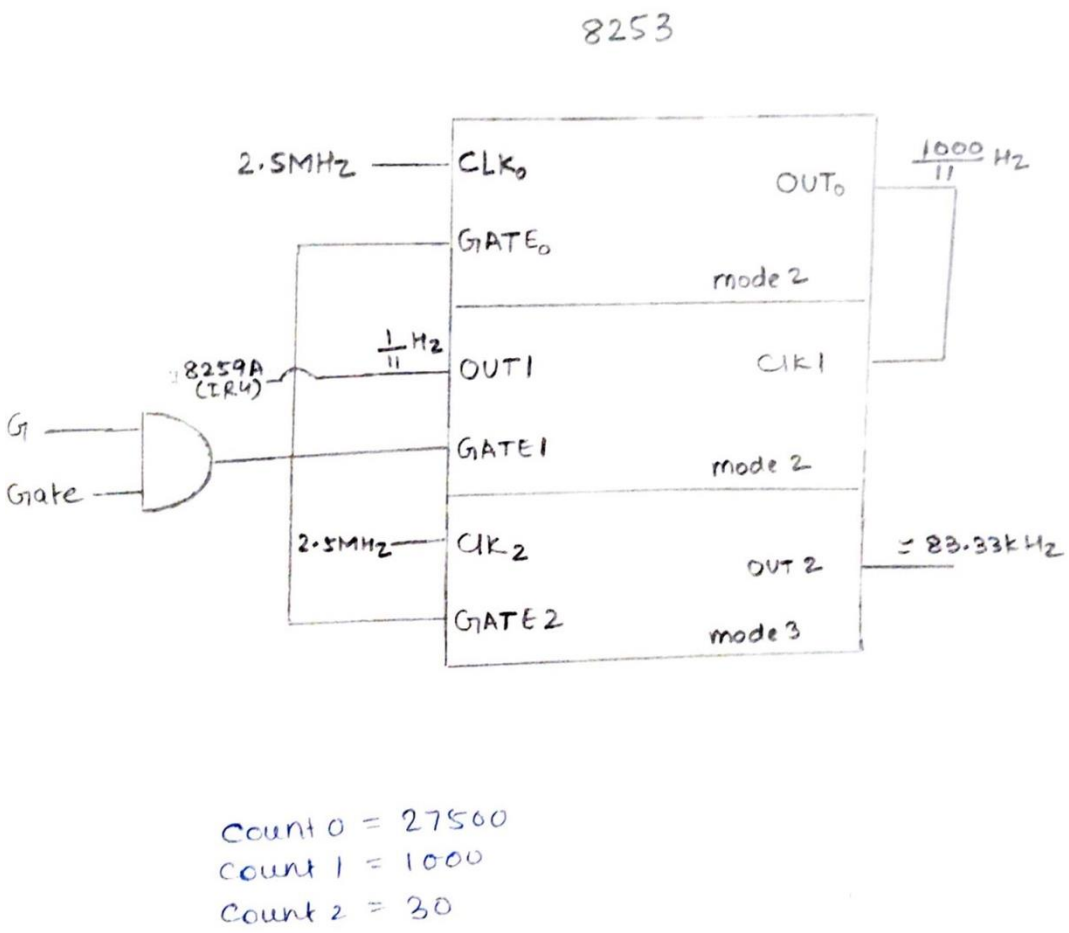


Fig 19.20

PRIORITY INTERRUPT CONTROLLER (PIC)

8259A Interrupt Controller is designed to transfer the interrupt with highest priority to the CPU, along with interrupt address information.
Interfacing of a single PIC provides 8 interrupts inputs from IR0-IR7.
We can mask individual bits of the interrupt request register.
By default priority decreases from IR0 to IR7.
Remote is given highest priority as in smart garage system valet will first open the gate and then use sensor assemblies. Then sensors, and 8253 interrupts are lowest priority as they are for closing or opening gate, and sensor 3 which is used for reset of 5 mins are given higher priority.

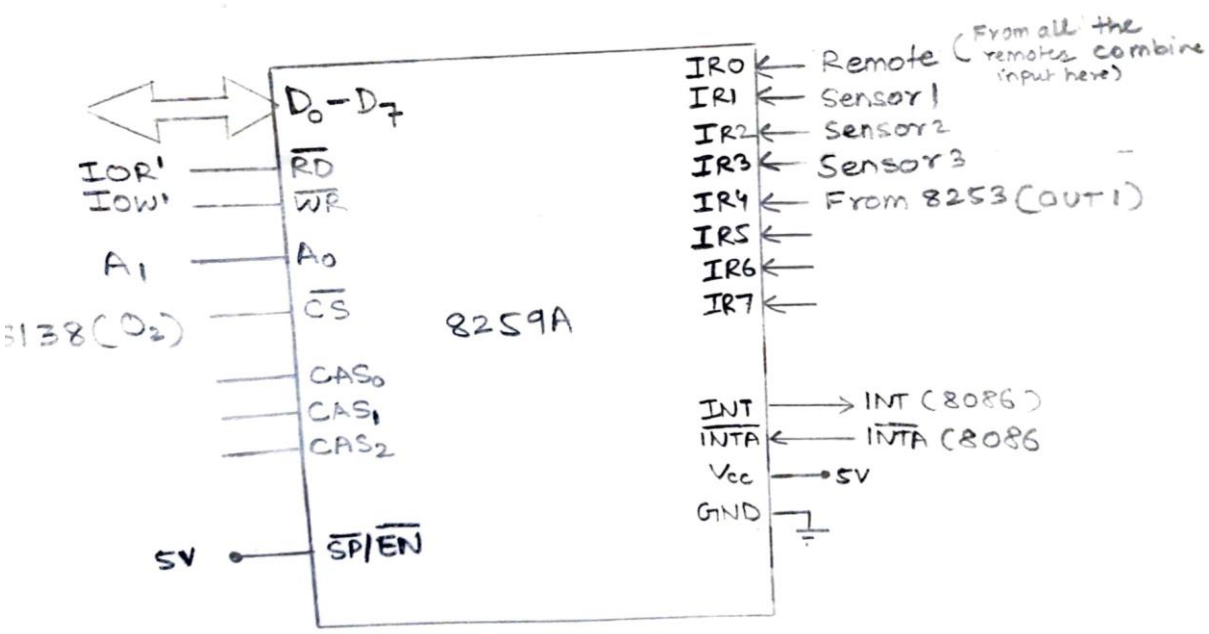


Fig 19.21