

PROJECT REPORT

Name: - Manav P. Prajapati

Project Title: - 8-bit subtractor

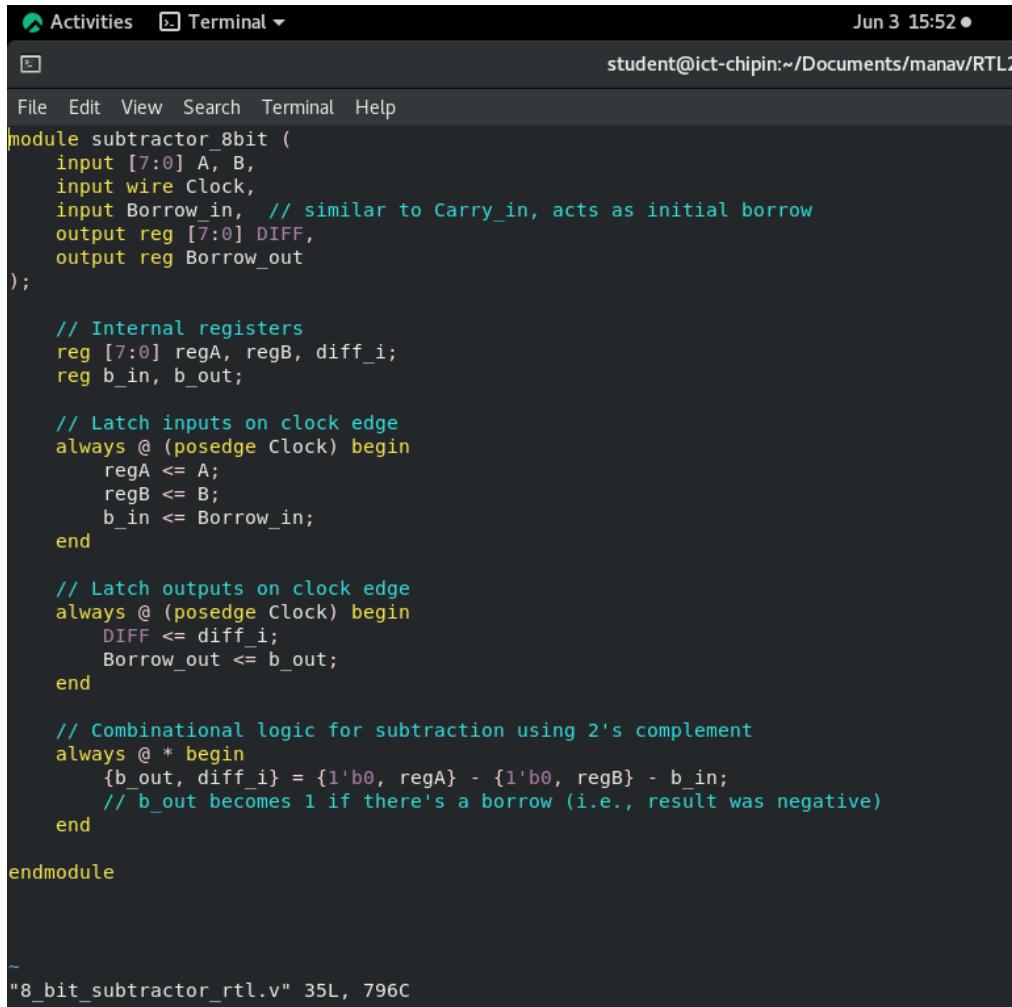
Content: -

- Verilog file content, VCS results: -
 1. Waveform in Verdi
 2. Verdi schematic
- Design Compiler (DC shell): -
 1. Library Used
 2. Constraints file
 3. Gates used in design
 4. Report (Area, power, cells, units)
 5. Schematic
 6. Slack time
- GDS-II layout of the design using Synopsys - flow scripts: -
 1. Scenario used
 2. Each Step (Floor planning, power planning, etc.)
 3. Report (Area, power, cells, units, etc.)
- Prime Time (PT shell): -
 1. Slack time
 2. Report (Area, cells, units, etc.)
 3. Schematic
 4. Waveform (Slack)

Verilog and Verdi

1). RTL code: -

File: - 8_bit_subtractor_rtl.v



A screenshot of a terminal window titled "Activities Terminal". The window shows Verilog code for an 8-bit subtractor module named "subtractor_8bit". The code includes input ports A and B, a clock input, a Borrow_in input, and output ports DIFF and Borrow_out. It features internal registers regA and regB, and variables diff_i and b_in. The code uses always@(posedge Clock) blocks for latching inputs and outputs. A combinational logic block calculates {b_out, diff_i} = {1'b0, regA} - {1'b0, regB} - b_in. The terminal window also displays the file name "8_bit_subtractor_rtl.v" and its line count (35L, 796C).

```
Activities Terminal Jun 3 15:52 ●
student@ict-chipin:~/Documents/manav/RTL2

File Edit View Search Terminal Help
module subtractor_8bit (
    input [7:0] A, B,
    input wire Clock,
    input Borrow_in, // similar to Carry_in, acts as initial borrow
    output reg [7:0] DIFF,
    output reg Borrow_out
);

// Internal registers
reg [7:0] regA, regB, diff_i;
reg b_in, b_out;

// Latch inputs on clock edge
always @ (posedge Clock) begin
    regA <= A;
    regB <= B;
    b_in <= Borrow_in;
end

// Latch outputs on clock edge
always @ (posedge Clock) begin
    DIFF <= diff_i;
    Borrow_out <= b_out;
end

// Combinational logic for subtraction using 2's complement
always @ * begin
    {b_out, diff_i} = {1'b0, regA} - {1'b0, regB} - b_in;
    // b_out becomes 1 if there's a borrow (i.e., result was negative)
end

endmodule

~"8_bit_subtractor_rtl.v" 35L, 796C
```

2). Testbench Code: -

File: - 8_bit_sub_tb.v

```
Activities Terminal Jun 3 15:50 ●
student@ict-chipin:~/Documents/manav/RTL2GDSII/rtl_simulation

File Edit View Search Terminal Help
`timescale 1ns/1ns
`include "8_bit_subtractor_rtl.v" // Make sure the subtractor module file is in the same directory

module testbench;
    reg [7:0] A, B;
    reg Clock, Borrow_in;
    wire [7:0] DIFF;
    wire Borrow_out;

    // Instantiate the module under test
    subtractor_8bit dut (
        .A(A),
        .B(B),
        .Clock(Clock),
        .Borrow_in(Borrow_in),
        .DIFF(DIFF),
        .Borrow_out(Borrow_out)
    );

    // Clock generation
    always #5 Clock = ~Clock; // Clock period = 10ns

    // Stimulus
    initial begin
        $fsdbDumpvars; // For waveform analysis (tool-specific, e.g., Verdi)

        // Initialize
        Clock = 0;
        A = 8'b00000000;
        B = 8'b00000000;
        Borrow_in = 0;

        // Wait for a few cycles
        #10;

        // Test Case 1: 10 - 5 - 0 = 5
        A = 8'b00000000;
        B = 8'b00000000;
        Borrow_in = 0;

        // Wait for a few cycles
        #10;

        // Test Case 1: 10 - 5 - 0 = 5
        A = 8'd10;
        B = 8'd5;
        Borrow_in = 0;
        #10 $display("A = %d, B = %d, Borrow_in = %b, DIFF = %d, Borrow_out = %b", A, B, Borrow_in, DIFF, Borrow_out);

        // Test Case 2: 5 - 10 - 0 = -5 → 2's complement = 251
        A = 8'd5;
        B = 8'd10;
        Borrow_in = 0;
        #10 $display("A = %d, B = %d, Borrow_in = %b, DIFF = %d, Borrow_out = %b", A, B, Borrow_in, DIFF, Borrow_out);

        // Test Case 3: 15 - 7 - 1 = 7
        A = 8'd15;
        B = 8'd7;
        Borrow_in = 1;
        #10 $display("A = %d, B = %d, Borrow_in = %b, DIFF = %d, Borrow_out = %b", A, B, Borrow_in, DIFF, Borrow_out);

        // Test Case 4: 0 - 1 - 1 = -2 → 2's complement = 254
        A = 8'd0;
        B = 8'd1;
        Borrow_in = 1;
        #10 $display("A = %d, B = %d, Borrow_in = %b, DIFF = %d, Borrow_out = %b", A, B, Borrow_in, DIFF, Borrow_out);

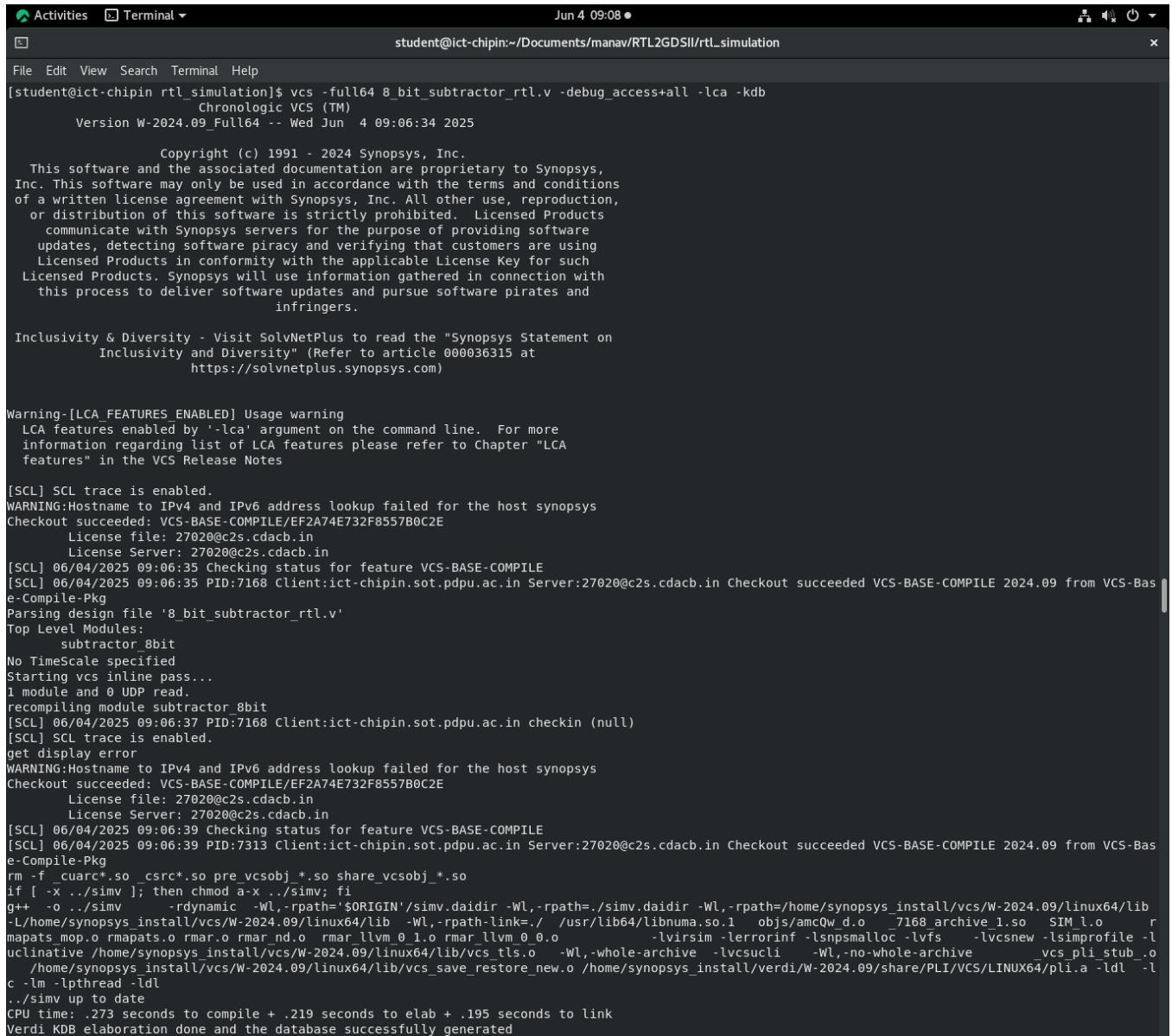
        #100 $finish;
    end

endmodule
```

3). VCS command output: -

Compiling RTL file

```
vcs -full64 8_bit_subtractor_rtl.v -debug_access+all -lca -kdb
```



```
Activities Terminal Jun 4 09:08 •
student@ict-chipin:~/Documents/manav/RTL2GDSII/rtl_simulation
File Edit View Search Terminal Help
[student@ict-chipin rtl_simulation]$ vcs -full64 8_bit_subtractor_rtl.v -debug_access+all -lca -kdb
Chronologic VCS (TM)
Version W-2024.09_Full64 -- Wed Jun 4 09:06:34 2025

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Warning-[LCA_FEATURES_ENABLED] Usage warning
LCA features enabled by '-lca' argument on the command line. For more
information regarding list of LCA features please refer to Chapter "LCA
features" in the VCS Release Notes

[SCL] SCL trace is enabled.
WARNING:Hostname to IPv4 and IPv6 address lookup failed for the host synopsys
Checkout succeeded: VCS-BASE-COMPILER/EF2A74E732F8557B0C2E
  License file: 27020@c2s.cdacb.in
  License Server: 27020@c2s.cdacb.in
[SCL] 06/04/2025 09:06:35 Checking status for feature VCS-BASE-COMPILER
[SCL] 06/04/2025 09:06:35 PID:7168 Client:ict-chipin.sot.pdpu.ac.in Server:27020@c2s.cdacb.in Checkout succeeded VCS-BASE-COMPILER 2024.09 from VCS-BASE-Compile-Pkg
Parsing design file '8_bit_subtractor_rtl.v'
Top Level Modules:
  subtractor_8bit
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module subtractor_8bit
[SCL] 06/04/2025 09:06:37 PID:7168 Client:ict-chipin.sot.pdpu.ac.in checkin (null)
[SCL] SCL trace is enabled.
get display error
WARNING:Hostname to IPv4 and IPv6 address lookup failed for the host synopsys
Checkout succeeded: VCS-BASE-COMPILER/EF2A74E732F8557B0C2E
  License file: 27020@c2s.cdacb.in
  License Server: 27020@c2s.cdacb.in
[SCL] 06/04/2025 09:06:39 Checking status for feature VCS-BASE-COMPILER
[SCL] 06/04/2025 09:06:39 PID:7313 Client:ict-chipin.sot.pdpu.ac.in Server:27020@c2s.cdacb.in Checkout succeeded VCS-BASE-COMPILER 2024.09 from VCS-BASE-Compile-Pkg
rm -f _cuarc*.so _csrc*.so pre_vcsobj*.so share_vcsobj*.so
if [ -x ./simv ]; then chmod a-x ./simv; fi
g++ -o ./simv -rdynamic -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=~/home/synopsys/install/vcs/W-2024.09/linux64/lib -L~/home/synopsys/install/vcs/W-2024.09/linux64/lib -Wl,-rpath-link= ./ /usr/lib64/libnuma.so.1 objjs/amCQw_d.o _7168_archive_1.so SIM.l.o mapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -l ucliniative /home/synopsys/install/vcs/W-2024.09/linux64/lib/vcs/tls.o -Wl,-whole-archive -lvcscli -Wl,-no-whole-archive vcs pli stub.o /home/synopsys/install/vcs/W-2024.09/linux64/lib/vcs_save_restore_new.o /home/synopsys/install/verdi/W-2024.09/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
.../simv up to date
CPU time: .273 seconds to compile + .219 seconds to elab + .195 seconds to link
Verdi KDB elaboration done and the database successfully generated
```

Compiling Testbench.

```
vcs -full64 8_bit_subt_tb.v -debug_access+all -lca -kdb
```

```
Activities Terminal Jun 4 09:13 ● student@ict-chipin:~/Documents/manav/RTL2GDSII/rtl_simulation
File Edit View Search Terminal Help
[student@ict-chipin rtl_simulation]$ vcs -full64 8_bit_sub_tb.v -debug_access+all -lca -kdb
Chronologic VCS (TM)
Version W-2024.09_Full64 -- Wed Jun 4 09:07:14 2025

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Warning-[LCA_FEATURES_ENABLED] Usage warning
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[SCL] SCL trace is enabled.
WARNING:Hostname to IPv4 and IPv6 address lookup failed for the host synopsys
Checkout succeeded: VCS-BASE-COMPIL/EF2A74E732F8557B0C2E
    License file: 27020@c2s.cdacb.in
    License Server: 27020@c2s.cdacb.in
[SCL] 06/04/2025 09:07:15 Checking status for feature VCS-BASE-COMPIL
[SCL] 06/04/2025 09:07:15 PID:7970 Client:ict-chipin.sot.pdpu.ac.in Server:27020@c2s.cdacb.in Checkout succeeded VCS-BASE-COMPILE 2024.09 from VCS-Bas
e-Compile-Pkg
Parsing design file '8_bit_sub_tb.v'
Parsing included file '8_bit_subtractor_rtl.v'.
Back to file '8_bit_sub_tb.v'.
Top Level Modules:
    testbench
TimeScale is 1 ns / 1 ns
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module testbench
[SCL] 06/04/2025 09:07:15 PID:7970 Client:ict-chipin.sot.pdpu.ac.in checkin (null)
[SCL] SCL trace is enabled.
get display error
WARNING:Hostname to IPv4 and IPv6 address lookup failed for the host synopsys
Checkout succeeded: VCS-BASE-COMPIL/EF2A74E732F8557B0C2E
    License file: 27020@c2s.cdacb.in
    License Server: 27020@c2s.cdacb.in
[SCL] 06/04/2025 09:07:17 Checking status for feature VCS-BASE-COMPIL
[SCL] 06/04/2025 09:07:17 PID:8078 Client:ict-chipin.sot.pdpu.ac.in Server:27020@c2s.cdacb.in Checkout succeeded VCS-BASE-COMPILE 2024.09 from VCS-Bas
e-Compile-Pkg
rm -f _cuar*c.so _csrc*.so pre_vcsobj_* .so share_vcsobj_* .so
if [ _x ..simv ]; then chmod a+x ..simv; fi
g++ -o ...simv -rdynamic -Wl,-rpath=$'ORIGIN'/simv.daidir -Wl,-rpath=~/home/synopsys_install/vcs/W-2024.09/linux64/lib
-L~/home/synopsys_install/vcs/W-2024.09/linux64/lib -Wl,-rpath-link= ./ /usr/lib64/libnuma.so.1 obj/amcQw_d.o _7970_archive_1.so _SIM_l.o r
mapats_mop rmapats_mop. rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0 . -lvirsim -errorinf -lsnpsmalloc -lvfs -lvcsnew -lssimprofile -l
oclunitive /home/synopsys_install/vcs/W-2024.09/linux64/lib/vcs_tis.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive vcs_pli_stub_o
/home/synopsys_install/vcs/W-2024.09/linux64/lib/vcs_save_restore_new.o /home/synopsys_install/verdi/W-2024.09/share/PLI/VCS/LINUX64/pli.a -ldl
c -lm -lpthread -ldl
.../simv up to date
CPU time: .240 seconds to compile + .202 seconds to elab + .193 seconds to link
Verdi KDB elaboration done and the database successfully generated
```

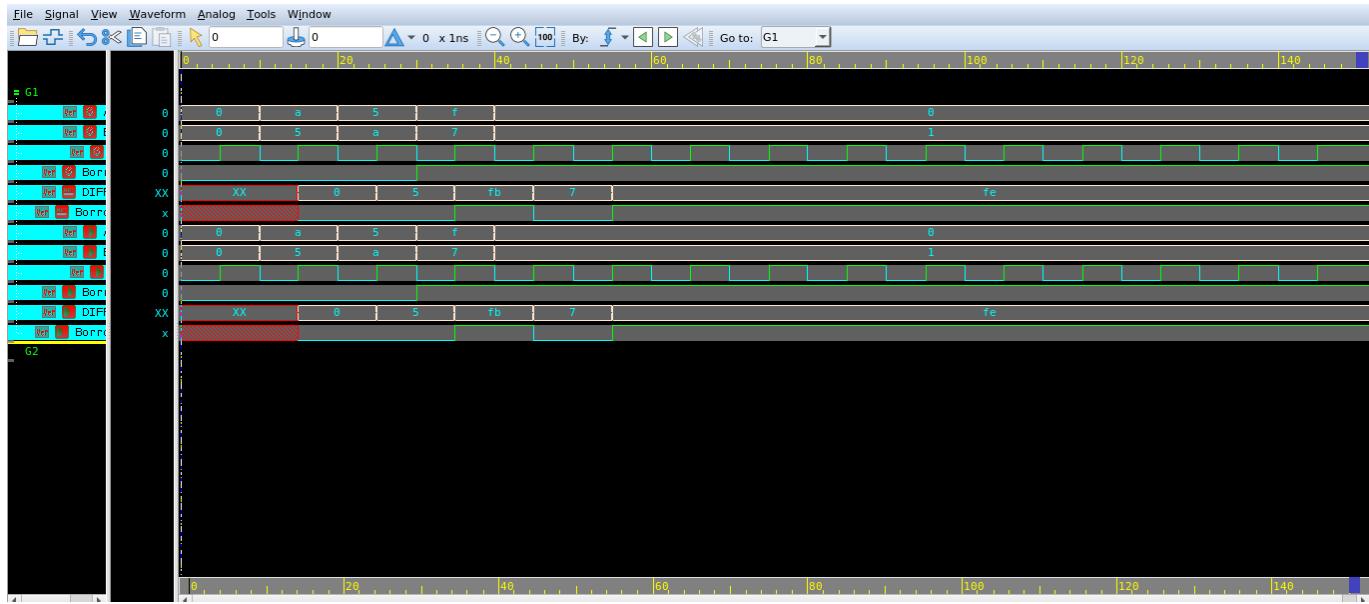
4). Run Simulation : - (./simv Verdi)

Executes the compiled simulation binary

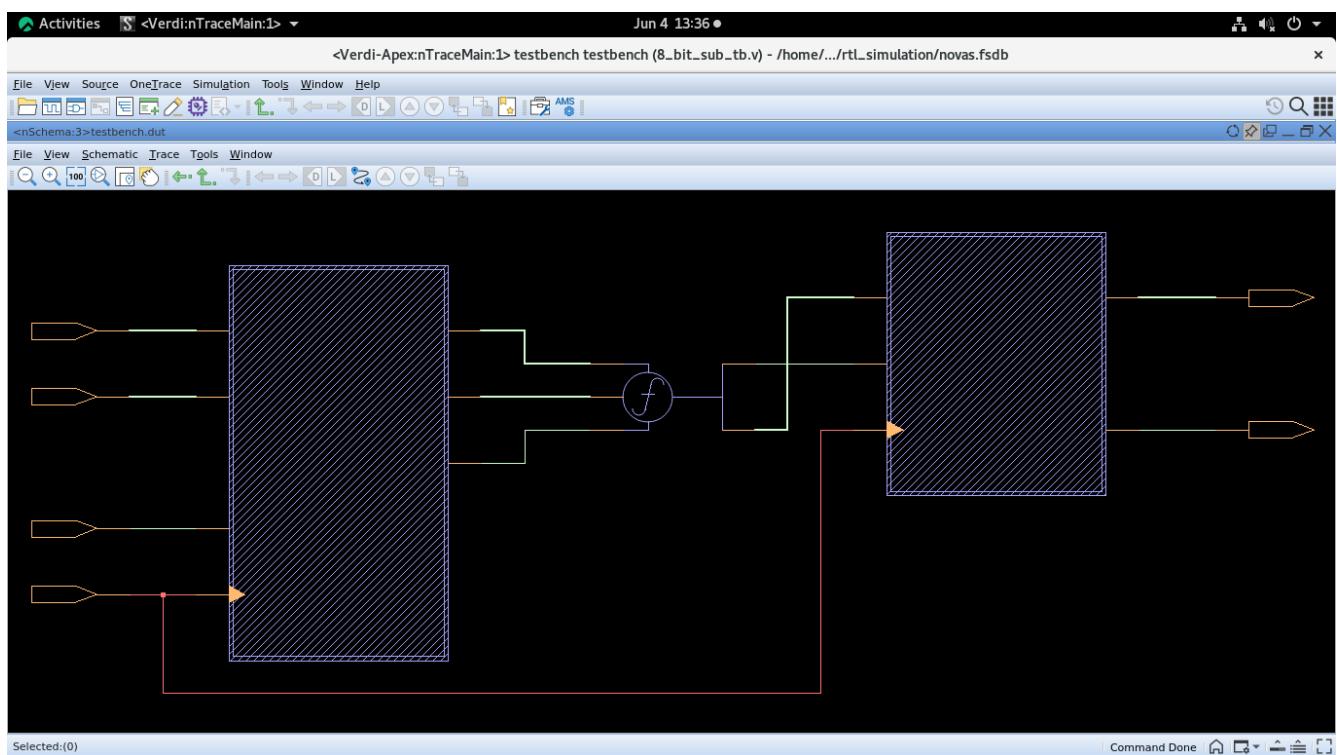
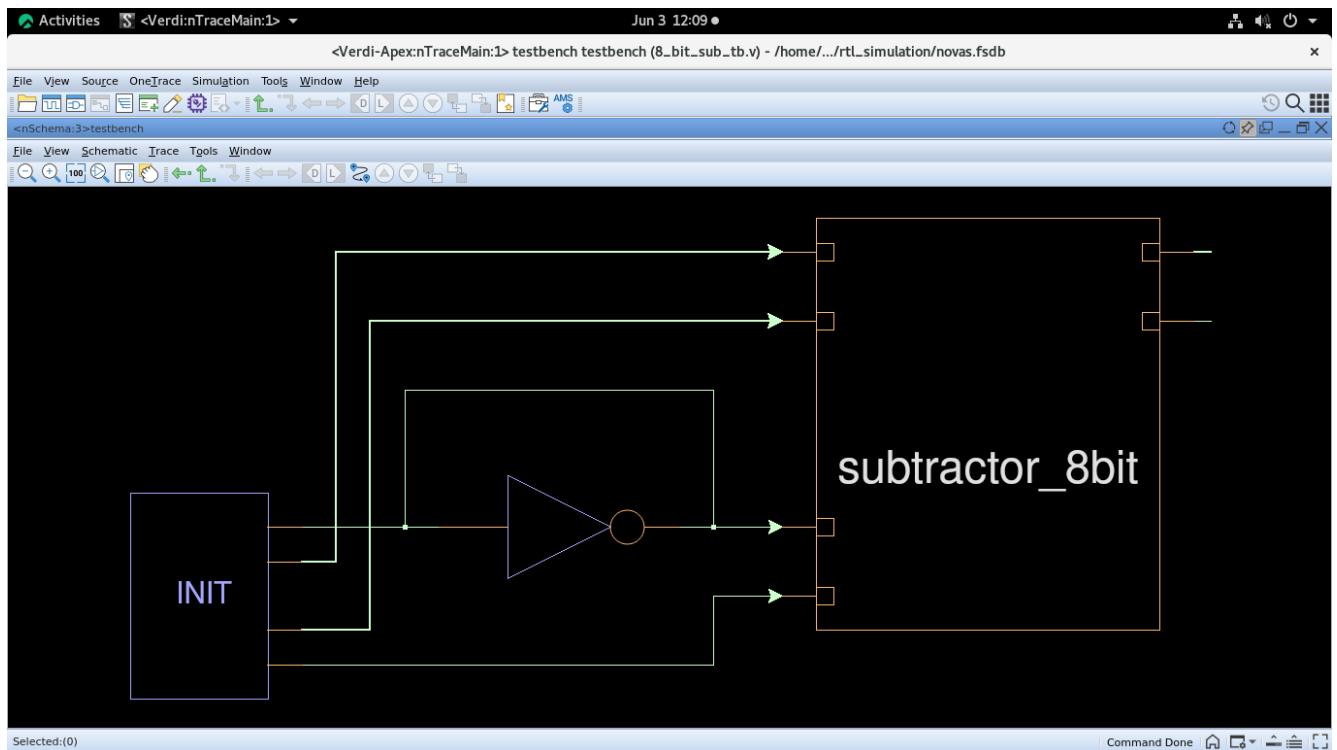
```
Activities Terminal Jun 4 09:26 ●
student@ict-chipin:~/Documents/manav/RTL2GDSII/rtl_simulation

File Edit View Search Terminal Help
.../simv up to date
CPU time: .240 seconds to compile + .202 seconds to elab + .193 seconds to link
Verdi KDB elaboration done and the database successfully generated
[student@ict-chipin rtl_simulation]$ ./simv Verdi
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $save functionality, ASLR will be switch ed off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message.
Chronologic VCS® simulator copyright 1991-2024
Contains Synopsys proprietary information.
Compiler version W-2024.09_Full64; Runtime version W-2024.09_Full64; Jun 4 09:07 2025
[SCL] SCL trace is enabled.
WARNING:Hostname to IPv4 and IPv6 address lookup failed for the host synopsys
Checkout succeeded: VCS-BASE-RUNTIME/AF3AD4D7787CF482B637
    License file: 27020@c2s.cdacb.in
    License Server: 27020@c2s.cdacb.in
[SCL] 06/04/2025 09:07:37 Checking status for feature VCS-BASE-RUNTIME
[SCL] 06/04/2025 09:07:37 PID:8305 Client:ict-chipin.sot.pdpu.ac.in Server:27020@c2s.cdacb.in Checkout succeeded VCS-BASE-RUNTIME 2024.09 from VCS-Bas e-Runtime-Pkg
*Verdi* Loading libsscore_vcs202409.so
FSDB Dumper for VCS, Release Verdi_W-2024.09, Linux x86_64/64bit, 08/17/2024
(C) 1996 - 2024 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'novas.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
A = 10, B = 5, Borrow_in = 0, DIFF = 0, Borrow_out = 0
A = 5, B = 10, Borrow_in = 0, DIFF = 5, Borrow_out = 0
A = 15, B = 7, Borrow_in = 1, DIFF = 251, Borrow_out = 1
A = 0, B = 1, Borrow_in = 1, DIFF = 7, Borrow_out = 0
$finish called from file "8_bit_sub_tb.v", line 60.
$finish at simulation time 150
VCSSimulation Report
Time: 150 ns
CPU Time: 0.190 seconds; Data structure size: 0.0Mb
Wed Jun 4 09:07:38 2025
[SCL] 06/04/2025 09:07:38 PID:8305 Client:ict-chipin.sot.pdpu.ac.in checkin (null)
[student@ict-chipin rtl_simulation]$ |
```

5). View Waveform in Verdi: - (verdi -ssf novas.fsdb -nologo)



6). Schematic: -



Design Compiler

Synthesis: - (Gates Used)

This is the main TCL script for synthesis.

Uncommented or modified this lines to choose the circuit to synthesize.

```
Activities Terminal Jun 3 15:38 ●
student@ict-chipin:~/Documents/manav/RTL2GDSII/DC

File Edit View Search Terminal Help
source -echo -verbose ./rm_setup/dc_setup.tcl

set RTL_SOURCE_FILES ../../rtl/8_bit_subtractor.v
set DESIGN_NAME subtractor_8bit

set RESULTS_DIR ./results
#set DCRM_FINAL_VERILOG_OUTPUT_FILE subtractor_8bit_synth.v

#set_option -seed 12345

define_design_lib WORK -path ./WORK

#set_dont_use [get_lib_cells */FADD*]
#set_dont_use [get_lib_cells */HADD*]
#set_dont_use [get_lib_cells */NAND*]
#set_dont_use [get_lib_cells */XNOR*]
#set_dont_use [get_lib_cells */MUX*]
set_dont_use [get_lib_cells */AO*]
set_dont_use [get_lib_cells */OA*]
set_dont_use [get_lib_cells */XOR*]
set_dont_use [get_lib_cells */NOR*]

analyze -format verilog ${RTL_SOURCE_FILES}
elaborate ${DESIGN_NAME}
link
current_design ${DESIGN_NAME}

read_sdc ../../CONSTRAINTS/8_bit_sub.sdc

compile_ultra

report_timing > timing.rpt
report_area > area.rpt
report_power > power.rpt
write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
report_timing -path_type full -delay_type max -max_paths 5 -nworst 5
```

2). Library used: - (**saed32rvt_ss0p7vn40c.db**)

```
Activities Terminal Jun 3 15:40 ● student@ict-chipin:~/Documents/manav/RTL2GDSII/DC/rm_setup
#####
set DESIGN_NAME          "subtractor_8bit" ;# The name of the top-level design
set PDK_PATH              "./../ref/" ;# to set the PDK path for the design
set DESIGN_REF_DATA_PATH  "" ;# Absolute path prefix variable for library/design data.
                            # Use this variable to prefix the common absolute path
                            # to the common variables defined below.
                            # Absolute paths are mandatory for hierarchical
                            # reference methodology flow.

#####
# Hierarchical Flow Design Variables
#####

set HIERARCHICAL_DESIGN NAMES      "" ;# List of hierarchical block design names "DesignA DesignB" ...
set HIERARCHICAL_CELLS        "" ;# List of hierarchical block cell instance names "u_DesignA u_DesignB" ...

#####
# Library Setup Variables
#####

# For the following variables, use a blank space to separate multiple entries.
# Example: set TARGET_LIBRARY_FILES "lib1.db lib2.db lib3.db"

set ADDITIONAL_SEARCH_PATH    "$PDK_PATH $SPDK_PATH/tech/milkyway $PDK_PATH/tech/star_rcxt" ;# Additional search path to be added to the default
search path

set TARGET_LIBRARY_FILES      "$PDK_PATH/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db" ;# Target technology logical libraries
set ADDITIONAL_LINK_LIB_FILES "" ;# Extra link logical libraries not included in TARGET_LIBRARY_FILES

set MIN_LIBRARY_FILES        "" ;# List of max min library pairs "max1 min1 max2 min2 max3 min3"...
set MW_REFERENCE_LIB_DIRS     "" ;# Milkyway reference libraries (include IC Compiler ILMs here)
set MW_REFERENCE_CONTROL_FILE "" ;# Reference Control file to define the Milkyway reference libs
```

4). Constraints: -

```
Activities Terminal Jun 3 10:23 ● student@ict-chipin:~/Documents/tapan/RTL2GDSII/CONSTRAINTS
File Edit View Search Terminal Tabs Help
student@ict-chipin:~... × student@ict-chipin:~... × student@ict-chipin:~... × student@ict-chipin:~... × student@ict-chipin:~... ×
create_clock -period 6.8 -name Clock -waveform {0 0.55} [get_ports Clock]

set_input_delay -max 1.5 -clock Clock [all_inputs]
set_output_delay -max 0.8 -clock Clock [all_outputs]

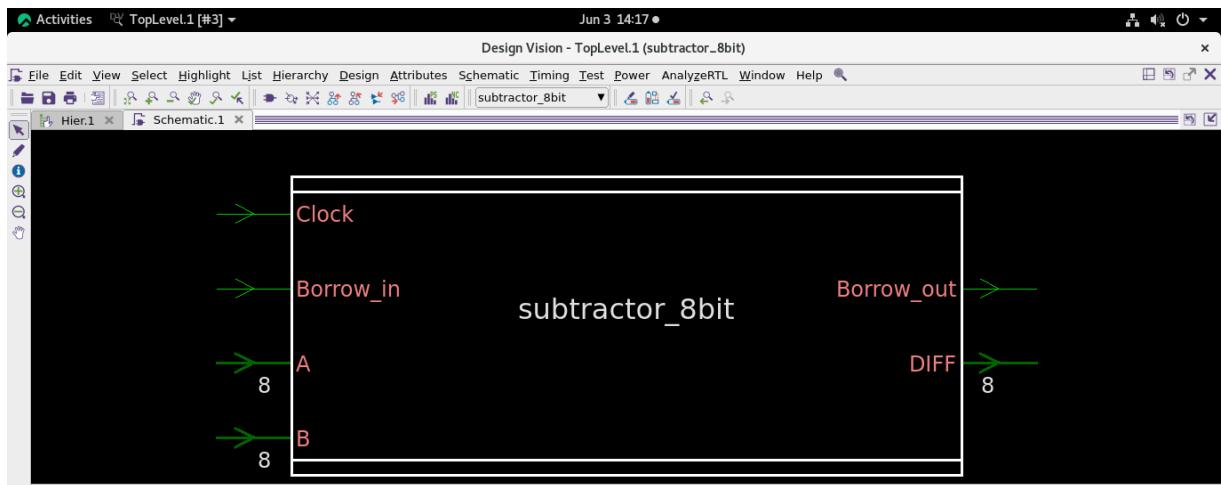
set_input_transition 0.5 [all_inputs]

set_clock_uncertainty -setup 1.6 [get_clocks Clock]
set_clock_uncertainty -hold 0.100 [get_clocks Clock]

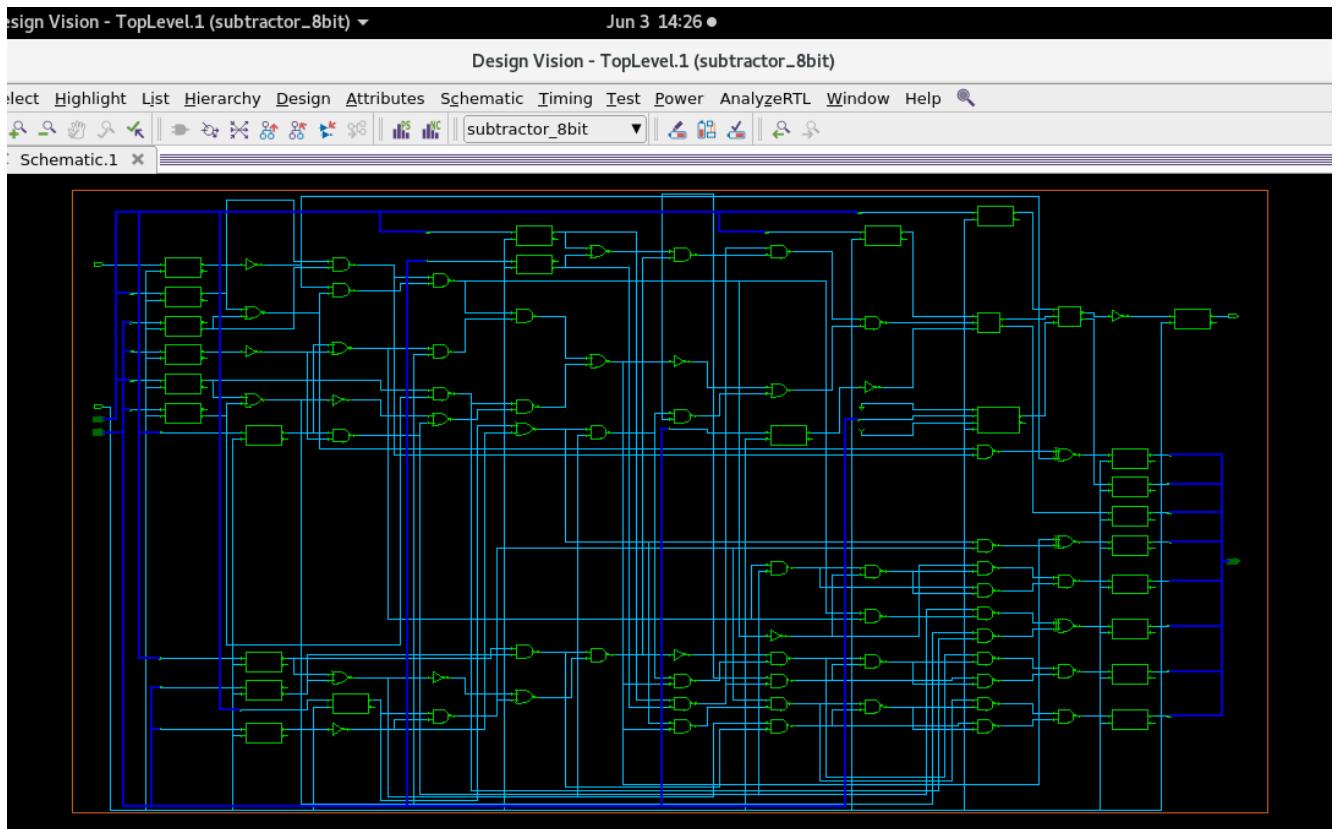
set_max_transition 0.25 [current_design]
set_max_transition -clock_path 0.15 [get_clocks Clock]

~
```

5). Block Diagram: -



6). Schematic: -



Slack time: - 0.40

Leaf Cell Count: - 92

Cell Area: - 297.6026

7). Timing Analysis: - (report_timing)

```
File Edit View Search Terminal Tabs Help
student@ict-chipin:~/Documents/m... × student@ict-chipin:~/Documents/m... × student@ict-chipin:~/Documents/n
Point           Incr      Path
-----
clock Clock (rise edge)      0.00      0.00
clock network delay (ideal)  0.00      0.00
regA_reg[0]/CLK (DFFX1_RVT)  0.00      0.00 r
regA_reg[0]/Q (DFFX1_RVT)   0.60      0.60 f
U17/Y (OR2X1_RVT)          0.36      0.96 f
U23/Y (NAND2X0_RVT)        0.20      1.16 r
U14/Y (NAND2X1_RVT)        0.40      1.56 f
U31/Y (AND2X1_RVT)         0.25      1.81 f
U34/Y (OR2X1_RVT)          0.40      2.21 f
U5/Y (INVX0_RVT)           0.15      2.37 r
U49/Y (OR2X1_RVT)          0.19      2.56 r
U11/Y (NAND2X1_RVT)        0.35      2.90 f
U70/CO (FADDX1_RVT)        0.52      3.43 f
U69/S (FADDX1_RVT)         0.76      4.19 f
DIFF_reg[7]/D (DFFX1_RVT)  0.00      4.19 f
data arrival time           0.00      4.19

clock Clock (rise edge)      6.80      6.80
clock network delay (ideal)  0.00      6.80
clock uncertainty            -1.60     5.20
DIFF_reg[7]/CLK (DFFX1_RVT)  0.00      5.20 r
library setup time           -0.61     4.59
data required time           0.00      4.59
-----
data required time           4.59
data arrival time             -4.19
-----
slack (MET)                 0.40

1
dc_shell>
```

8). Cell Count: - (report_qor)

```
Timing Path Group 'Clock'
-----
Levels of Logic:          10.00
Critical Path Length:    4.19
Critical Path Slack:     0.40
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:  0.00
Worst Hold Violation:   0.00
Total Hold Violation:   0.00
No. of Hold Violations: 0.00
-----

Cell Count
-----
Hierarchical Cell Count:  0
Hierarchical Port Count:  0
Leaf Cell Count:          92
Buf/Inv Cell Count:       10
Buf Cell Count:           0
Inv Cell Count:           10
CT Buf/Inv Cell Count:   0
Combinational Cell Count: 66
Sequential Cell Count:    26
Macro Count:              0
-----
```

9). Cell Area: - (report_qor)

```
Activities Terminal Jun 3 10:19
student@ict-chipin:~/Documents/
File Edit View Search Terminal Tabs Help
student@ict-chipin:~... student@ict-chipin:~... student@ict-chipin:~... student@i
Area
-----
Combinational Area:      125.292992
Noncombinational Area:   172.309638
Buf/Inv Area:           12.707200
Total Buffer Area:       0.00
Total Inverter Area:    12.71
Macro/Black Box Area:   0.000000
Net Area:               38.954851
-----
Cell Area:              297.602629
Design Area:             336.557481

Design Rules
-----
Total Number of Nets:    114
Nets With Violations:  32
Max Trans Violations:  32
Max Cap Violations:   0
-----

Hostname: ict-chipin.sot.pdpu.ac.in

Compile CPU Statistics
-----
Resource Sharing:        0.01
Logic Optimization:     0.24
Mapping Optimization:   0.24
-----
Overall Compile Time:   3.06
Overall Compile Wall Clock Time: 3.26
-----

Hostname: ict-chipin.sot.pdpu.ac.in

Compile CPU Statistics
-----
Resource Sharing:        0.01
Logic Optimization:     0.24
Mapping Optimization:   0.24
-----
Overall Compile Time:   3.06
Overall Compile Wall Clock Time: 3.26
-----

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0
```

10). Power report: - (**report_power**)

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
(0.00%)					
(0.00%)					
(0.00%)					
(79.70%) i					
(13.93%)					
(0.00%)					
(6.37%)					
Total	12.3041 uW	0.3702 uW	2.4190e+06 pW	15.0932 uW	
1					

11). Units Report: - (**report_units**)

```
*****
Units
-----
Time_unit      : 1.0e-09 Second(ns)
Capacitive_load_unit : 1.0e-15 Farad(FF)
Resistance_unit    : 1.0e+6 Ohm(Mohm)
Voltage_unit       : 1 Volt
Power_unit         : N/A
Current_unit       : 1.0e-06 Amp(uA)
```

Floor planning, Power planning, Placement, Clock Tree Synthesis, and Routing in ICC: -

• Launch ICC2

icc2_shell

start_gui

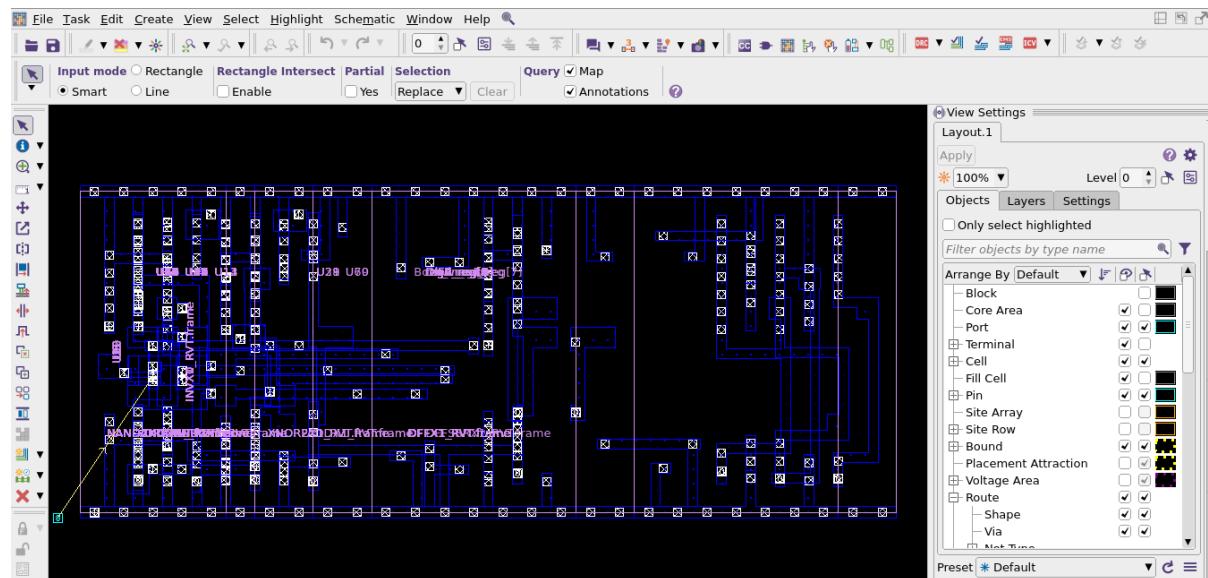
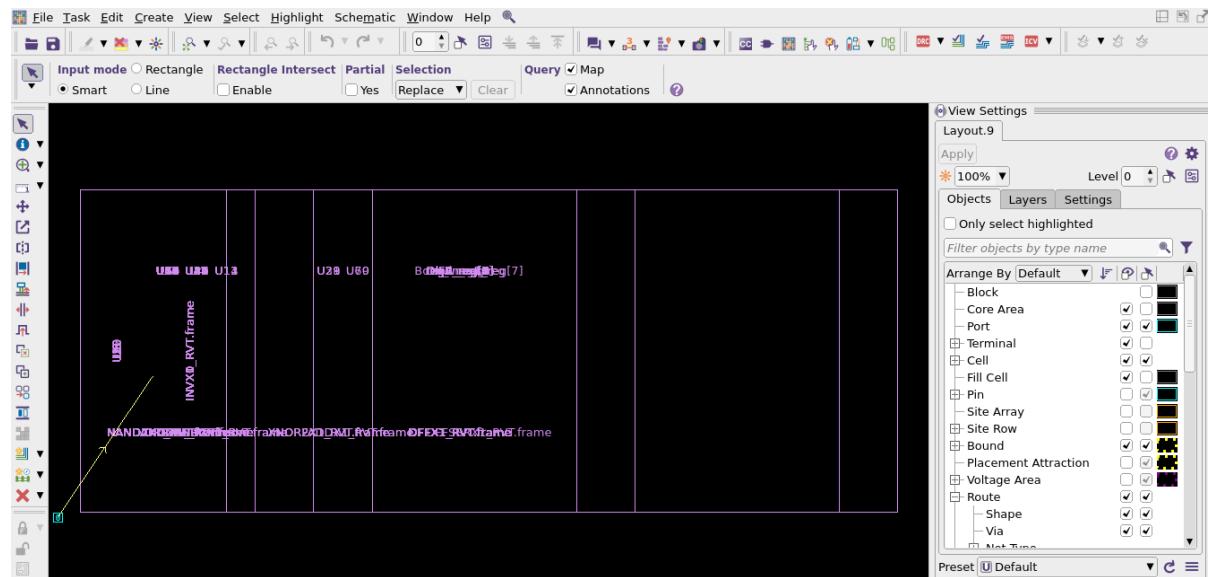
Access the ICCII directory in the terminal.

Navigated to the scripts

directory :-

Floor Planning

1). Implement The Circuit: -



(including pins)

2). Scenario Used : -

```

Open Save
floorplan.tcl
~/Documents/manav/RTL2GDSII/CCII/scripts
set PDK_PATH ../../ref

create_lib -ref_lib $PDK_PATH/lib/ndm/saed32rvt_c.ndm 8_BIT__SUB_LIB5
read_verilog {../../DC/results/subtractor_8bit.mapped.v} -library 8_BIT__SUB_LIB5 -design 8_bits -top 8_bits

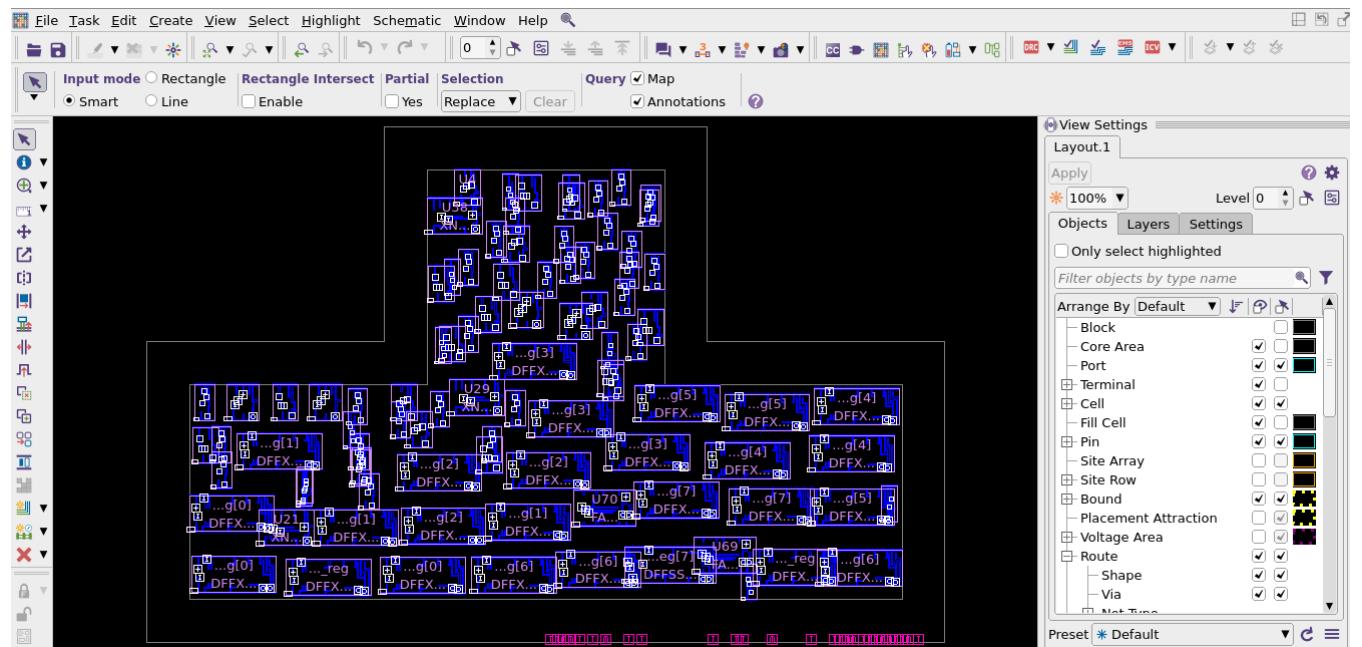
#open the lib and block after saving
open_lib 8_BIT__SUB_LIB5
open_block 8_bits

#scenario: -
initialize_floorplan -core_utilization 0.6 -shape T -orientation S -core_offset 2 -flip_first_row true
set_individual_pin_constraints -offset {1 20} -sides 8 -ports [get_ports]
place_pins -self
create_placement -floorplan
save_block
save_lib

Saving file "/home/student/Documents/manav/RTL2GDSII/CCII/scripts/floorplan.tcl"...
Tcl Tab Width: 8 Ln 19, Col 1 INS

```

3). Floor Planning (Scenario Implementation): -



Leaf Cell Count: - 92

Cell Area: - 297.60

4). Cell Count : - (report_qor)

The screenshot shows the 'Cell Count' report in the icc2_shell interface. The report displays various cell counts and ratios. The 'Macro Count' is 0.

Category	Value
Hierarchical Cell Count	0
Hierarchical Port Count	0
Leaf Cell Count	92
Buf/Inv Cell Count	10
Buf Cell Count	0
Inv Cell Count	10
Combinational Cell Count	66
Single-bit Isolation Cell Count	0
Multi-bit Isolation Cell Count	0
Isolation Cell Banking Ratio	0.00%
Single-bit Level Shifter Cell Count	0
Multi-bit Level Shifter Cell Count	0
Level Shifter Cell Banking Ratio	0.00%
Single-bit ELS Cell Count	0
Multi-bit ELS Cell Count	0
ELS Cell Banking Ratio	0.00%
Sequential Cell Count	26
Integrated Clock-Gating Cell Count	0
Sequential Macro Cell Count	0
Single-bit Sequential Cell Count	26
Multi-bit Sequential Cell Count	0
Sequential Cell Banking Ratio	0.00%
BitsPerflop	1.00
Macro Count	0

5). Cell Area: - (report_qor)

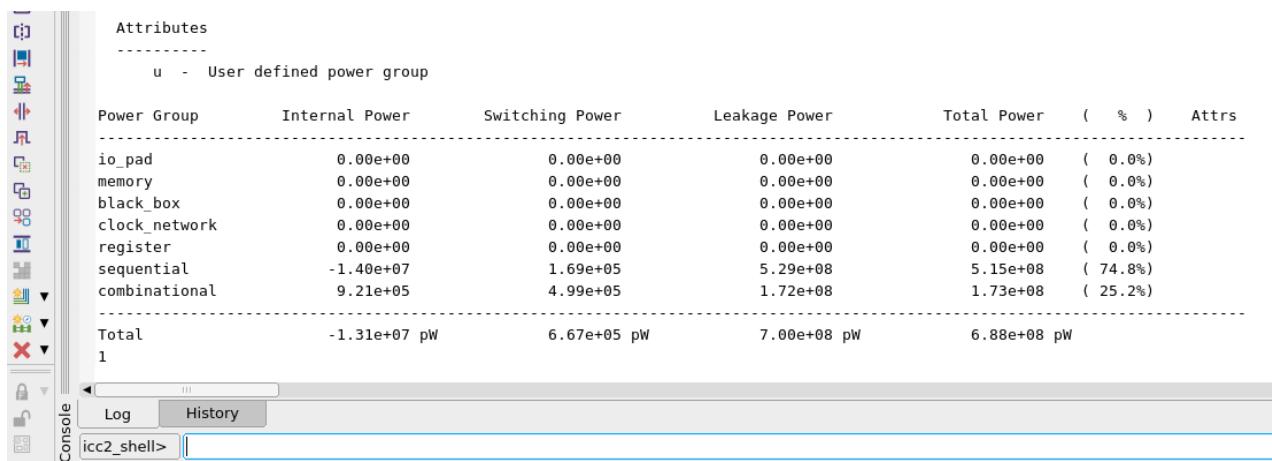
The screenshot shows the 'Area' report in the icc2_shell interface. It includes sections for Combinational Area, Noncombinational Area, and Design Rules. The 'Net Length' is 956.03.

Category	Value
Combinational Area	125.29
Noncombinational Area	172.31
Buf/Inv Area	12.71
Total Buffer Area	0.00
Total Inverter Area	12.71
Macro/Black Box Area	0.00
Net Area	0
Net XLength	499.55
Net YLength	456.47
Cell Area (netlist)	297.60
Cell Area (netlist and physical only)	297.60
Net Length	956.03

Design Rules

Category	Value
Total Number of Nets	119
Nets with Violations	0
Max Trans Violations	0
Max Cap Violations	0

6). Power Report: - (report_power)

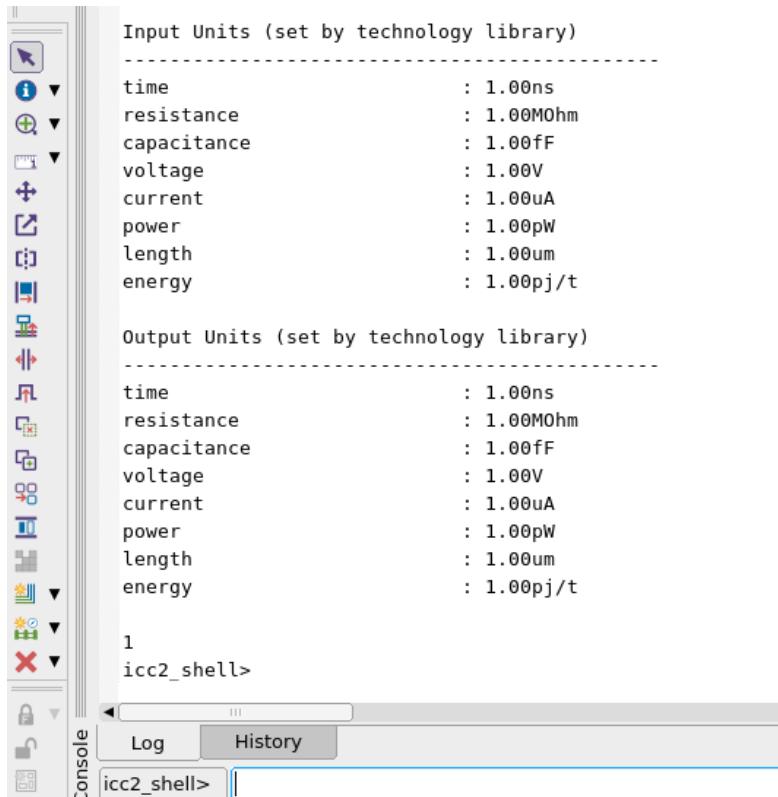


The screenshot shows the icc2_shell interface with a power report table. The table details power consumption across various groups:

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
clock_network	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
register	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
sequential	-1.40e+07	1.69e+05	5.29e+08	5.15e+08	(74.8%)	
combinational	9.21e+05	4.99e+05	1.72e+08	1.73e+08	(25.2%)	
Total	-1.31e+07 pW	6.67e+05 pW	7.00e+08 pW	6.88e+08 pW		
1						

Console Log History icc2_shell>

7). Units Report: - (report_units)



The screenshot shows the icc2_shell interface with a units report table. It lists input and output units defined by the technology library:

Input Units (set by technology library)	
time	: 1.00ns
resistance	: 1.00MΩ
capacitance	: 1.00fF
voltage	: 1.00V
current	: 1.00uA
power	: 1.00pW
length	: 1.00um
energy	: 1.00pj/t

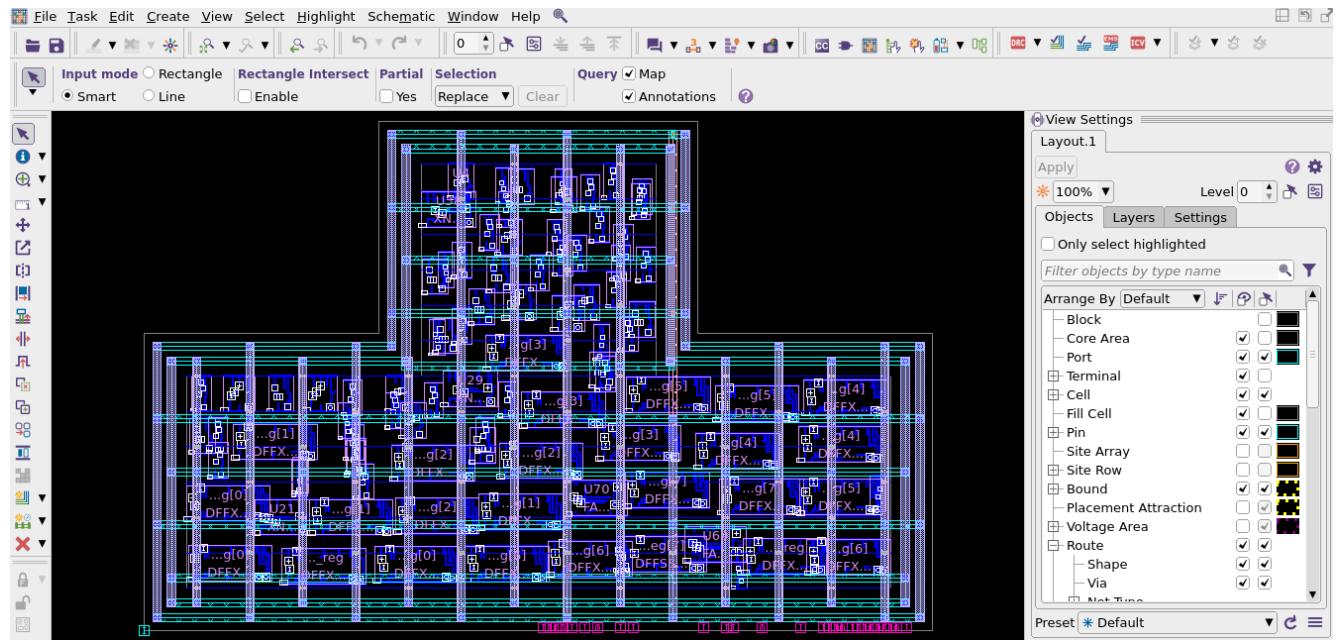
Output Units (set by technology library)	
time	: 1.00ns
resistance	: 1.00MΩ
capacitance	: 1.00fF
voltage	: 1.00V
current	: 1.00uA
power	: 1.00pW
length	: 1.00um
energy	: 1.00pj/t

1
icc2_shell>

Console Log History icc2_shell> |

Power Planning

1). Output: -



Leaf Cell Count: - 92

Cell Area: - 297.60

2). Cell Count : - (report_qor)

```
Cell Count
-----
Hierarchical Cell Count:          0
Hierarchical Port Count:         0
Leaf Cell Count:                 92
Buf/Inv Cell Count:              10
Buf Cell Count:                  0
Inv Cell Count:                  10
Combinational Cell Count:        66
    Single-bit Isolation Cell Count:      0
    Multi-bit Isolation Cell Count:      0
    Isolation Cell Banking Ratio:       0.00%
    Single-bit Level Shifter Cell Count: 0
    Multi-bit Level Shifter Cell Count: 0
    Level Shifter Cell Banking Ratio:   0.00%
    Single-bit ELS Cell Count:           0
    Multi-bit ELS Cell Count:           0
    ELS Cell Banking Ratio:            0.00%
Sequential Cell Count:             26
    Integrated Clock-Gating Cell Count: 0
    Sequential Macro Cell Count:        0
    Single-bit Sequential Cell Count:   26
    Multi-bit Sequential Cell Count:   0
    Sequential Cell Banking Ratio:     0.00%
    BitsPerflop:                      1.00
Macro Count:                      0

Log History
icc2_shell> 
```

2). Cell Area : - (report_qor)

```

Area
-----
Combinational Area: 125.29
Noncombinational Area: 172.31
Buf/Inv Area: 12.71
Total Buffer Area: 0.00
Total Inverter Area: 12.71
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 499.55
Net YLength: 456.47

-----
Cell Area (netlist): 297.60
Cell Area (netlist and physical only): 297.60
Net Length: 956.03

Design Rules
-----
Total Number of Nets: 119
Nets with Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0

1
icc2_shell>

```

The screenshot shows the Cadence IC Compiler interface with the 'Console' tab selected. The output window displays the results of the 'report_qor' command. It provides detailed area statistics for combinational, non-combinational, and buffer/inverter areas, along with net dimensions and design rule violations. The 'Log' and 'History' tabs are also visible in the interface.

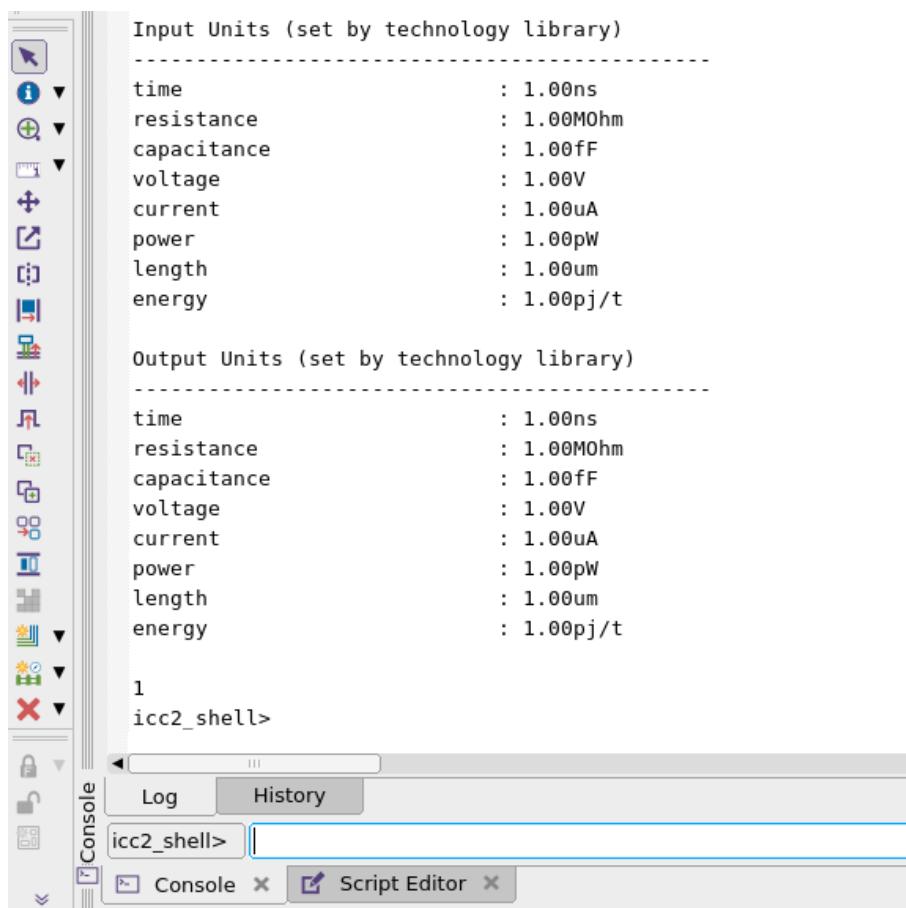
3). Power Report : - (report_power)

Attributes						
u - User defined power group						
Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
clock_network	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
register	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
sequential	-1.40e+07	1.69e+05	5.29e+08	5.15e+08	(74.8%)	
combinational	9.21e+05	4.99e+05	1.72e+08	1.73e+08	(25.2%)	
Total	-1.31e+07 pW	6.67e+05 pW	7.00e+08 pW	6.88e+08 pW		

1
icc2_shell>

The screenshot shows the Cadence IC Compiler interface with the 'Console' tab selected. The output window displays the results of the 'report_power' command. It provides a detailed power consumption breakdown by power group, including internal, switching, and leakage power, along with a total power summary. The 'Log' and 'History' tabs are also visible in the interface.

4). Units Report: - (**report_units**)



The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The main window displays the output of the 'report_units' command, which lists standard physical quantities and their corresponding units. The output is organized into two sections: 'Input Units (set by technology library)' and 'Output Units (set by technology library)'. Both sections show identical values for each unit type.

```
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MOhm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

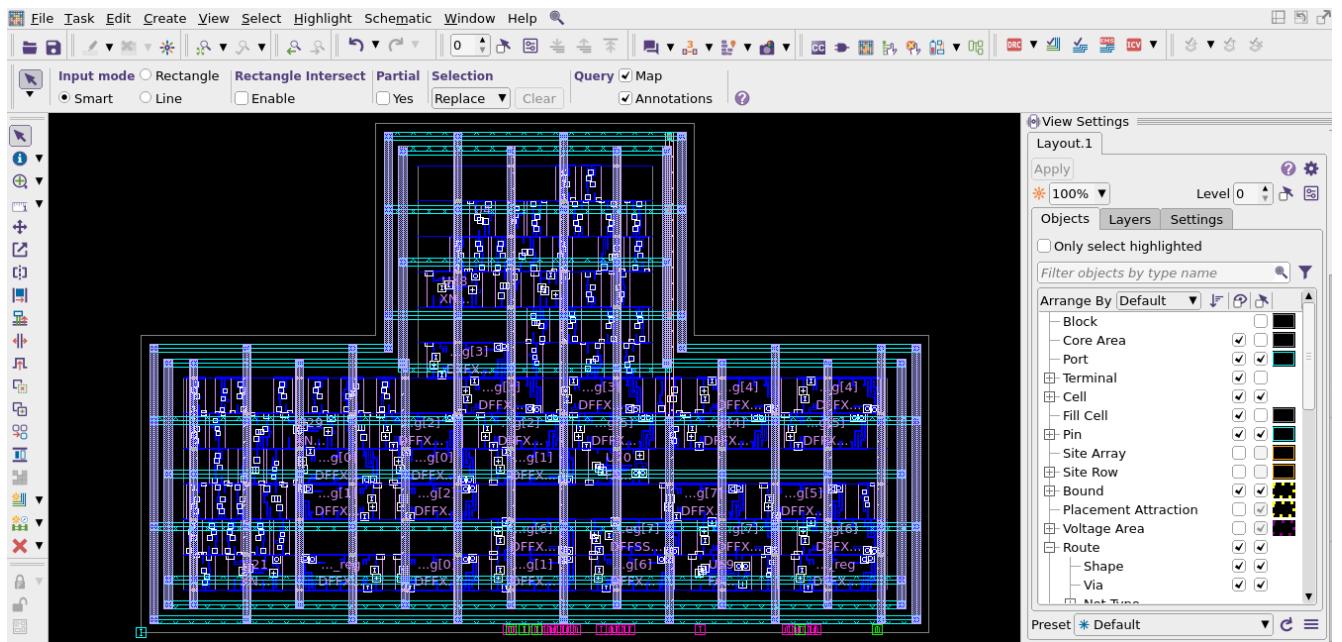
Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MOhm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

1
icc2_shell>
```

Below the main window, the 'Console' tab is highlighted in blue, indicating it is active. Other tabs like 'Log' and 'History' are also visible. At the bottom of the interface, there are tabs for 'Console' and 'Script Editor'.

Placement

1). Output: -



Slack time: - 3.53

Leaf Cell Count: - 85

Cell Area: - 309.55

2). Timing Analysis: - (report_timing)

Point	Incr	Path
<hr/>		
clock Clock (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	1.50	1.50 f
B[7] (in)	0.00	1.50 f
regB_reg[7]/SETB (DFFSSRX1_RVT)	0.00	1.50 f
data arrival time		1.50
<hr/>		
clock Clock (rise edge)	6.80	6.80
clock network delay (ideal)	0.00	6.80
regB_reg[7]/CLK (DFFSSRX1_RVT)	0.00	6.80 r
clock uncertainty	-1.60	5.20
library setup time	-0.17	5.03
data required time		5.03
<hr/>		
data required time		5.03
data arrival time		-1.50
<hr/>		
slack (MET)		3.53
<hr/>		
1		
icc2_shell>		
<hr/>		
Log		
History		
icc2_shell>		
<hr/>		
Console		
Script Editor		

3). Violating Paths: - (report_qor)

```
Scenario      'func::nom'
Timing Path Group  '**in2reg_default**'

-----
Levels of Logic:          0
Critical Path Length:    1.50
Critical Path Slack:     3.53
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0

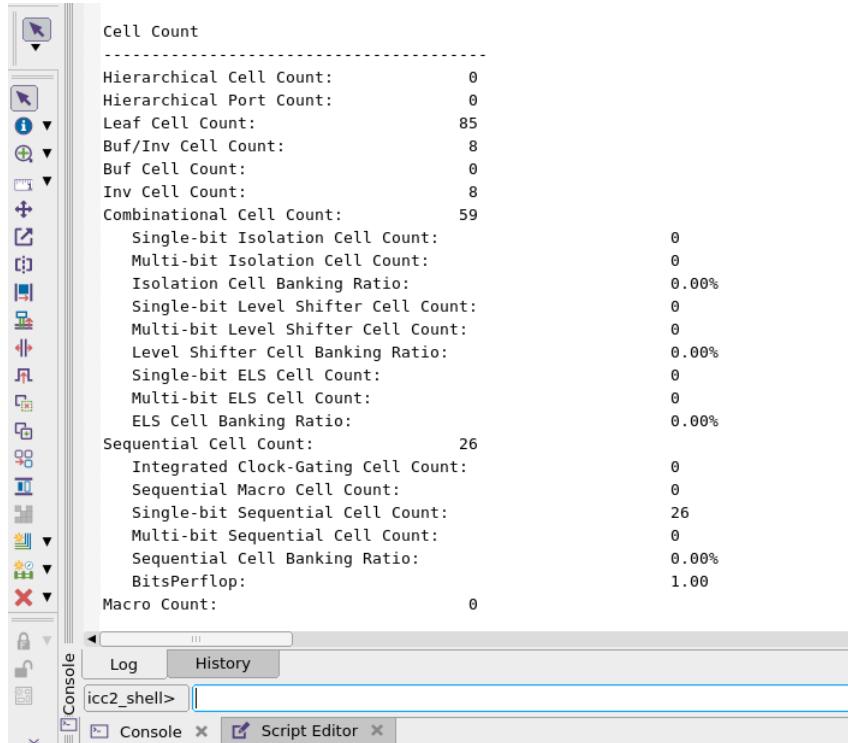
-----
Scenario      'func::nom'
Timing Path Group  '**reg2out_default**'

-----
Levels of Logic:          0
Critical Path Length:    0.08
Critical Path Slack:     4.32
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0

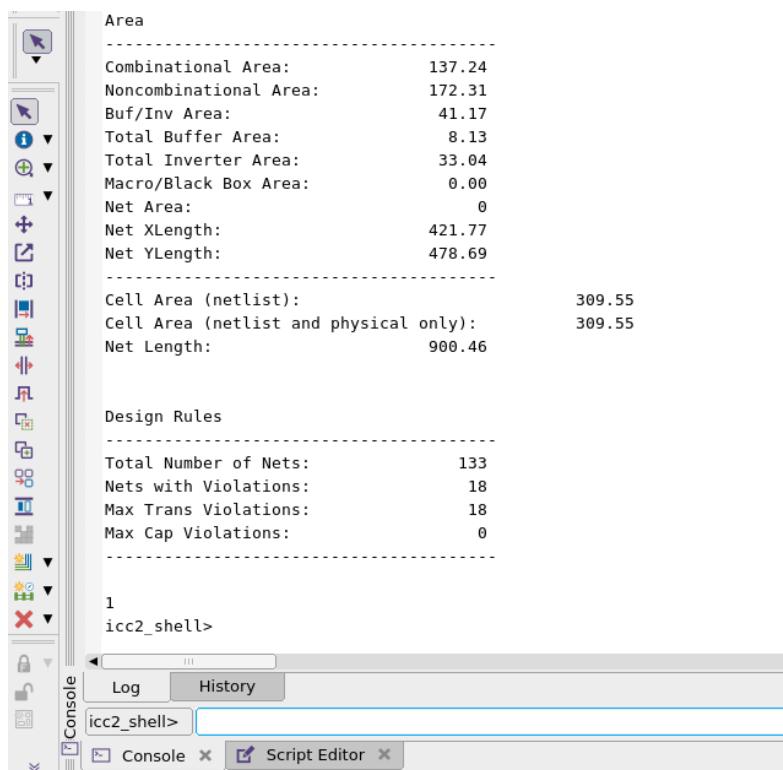
-----
Scenario      'func::nom'
Timing Path Group  'Clock'

-----
Levels of Logic:          9
Critical Path Length:    0.50
Critical Path Slack:     4.67
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
Worst Hold Violation:    0.00
Total Hold Violation:    0.00
No. of Hold Violations:  0
```

4). Cell Count: - (report_qor)



5). Cell Area: - (report_qor)



```

Area
-----
Combinational Area: 137.24
Noncombinational Area: 172.31
Buf/Inv Area: 41.17
Total Buffer Area: 8.13
Total Inverter Area: 33.04
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 421.77
Net YLength: 478.69

-----
Cell Area (netlist): 309.55
Cell Area (netlist and physical only): 309.55
Net Length: 900.46

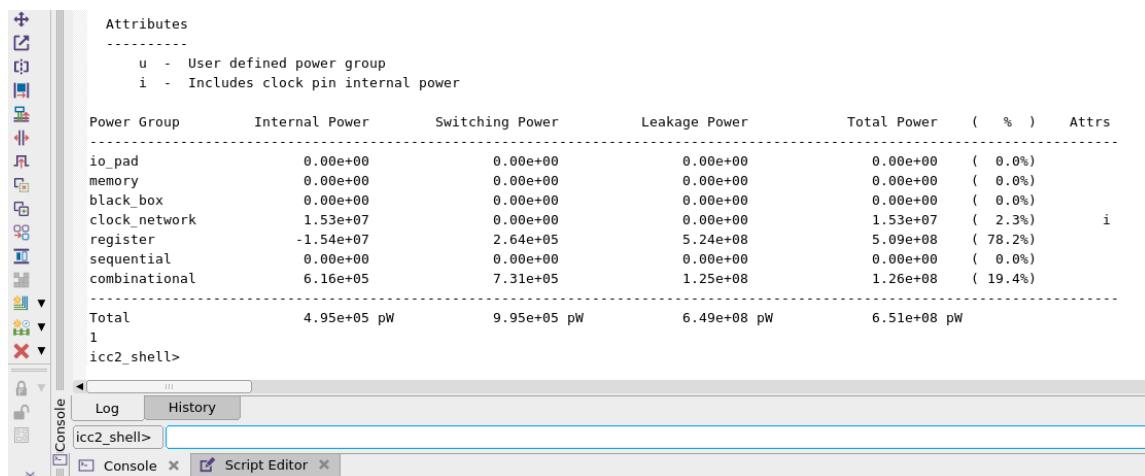
Design Rules
-----
Total Number of Nets: 133
Nets with Violations: 18
Max Trans Violations: 18
Max Cap Violations: 0

1
icc2_shell>

```

The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The output window displays the results of the 'report_qor' command, including detailed area statistics for combinational, non-combinational, and buffer/inverter areas, along with net length information. Below this, design rule violations are listed. The command prompt 'icc2_shell>' is visible at the bottom.

6). Power Report: - (report_power)

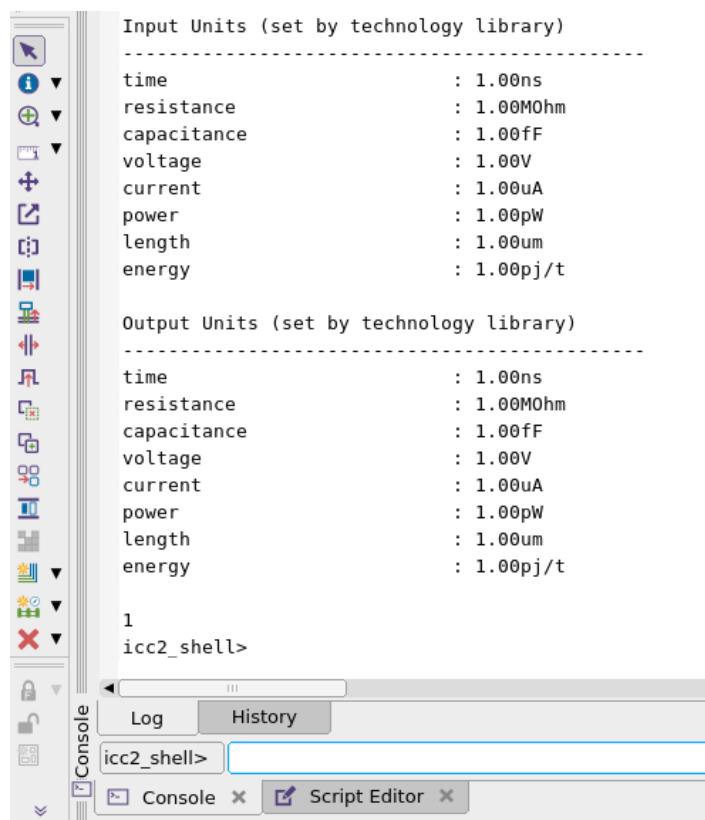


Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
clock_network	1.53e+07	0.00e+00	0.00e+00	1.53e+07	(2.3%)	i
register	-1.54e+07	2.64e+05	5.24e+08	5.09e+08	(78.2%)	
sequential	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
combinational	6.16e+05	7.31e+05	1.25e+08	1.26e+08	(19.4%)	
Total	4.95e+05 pW	9.95e+05 pW	6.49e+08 pW	6.51e+08 pW		

1
icc2_shell>

The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The output window displays the results of the 'report_power' command, providing a detailed power breakdown by power group (Internal, Switching, Leakage) and total power consumption. The command prompt 'icc2_shell>' is visible at the bottom.

7). Units Report: - (**report_units**)



The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The output window displays the results of the **report_units** command. It is divided into two sections: 'Input Units (set by technology library)' and 'Output Units (set by technology library)'. Both sections list the same units with their respective values.

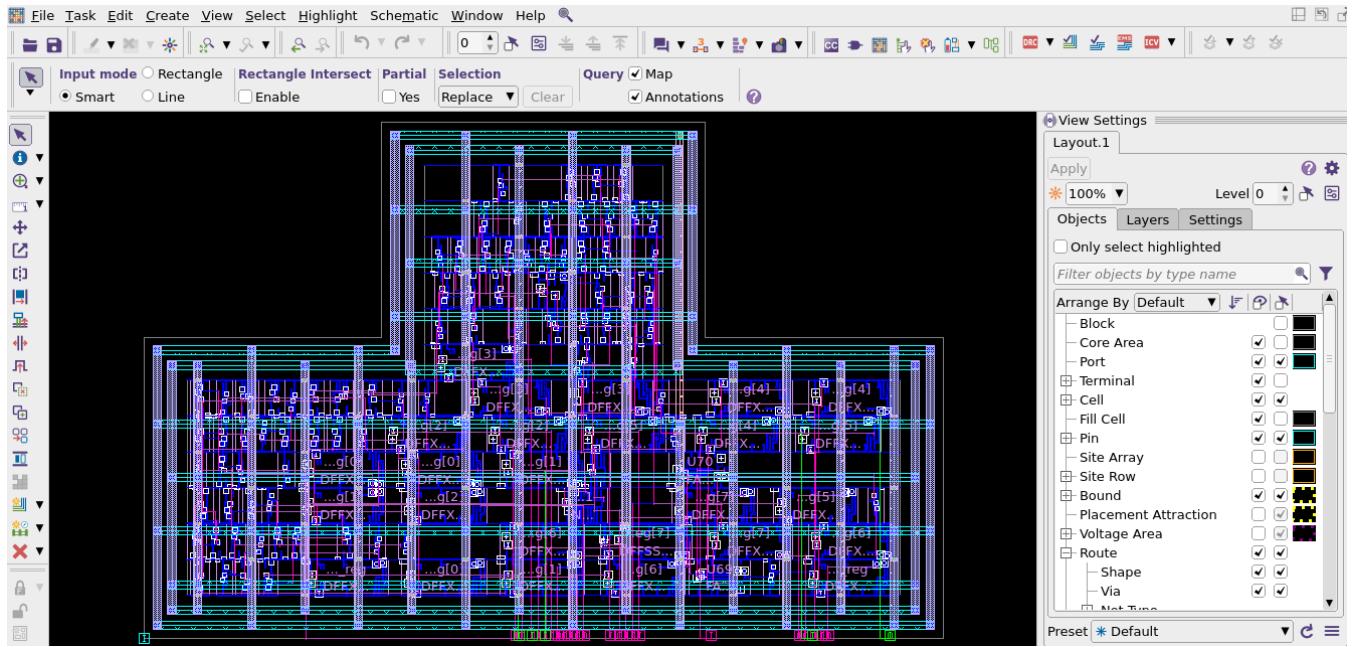
```
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00Mohm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00Mohm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

1
icc2_shell>
```

Clock Tree Synthesis (CTS)

1). Output: -



Slack time: - 3.53

Leaf Cell Count: - 111

Cell Area: - 309.55

2). Timing Analysis: - (report_timing)

Point	Incr	Path
<hr/>		
clock Clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.04	0.04
input external delay	1.50	1.54 f
B[7] (in)	0.00	1.54 f
regB_reg[7]/SETB (DFFSSRX1_RVT)	0.00	1.54 f
data arrival time		1.54
<hr/>		
clock Clock (rise edge)	6.80	6.80
clock network delay (propagated)	0.06	6.86
regB_reg[7]/CLK (DFFSSRX1_RVT)	0.00	6.86 r
clock uncertainty	-1.60	5.26
library setup time	-0.19	5.07
data required time		5.07
<hr/>		
data required time		5.07
data arrival time		-1.54
<hr/>		
slack (MET)		3.53

1
icc2_shell>

Log History
Console Script Editor

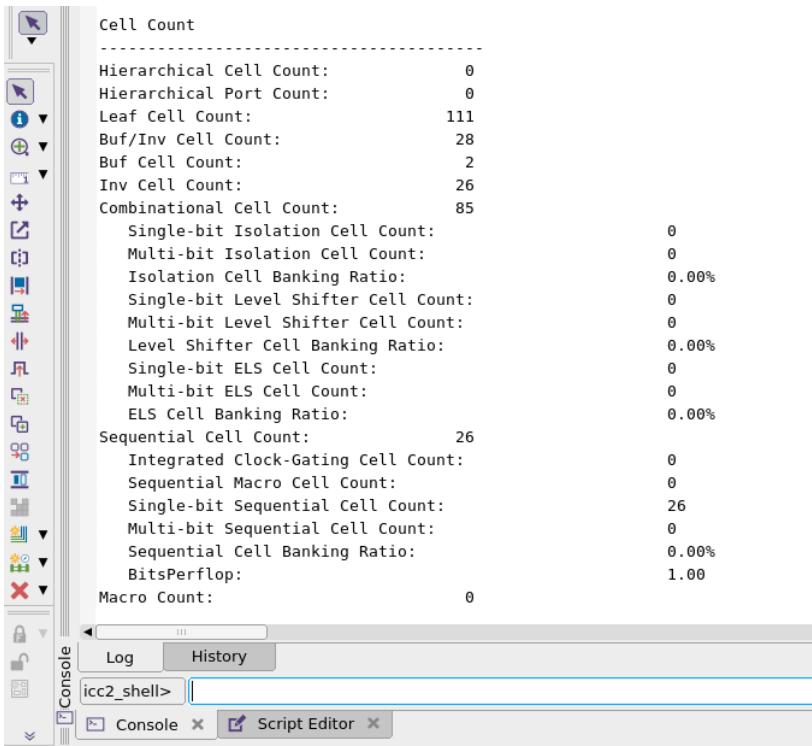
3). Violating Paths: - (report_qor)

```
Scenario      'func::nom'
Timing Path Group '**in2reg_default**'
-----
Levels of Logic:          0
Critical Path Length:    1.50
Critical Path Slack:     3.53
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
-----

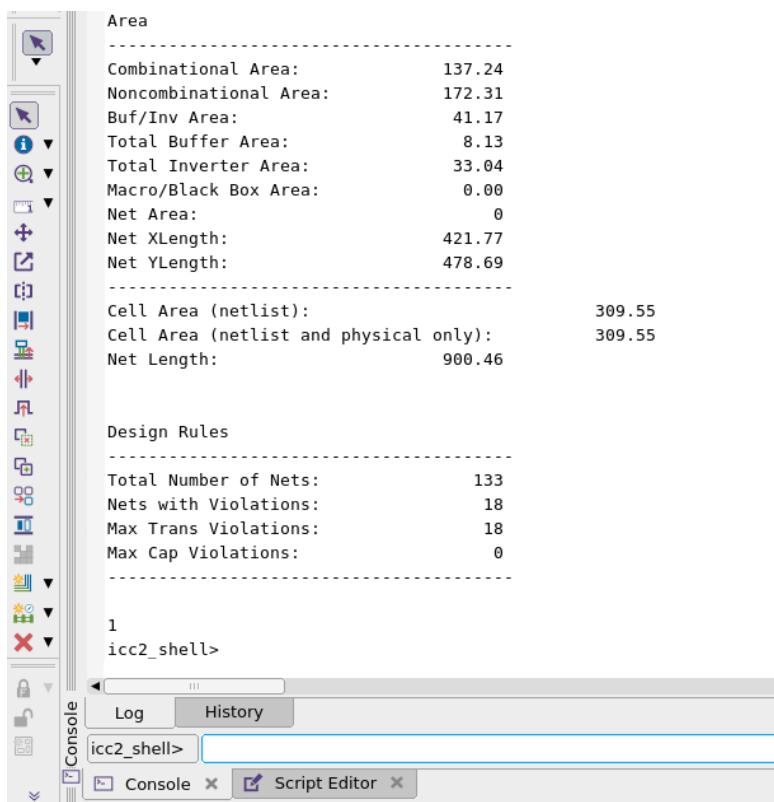
Scenario      'func::nom'
Timing Path Group '**reg2out_default**'
-----
Levels of Logic:          0
Critical Path Length:    0.09
Critical Path Slack:     4.28
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
-----

Scenario      'func::nom'
Timing Path Group 'Clock'
-----
Levels of Logic:          10
Critical Path Length:    0.52
Critical Path Slack:     4.65
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
```

4). Cell Count: - (report_qor)



5). Cell Area: - (report_qor)



```

Area
-----
Combinational Area: 137.24
Noncombinational Area: 172.31
Buf/Inv Area: 41.17
Total Buffer Area: 8.13
Total Inverter Area: 33.04
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 421.77
Net YLength: 478.69

-----
Cell Area (netlist): 309.55
Cell Area (netlist and physical only): 309.55
Net Length: 900.46

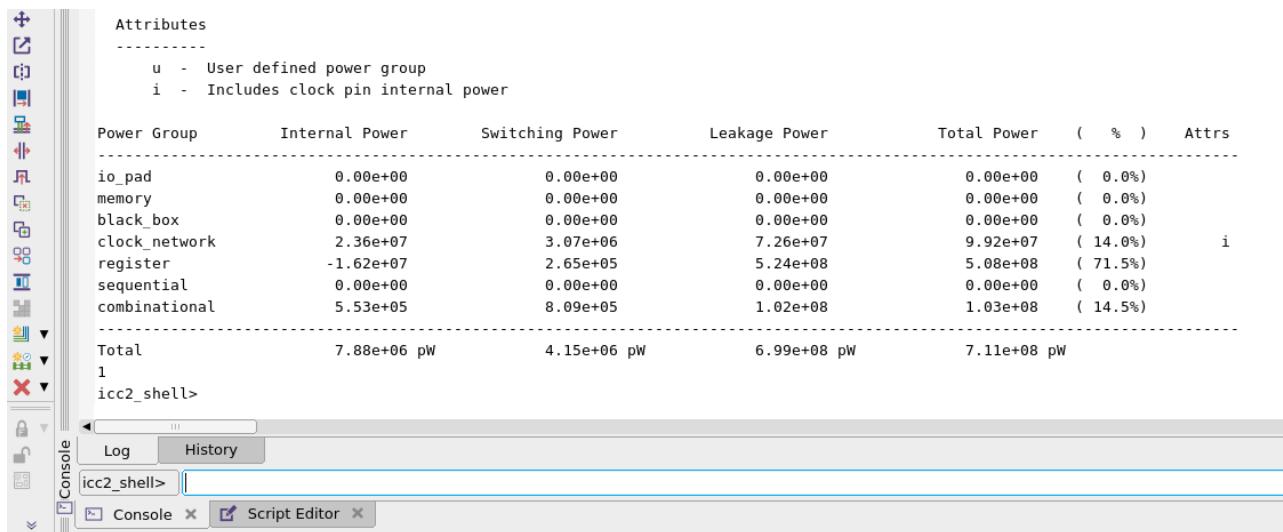
Design Rules
-----
Total Number of Nets: 133
Nets with Violations: 18
Max Trans Violations: 18
Max Cap Violations: 0

1
icc2_shell>

```

The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The 'Log' tab is active. The console window displays the output of the 'report_qor' command, which provides detailed area statistics for combinational, non-combinational, and buffer/inverter areas, along with total net lengths. It also includes a section on design rules, showing the total number of nets, nets with violations, and specific max trans and cap violation counts. The interface includes various toolbars and a script editor tab at the bottom.

6). Power Report: - (report_power)



```

Attributes
-----
  u - User defined power group
  i - Includes clock pin internal power

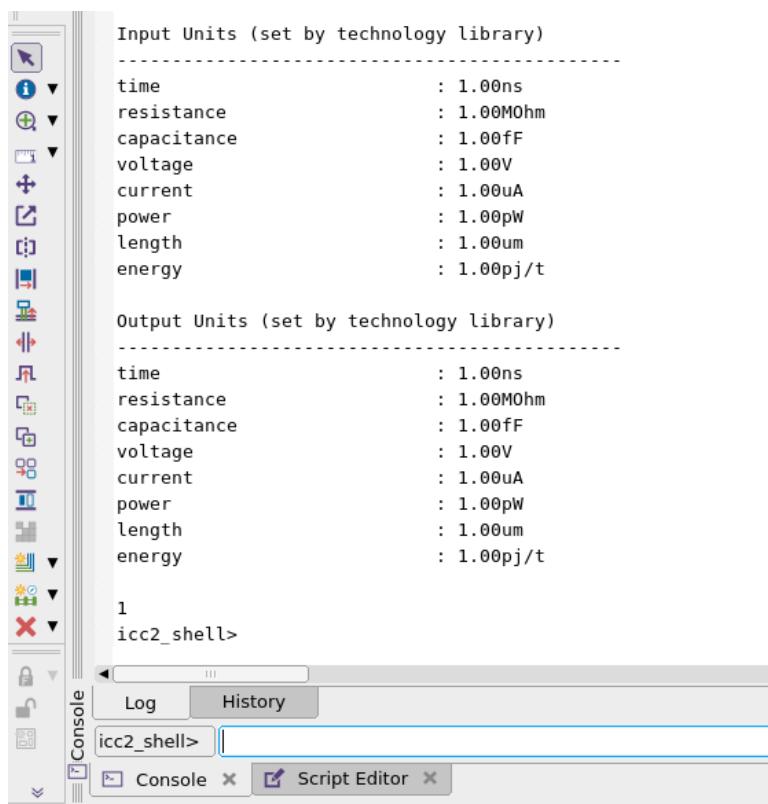
Power Group      Internal Power      Switching Power      Leakage Power      Total Power      ( % )      Attrs
-----
io_pad          0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
memory          0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
black_box        0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
clock_network   2.36e+07          3.07e+06          7.26e+07      9.92e+07      ( 14.0%)      i
register         -1.62e+07         2.65e+05          5.24e+08      5.08e+08      ( 71.5%)
sequential        0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
combinational    5.53e+05          8.09e+05          1.02e+08      1.03e+08      ( 14.5%)
-----
Total           7.88e+06 pW       4.15e+06 pW       6.99e+08 pW      7.11e+08 pW

1
icc2_shell>

```

The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The 'Log' tab is active. The console window displays the output of the 'report_power' command, which provides a detailed power report for various power groups. The report includes columns for Internal Power, Switching Power, Leakage Power, and Total Power, along with their respective percentages. The 'Attributes' section indicates that user-defined power groups are included. The interface includes various toolbars and a script editor tab at the bottom.

7). Units Report: - (**report_units**)



The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The main window displays the output of the 'report_units' command, which lists standard physical quantities and their base units. The output is organized into two sections: 'Input Units (set by technology library)' and 'Output Units (set by technology library)'. Both sections show identical values for each unit type.

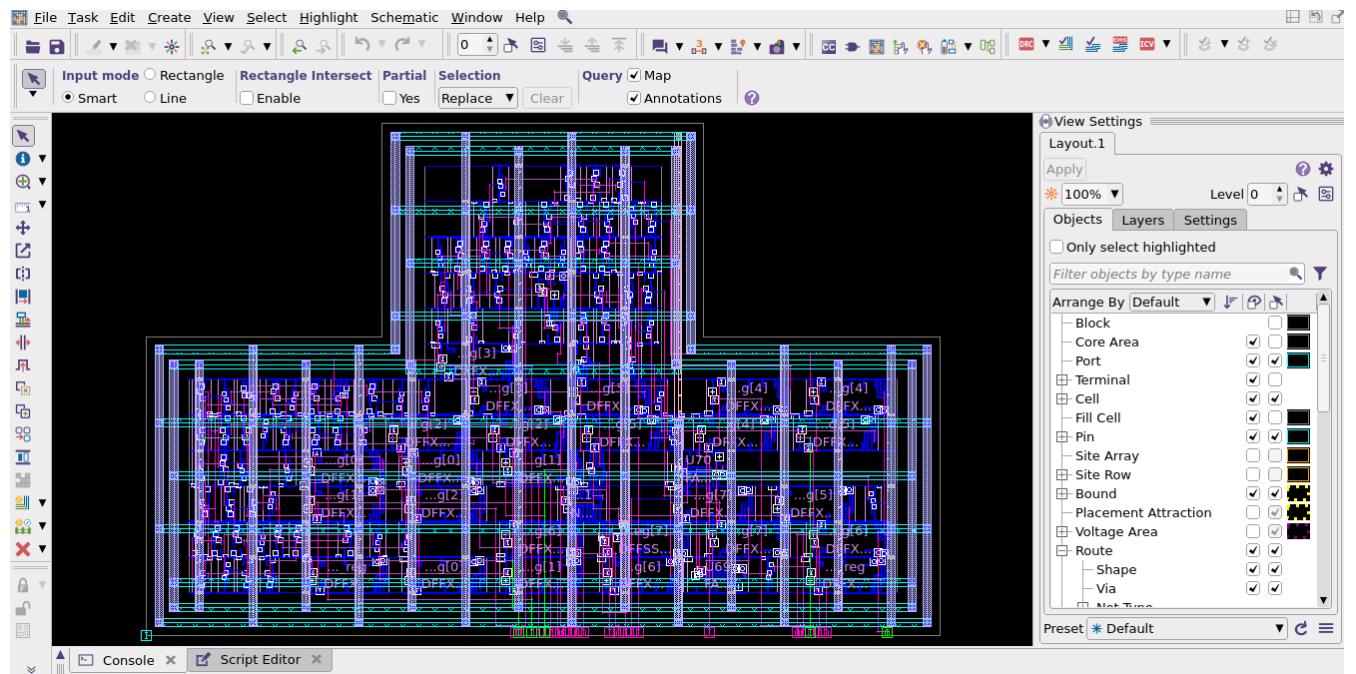
```
Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MOhm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00MOhm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

1
icc2_shell>
```

Routing

1). Output: -



Slack time: - 3.53

Leaf Cell Count: - 111

Cell Area: - 309.55

2). Timing Analysis: - (report_timing)

Point	Incr	Path
<hr/>		
clock Clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.04	0.04
input external delay	1.50	1.54 f
B[7] (in)	0.00	1.54 f
regB_reg[7]/SETB (DFFSSRX1_RVT)	0.00	1.54 f
data arrival time		1.54
<hr/>		
clock Clock (rise edge)	6.80	6.80
clock network delay (propagated)	0.06	6.86
regB_reg[7]/CLK (DFFSSRX1_RVT)	0.00	6.86 r
clock uncertainty	-1.60	5.26
library setup time	-0.19	5.07
data required time		5.07
<hr/>		
data required time	5.07	
data arrival time		-1.54
<hr/>		
slack (MET)		3.53
<hr/>		
1		
icc2_shell>		
<hr/>		
Log		
History		
icc2_shell>		
<hr/>		
Console		
Script Editor		

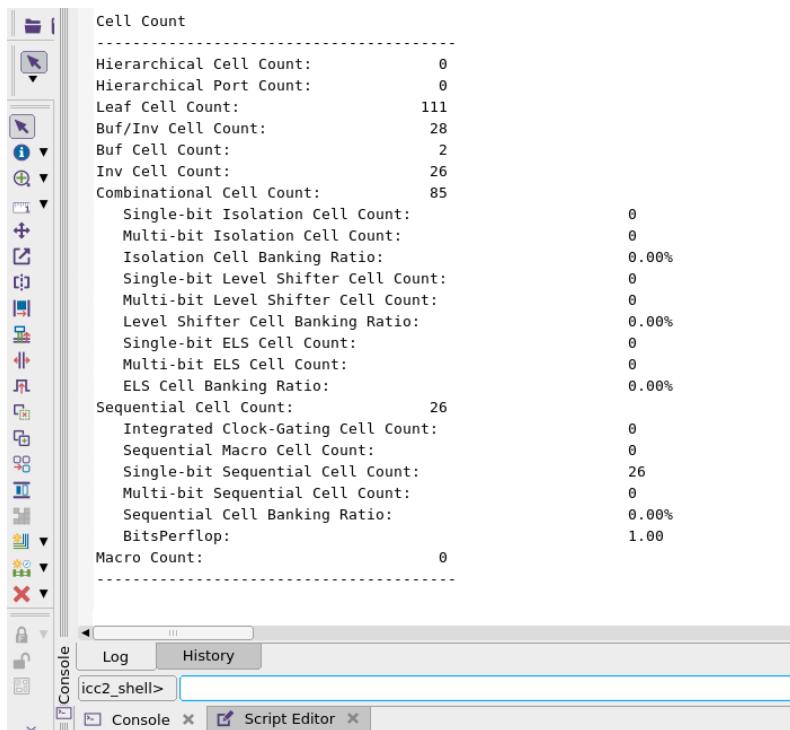
3). Violating Paths: - (report_qor)

```
Scenario      'func::nom'
Timing Path Group '**in2reg_default**'
-----
Levels of Logic:          0
Critical Path Length:    1.50
Critical Path Slack:     3.53
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
-----

Scenario      'func::nom'
Timing Path Group '**reg2out_default**'
-----
Levels of Logic:          0
Critical Path Length:    0.09
Critical Path Slack:     4.29
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
-----

Scenario      'func::nom'
Timing Path Group 'Clock'
-----
Levels of Logic:          10
Critical Path Length:    0.52
Critical Path Slack:     4.65
Critical Path Clk Period: 6.80
Total Negative Slack:    0.00
No. of Violating Paths:   0
Worst Hold Violation:    0.00
Total Hold Violation:    0.00
No. of Hold Violations:  0
```

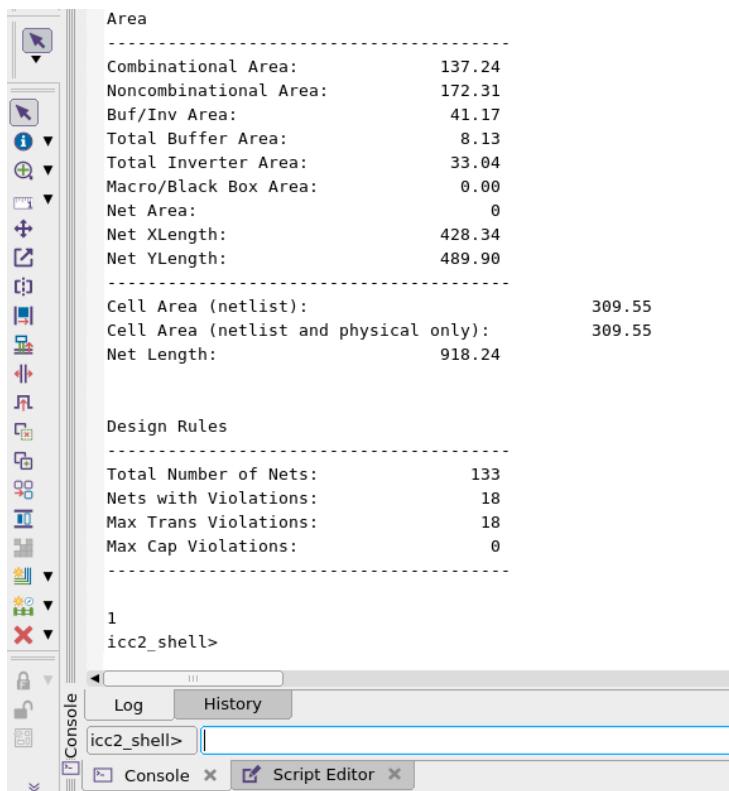
4). Cell Count: - (report_qor)



```
Cell Count
-----
Hierarchical Cell Count:          0
Hierarchical Port Count:         0
Leaf Cell Count:                 111
Buf/Inv Cell Count:              28
Buf Cell Count:                  2
Inv Cell Count:                  26
Combinational Cell Count:        85
  Single-bit Isolation Cell Count: 0
  Multi-bit Isolation Cell Count: 0
  Isolation Cell Banking Ratio:  0.00%
  Single-bit Level Shifter Cell Count: 0
  Multi-bit Level Shifter Cell Count: 0
  Level Shifter Cell Banking Ratio:  0.00%
  Single-bit ELS Cell Count:       0
  Multi-bit ELS Cell Count:       0
  ELS Cell Banking Ratio:        0.00%
Sequential Cell Count:            26
  Integrated Clock-Gating Cell Count: 0
  Sequential Macro Cell Count:      0
  Single-bit Sequential Cell Count: 26
  Multi-bit Sequential Cell Count: 0
  Sequential Cell Banking Ratio:  0.00%
  BitsPerflop:                   1.00
Macro Count:                      0
```

The screenshot shows the Quartus II software interface with the 'Cell Count' report open. The left side features a tree-view navigation pane with various icons for different design components like logic blocks, memory, and peripherals. The right side displays the detailed cell count statistics for the current design. At the bottom, there is a 'Console' window showing the command 'icc2_shell>' and tabs for 'Log' and 'History'. Below the console is a 'Script Editor' tab.

5). Cell Area: - (report_qor)



```

Area
-----
Combinational Area: 137.24
Noncombinational Area: 172.31
Buf/Inv Area: 41.17
Total Buffer Area: 8.13
Total Inverter Area: 33.04
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 428.34
Net YLength: 489.90

-----
Cell Area (netlist): 309.55
Cell Area (netlist and physical only): 309.55
Net Length: 918.24

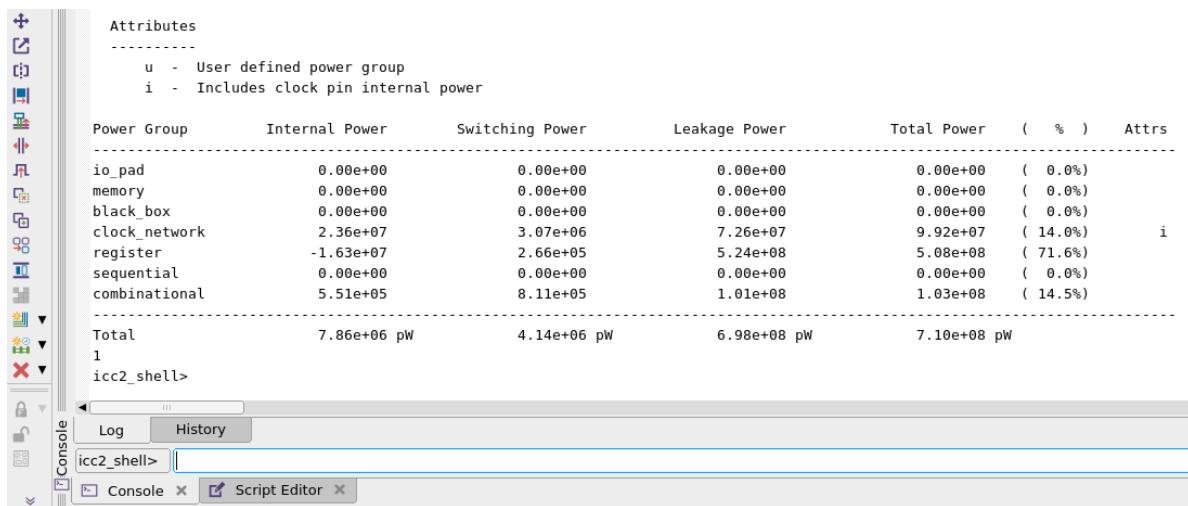
Design Rules
-----
Total Number of Nets: 133
Nets with Violations: 18
Max Trans Violations: 18
Max Cap Violations: 0

1
icc2_shell>

```

The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The 'Script Editor' tab is also visible at the bottom. The main window displays the output of the 'report_qor' command, providing detailed area statistics and design rule violations.

6). Power Report: - (report_power)



```

Attributes
-----
u - User defined power group
i - Includes clock pin internal power

Power Group      Internal Power      Switching Power      Leakage Power      Total Power      ( % )      Attrs
-----
io_pad          0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
memory          0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
black_box        0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
clock_network   2.36e+07          3.07e+06          7.26e+07      9.92e+07      ( 14.0%)      i
register         -1.63e+07         2.66e+05          5.24e+08      5.08e+08      ( 71.6%)
sequential        0.00e+00          0.00e+00          0.00e+00          0.00e+00      ( 0.0%)
combinational    5.51e+05          8.11e+05          1.01e+08      1.03e+08      ( 14.5%)

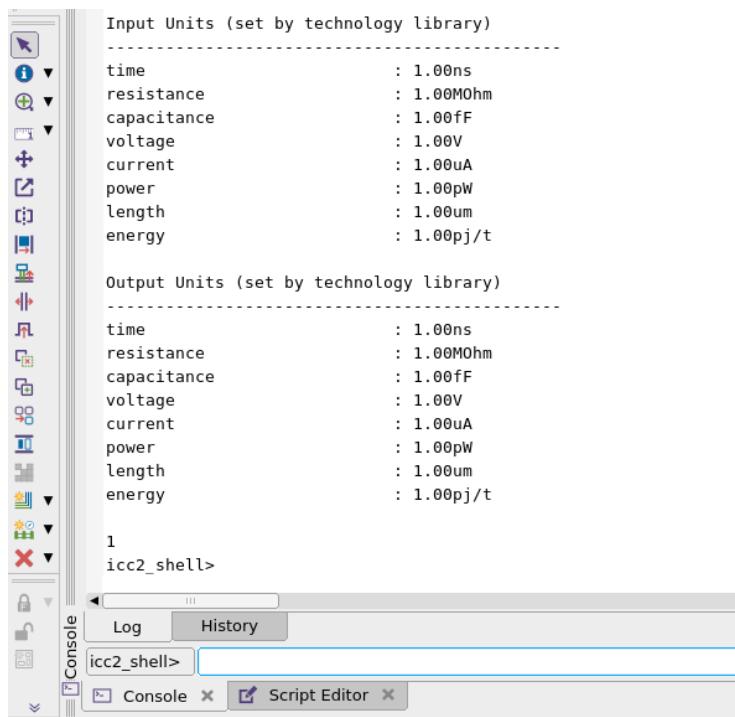
Total           7.86e+06 pW       4.14e+06 pW       6.98e+08 pW      7.10e+08 pW

1
icc2_shell>

```

The screenshot shows the Cadence Design System interface with the 'Console' tab selected. The 'Script Editor' tab is also visible at the bottom. The main window displays the output of the 'report_power' command, showing power consumption by various power groups.

7). Units Report: - (report_units)



```

Input Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00Mohm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

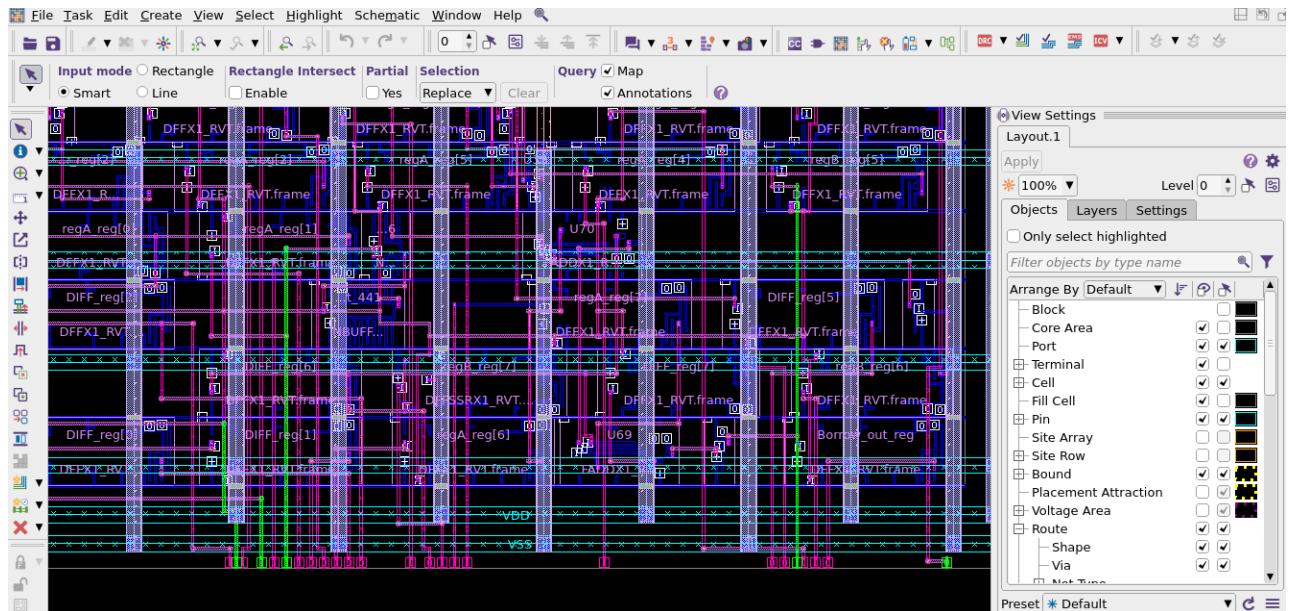
Output Units (set by technology library)
-----
time : 1.00ns
resistance : 1.00Mohm
capacitance : 1.00fF
voltage : 1.00V
current : 1.00uA
power : 1.00pW
length : 1.00um
energy : 1.00pj/t

1
icc2_shell>

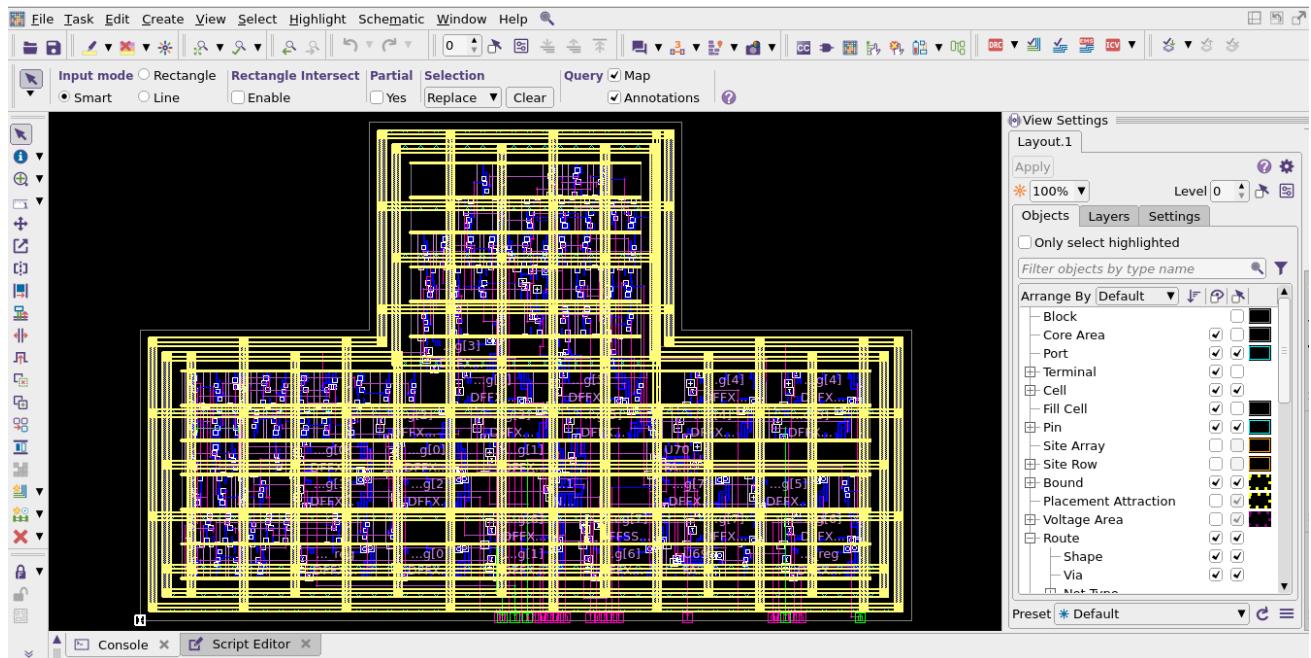
```

The screenshot shows the icc2_shell interface with the "Console" tab selected. The output window displays the results of the "report_units" command, showing input and output units for various physical quantities like time, resistance, and energy.

8). Port Connections



9). VSS & VDD connections: -

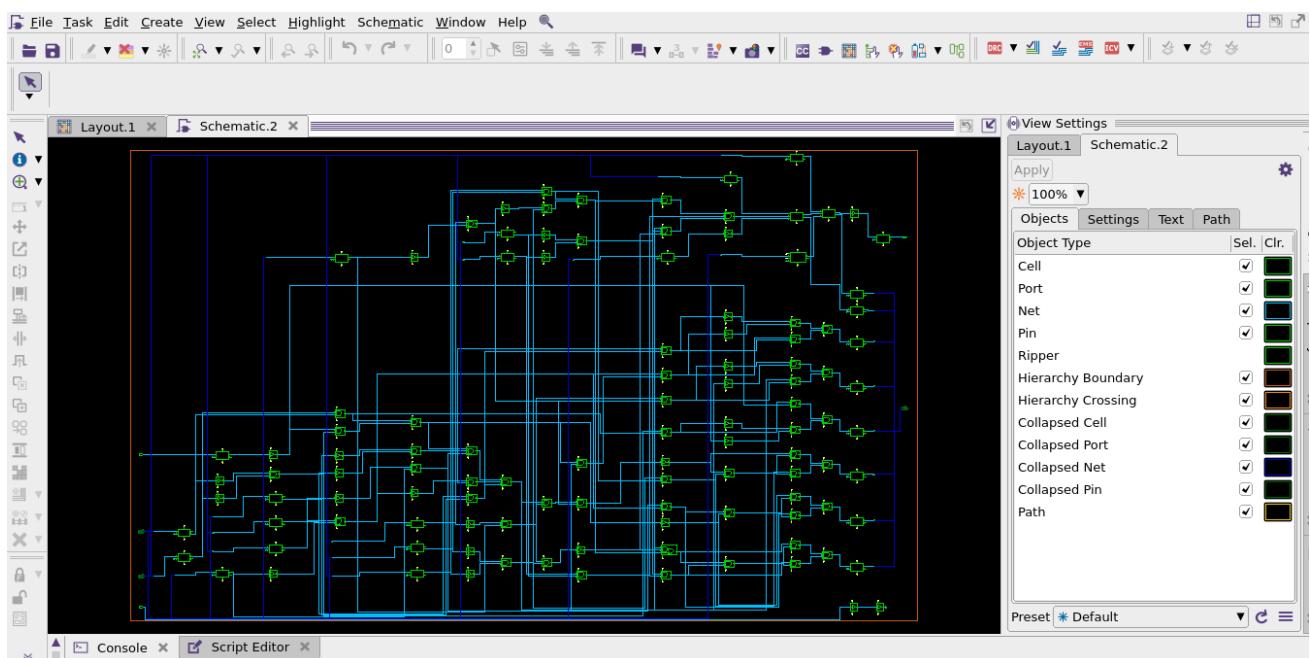
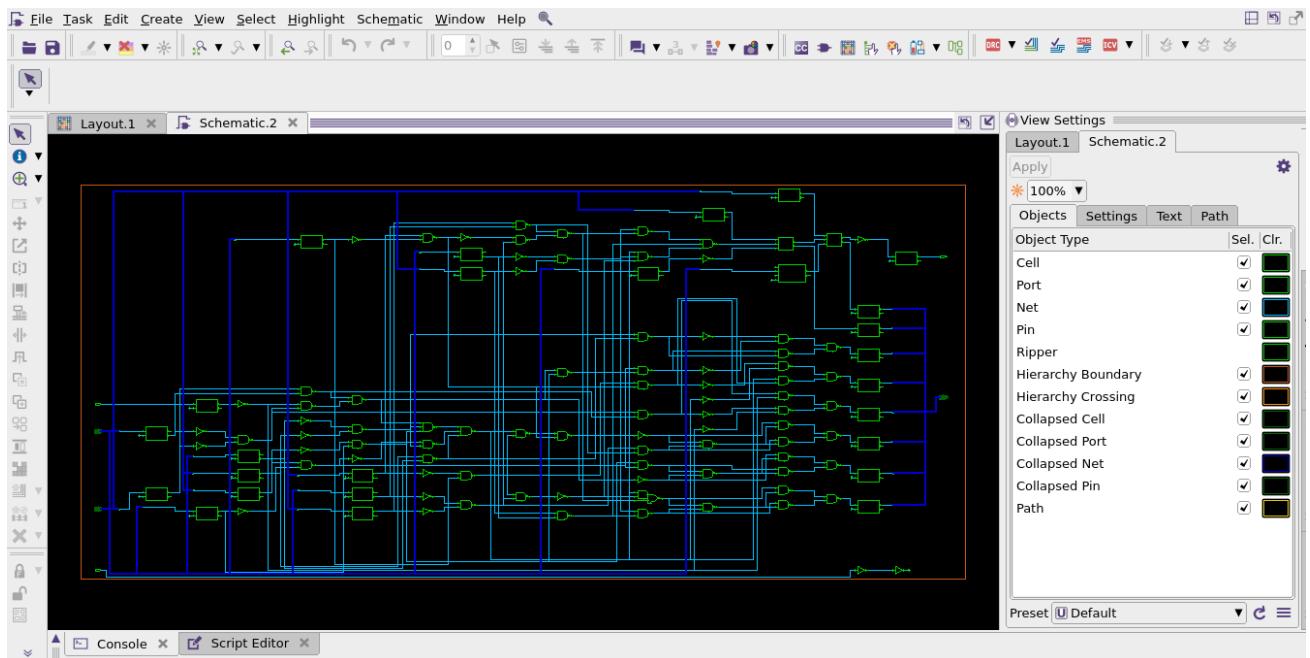


10). Cell and wires connectivity: - (check_pg_connectivity)

```

icc2_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD      Secondary Net:
Primary Net : VSS      Secondary Net:
Loading cell instances...
Number of Standard Cells: 111
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 34
Number of VDD Vias: 250
Number of VDD Terminals: 0
*****Verify net VDD connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 35
Number of VSS Vias: 213
Number of VSS Terminals: 0
*****Verify net VSS connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds.
icc2_shell>
    
```

10). Schematic (ICC2): -



(Schematic showing power components)

Prime Time

Launch Prime Time

```
cd ..../PT
```

```
pt_shell
```

```
source scripts/run_pt_p2.tcl
```

1). Library used in run_pt_p2.tcl: - (saed32rvt_ss0p7vn40c.db)

```
File Edit View Search Terminal Help
set report_default_significant_digits 6 ;

# Set the technology libraries
set link_path "../../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db"
set target_library "../../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db"

# Read routed netlist from ICC2
read_verilog "../../ICCII/results/8_bit_s.routed.v"

# Replace 'subtracter_8bit' with your actual top-level module name in the above .v file
link_design subtracter_8bit
current_design subtracter_8bit

# Read design constraints
read_sdc "../../CONSTRAINTS/8_bit_sub.sdc"

# Read parasitic data from ICC2
read_parasitics "../../ICCII/results/8_sub_func::nom.spf.p2_125.spf"

# Update timing with full analysis
update_timing -full

# Quick reports to terminal
report_timing
report_design

# Save detailed reports
check_timing -verbose > ./reports/check_timing/check_timing.p2_report
report_global_timing > ./reports/timing/report_global_timing.p2_report
report_clock -skew -attribute > ./reports/clock/report_clock.p2_report
report_analysis_coverage > ./reports/analysis_coverage/report_analysis_coverage.p2_report
report_timing -slack_lesser_than 0.0 -delay min_max -nosplit -input -net > ./reports/timing/report_timing.p2_report
```

Slack time: - 0.053991

Leaf Cell Count: - 111

Cell Area: - 309.55

2). Timing Analysis: - (report_timing)

```
student@ict-chipin:~/Documents/manav/RTL2GDSII/PT
File Edit View Search Terminal Help
Path Type: max
Point           Incr      Path
-----
clock Clock (rise edge)          0.000000  0.000000
clock network delay (ideal)     0.000000  0.000000
regA_reg[0]/CLK (DFFX1_RVT)     0.000000  0.000000 r
regA_reg[0]/Q (DFFX1_RVT)       0.737184 & 0.737184 r
ctmTdsLR_3_559/Y (INVX0_RVT)   0.122952 & 0.860136 f
ctmTdsLR_1_557/Y (NAND2X0_RVT) 0.245739 & 1.105875 r
U23/Y (NAND2X0_RVT)            0.260965 & 1.366840 f
U14/Y (NAND2X0_RVT)            0.353463 & 1.720303 r
ctmTdsLR_1_5/Y (NAND3X0_RVT)   0.313076 & 2.033379 f
ctmTdsLR_2_6/Y (NAND3X0_RVT)   0.457104 & 2.490483 r
ctmTdsLR_1_7/Y (NAND3X0_RVT)   0.300814 & 2.791296 f
ctmTdsLR_1_9/Y (NAND3X0_RVT)   0.392899 & 3.184195 r
U70/CO (FADDX1_RVT)             0.577901 & 3.762096 r
U69/S (FADDX1_RVT)              0.769283 & 4.531379 f
DIFF_reg[7]/D (DFFX1_RVT)       0.000003 & 4.531382 f
data arrival time                4.531382

clock Clock (rise edge)          6.800000  6.800000
clock network delay (ideal)     0.000000  6.800000
DIFF_reg[7]/CLK (DFFX1_RVT)     6.800000 r
clock reconvergence pessimism   0.000000  6.800000
clock uncertainty                 -1.600000 5.200000
library setup time               -0.614627 4.585373
data required time                4.585373
data arrival time                  -4.531382

slack (MET)                      0.053991

1
pt_shell> |
```

3). Violating Paths & Design Rule Violations: - (report_qor)

```
File Edit View Search Terminal Tabs Help
student@ict-chipin:~... x student@ict-chipin:~... x student@ict-chipin:~... x student@ict-chipin:~...
pt_shell> report_qor
*****
Report : qor
Design : subtractor_8bit
Version: W-2024.09
Date   : Tue Jun 3 10:22:08 2025
*****



Timing Path Group 'Clock' (max_delay/setup)
-----
Levels of Logic:                   11
Critical Path Length:            4.567899
Critical Path Slack:             0.017722
Total Negative Slack:            0.000000
No. of Violating Paths:          0
-----


Timing Path Group 'Clock' (min_delay/hold)
-----
Levels of Logic:                   2
Critical Path Length:            0.975065
Critical Path Slack:             0.947920
Total Negative Slack:            0.000000
No. of Violating Paths:          0
-----


Design Rule Violations
-----
Total No. of Pins in Design:      342
sequential_clock_pulse_width Count: 26
max_transition Count:             156
sequential_clock_pulse_width Cost: 35.990440
max_transition Cost:              21.139278
Total DRC Cost:                  57.129719
-----
```

4). Cell Count: - (**report_qor**)

```
Cell & Pin Count
-----
Pin Count:                      342
Hierarchical Cell Count:        0
Hierarchical Port Count:        0
Leaf Cell Count:                 111
-----
```

5). Cell Area: - (**report_qor**)

```
Area
-----
Net Interconnect area:          42.758636
Total cell area:                309.547363
Design Area:                   352.306000
-----
```

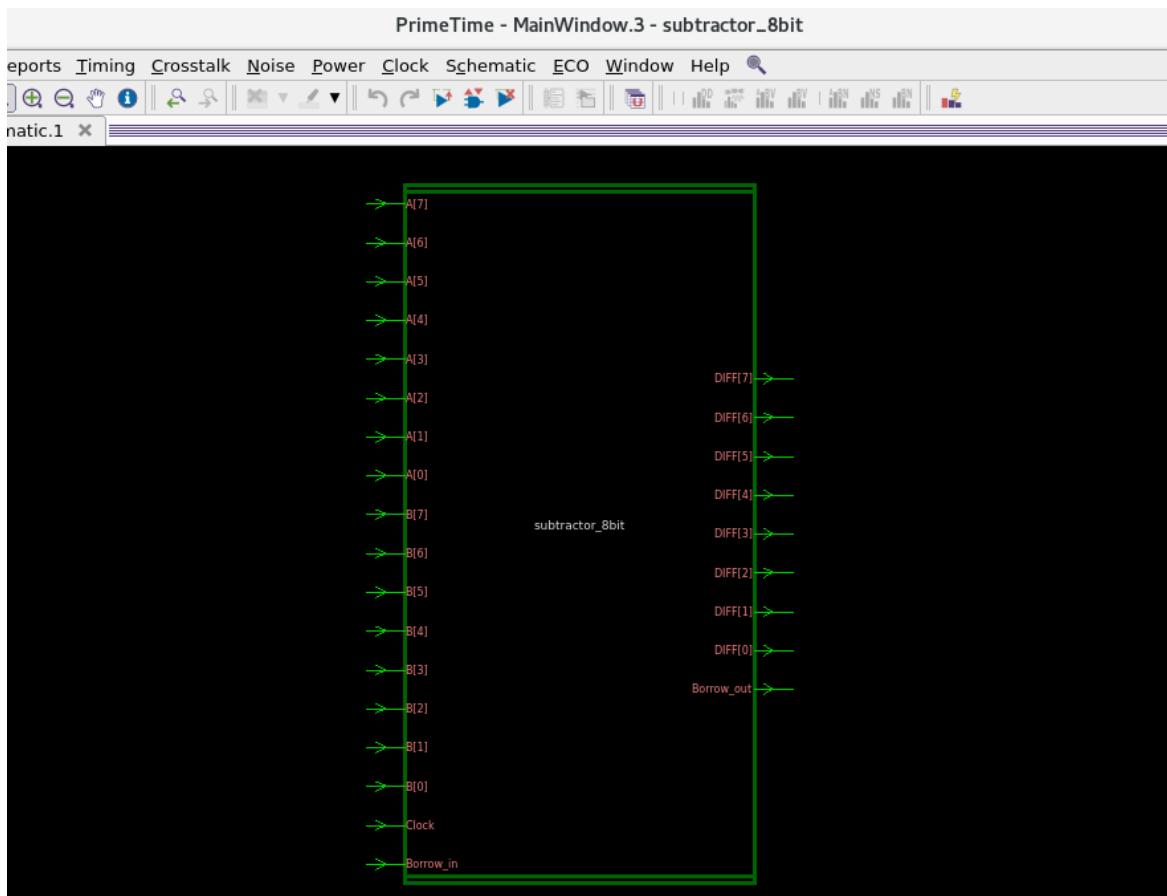
6). Power Report: - (**report_power**)

Power analysis was not done as the system had power analysis disabled.

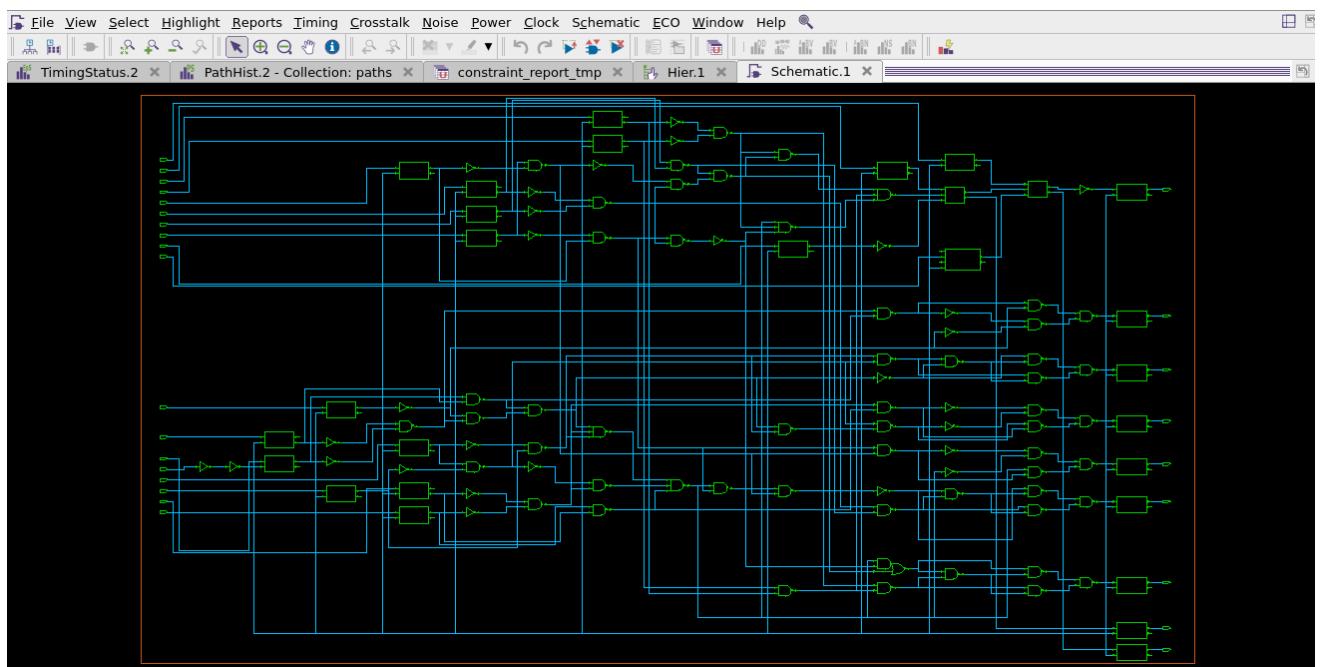
7). Units Report: - (**report_units**)

```
Units
-----
Capacitive_load_unit      : 1e-15 Farad
Current_unit               : 1e-06 Amp
Resistance_unit           : 1e+06 Ohm
Time_unit                  : 1e-09 Second
Voltage_unit               : 1 Volt
1
pt_shell>
```

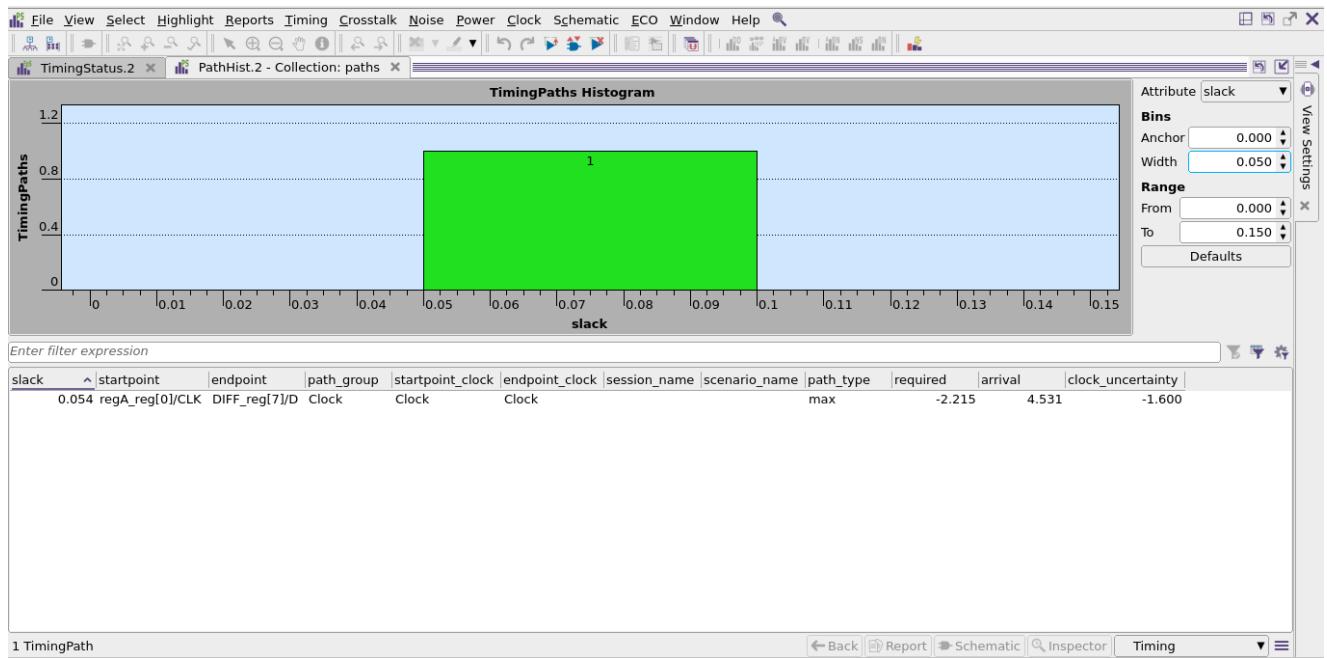
8). Block Diagram (Prime Time): -



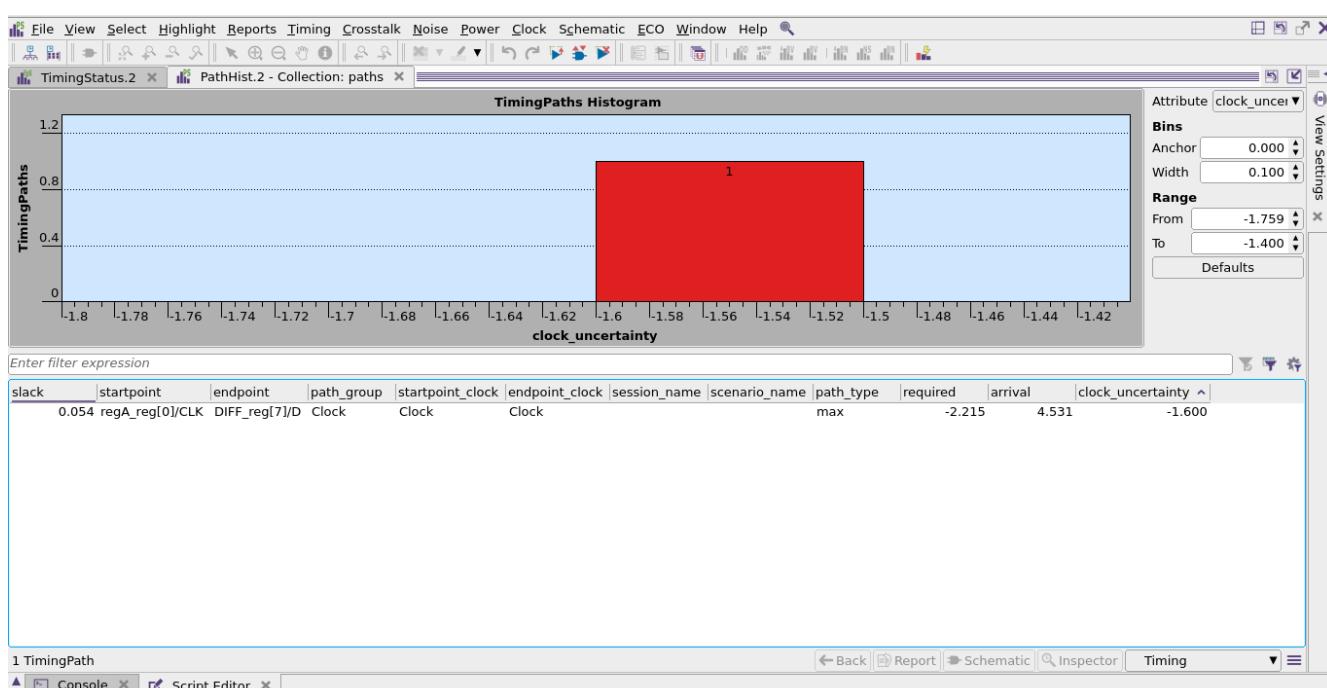
9). Schematic (Prime Time): -



10). Bar Graph: -



(slack time)



(clock uncertainty)

Learning & Outcomes

Through this workshop I learnt the complete **RTL-to-GDSII flow** (VCS → DC → ICC2 → PT) and making changes in libraries, constraints, and .tcl scripts.

Changes (path change, library change) in files like “**run_dc.tcl**”, “**.sdc file of CONSTRAINTS**”, “**placement.tcl**”, “**route.tcl**”, “**common_setup.tcl**”, “**run_pt_p2.tcl of Prime Time**”, use of “**saed32rvt_ss0p7vn40c.db**” library in **Design compiler & Prime time**.

Starting with RTL coding in Verilog, I created a clocked subtractor that operates over multiple cycles, and verified its functional correctness using VCS simulation and waveform analysis in Verdi. This phase helped me understand how sequential logic behaves across clock cycles and the importance of building a proper testbench for validation.

In the synthesis stage using Design Compiler (DC Shell), I used the SAED 32nm slow-slow (SS) corner library and applied constraints to generate a gate-level netlist. I learned how synthesis translates high-level RTL into optimized standard cell logic. The synthesized design reported a slack time of 0.40 ns, a leaf cell count of 92, and a cell area of 297.60 units². I also extracted detailed reports including area, power, timing, and unit usage through report_qor, report_power, and report_units.

Proceeding to physical design in ICC2, I completed the floor planning and power planning stages, maintaining the cell count and area from synthesis, and learning how physical layout begins with defining the core area, placing pins, and planning power distribution networks. During placement, I observed how optimization can reduce the leaf cell count to 85 while slightly increasing the area due to congestion management and standard cell spreading. After placement, I implemented clock tree synthesis (CTS), which inserted additional buffers to balance clock skew, increasing the cell count to 111 while preserving the slack time at 3.53 ns.

Routing finalized the design connectivity while keeping the cell count and area unchanged from CTS. Through this process, I gained valuable insights into how clocking and physical connectivity affect timing and area metrics. All relevant metrics were again extracted, including routing-based reports on timing, power, and utilization.

In the final stage, I performed static timing analysis (STA) using PrimeTime. Using the post-route netlist and the same SS library, I observed a final slack time of 0.053991 ns and confirmed that the design met all timing constraints. Although power analysis was disabled, all other critical reports including area, cell count, and units were verified. The design remained consistent with 111 leaf cells and a cell area of 309.55 units².

Throughout this project, I developed a deep understanding of how a sequential digital design flows from RTL to GDSII. I learned to edit key scripts (run_dc.tcl, run_pt_p2.tcl), update constraints, handle technology libraries, and interpret detailed design reports. I gained hands-on experience with how synthesis optimizations, physical placement, and clocking strategies impact timing, area, and cell utilization in a real-world VLSI flow.