High Performance VLSI Design

Experiment - 10

Cascode CS Amplifier with Cascode Current Source Load

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1 Aim

To design a high-gain Cascode Common Source Amplifier with Current Source Load using `gpdk180` library on the Virtuoso Design System by Cadence.

2 Theory

From the Fig. 1, M_1 is the driver transistor and M_2 is the cascode transistor. Any two transistor which are of the same type, N-type or P-type, are connected such that *Source* is connected to the *Drain*, then it is called Cascode Configuration. Similarly, M_4 is cascode since *drain* is connected to M_3's *source*, which is active load. Hence, this is a Cascode Common Source Amplifier with Cascode Current Source load.

The output resistance seen from the drain of M_3 transistor is approximately equal to $g_{m3}r_{o3}r_{o4}$ which is typically much higher than the output resistance of the single PMOS transistor.

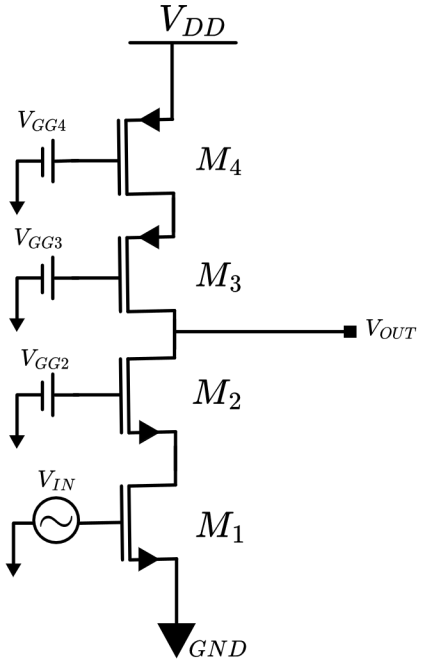

Figure 1: Cascode Common Source Amplifier with Current source load

Where, $R_{on} = g_{m2}r_{o2}r_{o1}$ is the output impedance of the cascode amplifier stage, and $R_{op} = g_{m3}r_{o3}r_{o4}$

is the output resistance of the cascode current source. Using the cascode amplifier along with the cascode current source, the gain of the amplifier can be improved significantly. And typically, this configuration is used in the integrated circuits to achieve a large gain.

Advantages	Disadvantages
Reduced Miller Effect: A cascode configuration reduces the Miller capacitance effect and improves stability by minimizing effective input capacitance.	**Complexity:** A cascode configuration has two amplifier stages, so the circuit is more complex than a one-stage amplifier.
Improved Bandwidth: The cascode arrangement reduces the Miller effect, so it's better at high frequencies and has a broader bandwidth. As a result, cascode amplifiers are suitable for applications requiring higher frequency response.	**Reduced Voltage Swing:** Cascode can reduce the amplifier's overall output voltage swing by limiting the common-emitter stage's voltage swing.
High Voltage Gain: The cascode configuration provides a high voltage gain due to the cascaded amplification stages. As the common-base stage has a high input impedance, the common-emitter stage can drive it effectively.	**Power Consumption:** Two amplifier stages can increase power consumption compared to simpler amplifier configurations.
Enhanced Linearity: A high input impedance on the common-base stage helps reduce the loading effect on the common-emitter stage, contributing to enhanced linearity.	**Limited Input Range:** The cascode configuration's common-base stage can limit the input voltage range because of its input biasing requirements.
High Output Impedance: Cascode configurations are less sensitive to load variations because the common-emitter stage has a high output impedance. In impedance-matching applications, this can be helpful.	**Additional Components and Cost:** Cascode configurations require additional components for biasing and interconnecting the two stages, which adds cost.

Table 1: Cascode Advantages and Disadvantages

High voltage gain, better bandwidth, and improved linearity are some of the benefits of cascode configurations. However, there are trade-offs in complexity, power consumption, and input range. Designers need to consider these factors to determine if a cascode configuration is right for their application.

3 Design

The design steps involve the following steps:

1. Decide the topology for which the design must be carried out, refer Fig. 1.
2. Find out the $(\frac{W}{L})$ of the nMOSFETs first (M1 in Fig. 1), by applying the Bias voltages V_b and V_{ds}. Finish the calculation for all the nMOSFETs then proceed with pMOSFETs (M4 in Fig. 1).
3. Design process is an iterative process. For the required current, in our case, it is 100μA, *width* of the nMOS must be obtained. In order to do this, construct the schematic in the Cellview and keep *width* as variable W. Perform DC analysis on the MOS under design and plot the *Current vs Width* graph. From the plot obtained, note the value of *width* corresponding to 100μA.

   Here,

$$V_{bias} = V_T + 0.05 * V_{DD}$$
$$V_{DD} = 1.8V$$
$$\text{and, } V_T \approx 500mV$$

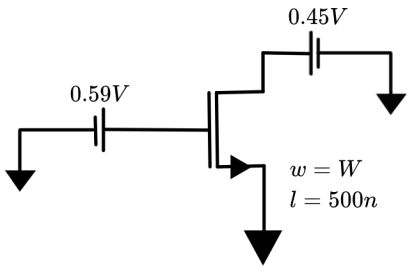

Figure 2: Design schematic for M1

Plus, after every MOS there must be a $(V_{DD}/4)$ V reduction. Hence, V_{DS1} must be $(V_{DD} - 3V_{DD}/4)$ which is equal to $0.45V$.

4. After performing the design, the following are the *width* of the MOSFETs obtained.

MOSFET	**Width**
M1	14.94μ m
M2	15.585μ m
M3	41.895μ m
M4	77.34μ m

Table 2: Widths of MOSFETs

5. Based on the above V_{bias} formula, we obtain following voltages:

MOSFET	V_{bias}
M2	0.76Vμ m
M3	1.04Vμ m
M4	0.59Vμ m

Table 3: Bias Voltages

6. Create schematic according to the *aspect ratios* obtained, and simulate design for Magnitude and Phase Response, Bandwidth and *Transient Analysis* to show *input* and *Output*.

4 Circuit Schematic

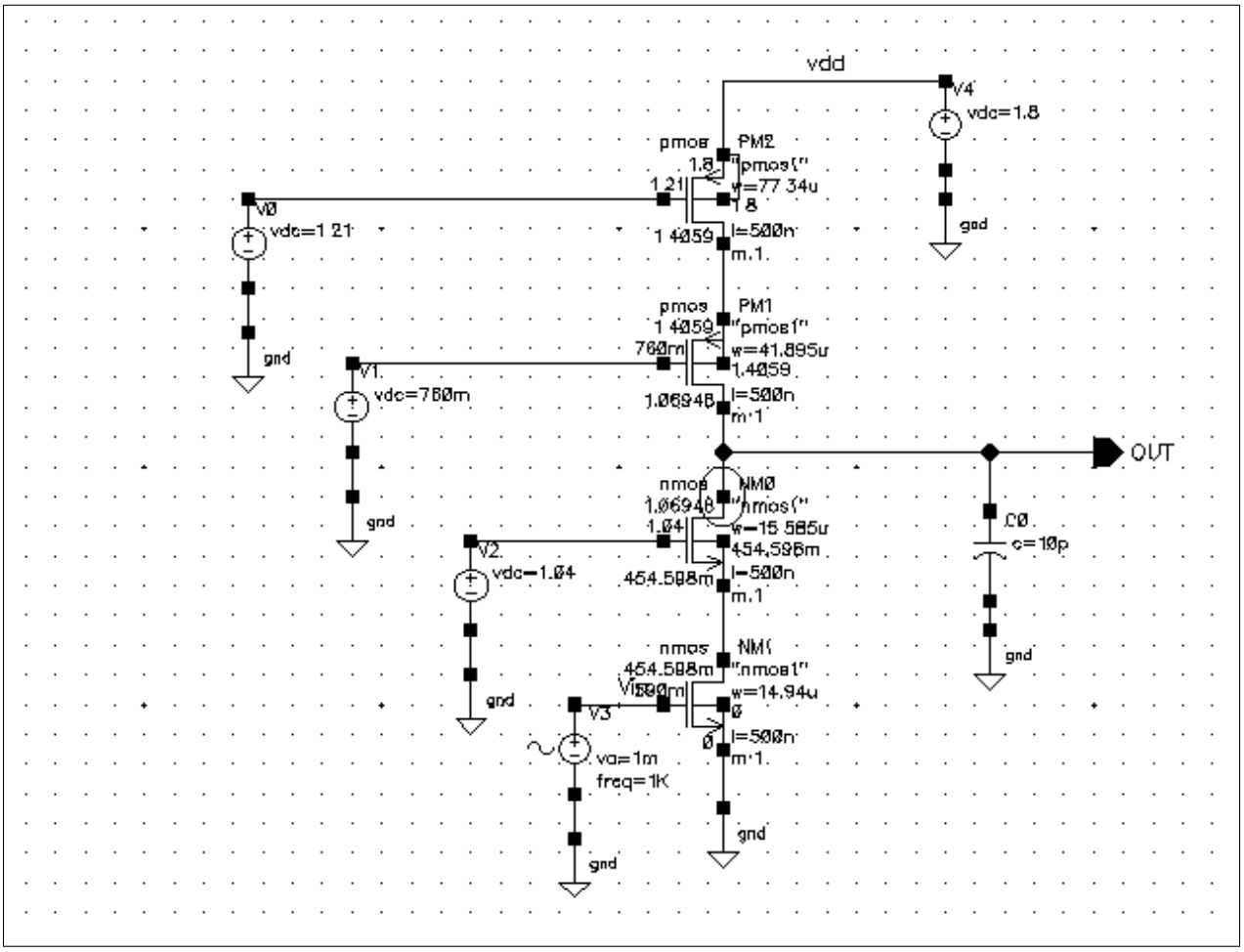

Figure 3: Schematic (Cellview) of the Design

5 Results

5.1 Magnitude Response

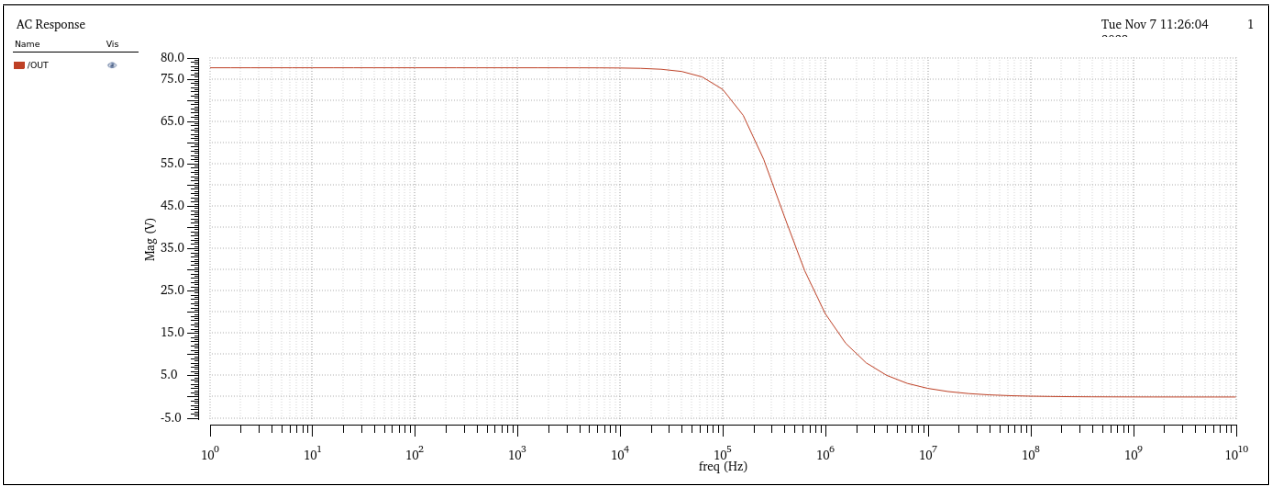

Figure 4: Gain

5.2 Magnitude Response (dB)

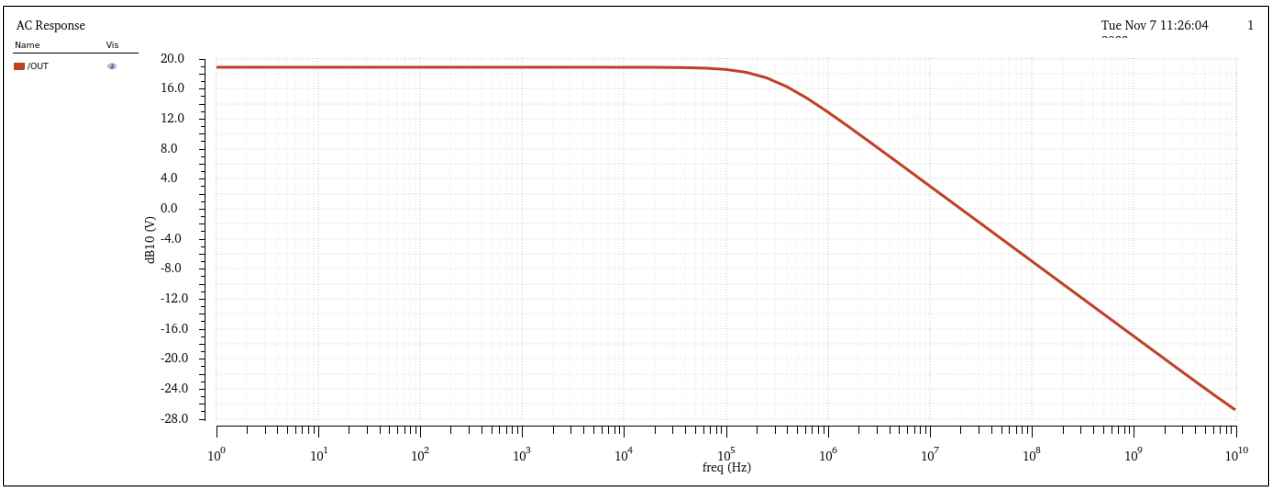

Figure 5: Gain in dB

5.3 Phase Response

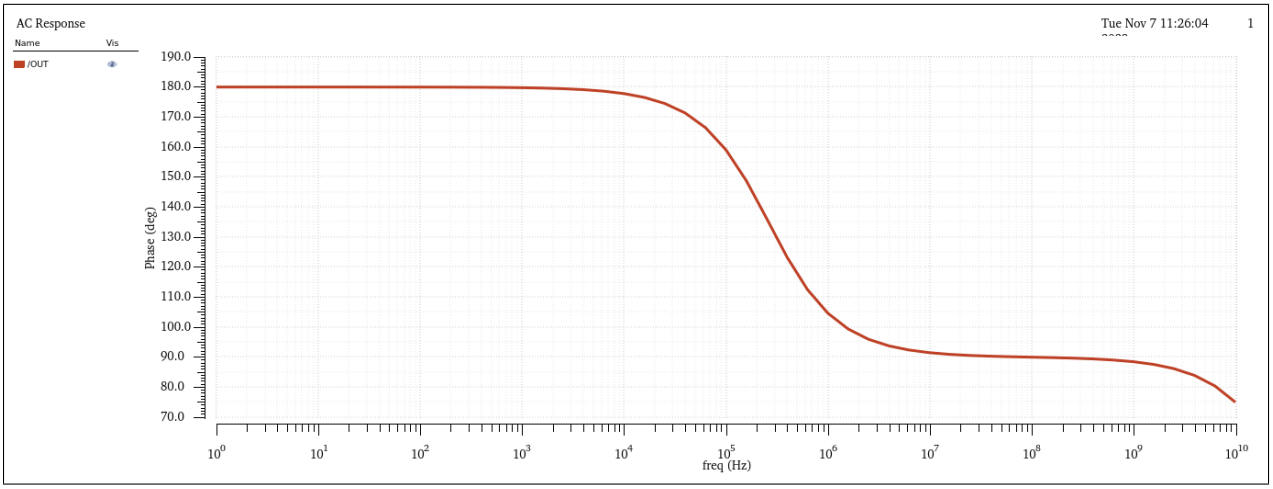

Figure 6: Phase Response

5.4 Bandwidth

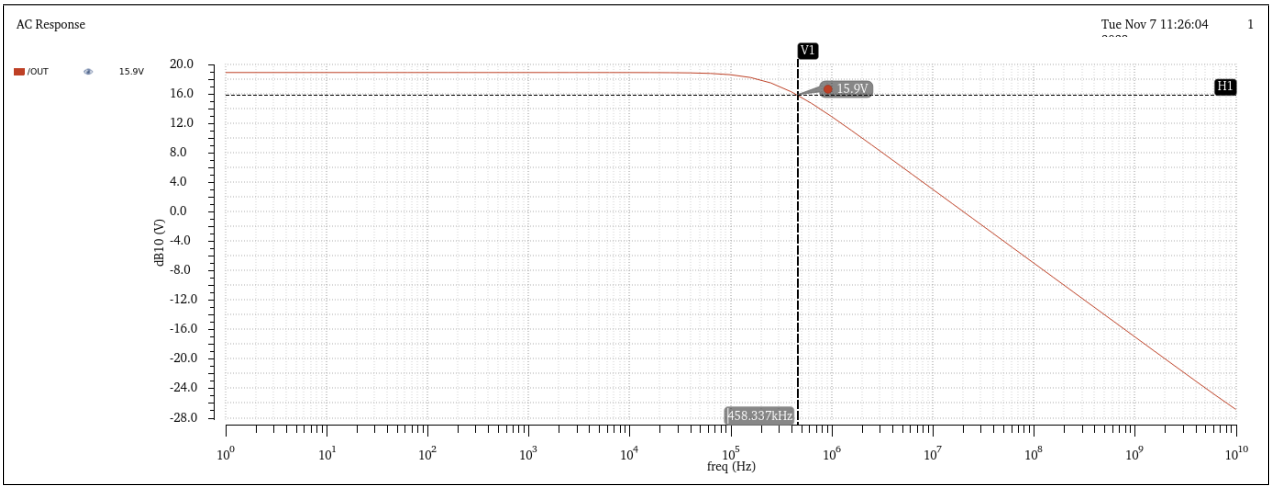

Figure 7: Bandwidth ≈ 500KHz

5.5 Transient Analysis

It can be observed from the waveform, we get peak to peak swing of $155mV$. Hence 1mV is amplified 77 times i.e. Gain of the Amplifier, refer Fig. 4.

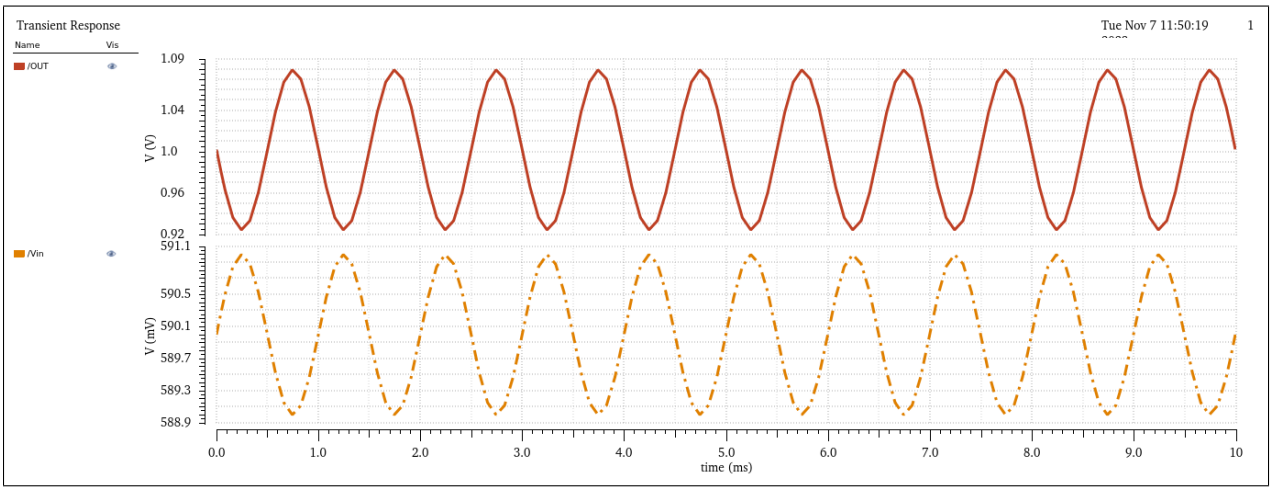

Figure 8: Transient Analysis

6 Conclusion

The Cascode Common Source Amplifier with Current Source Load designed in this experiment has exhibited several key characteristics in its performance analysis.

The amplifier's magnitude response demonstrates a high gain that remains relatively constant across a considerable frequency range. The phase response showcases stability, portraying consistent phase behavior within the operational frequency band. With a calculated bandwidth of approximately 500 kHz, this amplifier effectively covers a broad spectrum of frequencies.

Additionally, the transient analysis depicts a desirable output response to an input signal, indicating a stable and efficient amplification behavior over time.

The designed circuit, based on the obtained MOSFET widths and bias voltages, aligns well with the theoretical expectations. Overall, the amplifier configuration using the Cascode topology, the chosen MOSFET aspect ratios, and bias voltages have resulted in a high-performance design meeting the set objectives of achieving a high-gain, stable operation, and adequate bandwidth for the specified load conditions.