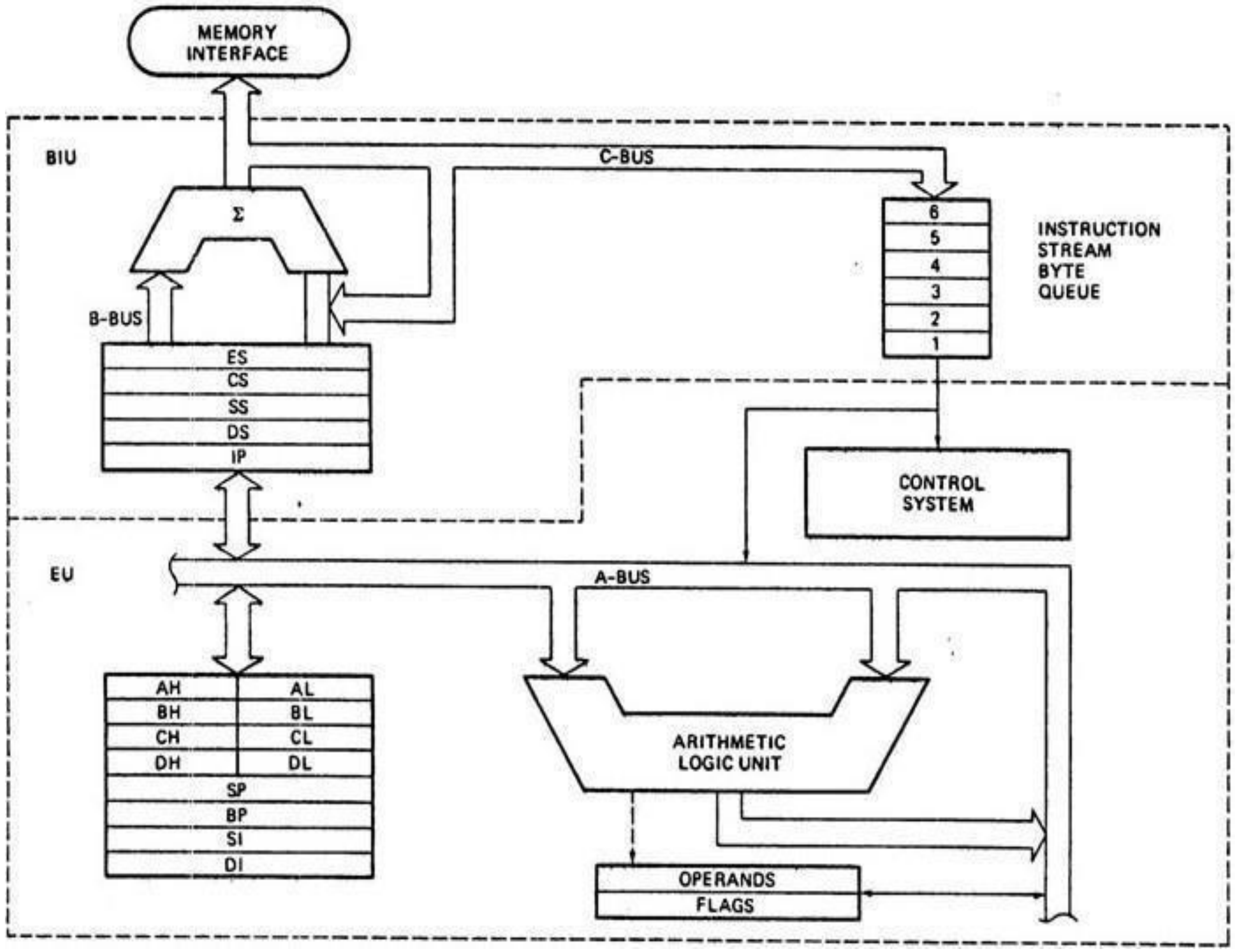
1. **Draw block diagram of microprocessor 8086. Explain its each functional part in brief. OR Explain BIU & EU in 8086 Microprocessor with diagram. OR Describe Architecture of any one 16 bit microprocessor.**



The 8086 CPU is divided into two functional parts, the bus interface unit (BIU), and the execution unit (EU).

The Bus Interface Unit

- The BIU is responsible for all type of interfacing with external environments.
- The BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands. The instruction bytes are transferred to the instruction queue.
- In BIU there are so many functional groups or parts these are as follows:-

1) Instruction Queue

- This queue permits pre-fetch of up to 6 bytes of instruction code. While current instruction is executing next instruction is fetch is called as instruction pipelining.
- This is shown in figure below.

Fetch	Decode	Execute		
	Fetch	Decode	Execute	
		Fetch	Decode	Execute

2) Segment Registers

- The BIU contains four 16-bit segment registers. They are: the extra segment (ES) register, the code segment (CS) registers, the data segment (DS) registers, and the stack segment (SS) registers.
- These segment registers are used to hold the upper 16 bits of the starting address for each of the segments.

3) Instruction Pointer (IP)

- The instruction pointer (IP) holds the 16-bit address of the next code byte within code segment.

The Execution Unit

- The execution unit (EU) tells the BIU where to fetch instructions or data from; it decodes instructions, and executes instructions.
- A decoder in the EU translates instructions fetched from memory to generate different internal or external control signals that required performing the operation.
- The EU has a 16-bit ALU, which can perform arithmetic operations such as add, subtract etc. and logical operations such as AND, OR, XOR, increment, decrement etc.

1) Flag Register

- A 16-bit flag register is a flip-flop which indicates some condition produced by the execution of an instruction or controls certain operations of the EU.
- They are modified automatically by CPU after mathematical operations. It has total 9 flags.

2) General Purpose Registers

- The EU has eight general purpose registers labeled AH, AL, BH, BL, CH, CL, DH, and DL.
- These registers can be used individually for temporary storage of 8-bit data.
- The AX register is also called the accumulator

3) Stack Pointer Register

- The stack pointer (SP) register contains the 16-bit offset from the start of the segment to the memory location where a word was most recently stored on the stack.

4) Other Pointer and Index Registers

- The EU also contains a 16-bit source index (SI) register, base pointer (BP) registers, and Destination Index (DI) registers.
- These three registers can be mainly used for temporary storage of 16-bit data just like a general purpose registers.

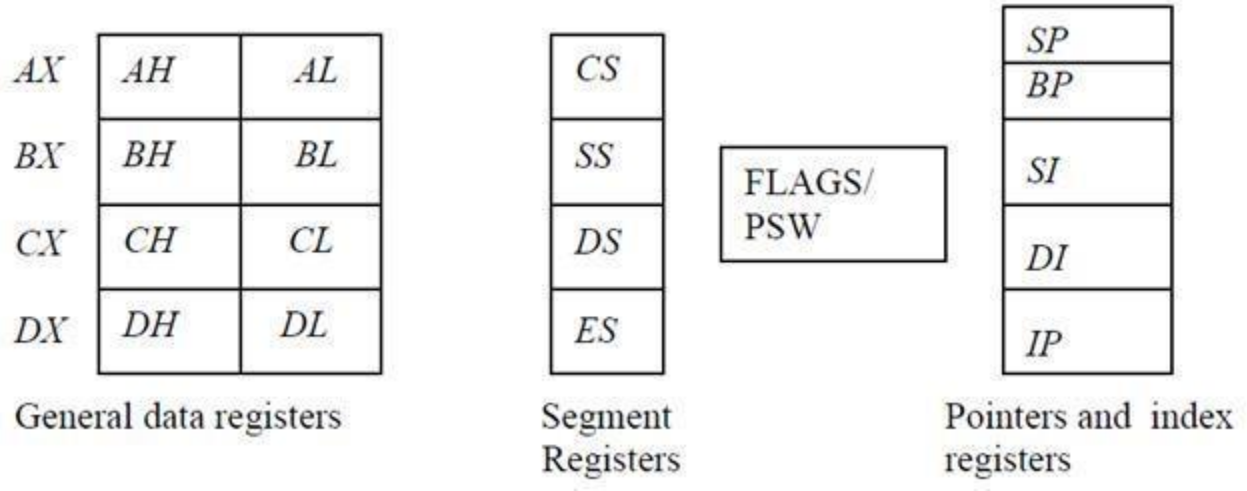
2. Explain General Data Registers OR Draw and Explain Register organization of 8086 Microprocessor OR Explain Programming Model Of 8086 microprocessor.

All the registers of 8086 are 16-bit registers. The register set of 8086 can be divided into 4 different groups. The register organization of 8086 is shown in the figure.

General Data Registers:

- The general purpose registers can be used as either 8-bit registers or 16-bit registers. The registers AX, BX, CX and DX are the general purpose 16-bit registers.
- AX is used as 16-bit accumulator. The lower 8-bit is designated as AL and higher 8-bit is designated as AH. AL can be used as an 8-bit accumulator for 8-bit operation.

- BX is a 16 bit register, but BL indicates the lower 8-bit of BX and BH indicates the higher 8-bit of BX. The register BX is used as offset storage for forming physical address in case of certain addressing modes.
- The register CX is used default counter in case of string and loop instructions.
- DX register is a general purpose register which may be used as an implicit operand or destination in case of a few instructions.



Segment Registers:

- The 8086 architecture uses the concept of segmented memory.
- 8086 able to address a memory capacity of 1 megabyte and it is byte organized. This 1 megabyte memory is divided into 16 logical segments.
- Each segment contains 64 Kbytes of memory.
- There are four segment register in 8086:
  - Code segment register (CS)
  - Data segment register (DS)
  - Extra segment register (ES)
  - Stack segment register (SS)
- *Code segment register* (CS): is used for addressing memory location in the code segment of the memory, where the executable program is stored.
- *Data segment register* (DS): points to the data segment of the memory where the data is stored.
- *Extra Segment Register* (ES): also refers to a segment in the memory which is another data segment in the memory.
- *Stack Segment Register* (SS): is used for addressing stack segment of the memory. The stack segment is that segment of memory which is used to store stack data.

Pointers and Index Registers.

→ The pointers contain offset within the particular segments.

- The pointer register IP (instruction Pointer) contains offset within the code segment.
- The pointer register BP (base pointer) contains offset within the data segment.
- The pointer register SP (stack pointer) contains offset within the stack segment.
- The register SI (source index) is used to store the offset of source data in data segment.
- The register DI (destination index) is used to store the offset of destination in data or extra segment.

- The index registers are particularly useful for string manipulation.

Flag Register

- The 8086 flag register contents indicate the results of computation in the ALU. It also contains some flag bits to control the CPU operations

3. What is flag register? Explain each flag bit of the flag register in 8086.

- Flag is a 16 bit register used in 8086 to indicate some condition produce after arithmetic and logical operation.
- It is divided into two parts.
  (a) Condition or status flags
  (b) Control flags

(a) Condition or status flags

- The condition flags are the lower byte of the 16-bit flag register.
- It indicates some condition produce after arithmetic and logical operation.
- It contains five flag namely sign(s), Zero (z), Auxilary Carry (AC), parity (P), Carry (CY).

(b) Control flags

- The control flag is the higher byte of the flag register.
- It contains three flags namely direction flag (D), interrupt flag (I) and trap flag (T).

The complete bit configuration of 8086 Flag register is shown in the figure.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	OF	DF	IF	TF	SF	ZF	X	AC	X	PF	X	CY

1) ***SF-Sign Flag***: This flag is set, when the result of any computation is negative.
2) ***ZF-Zero Flag***: This flag is set, if the result of the computation or comparison performed by the previous instruction is zero.
3) ***PF-Parity Flag***: This flag is set, if the lower byte of the result contains even number of 1's (even parity) otherwise it reset (for Odd parity).
4) ***CF-Carry Flag***: This flag is set, when there is a carry out of MSB in case of addition or a borrow in case of subtraction.
5) ***AC-Auxiliary Carry Flag***: This flag is set, if there is a carry or borrow from the lowest nibble, i.e., from bit three during addition subtraction respectively. This flag is use only for BCD addition.

6) TF-Tarp Flag: If this flag is set, the processor enters the single step execution mode.

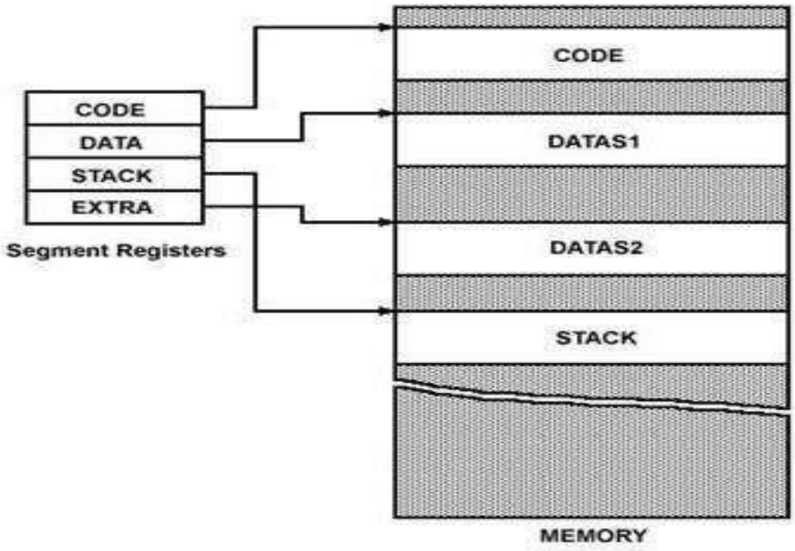
7) IF-Interrupt Flag: If this flag is set, the interrupts are enabling, otherwise they are ignored.

8) DF-Direction Flag: This is used by string manipulation instructions. If this flag bit is '0', the string is processed beginning from the lowest address to the highest address, i.e., auto incrementing mode. Otherwise, the string is processed from the highest address towards the lowest address, i.e., auto decrementing mode.

9) OF-Over flow Flag: This flag is set, if an overflow occurs i.e., if the result of a signed operation is large enough to accommodate in a destination register.

4. What is memory segmentation in 8086? Explain logical and physical memory addressing.

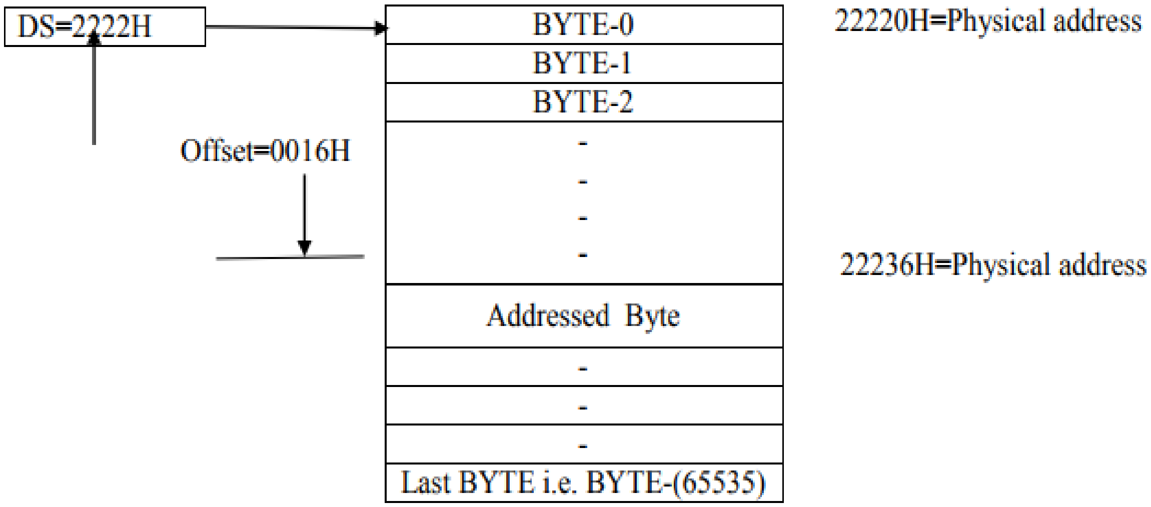
- The total memory size is divided into segments of various sizes. The process of dividing memory this way is called Segmentation.
- In memory, data is stored as bytes. Each byte has a specific address. Intel 8086 has 20 lines address bus. With 20 address lines, the memory that can be addressed is 2^{20} = 1,048,576 bytes (1 MB).
- 8086 can access memory with address ranging from 00000 H to FFFFFH.
- In 8086, memory has four different types of segments. These are:
  - Code Segment
  - Data Segment
  - Stack Segment
  - Extra Segment
- Each of these segments is addressed by an address stored in corresponding segment register. i.e. CS,DS,SS,ES respectively.
- These registers are 16-bit in size. Each register stores the base address (starting address) of the corresponding segment. Because the segment registers cannot store 20 bits, they only store the upper 16 bits.



- A memory location is specified by an offset within a segment.
- Logical address: segment: offset i.e.2222h:0016h means offset 0016h within segment 2222h.
- Physical address: segment * 10H + offset i.e. 2222h*10h + 0016 = 22220h + 0016h = 22236h (20-bit address)

<u>Where to Look for the Offset:</u>

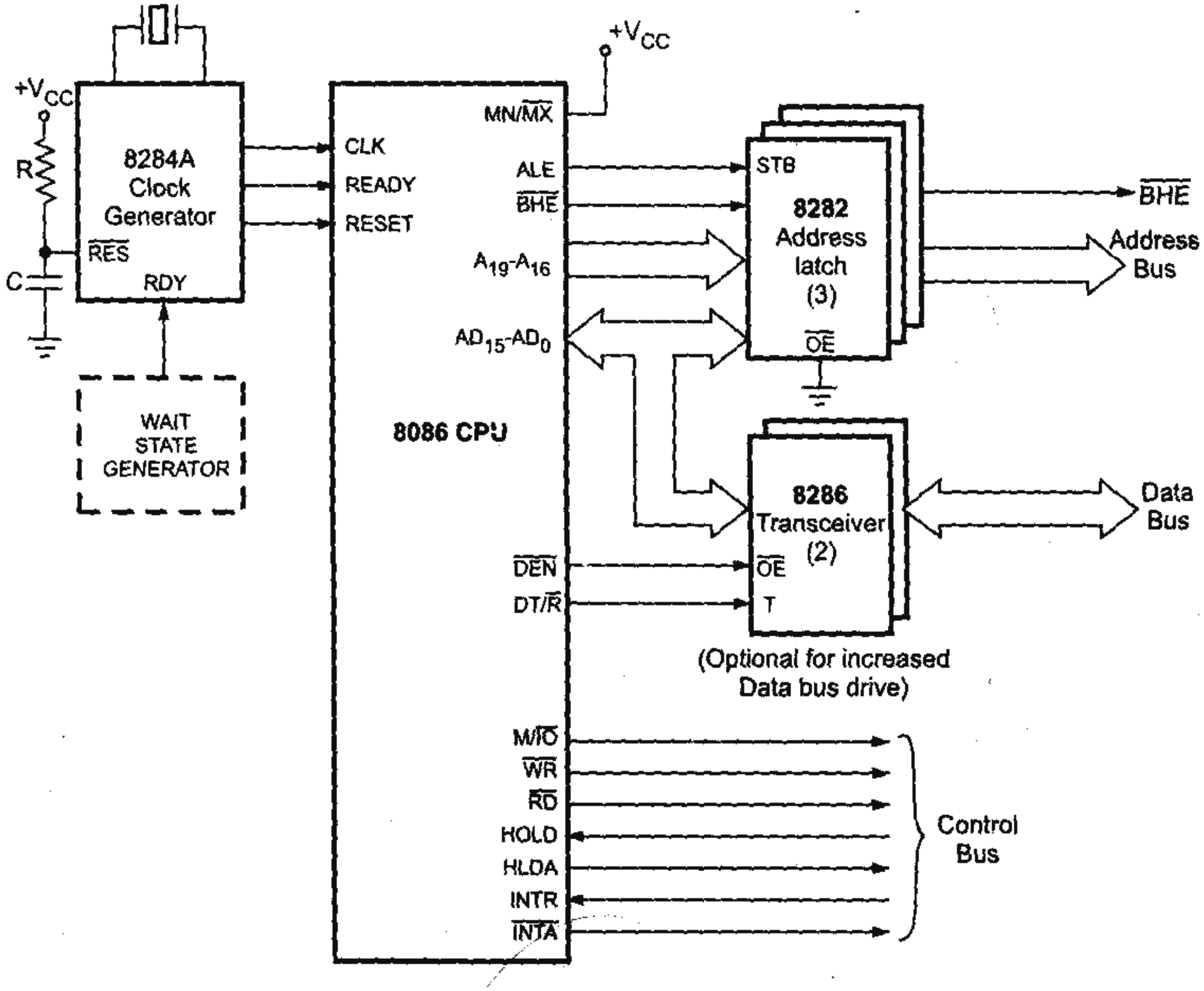
Segment	Offset Registers	Function
CS-Code Segment	IP	Address of the next instruction
DS-Data Segment	BX, DI, SI	Address of data
SS-Stack Segment	SP,BP	Address in the stack
ES-Extra Segment	BX, DI, SI	Address of destination data(for string operations)



5. Explain minimum mode and maximum mode of 8086 microprocessor.

Minimum mode 8086 system

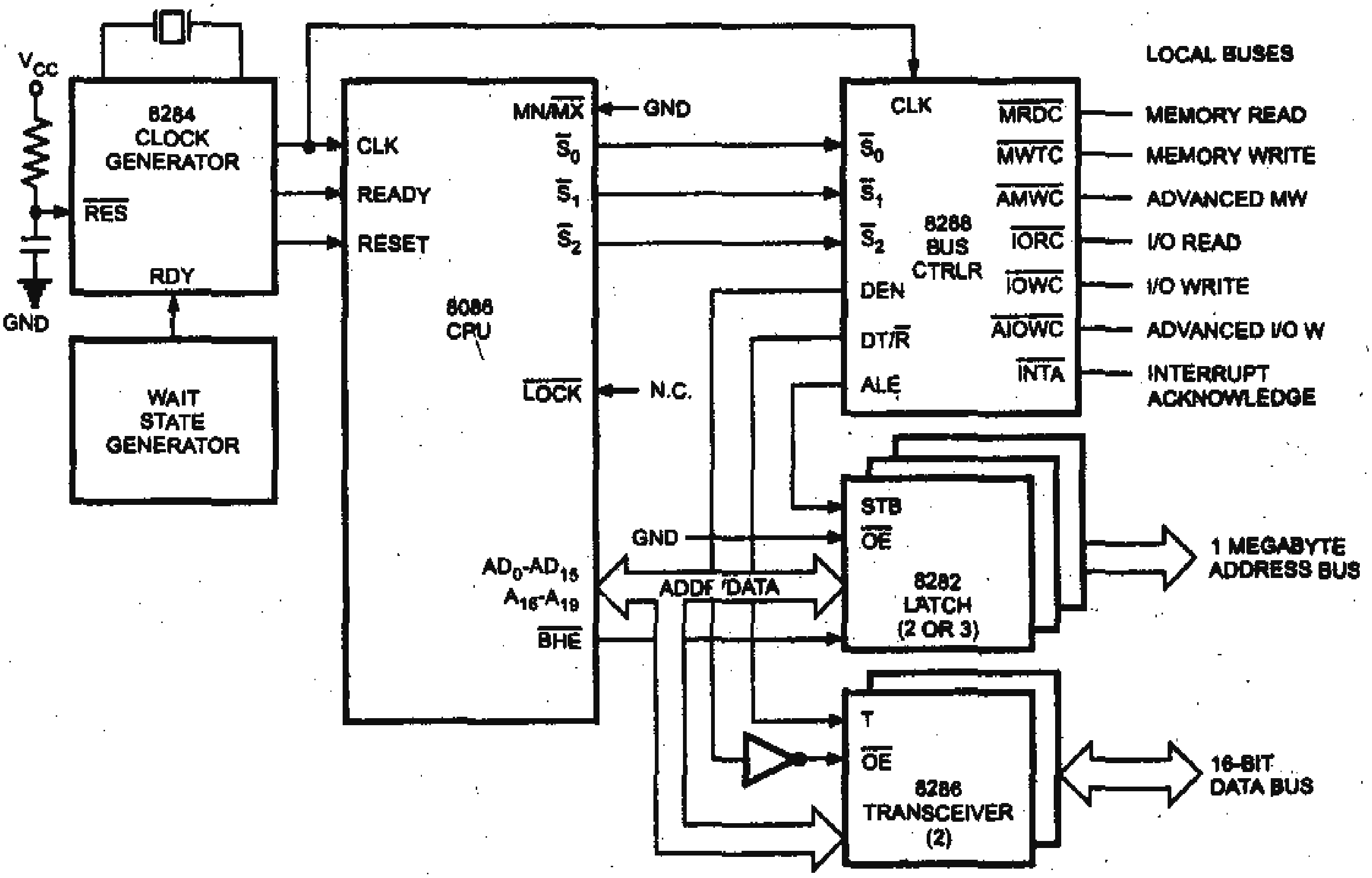
- In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its $MN/\overline{MX}$ pin to logic 1.



- In this mode, all the control signals are given out by the microprocessor chip itself.
- There is a single microprocessor in the minimum mode system. The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.
- Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.

Maximum mode 8086 system

- In the maximum mode, the 8086 is operated by connecting the MN   in to ground.
- In the maximum mode, there may be more than one microprocessor in the system configuration.
- The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.
- Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.
- All the control signal is given by the external bus controller called 8288
- The basic function of the bus controller chip IC8288, is to derive control signals like $\overline{RD}$and $\overline{WR}$DEN, DT/$\overline{R}$, ALE etc. using the information by the processor on the status lines.
- The bus controller chip has input lines S2, S1, S0 and CLK from the microprocessor.
- It derives the outputs ALE, $\overline{DEN}$, DT/$\overline{R}$, $\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{AIOWC}$.
- The $\overline{AEN}$, IOB and CEN pins are specially useful for multiprocessor systems.

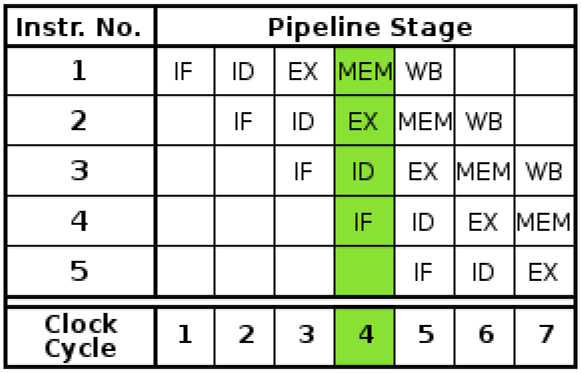


6. Explain Instruction Pipelining.

- An instruction pipeline is a technique used in the design of computers to increase their instruction throughput (the number of instructions that can be executed in a unit of time).
- The basic instruction cycle is broken up into a series called a pipeline. Rather than processing each instruction sequentially (one at a time, finishing one instruction before starting the next), each instruction is split up into a sequence of steps so different steps can be executed concurrently (at the same time) and in parallel (by different circuitry).
- Each instruction is split into a sequence of dependent steps. The first step is always to fetch the instruction from memory; the final step is usually writing the results of the instruction to processor registers or to memory.
- Pipelining seeks to keep every portion of the processor busy with some instruction.

Number of steps:

- The number of dependent steps varies with the machine architecture. For example:
- There are five stages of pipelining:
  1. Instruction fetch
  2. Instruction decode and register fetch
  3. Execute
  4. Memory access
  5. Register write back



Instr. No.	Pipeline Stage						
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

Above diagram contains following points:

1. All stages will be of equal duration.
2. Each instruction goes through all five stages of pipeline.
3. All the stages will be performed parallel.
4. No memory conflicts.
5. All the accesses occur simultaneously.

Factors affecting pipeline performance:

1. If five stages are not of equal duration, then there will be some waiting time at various stages.
2. Conditional branch instruction which can invalidate several instructions fetches.
3. Interrupt which is unpredictable event.
4. Register and memory conflicts.