1. What is an interrupt? Gives the general steps when interrupt occurs

- **Interrupt**: It means *interrupting* the normal execution of the microprocessor. When microprocessor receives interrupt signal, it discontinues whatever it was executing. It starts executing new program indicated by the interrupt signal.
- **Interrupt Service Routine(ISR):** A small program that is executed when corresponding interrupt signal is received.

- **Sequence of Steps Whenever There is an Interrupt**
  1) It completes the current instruction and suspends the current program.
  2) It pushes the content of PC (Program Counter) to stack.
  3) Then loads the vector address in PC and starts executing the Interrupt Service Routine (ISR) stored in this vector address.
  4) Resumes suspended program by getting its address from stack.

- **Classification of Interrupts**
  (1) Software and Hardware
  (2) Maskable and Non-Maskable
  (3) Vectored and Non-Vectored
  (4) Edge Triggered and Level Triggered
  (5) Priority Based Interrupts

2. Explain Hardware and software Interrupts in 8085

- **Hardware interrupt**

Hardware interrupt is caused by sending a signal on one of the interrupt pins of the processor.
(1) TRAP
(2) RST 7.5
(3) RST 6.5
(4) RST 5.5
(5) INTR

The addresses to which program control goes:

Name	Vectored Address
RST 7.5	003C H (7.5 x 0008 H)
RST 6.5	0034 H (6.5 x 0008 H)
RST 5.5	002C H (5.5 x 0008 H)
TRAP	0024 H (4.5 x 0008 H)

Steps for hardware interrupts:

1. The 8085 checks for hardware interrupt during each machine cycle at the end of the instruction.
2. If a valid signal is present
   a. If it is TRAP interrupt, processor saves the address of next instruction, jumps to specific location, executes ISR and resumes the original program.
   b. If it is one of the other four (RST 7.5,RST 6.5, RST 5.5, INTR) then

i. If interrupt is enabled processor saves the address of next instruction, jumps to specific location, executes ISR and resumes the original program.
ii. Otherwise it is ignored.

➢ **Software Interrupts**

- The software interrupts are program instructions.
- These instructions are inserted at desired locations in a program.
- While running a program, if software interrupt instruction is encountered, then the processor executes an interrupt service routine (ISR).
- When the instruction is executed, the processor executes an interrupt service routine stored in the vector address of the software interrupt instruction.
- The software interrupts of 8085 are RST 0, RST1, RST 2, RST 3, RST 4, RST 5, RST6 and RST 7.
- All software interrupts of 8085 are vectored interrupts. The software interrupts cannot be masked and they cannot be disabled.

The vector addresses of software interrupts are given in table below

Interrupt	Vector Address
RST0	0000H (0x0008H)
RST1	0008H (1x0008H)
RST2	0010H (2x0008H)
RST3	0018H (3x0008H)
RST4	0020H (4x0008H)
RST5	0028H (5x0008H)
RST6	0030H (6x0008H)
RST7	0038H (7x0008H)

3. Explain Maskable and Non Maskable interrupt

➢ **Maskable Interrupts**

- Maskable interrupts are those interrupts which can be *enabled* or *disabled*.
- Enabling and Disabling is done by software instructions.
- The interrupts can be masked by moving an appropriate data to accumulator and then executing SIM instruction. (SIM - Set Interrupt Mask).
- The status of maskable interrupts can be read into accumulator by executing RIM instruction (RIM - Read Interrupt Mask).
- List of Maskable Interrupts: RST 7.5
  RST 6.5
  RST 5.5
  INTR

➢ **Non-Maskable Interrupts**

- The interrupts which are always in *enabled* mode are called nonmaskable interrupts.
- These interrupts can never be disabled by any software instruction.
- TRAP is a non-maskable interrupt.

4. Explain vectored and Non vectored interrupt

➢ **Vectored Interrupts**

- The interrupts which have fixed memory location for transfer of control from normal execution.
- List of vectored interrupts: RST 7.5
  RST 6.5
  RST 5.5
  TRAP

The addresses to which program control goes:

Name	Vectored Address
RST 7.5	003C H (7.5 x 0008 H)
RST 6.5	0034 H (6.5 x 0008 H)
RST 5.5	002C H (5.5 x 0008 H)
TRAP	0024 H (4.5 x 0008 H)

➢ **Non-Vectored Interrupts**

- The interrupts which don't have fixed memory location for transfer of control from normal execution is called Non-Vectored Interrupts.
- The address of the memory location is sent along with the interrupt. INTR is a non-vectored interrupt.

5. Explain Edge Triggered Interrupts and Level Triggered Interrupts

➢ **Edge Triggered Interrupts**

- The interrupts which are triggered at leading or trailing edge are called edge triggered interrupts.
- RST 7.5 is an edge triggered interrupt. It is triggered during the leading (positive) edge.

➢ **Level Triggered Interrupts**

- The interrupts which are triggered at high or low level are called level triggered interrupts.RST 6.5 RST 5.5, INTR are level trigger.
- TRAP is edge and level triggered interrupt

6. Explain Priority Based Interrupts

➢ **Priority Based Interrupts**

- Whenever there exists a simultaneous request at two or more pins then the pin with higher priority is selected by the microprocessor.
- Priority is considered only when there are simultaneous requests.

Priority of interrupts:

Interrupt	Priority
TRAP	1
RST 7.5	2
RST 6.5	3
RST 5.5	4
INTR	5