(1) Define following terms: Instruction, Machine Cycle, Opcode, Oprand & Instruction Cycle.

Instruction:

- Instruction is the command given by the programmer to the Microprocessor to Perform the Specific task. For example, transfer a data, to do addition etc.

T-state:

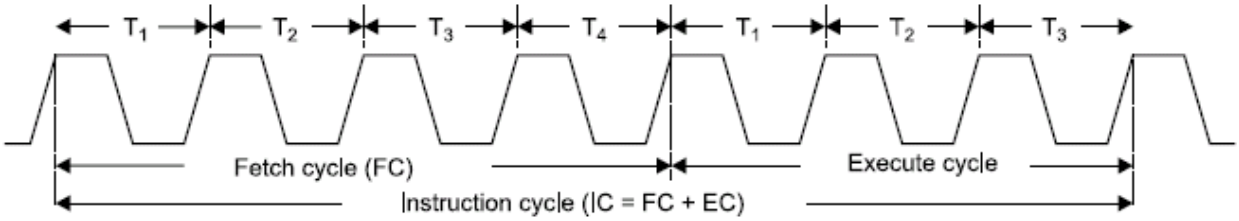
- Microprocessor performs an operation in specific time period that is specific clock cycles. Each clock cycle is called T-state.

Machine Cycle:

- Machine cycle is the time required to transfer data to or from memory or I/O devices. Each read or writes operation constitutes a machine cycle.
- The instructions of 8085 require 1–5 machine cycles containing 3–6 clocks.
- The 1st machine cycle of any instruction is always an Opcode fetching cycle in which the processor decides the nature of instruction. It is of at least 4-clocks.

Instruction Cycle:

- An instruction cycle is defined as the time required for fetching and executing an instruction.
- For executing any program, basically 3-steps are followed sequentially that is Fetch, Decode and Execute.
- The time taken by the μP in performing the fetch operations is called fetch cycle (Opcode fetch). The time taken by the μP in performing the execution operations is called execute cycle
- Thus, sum of the fetch and execute cycle is called the instruction cycle as indicated in Fig



Instruction Cycle (IC) = Fetch cycle (FC) + Execute Cycle (EC

Opcode:

Operation Perform by the microprocessor is called Opcode.

Operand:

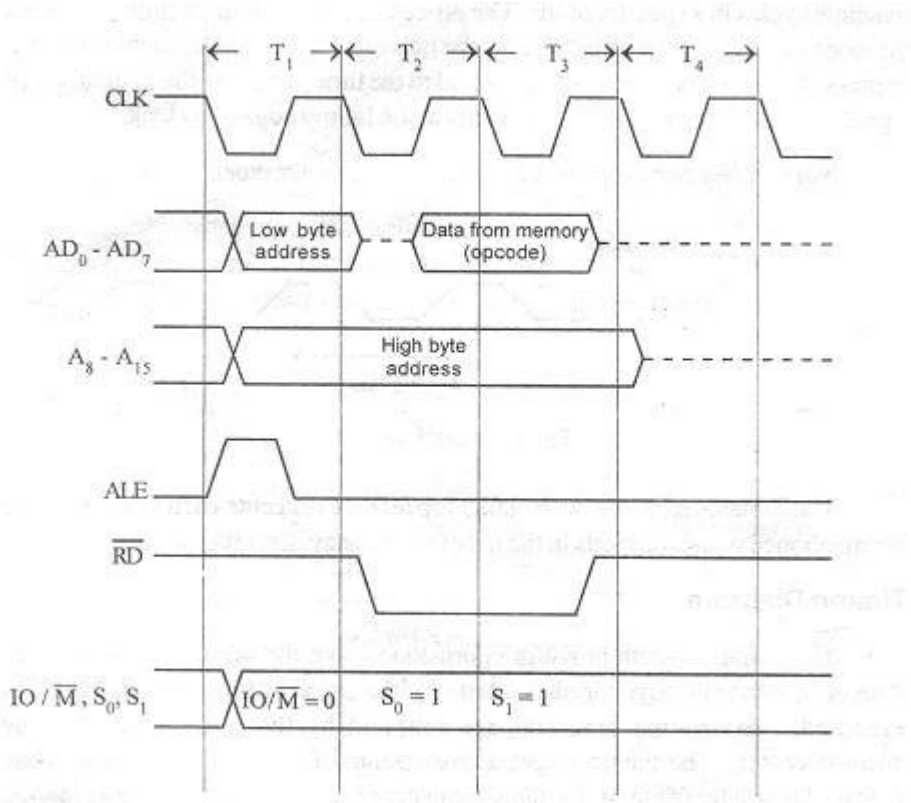
The Data on which Microprocessor perform operation is called Operand.

Timing diagram:

- Graphical presentation of steps with respect to time i.e. clock. This graphical representation is called Timing diagram.

(2) Draw and explain the Timing Diagram for Opcode Fetch operation.

- Each instruction of the processor has one byte Opcode.
- The Opcode are stored in memory. So, the processor executes the Opcode fetch machine cycle to fetch (Read) the Opcode from memory. Hence, every instruction starts with Opcode fetch machine cycle.
- The time taken by the processor to execute the Opcode fetch cycle is 4T or 6T.
- In this time, the first, 3 T-states are used for fetching the Opcode from memory and the remaining T-states are used for internal operations by the processor.
- Timing diagram of Opcode fetch cycle is shown in figure.



T1 State: -

- The microprocessor sends the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines.
- ALE is sending high to enable the address latch.

- The other control signals are **IO/$\overline{\mathbf{M}}$**=0, S0=1, S1=1

T2 State:-

- The microprocessor send the **$\overline{\mathbf{RD}}$** to the memory.
- When **$\overline{\mathbf{RD}}$**goes to low the memory is enabled for placing the data on the data bus

T3 State: -

- The read signal goes to high. On the rising edge of read signal the data is latched into microprocessor other control signals remains in the same state

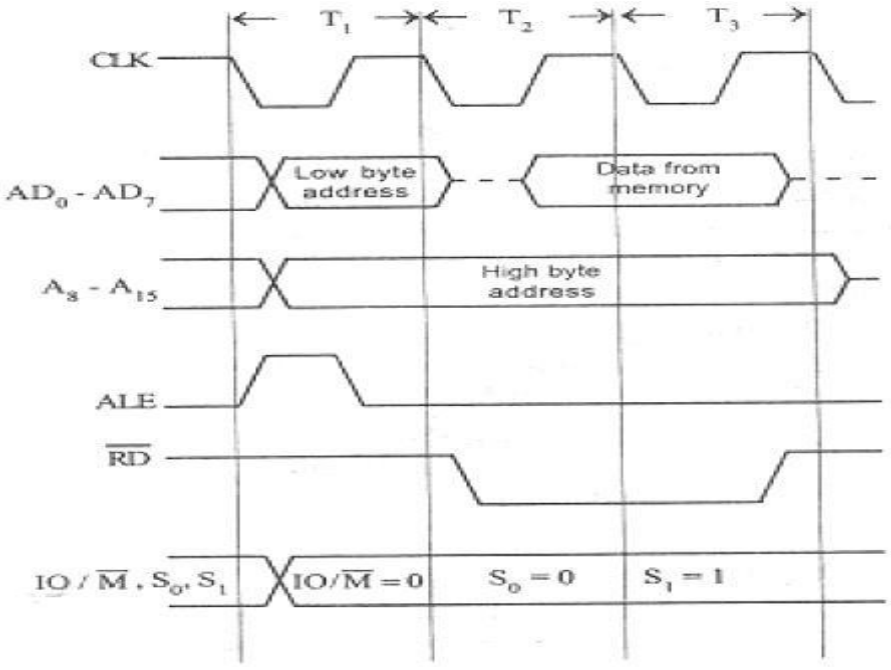
T4 State: -

- The T4-state is used by the processor for internal operations to decode the instruction and encode into various machine cycles.
- During this cycle the address and data bus will be in high impedance state.

(3) Explain memory read and Write operation with help of timing diagram.

Memory read Operation:-

- The memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to execute this cycle.
- Timing diagram of Memory Read cycle is shown in figure.



T1 State: -

- The microprocessor sends the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines.
- ALE is sending high to enable the address latch
- The other control signals are **IO**/$\overline{\mathbf{M}}$=0, S0=0, S1=1

T2 State: -

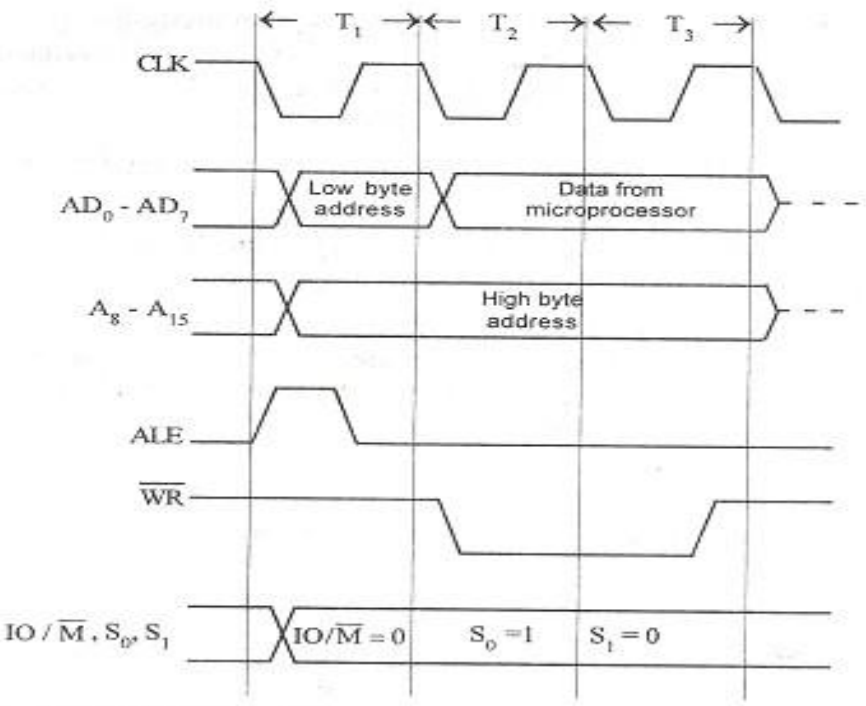
- The microprocessor sends the $\overline{\mathbf{RD}}$ to the memory.
- When $\overline{\mathbf{RD}}$ goes to low the memory is enabled for placing the data on the data bus.

T3 State: -

- The read signal goes to high. On the rising edge of read signal the data is latched into microprocessor other control signals remains in the same state

Memory write Operation:-

- The memory write cycle is executed by processor to write a data byte in a memory location.
- The processor takes 3T states to execute this machine cycle.
- The timing of various signals during memory write cycle is shown in fig below.



($\overline{RD}$ will be high ; READY is tied high either permanently or temporarily in the system.)

Memory write machine cycle of 8085

T1 State:

- The microprocessor sends the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines.
- ALE is sending high to enable the address latch.
- The other control signals are **IO**/$\overline{\mathbf{M}}$=0, S0=1, S1=0.

T2 State:-

- The microprocessor send the $\overline{\mathbf{WR}}$ to the memory.
- When $\overline{\mathbf{WR}}$ goes to low the memory is enabled for placing the data on the data bus. The time allowed for memory to write the data is the time during which $\overline{\mathbf{WR}}$ remains low.

T3 State: -

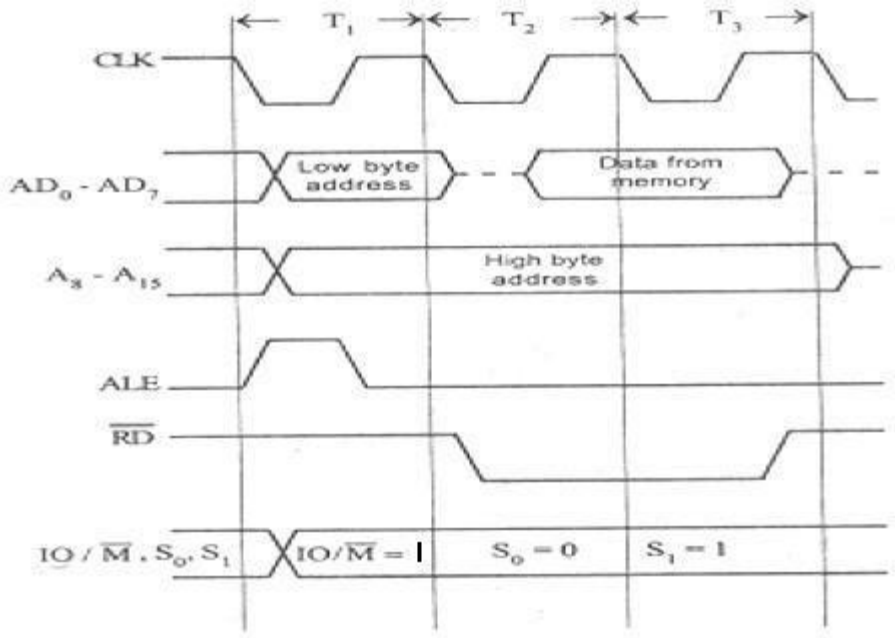
- The write signal goes to high.
- On the rising edge of write signal the data is write to memory other control signals remains in the same state until the next machine cycle.

(4) Explain I/O read and I/O Write operation with help of timing diagram.

I\O read Operation:-

- I\O read machine cycle is executed by the processor to read a data byte from input device.
- The processor takes 3T states to execute this cycle.

Timing diagram of I\O Read cycle is shown in figure.



T1 State: -

- The microprocessor sends the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines.
- ALE is sending high to enable the address latch.
- The other control signals are **IO/$\overline{\mathbf{M}}$**=1, S0=0, S1=1

T2 State:-

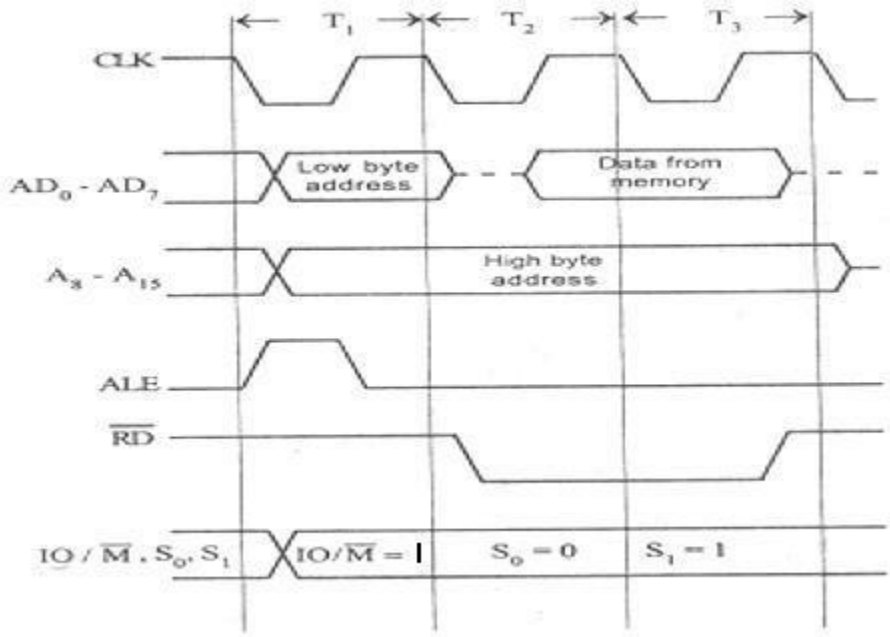
- The microprocessor send the **$\overline{\mathbf{RD}}$** to the memory.
- When **$\overline{\mathbf{RD}}$** goes to low the memory is enabled for placing the data on the data bus.

T3 State:-

- The read signal goes to high.
- On the rising edge of read signal the data is latched into microprocessor

I\O write Operation:-

- The I\O write cycle is executed by processor to write a data byte in a memory location.
- The processor takes 3T states to execute this machine cycle.
- The timing of various signals during memory write cycle is shown in fig below.



T1 State: -

- The microprocessor sends the low byte address on AD0-AD7 lines and high byte address on A8 to A15 lines.
- ALE is sending high to enable the address latch.
- The other control signals are **IO/$\overline{\mathbf{M}}$**=1, S0=1, S1=0

T2 State:-

- The microprocessor send the $\overline{\mathbf{WR}}$ to the memory.
- When $\overline{\mathbf{WR}}$ goes to low the memory is enabled for placing the data on the data bus.
- The time allowed for memory to write the data is the time during which $\overline{\mathbf{WR}}$ remains low.

T3 State:-

- The write signal goes to high.
- On the rising edge of write signal the data is write to memory other control signals remains in the same state until the next machine cycle.

PRACTICE QUESTION

(5) Draw the timing diagram of MVI B, 40 instruction. OR Draw timing diagram for MVI A, 55H and explain. OR What is timing diagram? Draw timing diagram for MVI B, 30H instruction.

Timing diagram is the display of initiation of read/write and transfer of data operations under the control of 3-status signals IO /$\overline{M}$, S1, and S0.

MVI B, 40h is the two by instruction one is for opcode fetch and second is Memory Read Operation. Timing Diagram is shown in figure below.