ECE 4515: Digital Design 2

Project 2: Optimizing Performance.

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"*I have neither given nor received unauthorized assistance on this assignment.*"
March 2, 2025
~Manav Shah

1. Introduction

The objective of this project is to become acquainted with different trade-offs a designer might have to make to satisfy design constraints. This assignment extends the objectives of the previous project in seeking a high-performance solution to the computation of the first four-term Maclaurin series for the exponential function:

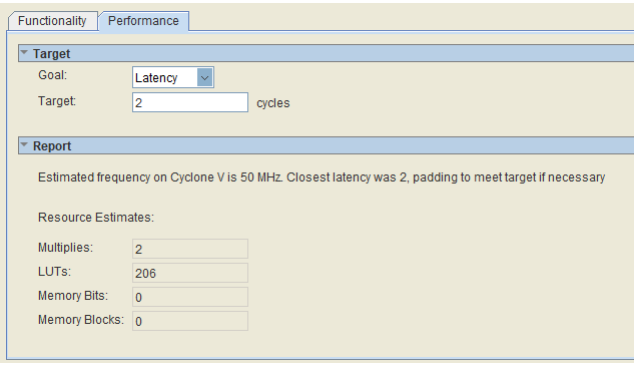
$$e^x - 1 = \sum_{n=1}^{\infty} \frac{x^n}{n!} = x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} \ldots$$

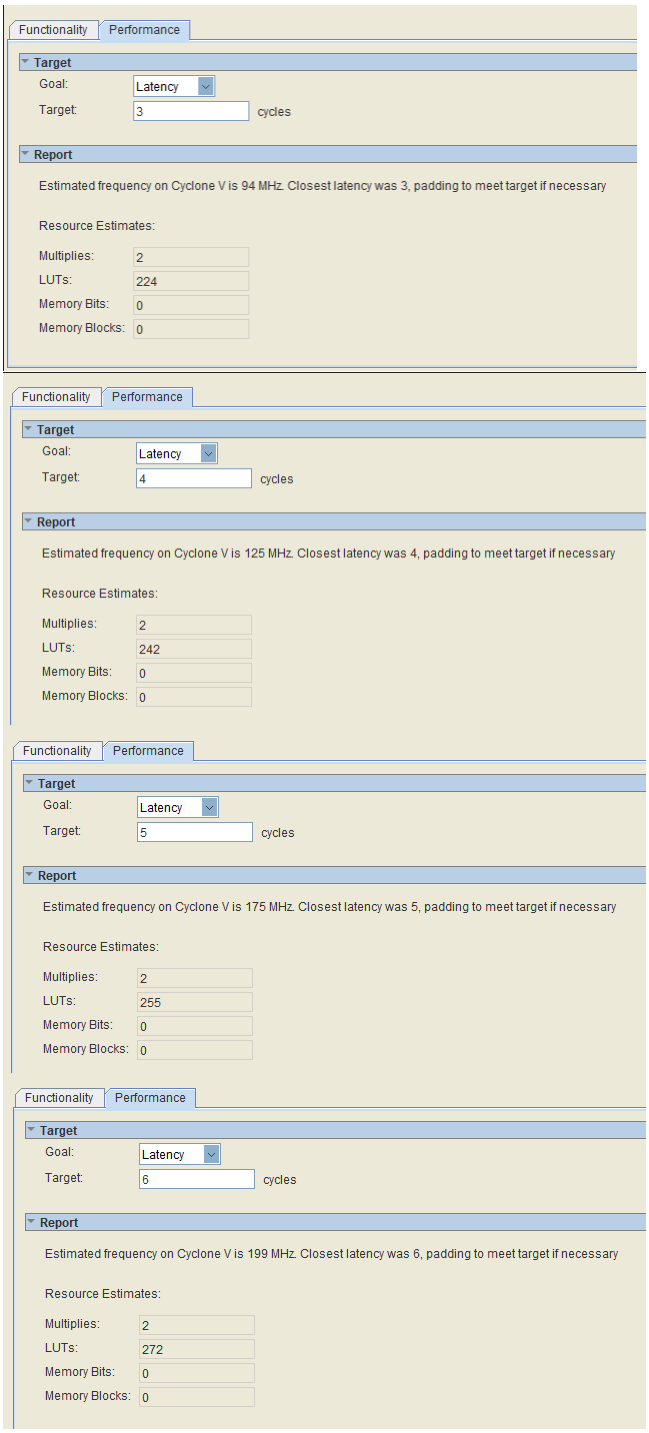
2. Reducing Operating Complexity

$$x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} = \frac{x}{24}(24 + 12x + 4x^2 + x^3) = (0.04166668x)(24 + 12x + 4x^2 + x^3)$$

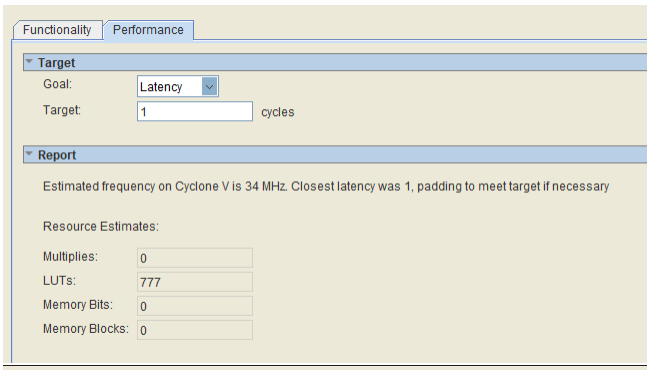
For implementing this system, I tried to reduce the space overhead from the division operation Floating point IP. This means that the three division operations were replaced by multiplication operations instead. In the original equation, there are 3 additions, 3 multiplications and 3 division operations necessary to get the output. In the final hardware optimized equation, you have 3 addition and 6 multiplication operations to get the same result. In this project, we are not bound by the 50MHz clock and can explore Ips with different latencies and a higher possible maximum frequency.

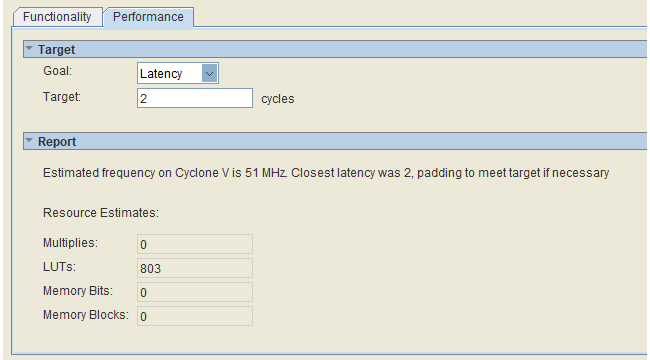
The following images show the predicted resource consumption for a different latency **multiplier** IPs

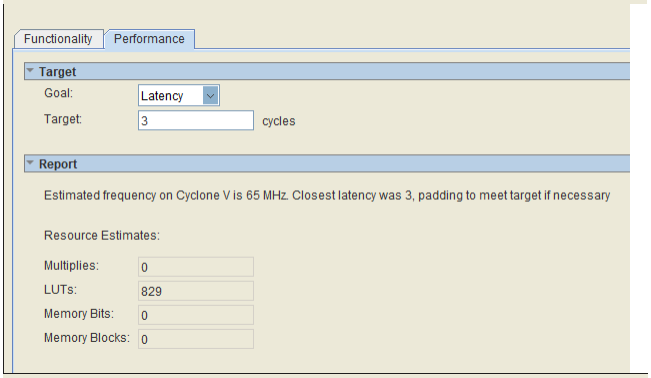


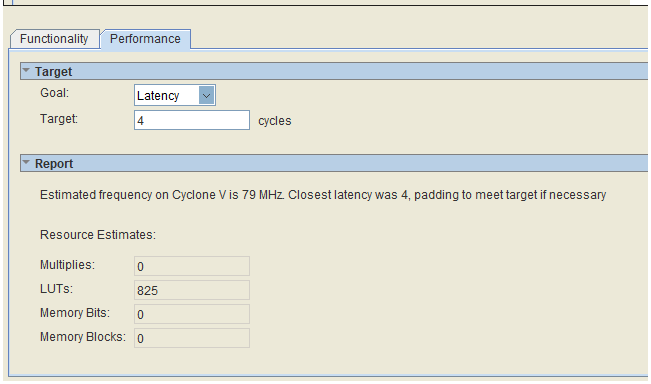


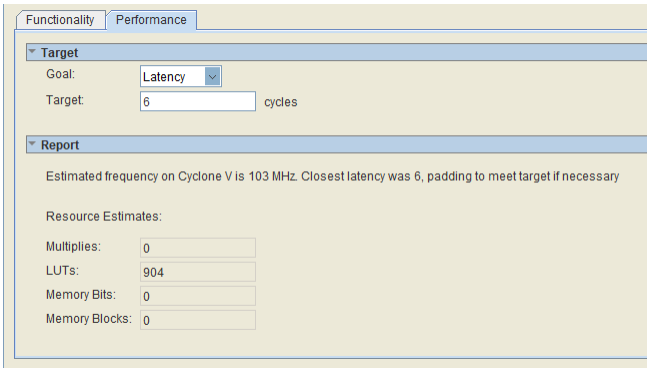
The following images show the predicted resource consumption for a different latency **adder** Ips


Functionality
Performance
Target
Goal:
Latency
Target:
1
cycles
Report
Estimated frequency on Cyclone V is 34 MHz. Closest latency was 1, padding to meet target if necessary
Resource Estimates:
Multiplies:
0
LUTs:
777
Memory Bits:
0
Memory Blocks:
0

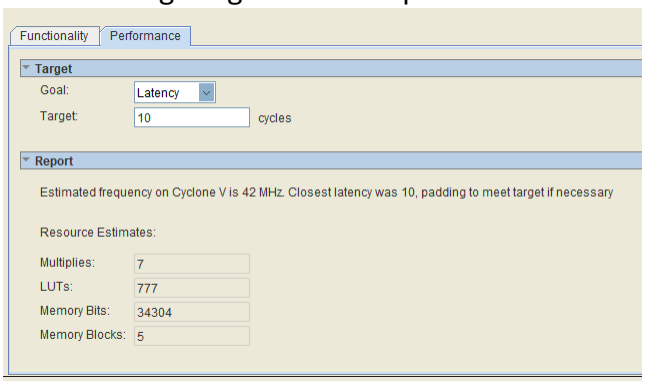

Functionality
Performance
Target
Goal:
Latency
Target:
2
cycles
Report
Estimated frequency on Cyclone V is 51 MHz. Closest latency was 2, padding to meet target if necessary
Resource Estimates:
Multiplies:
0
LUTs:
803
Memory Bits:
0
Memory Blocks:
0

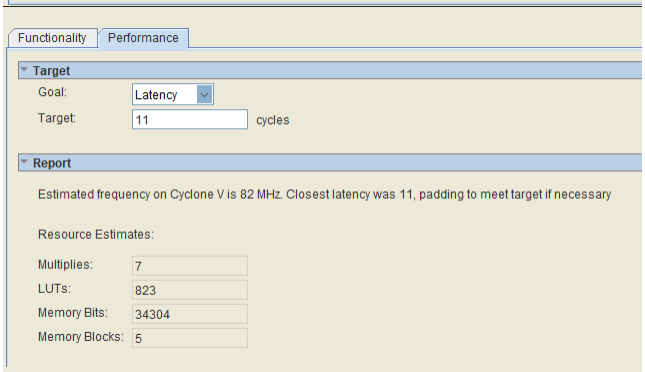

Functionality
Performance
Target
Goal:
Latency
Target:
3
cycles
Report
Estimated frequency on Cyclone V is 65 MHz. Closest latency was 3, padding to meet target if necessary
Resource Estimates:
Multiplies:
0
LUTs:
829
Memory Bits:
0
Memory Blocks:
0

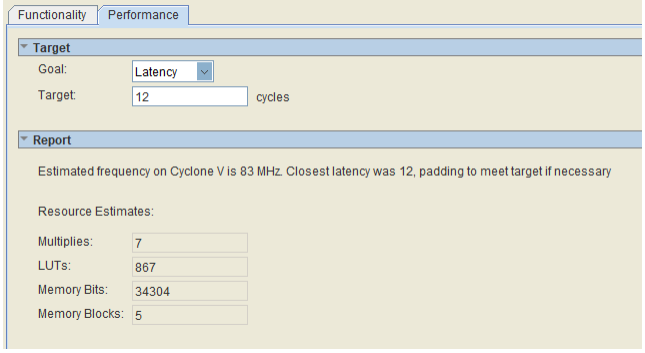

Functionality
Performance
Target
Goal:
Latency
Target:
4
cycles
Report
Estimated frequency on Cyclone V is 79 MHz. Closest latency was 4, padding to meet target if necessary
Resource Estimates:
Multiplies:
0
LUTs:
825
Memory Bits:
0
Memory Blocks:
0



The following images show the predicted resource consumption for a different latency **divider** lps.



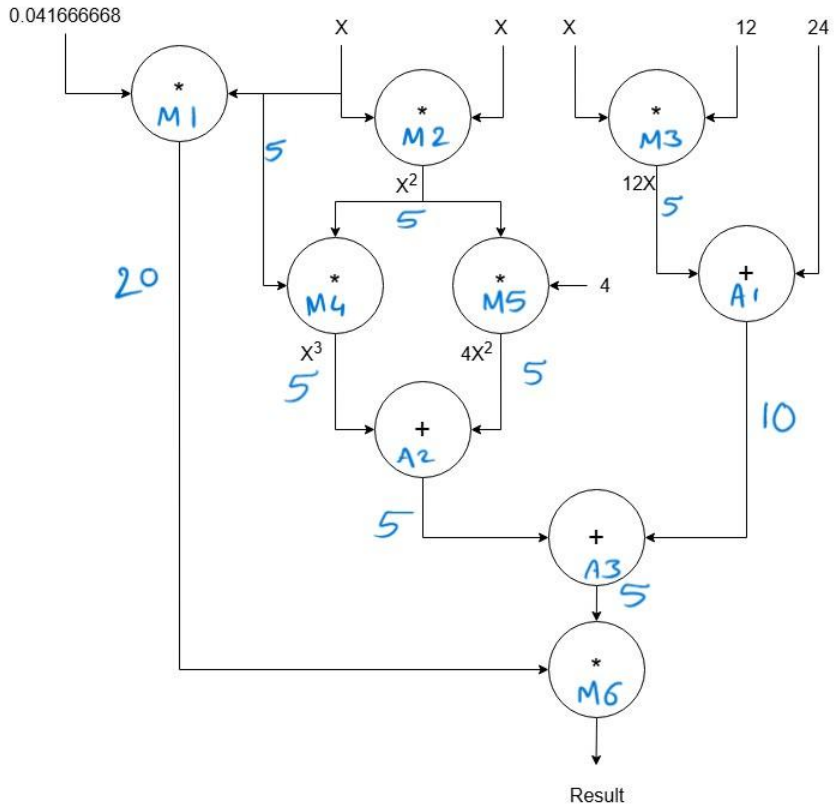




After performing several checks on estimated resource consumption and maximum operation frequency of several modules, I selected 5 cycle latency modules for adder and multipliers and used a delay module which allows me to add delays between intermediate results to equate path lengths.

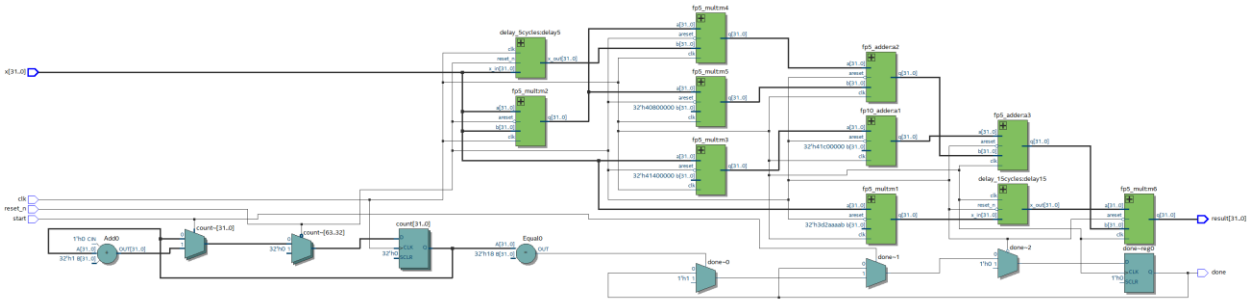
To create the delay module, I use flip flops to propagate the signal. The number of flipflops determines the latency.

3. Data Flow Graph for Optimized Equation



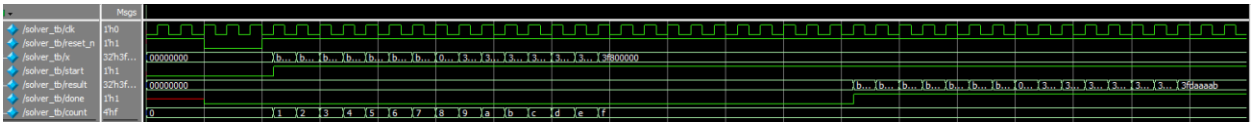
The latency of these Ips has been individually configured. The multipliers M1, M2, M3, M4, M5 and M6 all have a latency of 5 cycles. A 20-cycle latency multiplier was not possible, so I implanted a 5-cycle multiplier and 15 cycle delay module to adjust path lengths. The A1, A2 and A3 adders have latencies of 5 cycles with a 5-cycle delay connected after the A1 adder adjusts path length.

4. RTL of Solver

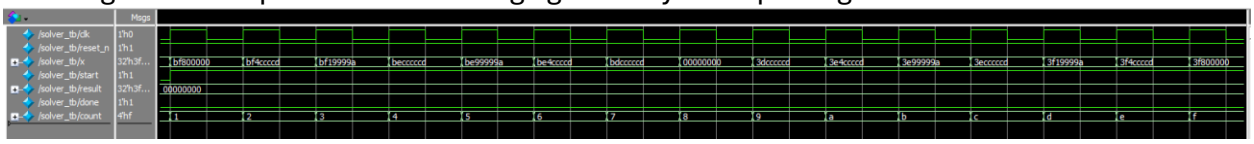


5. Testbench and simulation Design.

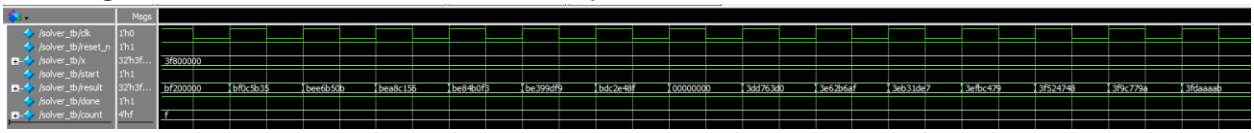
For the Testbench, a system Verilog file was written which provides stimulus values of x, start signal and clock pulses for operation of the design. The figure below shows the testbench waveforms.



Zooming in on the input stimulus x changing on every clock posedge



Zooming in on the Result values which are outputs of the Solver Module.

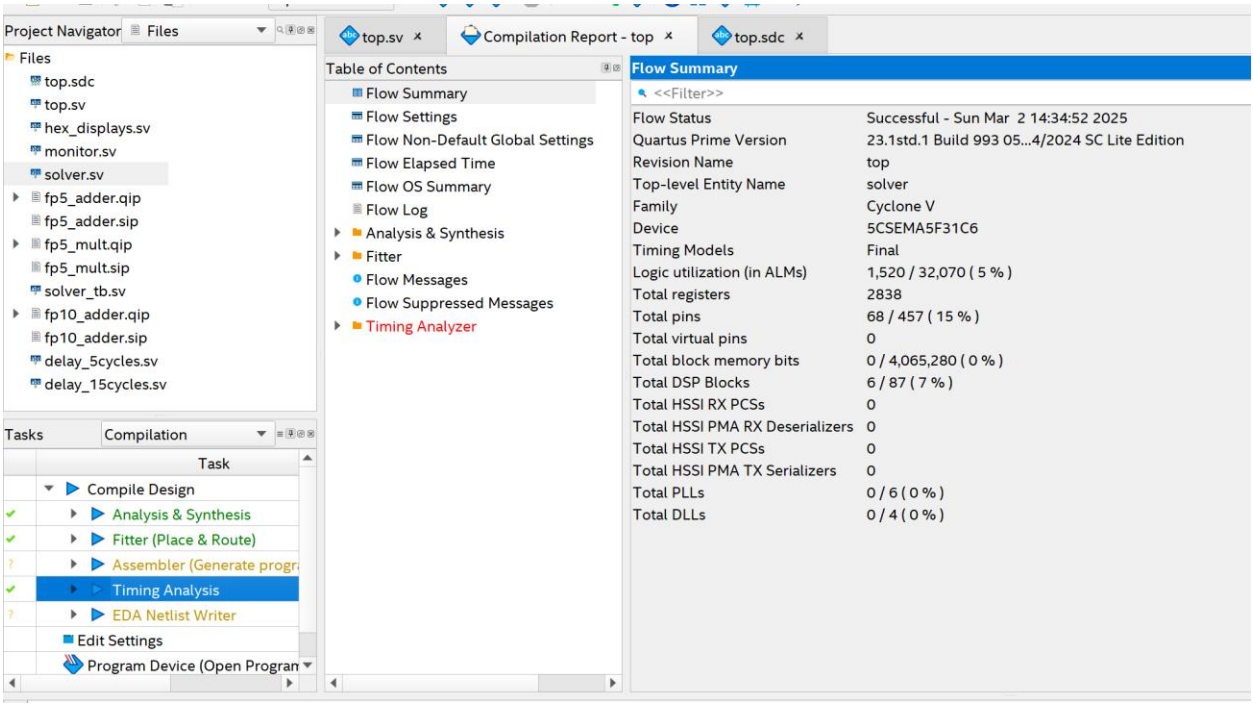


INDEX	Maclaurin Input (x)	Expected Values	Values on HEX display
0	-1	-0.625	bf200000
1	-0.8	-0.548266667	bf0c5b64
2	-0.6	-0.4506	bee6b506
3	-0.4	-0.3296	bea8c155
4	-0.3	-0.2591625	be84b0f2
5	-0.2	-0.181266667	be399df8
6	-0.1	-0.0951625	bdc2e48f
7	0	0	0
8	0.1	0.105170833	3dd763cf
9	0.2	0.2214	3e62b6ae
10	0.3	0.3498375	3eb31de8
11	0.4	0.491733333	3efbc479
12	0.6	0.8214	3f524746
13	0.8	1.2224	3f9c779b
14	1	1.708333333	3fdaaaaa

Table Showing the actual results expected from solver.

The result values seen in the waveforms are compared with the actual expected outputs from the table above and this is how the validity/correctness of the solver is established.

6. Flow Summary, Area and Max Operating Frequency.



Area Calculations:

*Area = (75 * DSP) + (ALM) + (0.001 * BLOCK_MEMORY_BITS)*
*= (75 * 6) + (1520) +(0.001*0)*
= 1,970.

Conclusion:
The project helped me understand the tradeoffs and optimizations which need to be considered while designing a system. Increasing operating frequency, reducing resource consumption are all valid goals and trying to find a middle ground which is optimal based on specifications is crucial.