

# 5

## Bipolar Junction Transistors and Field Effect Transistors

### 5.1 Introduction

Bipolar junction transistor (BJT) was invented in 1948 by Bardeen and Brattain under the guidance of William Shockley. It is a three terminal doped semiconductor device, which is widely used in electronic circuits (analog and digital both). For example, amplifier, oscillators, switches and logical circuits. There are two types of charged carriers which may involve in the transistor operations, so referred as electrons and holes, that is why this device is known as bipolar junction transistor or BJT.

The BJT is analogous to a vacuum triode. The main difference between the two is that the BJT is a current controlled device whereas vacuum triode is a voltage controlled device. BJT has many advantages over the vacuum tube such as smaller in size, light weight, more resistive to shocks and vibrations, quick operation, low operating voltage and long life etc. The BJT has some drawbacks as limited operating frequency (upto few MHz) and has restriction for operating temperature range in comparison to vacuum triode.

The Field-Effect-Transistor (FET) is a unipolar transistor which involves single carrier (either electrons or holes) operation. FET uses an electric field to control the flow of charge carriers through a channel in a semiconducting material. FETs are manufactured using a variety of materials such as silicon carbide (SiC), gallium arsenide (GaAS), gallium nitride (GaN). It is a voltage controlled device and hence shows a high degree of isolation between input and output. Main advantage of FET is its high input impedance (of the order of  $100\text{ M}\Omega$ ). The FET has low gain bandwidth product compare to BJT. It produces less noise and also has better thermal stability than BJT.

## 5.2 Construction of Transistor

It consists of two PN-junction diodes, which are cemented back-to-back or front-to-front. In other words, it may either have a N-type semiconductor sandwiched between two P-type semiconductors or a P-type semiconductor inserted between two N-type semiconductors. These arrangements are referred as PNP or NPN as shown in Figs. 5.1(a) and (b) respectively.

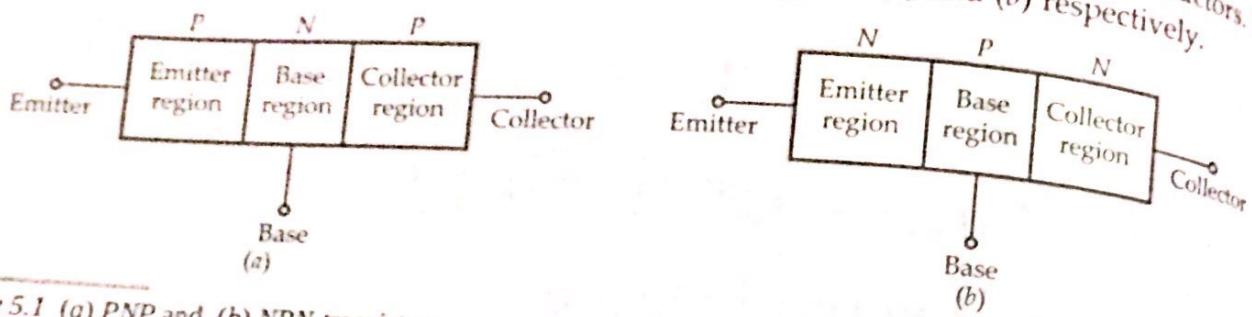


Figure 5.1 (a) PNP and (b) NPN transistors.

The BJT (PNP or NPN transistor) has three regions – emitter, base and collector and having two junctions i.e., emitter-base and collector-base. Usually emitter has large doping so that it can provide more majority carriers. Base is lightly doped and thin (less majority carriers available). Collector is thick and collects almost all the majority carriers emitted from emitter region. In actual construction, emitter and collector are not symmetrical, thus cannot be interchanged.

## 5.3 BJT Biasing

Different modes of transistor operation depend upon the bias condition of each of the two junctions, namely, emitter-base and collector-base as listed in Table 5.1.

Table 5.1 Bias conditions for different modes of transistor operations.

Operation Mode	Emitter-Base Junction (E-B)	Collector-Base Junction (C-B)
Active	Forward bias	Reverse bias
Cut-off	Reverse bias	Forward bias
Saturation	Forward bias	Forward bias

For transistor to be operated in the active mode E-B junction should be forward biased and C-B junction should be in reverse bias. In amplifiers and oscillator circuits, transistor must operate in *active mode*, whereas in switching and other logical circuits, transistor must operate in either *cut off* or in *saturation mode*.

The circuit symbols of PNP and NPN type transistors are shown in Figs. 5.2(a) and (b) respectively. The arrow in the emitter indicates the direction of emitter current.

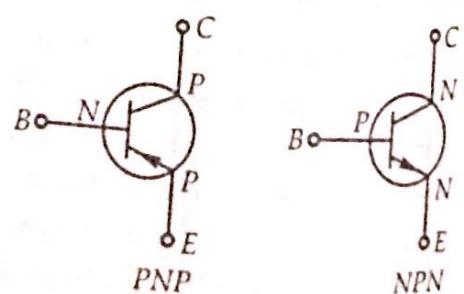


Figure 5.2 (a) Circuit symbols of PNP and (b) NPN bipolar transistors.

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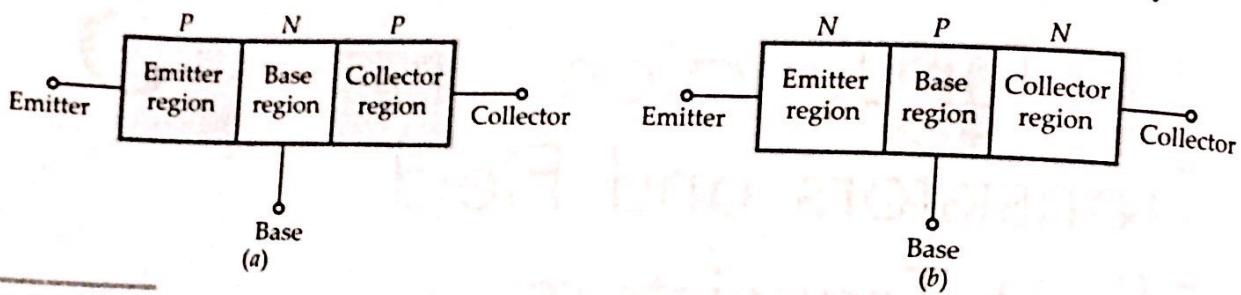


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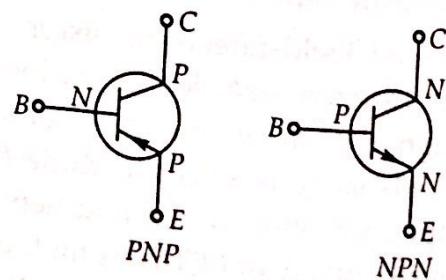


Figure 5.2 (a) Circuit symbols of PNP and (b) NPN.

## 5.4 Transistor Operation

The action of *PNP* transistor in *active mode* (normal mode) is explained as follows (Fig. 5.3):

Electrons are majority carriers in the *P*-region and holes are majority carriers in the *N*-region. The forward bias on emitter-base (*E-B*) junction forces the holes in the emitter to travel from emitter to base region. Few holes recombine with the electrons present in the base while most of them ( $\approx 95\%$ ) cross the base and enter into the mild doped collector region. This happens because base region is thin and lightly doped. The collector-base junction is reverse biased, therefore negative terminal of the  $V_{CB}$  will attract the holes. The current flow in the emitter, base and collector leads, due to carriers movement, can be explained as follows : total current ( $I_E$ ) consists of base current ( $I_B$ ) and collector current ( $I_C$ ). The number of electrons in base region is very small ; hence very few holes will recombine with electrons to constitute base current  $I_B$ . The rest of holes cross the base to reach the collector region constitute collector current  $I_C$ . Further collector current consists of two components one is due to holes reaching collector region from emitter region after crossing the base region and other is due to reverse saturation current  $I_{CBO}$  (contribution of minority carriers). If  $\alpha$  is the fraction of emitter current reaching the collector region, then total collector current will be sum of  $\alpha I_E$  and reverse saturation current ( $I_{CBO}$ ).

Thus

$$I_E = I_C + I_B \quad \dots(5.1)$$

and

$$I_C = \alpha I_E + I_{CBO} \quad \dots(5.2)$$

where  $I_{CBO} = I_{CO}$  = reverse saturation current flowing through the reverse biased collector-base junction ; or collector to base leakage current when emitter is open.

From Eq. (5.2),  $I_C = \alpha I_E + I_{CO}$

or  $I_C = \alpha(I_C + I_B) + I_{CO}$  [From Eq. (5.1)]

or  $(1-\alpha)I_C = \alpha I_B + I_{CO}$

or  $I_C = \left(\frac{\alpha}{1-\alpha}\right)I_B + \left(\frac{1}{1-\alpha}\right)I_{CO} \quad \dots(5.3)$

We will define another parameter as  $\beta = \frac{\alpha}{1-\alpha} \quad \dots(5.4)$

We get,  $I_C = \beta I_B + (\beta + 1)I_{CO} \quad \dots(5.5)$

where  $\alpha$  and  $\beta$  are current amplification factors in common base configurations. Usually reverse saturation current is negligible therefore ( $I_{CO} \approx 0$ ).

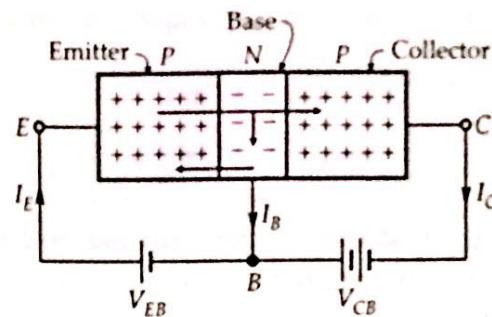


Figure 5.3 Biasing for a BJT + and - signs show the holes and electrons as majority carriers in *P* and *N* layers respectively.

The expression for collector current  $I_C$  reduces to,

$$I_C = \beta I_B$$

Typical values of  $\alpha$  ranging from 0.9 to 0.95 and of  $\beta$  varies from 50 to 150 or more. Equations (5.1) - (5.6) are general equations of a transistor for any configuration (PNP or NPN). ... (5.6)

**DC Current Gain ( $\beta_{dc}$  or  $h_{FE}$ )**

$$\beta_{dc} = \frac{E_C}{I_B}$$

... (5.7)

$\beta_{dc}$  is defined as ratio of collector current to base current. This parameter is very important for transistor circuit design. Its value is provided by the transistor manufacturer. Usually  $\beta_{dc}$  and  $\beta_{ac}$  remain same.

The action of NPN transistor is similar to that of a PNP type except that role of electrons and holes is interchanged. Biasing and current directions in NPN configuration are shown in Fig. 5.4.

General transistor equation is,  $I_E = I_B + I_C$ .

**Relationship between  $I_{CBO}$  and  $I_{CEO}$**

Consider Eq. (5.3),

$$I_C = \left( \frac{\alpha}{1-\alpha} \right) I_B + \left( \frac{1}{1-\alpha} \right) I_{CBO}$$

... (5.8)

If  $I_B = 0\mu A$  and  $\alpha = 0.996$  (typical value), then collector current  $I_C$  reduces to,

$$I_C = \left( \frac{1}{1-\alpha} \right) I_{CBO} = 250 I_{CBO}$$

... (5.9)

We define a new parameter,  $I_{CEO}$  as :

$$I_{CEO} = \left( \frac{I_{CBO}}{1-\alpha} \right)_{I_B=0\mu A} = (1+\beta_{dc}) I_{CBO}$$

... (5.10)

$$I_{CEO} > I_{CBO}$$

where  $I_{CBO}$  = collector-to-base reverse saturation current and

$I_{CEO}$  = collector-to-emitter current when base is open.

Therefore, in a transistor operation  $I_{CEO}$  is much greater than  $I_{CBO}$ .

**Example 5.1** In a transistor, emitter current is  $3\text{ mA}$ ,  $\alpha = 0.95$ , leakage current  $I_{CBO} = 5\mu A$ . Calculate base current and collector current.

**Solution.** Given  $I_E = 3\text{ mA}$ ,  $\alpha = 0.95$ ,  $I_{CBO} = 5\mu A$

(i) The collector current  $I_C = \alpha I_E + I_{CBO} = 0.95 \times 3 + 0.005 = 2.855\text{ mA}$

(ii) The base current  $I_B = I_E - I_C \quad \therefore I_B = I_E - I_C = 3 - 2.855 = 0.145\text{ mA}$ .

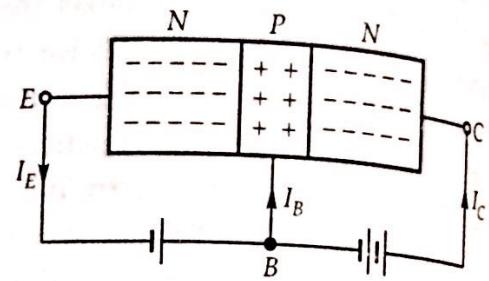


Figure 5.4 Biasing and flow of currents in NPN configuration.

**Example 5.2** In common base configuration circuit, collector current is 0.96 mA and base current is 50 µA. Calculate  $\alpha$  and  $\beta$ .

Solution. Given  $I_C = 0.96 \text{ mA}$ ,  $I_B = 50 \mu\text{A}$

$$(i) \quad \alpha = \frac{I_C}{I_E} = \frac{0.96}{0.96+0.05} = 0.95 \quad (\because I_E = I_C + I_B)$$

$$(ii) \quad \beta = \frac{I_C}{I_B} = \frac{0.96}{0.05} = 19.2 \quad (\because I_{CBO} \approx 0, \text{ neglected})$$

**Example 5.3** In CB arrangement, a voltage drop of 5 V is obtained across load  $5 \text{ k}\Omega$ , connected in collector circuit. If  $\alpha = 0.99$ , find the collector and base current.

Solution. Given  $V_C = 5 \text{ V}$ ,  $R_C = 5 \text{ k}\Omega = 5 \times 10^3 \text{ }\Omega$ .

$$(i) \text{ The collector current } I_C = \frac{V_C (= V_L)}{R_C} = \frac{5}{5 \times 10^3} = 1 \text{ mA}$$

$$(ii) \text{ The base current } \alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha} = \frac{1}{0.99} = 1.01 \text{ mA}$$

$$\therefore \text{Base current } I_B = I_E - I_C = 1.01 - 1 = 0.01 \text{ mA}$$

**Example 5.4** Calculate emitter current in a transistor for which  $\beta = 40$  and  $I_B = 25 \mu\text{A}$ .

Solution. Given  $\beta = 40$  and  $I_B = 25 \mu\text{A} = 0.025 \text{ mA}$

$$\text{Then } I_C = \beta I_B = 40 \times 25 \times 10^{-3} \text{ mA} = 1 \text{ mA}$$

$$I_E = I_C + I_B = 1 + 0.025 = 1.025 \text{ mA}$$

and,  $I_C, I_B, I_E, I_{CEO}$  and  $\beta$ .

**Example 5.5** In a transistor,  $\alpha = 0.99$ ,  $I_E = 10 \text{ mA}$ ,  $I_{CBO} = 0.5 \mu\text{A}$ . Calculate  $I_C$ ,  $I_B$ ,  $I_{CEO}$  and  $\beta$ .

Solution. Given  $\alpha = 0.99$ ,  $I_E = 10 \text{ mA}$ ,  $I_{CBO} = 0.5 \mu\text{A}$

$$(i) \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99 \quad (ii) \quad I_C = \alpha I_E + I_{CBO} = 0.99 \times 10 + 0.5 \times 10^{-3} (\text{mA}) = 9.90 \text{ mA}$$

$$(iii) \quad I_E = I_C + I_B ; \quad I_B = I_E - I_C = 10 \text{ mA} - 9.90 \text{ mA} = 0.10 \text{ mA}$$

$$(iv) \quad I_{CEO} = \left( \frac{I_{CBO}}{1-\alpha} \right) = (1+\beta) I_{CBO} = (1+99) \times 0.5 \times 10^{-3} \text{ mA} = 0.05 \text{ mA}$$

**Example 5.6** In an NPN transistor,  $\alpha = 0.995$ .  $I_E = 10 \text{ mA}$ ,  $I_{CO} = 0.5 \mu\text{A}$ . Determine the values of  $I_C$ ,  $I_B$  and  $I_{CEO}$ . [GGSIPU, Nov. 2013 (2.5 marks)]

Solution. Given  $\alpha = 0.995$ ,  $I_E = 10 \text{ mA}$ ,  $I_{CO} = 0.5 \mu\text{A} = 0.5 \times 10^{-3} \text{ mA} = 0.0005$

$$(i) \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.995}{1-0.995} = 199 \quad (\because I_{CBO} = I_{CO})$$

$$(ii) \quad I_C = \alpha I_E + I_{CO} = (0.995 \times 10 + 0.0005) \text{ mA} = 9.9505 \text{ mA}$$

$$(iii) \quad I_{CEO} = (1+\beta) I_{CBO} = (1+\beta) I_{CO} = [(1+199) \times 0.5] \mu\text{A} = 100 \mu\text{A}$$

$$(iv) \quad I_B = I_E - I_C = 10 - 9.9505 = 0.0495 \text{ mA}$$

## 5.5 Transistor Configurations

BJT can be connected in *three* ways in a circuit as follows :

- Common emitter configuration, in which emitter terminal is common between input and output circuits. Here base and collector are input and output terminals respectively.
- Common base configuration, in which base terminal is common between input (emitter) and output (collector) circuits.
- Common collector configuration, in which collector terminal is common between input (base) and output (emitter) circuits.

Usually common terminal is grounded. Figure 5.5 shows the circuit arrangement for normal (active) mode operation of an *NPN* transistor in all three configurations.

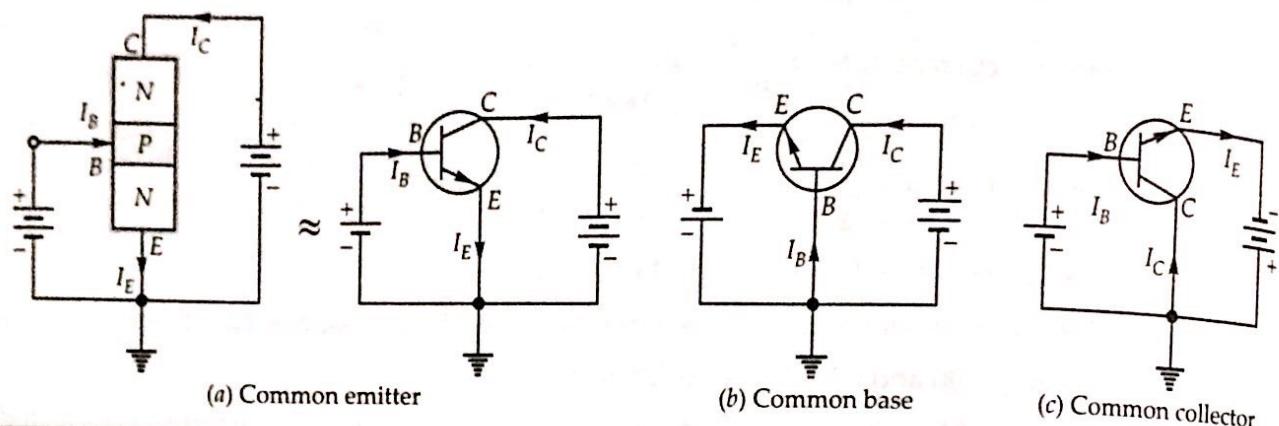


Figure 5.5 Different configuration of *NPN* transistor.

## 5.6 Transistor Characteristics

The transistor circuit behaviour and characteristic curves are very different in the three biasing cases *i.e.*, *CB*, *CE* and *CC* configurations. To study the input and output characteristics of the transistor, hybrid model is used in which input current and output voltage are considered as independent variables while input voltage and output current are dependent on them.

### 5.6.1 The Common Base (CB) Configuration

Practical circuit for input and output characteristics of an *NPN* transistor is shown in Fig. 5.6.

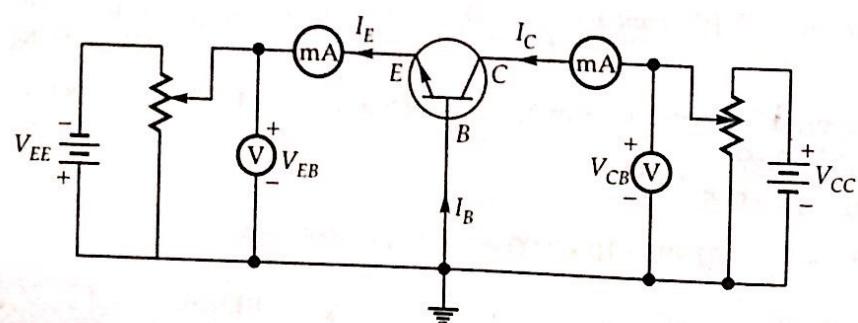


Figure 5.6 Circuit for *NPN* transistor characteristics in common-base arrangement.

For forward biased base junction,  $V_{EB}$  is negative and for reverse biased collector junction,  $V_{CB}$  is kept positive with respect to base which is grounded.

*Input characteristics.*  $V_{EB} = f_1(V_{CB}, I_E)$

By keeping collector-base voltage ( $V_{CB}$ ) constant, variation of emitter-base voltage ( $V_{EB}$ ) with emitter current ( $I_E$ ) gives the input characteristics of the transistor as shown in Fig. 5.7.

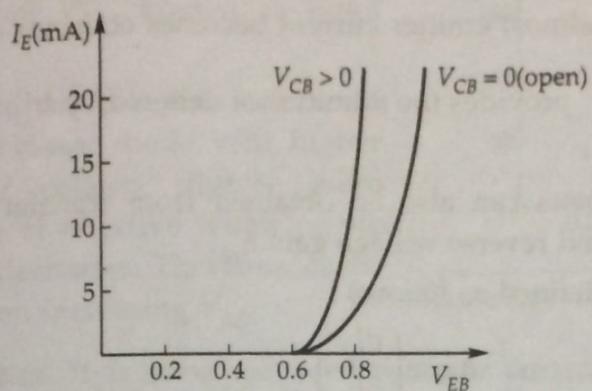


Figure 5.7 Input characteristics.

In the normal operation, the input diode is forward biased. So the input characteristic is similar to forward diode characteristic. Below the cut-in voltage (0.3 or 0.7 V) emitter current is very small. When  $V_{CB} = 0$ , circuit will represent the forward biased emitter diode when  $V_{CB}$  is increased by keeping  $V_{EB}$  constant,  $I_E$  increases. Therefore, curve shifted towards the left. The

slope of the curve  $\left( \frac{\partial V_E}{\partial I_E} \right)_{V_{CB}}$  provides the input impedance represented by  $h_{11}$  or  $h_{ib}$ .

*Output characteristics.*  $I_C = f_2(V_{CB}, I_E)$

It is obtained by plotting the variation of collector current  $I_C$  with collector-base ( $V_{CB}$ ) voltage by keeping emitter current as constant as shown in Fig. 5.8.

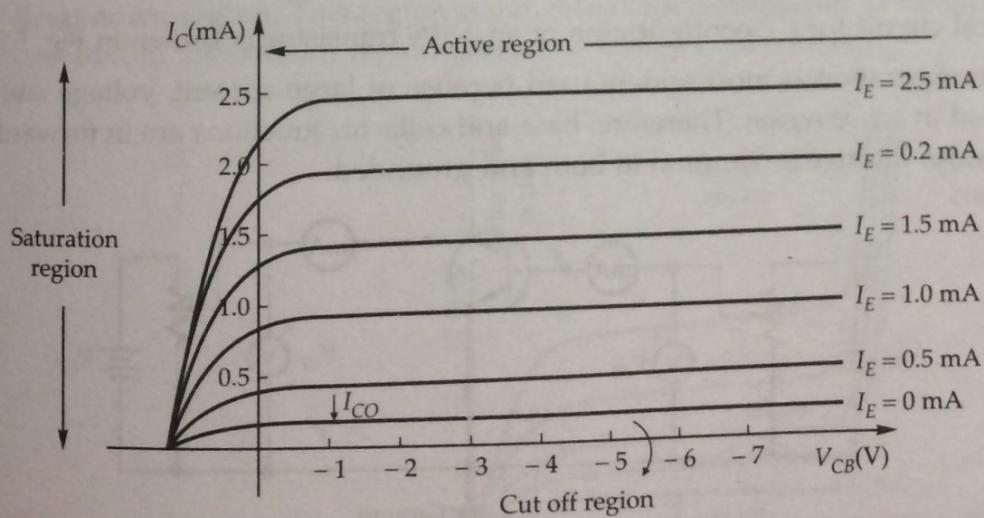


Figure 5.8 Output characteristics.

From characteristics curve (Fig. 5.8), it is clear that the collector current ( $I_C$ ) is very small when  $I_E = 0$  and becomes reverse saturation current  $I_{CO}$  of the collector junction. Collector current slightly increases with the  $V_{CB}$  and curves are parallel to the  $V_{CB}$  horizontal axis. This is due to early effect. At higher  $V_{CB}$  voltage collector collects a few more electrons. This reduces the base current. This difference is very small and hence neglected. If collector voltage is increased, depletion width increases, this decreases the effective width of the base. As a result, less chance of recombination in the base region. Therefore almost emitter current becomes collector current,  $I_C \approx I_E (I_B = 0)$ . The

slope of this curve  $\left( \frac{\partial I_C}{\partial V_{CB}} \right)_{I_E}$  provides the admittance denoted by  $h_{22}$  or  $h_{ob}$ .

Further two parameters can also be obtained from transfer characteristics, termed as forward current gain,  $h_{fb}$  and reverse voltage gain  $h_{rb}$ .

The parameters are defined as follows :

$$h_{fb} = \left( \frac{\partial I_C}{\partial I_E} \right)_{V_{CB}} \quad \dots(5.11)$$

$$h_{rb} = \left( \frac{\partial V_{EB}}{\partial V_{CB}} \right)_{I_E} \quad \dots(5.12)$$

Typical values of input impedance  $h_{ib}$  varying from 15 to 50  $\Omega$ ,  $h_{ob}$  can take value of the order of 5  $\mu$ mohs,  $h_{fb}$  has value ranging from 0.9 to 0.999 and typical value of  $h_{rb}$  is about  $10^{-5}$ .

Saturation region in the output characteristic, lies on the left of ordinate  $V_{CB} = 0$  and above  $I_E = 0$ . In this region both emitter and collector junctions are forward biased. If diodes are sufficiently forward biased then  $I_C$  changes fast and does not depend on the emitter current.

Cut-off region lies on the right of  $V_{CB}$  i.e.,  $V_{CB} = 0$  and below  $I_E = 0$ , where both emitter and collector junctions are reverse biased. As  $I_E = 0$ ,  $I_C = I_{CO}$  i.e., reverse saturation current in the output. This current ( $I_{CO}$ ) strongly increases with temperature.

### 5.6.2 The Common Emitter (CE) Configuration

Practical circuit for CE configuration of an NPN transistor is shown in Fig. 5.9.

This configuration is most widely used because of large current, voltage and power gain. BJT is operated in *active region*. Therefore, base and collector junctions are in forward and reverse bias respectively. Emitter is common in both and grounded.

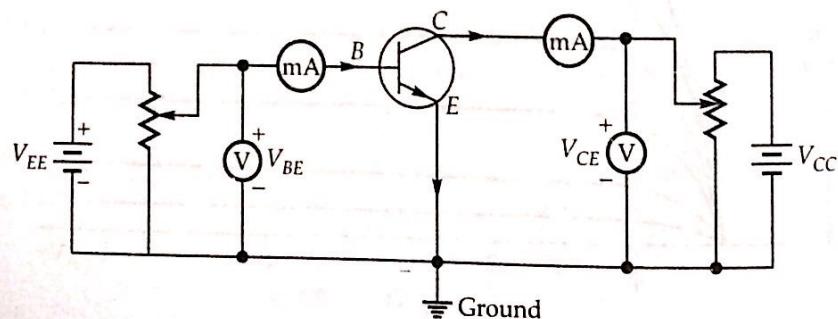


Figure 5.9 Circuit for NPN transistor characteristics in common-emitter arrangement.

**Input characteristics.** In this case, base-current ( $I_B$ ) and output collector-emitter voltage ( $V_{CE}$ ) are taken as independent parameters and input voltage ( $V_{BE}$ ) and output current ( $I_C$ ) as dependent parameters.

Thus  $V_{BE} = f_1(I_B, V_{CE})$  and  $I_C = f_2(I_B, V_{CE})$

Figure 5.10 shows the curves between  $I_B$  and  $V_{BE}$  for different values of  $V_{CE}$ , known as input characteristic curves.

At  $V_{CE} = 0\text{V}$ , emitter-base junction is forward biased, it acts as a forward biased diode. With higher values of  $V_{CE}$ , collector collects slightly more electrons due to decrease of effective width of the base, hence base current decreases. Therefore curve shifted towards the right on increasing  $V_{BE}$ .

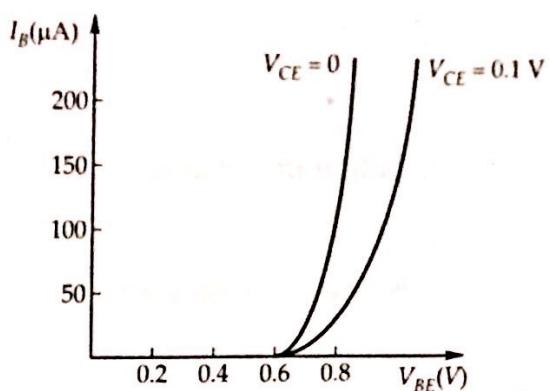


Figure 5.10 Input characteristics

**Output characteristics.** It is curve between collector current ( $I_C$ ) and collector-emitter voltage ( $V_{CE}$ ) for different values of  $I_B$  as shown in Fig. 5.11.

- Active region.** In this case emitter and collector junctions are forward and reverse biased respectively. The region above  $I_B = 0$  and between two dotted vertical lines. Here collector gathers almost all electrons, emitted and injected from the emitter. Therefore any change in  $V_{CE}$  has no effect on  $I_C$ . This region is more sensitive to base current ( $I_B$ ). For amplifier circuit, transistor must operate in this region.
- Cut-off region.** This region is defined by  $I_B = 0$  and  $I_C = I_{CO}$ . This bottom curve is called the collector cut-off current. For a given transistor 2N3904, approximately 50 nA collector cut-off current flows.
- Saturation region.** Region between ordinate ( $V_{CE} = 0$ ) and first dotted vertical line ( $V_{CE} \approx 0.1\text{V}$ ) is called the *saturation region*. Both the junctions now act as forward biased diode. In this case,  $I_B$  is larger than the normal value and current gain  $\beta_{dc}$  is smaller than the normal values. In this region, collector current  $I_C$  is almost independent of  $I_B$ .
- Breakdown region.** This region is dangerous for a transistor. Transistor must not be operated in breakdown region otherwise it may be destroyed.

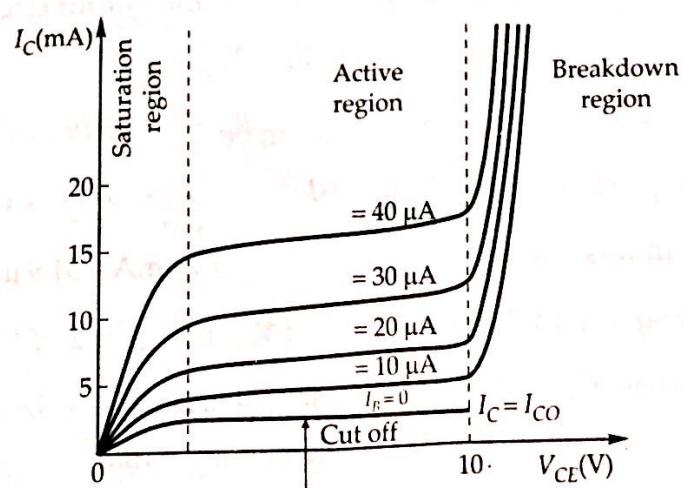


Figure 5.11 Output characteristics.

The four transistor parameters can be easily obtained by input and output characteristics in CE configurations.

$$(a) \text{ Input impedance, } h_{ie} = \left( \frac{\partial V_{BE}}{\partial I_B} \right)_{V_{CE}}, \text{ slope of input curve.}$$

$$(b) \text{ Output impedance, } h_{oe} = \left( \frac{\partial I_C}{\partial V_{CE}} \right)_{I_B}, \text{ slope of output curve.}$$

$$(c) \text{ Forward current gain, } h_{fe} = \left( \frac{\partial I_C}{\partial I_B} \right)_{V_{CE}}$$

$$(d) \text{ Reverse voltage gain, } h_{re} = \left( \frac{\partial V_{BE}}{\partial V_{CE}} \right)_{I_B}$$

Typical values of  $h_{ie}$ ,  $h_{oe}$ ,  $h_{fe}$  and  $h_{re}$  are  $1\text{k}\Omega$ ,  $10\mu\text{mhos}$ ,  $150$  and  $10^{-5}$  respectively.

**Example 5.7** A transistor is connected in CE configuration as shown in Fig. 5.12. Use the ideal transistor. Determine (i)  $V_{BE}$  (ii)  $I_B$  (iii)  $I_C$  (iv)  $V_{CE}$  (v)  $I_E$ .

**Solution.** Given  $R_B = 470\text{k}\Omega$ ,  $R_C = 3.6\text{k}\Omega$ ,  $V_{in} = 15\text{V}$ ,  $V_0 = 15\text{V}$  and  $\beta_{dc} = 100$

(i) For ideal transistor,  $V_{BE} = 0$ .

(ii)  $I_B$  determination. Apply KVL in the input circuit (base circuit)

$$V_{in} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{in}}{R_B} = \frac{15}{470 \times 10^3} \quad (\because V_{BE} = 0\text{V})$$

$$= 31.9\mu\text{A}$$

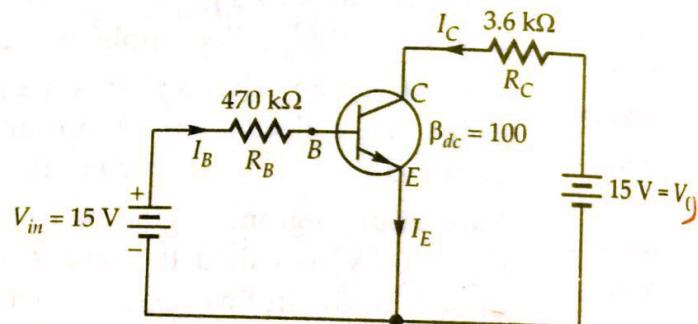


Figure 5.12

(iii)  $I_C$  determination.  $\because I_C = \beta I_B \quad \therefore I_C = 100 \times 31.9\mu\text{A} = 3.19\text{mA}$ .

(iv)  $V_{CE}$  determination. Apply KVL in the output circuit i.e., collector circuit.

$$V_0 = I_C R_C + V_{CE}$$

$$\therefore V_{CE} = V_0 - I_C R_C = 15 - (3.19 \times 10^{-3}) \times 3.6 \times 10^3 = 15 - 11.48 = 3.52\text{V}$$

(v)  $I_E$  determination. Usually  $I_E \approx I_C$ , because  $I_B$  is very small.

In this case

$$I_E = I_C + I_B = 3.19\text{mA} + 31.9\mu\text{A} = 3.22\text{mA}$$

**Example 5.8** What are  $I_B$ ,  $I_C$  and  $V_{CE}$  in Fig. 5.12, if  $V_{BE} = 0.7\text{V}$ ?

**Solution.** Given  $V_{BE} = 0.7\text{V}$ ,  $R_B = 470\text{k}\Omega$ ,  $R_C = 3.6\text{k}\Omega$ ,

$$V_{in} = V_0 = 15\text{V} \text{ and } \beta_{dc} = 100.$$

(i) KVL in the input circuit,  $V_{in} = I_B R_B + V_{BE}$

$$\therefore I_B = \frac{V_{in} - V_{BE}}{R_B} = \frac{15 - 0.7}{470 \times 10^3} = 30.4 \mu\text{A}$$

(ii)  $I_C = \beta \cdot I_B = 100(30.4 \times 10^{-3}) \text{ mA} = 3.04 \text{ mA}$

(iii) KVL in the output circuit

$$V_0 = I_C R_C + V_{CE}$$

$$\therefore V_{CE} = V_0 - I_C R_C = 15 - 3.04 \times 10^{-3} \times 3.6 \times 10^3 = 4.06 \text{ V}$$

**Example 5.9** In a CE transistor circuit, collector to emitter ( $V_{CE}$ ) voltage changes from 5 V to 10 V, causes the change in collector current from 5 mA to 5.8 mA. Determine the dynamic output resistance.

$$\begin{aligned} \text{Solution. Dynamic output resistance } (r_0) &= \frac{\Delta V_{CE}}{\Delta I_C} = \frac{10 - 5}{(5.8 - 5) \times 10^{-3}} \\ &= \frac{5}{0.8 \times 10^{-3}} = 6.25 \text{ k}\Omega \end{aligned}$$

### 5.6.3 Common Collector (CC) Configurations

In this arrangement, collector of the transistor is common in both input and output circuits as shown in Fig. 5.13. Here NPN transistor is considered for determination of transistor characteristics. The common collector configuration offers high input impedance and low output impedance and hence it is used for impedance matching applications. Voltage gain offered by this arrangement is less than unity and current gain is high. Power gain is also very small. Therefore such configuration is rarely used for amplification.

The input and output characteristics are shown in Figs. 5.14 and 5.15 respectively.

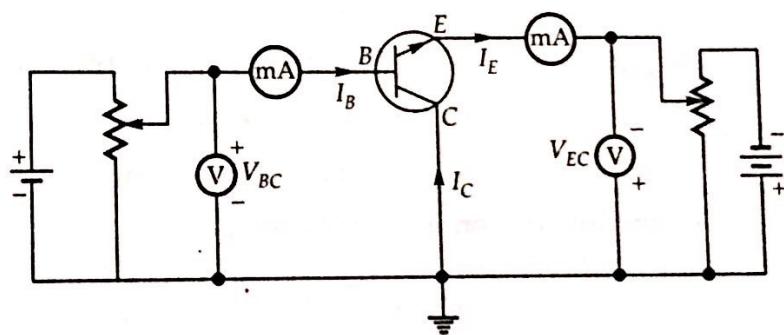


Figure 5.13 Circuit for transistor characteristics in CC arrangement.

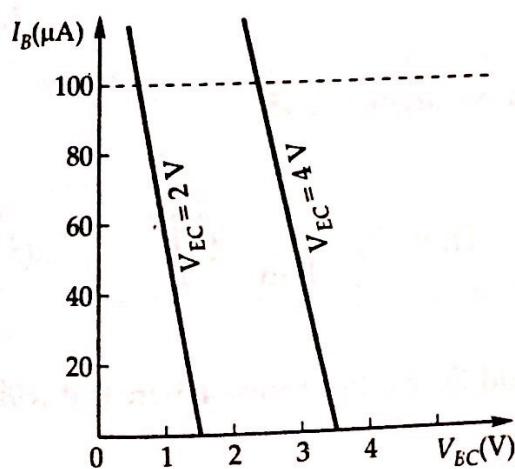


Figure 5.14 Input characteristics of CE arrangement.

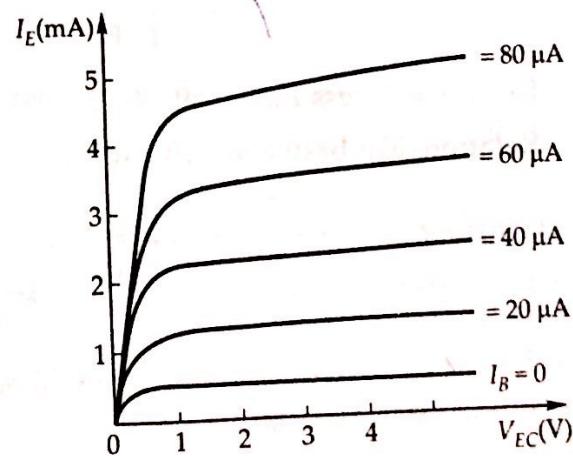


Figure 5.15 Output characteristics of CE arrangement.

Relationship between current amplification factors, i.e.,  $\alpha$ ,  $\beta$  and  $\gamma$  in three configurations, CB, CE and CC respectively can be obtained as follows :

(i)  $\alpha$  is defined as ratio of change in collector current (output) to corresponding change in emitter current by keeping output collector current  $V_{CB}$  as constant. Therefore

$$\alpha = \left( \frac{\partial I_C}{\partial I_E} \right)_{V_{CB}} \quad \dots(5.13)$$

(ii) Similarly, in CE configuration, current gain  $\beta_{dc}$  is defined as

$$\beta = \left( \frac{\partial I_C}{\partial I_B} \right)_{V_{CE}} \quad \dots(5.14)$$

(iii) In CC configuration, current gain  $\gamma_{dc}$  is defined as

$$\gamma = \left( \frac{\partial I_E}{\partial I_B} \right)_{V_{EC}} \quad \dots(5.15)$$

In any transistor arrangement  $I_E = I_C + I_B$  ... (5.16)

and  $I_C = \alpha I_E + I_{CO}$  ... (5.17)

From Eq. (5.16), we can write  $\partial I_E = \partial I_C + \partial I_B$  ... (5.18)

From Eq. (5.17), we can write  $\partial I_C = \alpha \partial I_E + \partial I_{CO}$  ... (5.19)

On putting  $\partial I_C$  from Eq. (5.19) to Eq. (5.18), we get,  $\partial I_E = \alpha (\partial I_E + \partial I_{CO}) + \partial I_B$

Since  $\partial I_{CO}$  is almost negligible. Hence

$$\partial I_E = \alpha \partial I_E + \partial I_B \quad \text{or} \quad \partial I_E (1 - \alpha) = \partial I_B \quad \dots(5.20)$$

By dividing  $\partial I_C$  on both sides, we get

$$\frac{\partial I_E}{\partial I_C} (1 - \alpha) = \frac{\partial I_B}{\partial I_C} \Rightarrow \frac{1}{\alpha} (1 - \alpha) = \frac{1}{\beta} \quad \dots(5.21)$$

Therefore  $\beta = \frac{\alpha}{1 - \alpha}$  ... (5.21)

or

$$\alpha = \frac{\beta}{1 + \beta} \quad \dots(5.22)$$

Usually  $\alpha$  is less than unity (say 0.98). Then  $\beta$  should be larger i.e., 45.

**Relationship between  $\alpha$ ,  $\beta$  and  $\gamma$**

Consider  $\gamma = \frac{\partial I_E}{\partial I_B} = \frac{\partial I_E}{\partial I_E - \partial I_C} = \frac{1}{1 - \frac{\partial I_C}{\partial I_E}} = \frac{1}{1 - \alpha}$  Thus  $\gamma = \frac{1}{1 - \alpha} = 1 + \beta$  ... (5.23)

which shows that current amplification will be large in CE and CC configuration whereas it will be less than unity in CB configuration.

### Comparison of different Configurations

The various characteristics of the CB, CE and CC arrangements are given in Table 5.2.

Table 5.2 The comparison of various characteristics of three connections.

S.No.	Characteristic	CB	CE	CC
1	Input resistance ( $h_i$ )	Low (about $100\Omega$ )	Moderate (about $1\text{k}\Omega$ )	Very high (about $750\text{k}\Omega$ )
2	Output resistance ( $1/h_o$ )	Very high about ( $0.5\text{M}\Omega$ )	High to moderate ( $45\text{k}\Omega$ )	Low (about $50\Omega$ )
3	Voltage gain ( $1/h_v$ )	About 150	About 500	Less than unity
4	Current gain ( $h_f$ )	Less than unity	High	High
5	Phase change between input and output signal voltage	0 or $2\pi$ (No change)	$\pi$ (phase reversal)	0 or $2\pi$ (No change)
6	Applications	Used in high frequency circuits	Used in audio frequency circuits as an amplifier	Used for impedance matching

## 5.7 Transistor as an Amplifier

If we compare different type transistors in Table 5.2, we find that CE arrangement is most suited for signal application. Figure 5.16 shows the CE, NPN amplifier circuit. A dc voltage source ( $V_{BB}$ ) is applied to the input circuit so that emitter-base (E-B) junction operates in the forward bias irrespective of polarity of input ac signal. A dc voltage source ( $V_{CC}$ ) is connected to the output circuit in such a way that collection-base (C-B) junction operates in reverse biased.

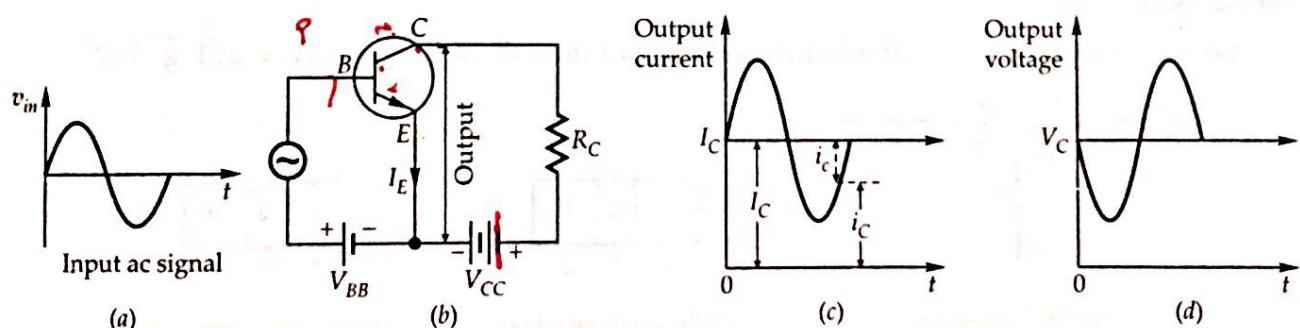


Figure 5.16 CE Amplifier circuit.

When ac input signal is applied in the input, base-emitter voltage ( $V_{BE}$ ) begins to oscillate with the polarity of signal. During positive half-cycle,  $V_{BE}$  is increased which results  $I_B$  increases. This causes an increase in the collector current and larger voltage drop will appear across the load  $R_C$ . As  $V_{CC}$  is constant, therefore, output voltage  $V_{CE}$  ( $V_C$ , as E is grounded) decreases. In other words, as the signal voltage is increasing in the positive half of the cycle, the output is increasing in

the negative sense i.e., output is  $180^\circ$  output of phase with the input. While in negative half of the cycle,  $V_{BE}$  decreases (i.e.,  $I_B$  decreases) causes smaller voltage drop and current through load  $R_C$ . This leads to increase in output voltage  $V_C$ . In conclusion we can say that in CE amplifier, the positive half-cycle of the signal appears as amplified negative half-cycle in the output and vice-versa. Here amplification is not affected by the phase reversal.

In every type of amplifier, the input and output currents are in phase. As shown in Fig. 5.16, collector current consists of two components :

- (i) dc collector current  $I_C$  (absence of input ac signal)
- (ii) ac collector current  $i_c$  (presence of input ac signal)

Thus resultant collector current  $i_C = I_C + i_c$

Table 5.3 provides the standard notations for currents and voltages in transistor operations where ac signals are superimposed over the dc. (Refer to Fig. 5.16)

Table 5.3 Standard notations for currents and voltages in a transistor.

S.No.	Particular	dc	ac Instantaneous	Total
1	Emitter-base voltage	$V_{EB}$	$v_{eb}$	$v_{EB}$
2	Base current	$I_B$	$i_b$	$i_B$
3	Collector-base voltage	$V_{CB}$	$v_{cb}$	$v_{CB}$
4	Collector current	$I_C$	$i_c$	$i_C$

## 5.8 Eber-Moll's Model

Eber-Moll model is called the coupled diode model which describes the dc characteristics of a transistor. This model generalizes the behaviour of a transistor by considering the normal and inverted mode of operations.

Let us consider the PNP transistor, and current flow through it as given in Fig. 5.17.

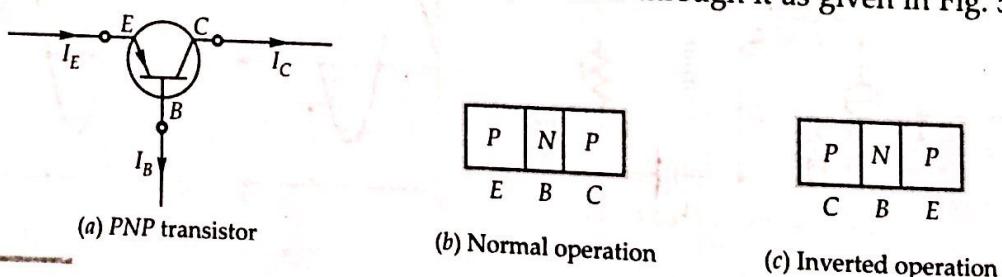


Figure 5.17

During normal operation,  $V_{EB}$  is forward and  $V_{CB}$  is reverse biased.

Therefore,

$$I_{EN} = I_{EO}(e^{V_{EB}/V_T} - 1) \quad (\text{diode current equation}) \quad \dots(5.24)$$

and

$$I_{CN} = \alpha_N I_{EN} = \alpha_N I_{EO}(e^{V_{EB}/V_T} - 1) \quad \dots(5.25)$$

where  $I_{EO}$  and  $\alpha_N$  are reverse saturation currents at emitter junction and current amplification factor in normal operation respectively. Here  $I_{EN}$  and  $I_{CN}$  are emitter and collector current respectively in normal mode.

Under inverted mode,  $V_{EB}$  is reverse and  $V_{CB}$  is forward biased.

Therefore,  $I_{CI} = -I_{CO}(e^{V_{CB}/V_T} - 1)$  (diode current equation) ... (5.26)

and  $I_{EI} = \alpha_I I_{CI} = -\alpha_I I_{CO}(e^{V_{CB}/k_B T} - 1)$  ... (5.27)

where  $I_{CO}$  and  $\alpha_I$  are reverse saturation currents of diode at collector junction and current amplification factor in inverted mode respectively. Here  $I_{EI}$  and  $I_{CI}$  are emitter and collector current respectively in the inverted operation.

Superposition of normal and inverted mode operations provides the generalized emitter current ( $I_E$ ) and collector current ( $I_C$ ), given by :

$$I_E = I_{EN} + I_{EI} = I_{EO}(e^{V_{EB}/V_T} - 1) - \alpha_I I_{CO}(e^{V_{CB}/V_T} - 1) \quad \dots (5.28)$$

and  $I_C = I_{CI} + I_{CN} = -I_{CO}(e^{V_{CB}/V_T} - 1) + \alpha_N I_{EO}(e^{V_{EB}/V_T} - 1) \quad \dots (5.29)$

Equations (5.28) and (5.29) are Eber-Moll equations.  $I_E$  contains two terms, first represents the diode equation at emitter junction and second represents a current controlled by collector diode. Similarly, first term of  $I_C$  indicates the diode equation at collector junction and second term is for a current controlled by emitter diode.

Therefore, equivalent circuit from Eber-Moll equations gives the Eber-Moll model (Fig. 5.18).

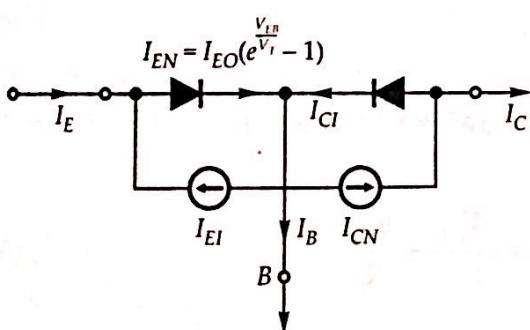


Figure 5.18 Eber-Moll Model of a PNP transistor.

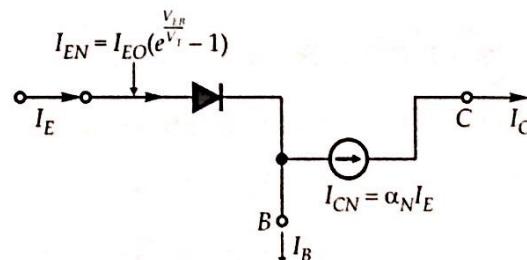


Figure 5.19 Eber-Moll model for normal PNP operation.

For a PNP transistor in normal mode, common base arrangement,  $V_{EB}$  = forward and  $V_{CB}$  = reverse biased. Hence,  $I_{CI} = 0$  (collector-base diode behaves as open) and  $I_{EI} = 0$ . Thus Eber-Moll equivalent circuit is shown in Fig. 5.19.

This circuit acts as bridge between internal physical device parameter and device terminal characteristics.

## 5.9 Bias Stability

### 5.9.1 Need for Biasing

In most of the operations, transistor acts as an amplifier, which amplifies the input alternating signal and produces the amplified output. To get the distortion-free output, transistor must be properly biased and it is obtained by the proper selection of supply voltages and resistances in the circuit. This means forward biasing the base-emitter junction and reverse biasing the collector-base junction. For distortion-free and linear amplification, the transistor should operate in the *active region* (i.e., if  $I_E$  increases,  $I_C$  increases and  $V_{CE}$  decreases proportionally). On the other hand, if transistor is not biased properly, it will work inefficiently and unfaithful distorted signal will be produced in the output. An important factor that determines the amplification characteristic of an amplifier is the region of the output characteristic curve over which the transistor operates. This can be obtained by locating the dc operating point on the output characteristic curve as discussed in the next section.

### 5.9.2 dc Load Line

Let us consider a CE amplifier circuit with base resistor  $R_B$  and collector (load) resistor  $R_C$  as visualised in Fig. 5.20.

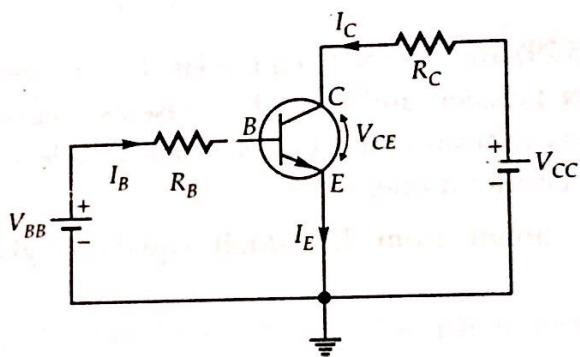


Figure 5.20 CE, NPN transistor amplifier circuit.

In the output circuit, applying Kirchhoff's voltage law (KVL), we get

$$\Rightarrow V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C \quad \text{or} \quad I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C} \quad \dots(5.30)$$

As  $V_{CC}$  and  $R_C$  are fixed values i.e.,  $\frac{V_{CC}}{R_C}$  is a constant, therefore above equation is a straight line like  $y = mx + C$ , where  $m$  = slope of line  $= -\frac{1}{R_C}$  and  $\frac{V_{CC}}{R_C}$  is the intercept of line on the vertical current axis of the output characteristics. Consider the two extreme points on the straight line.

(i) When  $I_C = 0$ ,  $V_{CE} = V_{CC}$ ; cut off point A

(ii) When  $V_{CE} = 0$ ,  $I_C = \frac{V_{CC}}{R_C}$ ; saturation point B

The dc load line is obtained by joining points A and B. The intersection of dc load line and characteristic curve gives the *operating point* (or *quiescent point*) as shown in Fig. 5.21. The dc load line gives the dynamic behaviour of the circuit and Q-point provides the value of  $I_C$  and  $V_{CE}$  of the circuit. When signal is applied to the input, values of  $I_C$  and  $V_{CE}$  vary about the Q-point accordingly. Q-point is also known as *operating point*.

### 5.9.3 ac Load Line

On applying the ac signal to the input, Q-point remains stable while transistor voltage  $V_{CE}$  and collector current  $I_C$  vary about the point. If we draw ac load line, it has steeper (greater slope,  $-\frac{1}{R_{ac}}$ ) slope than the dc load line but two lines will intersect at the *quiescent point* Q. The effective ac load resistance  $R_{ac}$  can be obtained as follows (Refer to Fig. 5.22) :

$$\frac{1}{R_{ac}} = \frac{1}{R_C} + \frac{1}{R_L} = \frac{R_L + R_C}{R_C R_L} \quad (R_L \parallel R_C) \quad \dots(5.31)$$

$$\therefore R_{ac} = \frac{R_C R_L}{R_C + R_L} \quad (\because R_{ac} < R_{dc}) \quad \dots(5.32)$$

$$R_{dc} = R_C \quad \dots(5.33)$$

where  $R_L$  is effective in case of ac signal and ineffective when dc is applied (no signal). This happens due to coupling capacitor  $C_0$ . It becomes short for ac signal and open for dc.

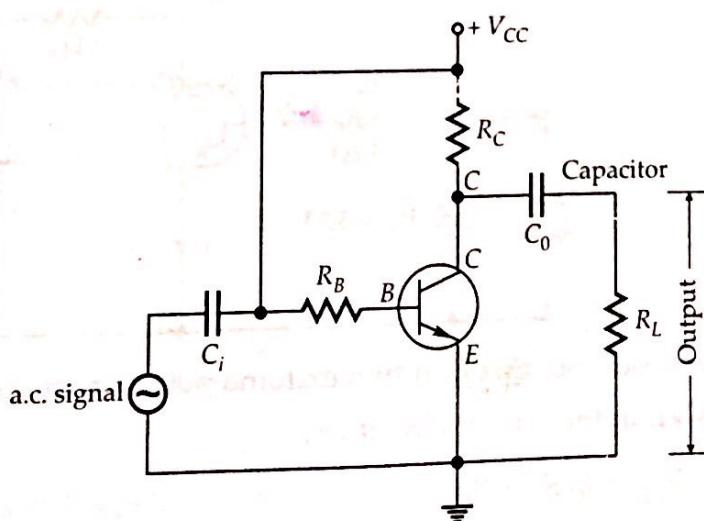


Figure 5.22 CE amplifier circuit

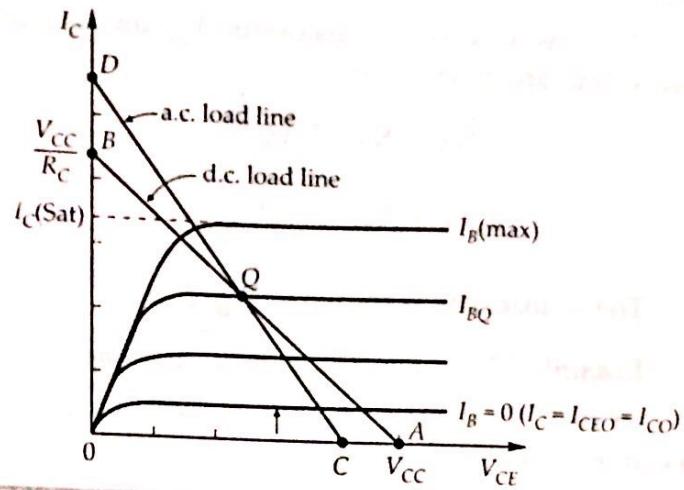


Figure 5.21 Common-emitter output characteristics and load lines.

To draw ac load line, maximum  $V_{CE}$  and maximum  $I_C$  is required in presence of ac signal. These values are given below :

$$V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$$

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

(cut off point C)

... (5.34)

(saturation point D)

... (5.35)

The ac load line is shown in Fig. 5.21.

**Example 5.10** In Fig. 5.23, draw dc load line.

**Solution.** To draw dc load line, we will obtain two extreme points from output circuit.

(i) KVL in the output circuit :

$$V_{CE} = V_{CC} - I_C R_C$$

When  $I_C = 0$ ,

$$V_{CE} = V_{CC} = 12.5 \text{ V} \quad (\text{cut off region})$$

∴ Point A(12.5, 0) on the X-axis.

(ii) When  $V_{CE} = 0 \text{ V}$ ,

$$I_C = \frac{V_{CC}}{R_C} = \frac{12.5}{2.5 \times 10^3} = 5 \text{ mA} \quad (\text{saturation region})$$

∴ Point B(0 V, 5 mA) lies on Y-axis. On joining these two points, dc load line is obtained as shown in Fig. 5.24.

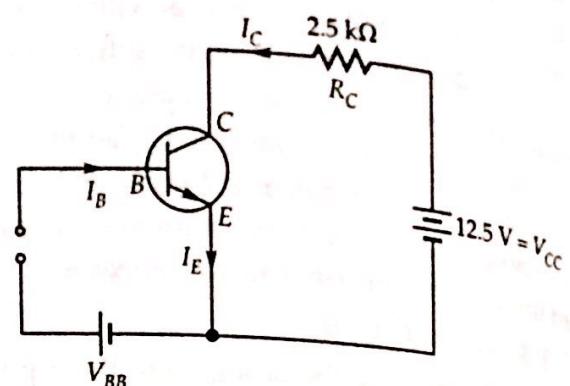


Figure 5.23

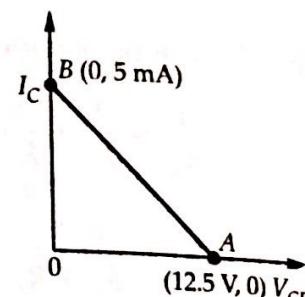


Figure 5.24 dc load line

**Example 5.11** A NPN transistor is used in Fig. 5.25 from the circuit. Find dc load line and Q-point on the output characteristics of CE configuration. (Si material is used).

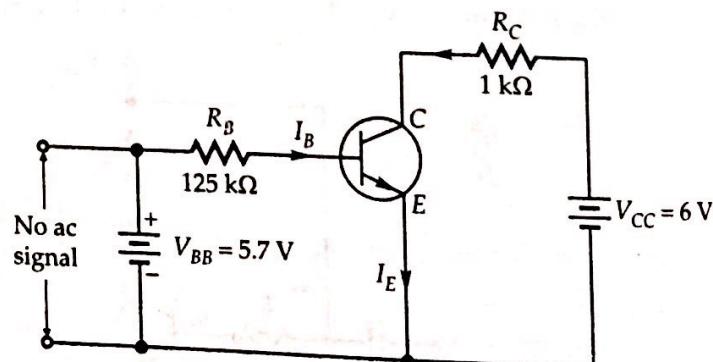


Figure 5.25

**Solution.** To draw dc load line, first find two extreme points from output characteristics.

(i) Point A. Apply KVL in the output circuit i.e.,

$$V_{CC} = I_C R_C + V_{CE}$$

When  $I_C = 0$ ,

$$V_{CE} = V_{CC} = 6 \text{ V}. \text{ Thus } A \text{ will be } (6 \text{ V}, 0 \text{ mA}).$$

$$(ii) \text{ Point } B \text{ When } V_{CE} = 0, I_C = \frac{V_{CC}}{R_C} = \frac{6}{1 \times 10^3} = 6 \text{ mA}$$

Therefore, B will be (0 V, 6 mA).

So the straight line AB joining these two points is the dc load line.

(iii) To find Q-point  $I_B$  is required. Consider input circuit and apply KVL,

$$V_{BB} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5.7 - 0.7}{125 \times 10^3} = 40 \mu\text{A}$$

So Q-point is the point of intersection of the dc load line and output characteristic curve at  $I_B = 40 \mu\text{A}$ .

If  $\beta$  would be given, Q-point,  $I_C$  and  $V_{CE}$  can also be calculated.

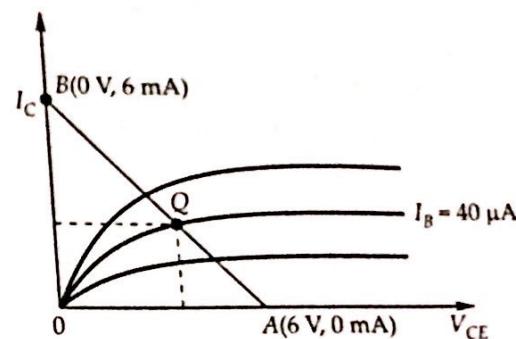


Figure 5.26

**Example 5.12** Draw the dc and ac load lines for the given CE circuit shown in Fig. 5.27. Also determine Q.

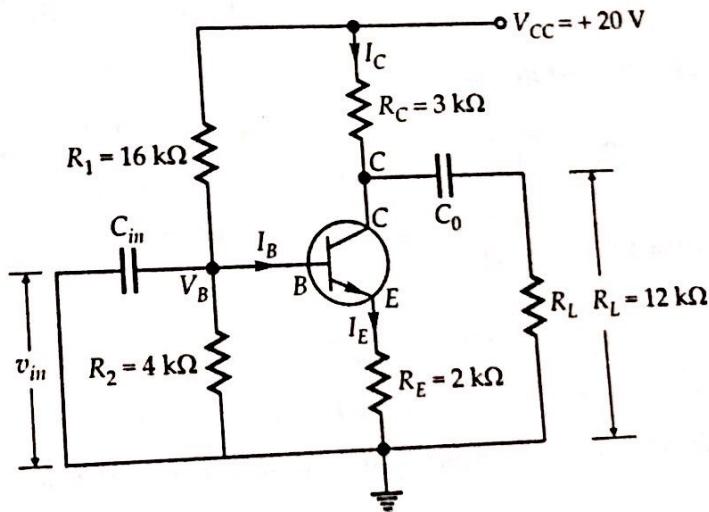


Figure 5.27

**Solution. (a) Calculation of dc load line**

$$(i) \text{ At cut-off, } I_C = 0, V_{CE} = V_{CC} = 20 \text{ V}$$

∴ Point A (20 V, 0 mA)

$$(ii) \text{ At saturation, } V_{CE} = 0$$

$$I_C = \frac{V_{CC}}{R_C + R_E} = \frac{20}{3 \times 10^3 + 2 \times 10^3} = 4 \text{ mA}$$

(because KVL,  $V_{CC} = I_C R_C + V_{CE} + I_E R_E$ )

Point B = (0 V, 4 mA)

The straight line joining A and B is called the dc load line.

## (b) Calculation of Q-point

Under given condition, we will determine collector current and collector to emitter voltage, i.e.,  $I_C(Q)$  and  $V_{CE}(Q)$ . Consider voltage at the base,

$$V_B = \left( \frac{V_{CC}}{R_1 + R_2} \right) R_2 = \frac{20 \times 4 \times 10^3}{(16 + 4) \times 10^3} = 4 \text{ V}$$

Apply KVL in loop containing  $R_2$ , base and  $R_E$ , i.e.,

$$V_B = V_{BE} + I_E R_E$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{4 - 0.7}{2 \times 10^3} = 1.65 \text{ mA}$$

(consider Si transistor,  $V_{BE} = 0.7 \text{ V}$ )

( $\because I_B \approx 0 \text{ mA}$ )

$$\therefore I_C \approx I_E = 1.65 \text{ mA}$$

$$\text{So } I_C(Q) = 1.65 \text{ mA}$$

Again apply KVL to output to obtain  $V_{CE}(Q)$  i.e.,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E = I_C (R_C + R_E) + V_{CE} \quad (\text{Let } I_C \approx I_E)$$

$$V_{CC} = 1.65 \times 10^{-3} (3 + 2) \times 10^3 = 11.75 \text{ V}$$

$$\therefore V_{CE}(Q) = V_{CC} - I_C(Q) (R_C + R_E) = 20 - 1.65 \times 10^{-3} (3 + 2) \times 10^3 = 11.75 \text{ V}$$

## (c) Calculation of ac load line

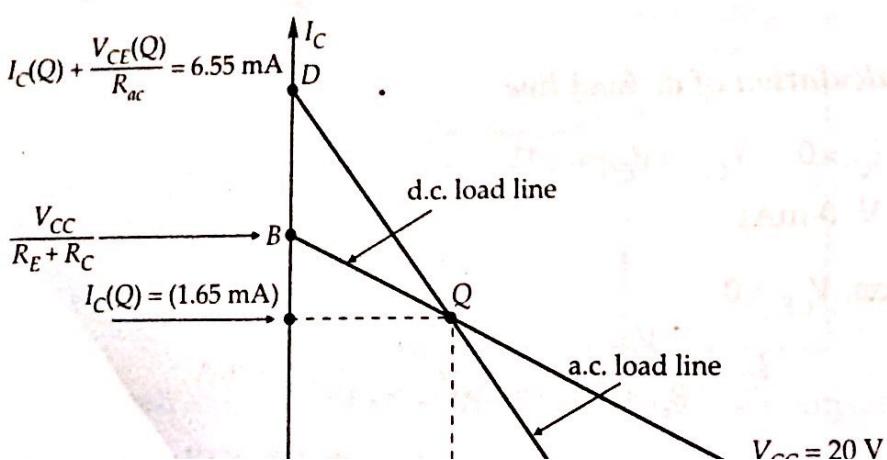
$$\text{Here } R_{ac} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L} = \frac{(3 \times 12) \times 10^6}{(3 + 12) \times 10^3} = 2.4 \text{ k}\Omega$$

$$\therefore I_C(\text{saturation}) = I_C(Q) + \frac{V_{CE}(Q)}{R_{ac}} = 1.65 + \frac{11.75}{2.4} = 6.55 \text{ mA} \quad (\text{Point D})$$

$$\text{and } V_{CE}(\text{cut off}) = V_{CE}(Q) + I_C(Q) R_{ac} = 11.75 + 1.65 \times 2.4 = 15.71 \text{ V} \quad (\text{Point C})$$

Straight line joining points C and D is ac load line.

## (d) Graphical representation of dc, ac load line with Q-point.



### 5.9.4 Thermal Runaway

The collector current (or current gain,  $\beta_{dc}$ ) of a transistor strongly depends on :

- (i) Transistor
- (ii) Temperature

In a circuit, if transistor is replaced by another, then  $I_C$  and  $V_{CE}$  also change. Similarly, current  $I_C$  (or  $\beta_{dc}$ ) varies with the temperature variations. For example, data sheet of a transistor 2N3904 shows that the  $\beta_{dc}$  may vary from 100 to 300 at 25°C temperature. Circuit analysis of transistor indicates that  $\beta_{dc}$  increases with increasing temperature and decreases with decreasing temperature.

However, for faithful amplification of input signal, Q-point must remain fixed, irrespective of these variations. This process is known as *stabilization*.

Thermal runaway is the process in which collector current increases with temperature. As collector current increases, temperature of the junction increases due to power dissipation,  $I^2R$  at the collector junction. This increase in temperature  $\Delta T$  can cause further collector current to increase thereby further increasing temperature. As a result self destruction of the transistor. It can be explained mathematically as follows :

Collector current,  $I_C$  in a CE configuration is given by

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO} \quad \dots(5.36)$$

where  $I_{CEO}$  and  $I_{CBO}$  are leakage currents.

Since leakage current  $I_{CBO}$  is strongly temperature dependent. The collector current  $I_C$  produces heat,  $I^2R$ , within the transistor. This raises the temperature and as a result  $I_{CBO}$  increases. From Eq. (5.36), it is obvious that  $I_C$  will increase. The increased  $I_C$  further increases the temperature, leads to increased  $I_{CBO}$ . This process is cumulative and fast and may cause the transistor to be destroyed or damaged. Therefore, in any transistor circuit, this effect should be avoided.

### 5.9.5 Stability Factor

In a transistor circuit, it is necessary and desirable to keep  $I_C$  and  $V_{CE}$  constant so that Q-point (or operating point) becomes stable. There are two methods to make operating point fixed as follows : (i) Stabilization      (ii) Compensation

In the first case, biasing circuit is used, which allows  $I_B$  to vary such that  $I_C$  remains constant with the variations in  $\beta_{dc}$ ,  $I_{CO}$  and  $V_{BE}$ . In second case, diodes, sensors, thermistor etc. (temperature sensitive devices) are used to compensate the variations in voltages and currents to keep operating point ( $I_{CQ}$ ,  $V_{CEQ}$ ) constant.

Performance of different biasing circuits can be compared by a parameter  $S$ , known as stability factor.  $S$  is defined as the rate of change of collector current with respect to  $I_{CO}$  (collector-base leakage) current, keeping  $\beta_{dc}$  and  $V_{CE}$  constant.

$$S = \left( \frac{\partial I_C}{\partial I_{CO}} \right)_{\beta_{dc} \text{ and } V_{CE}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \quad \dots(5.37)$$

where  $\beta_{dc}$  and  $V_{CE}$  are constant. The large value of  $S$  means circuit is thermally unstable. Therefore  $S$  should be as small as possible.

In CE amplifier, collector current is :

$$I_C = \beta_{dc} I_B + (1 + \beta_{dc}) I_{CO} \quad \dots(5.38)$$

Differentiating with respect to  $I_C$

$$I = \beta_{dc} \frac{\partial I_B}{\partial I_C} + \frac{(1 + \beta_{dc})}{S}$$

$$\therefore S = \frac{1 + \beta_{dc}}{1 - \beta_{dc} \left( \frac{\partial I_B}{\partial I_C} \right)} \quad \dots(5.39)$$

For a circuit in which  $I_B$  and  $I_C$  are independent i.e.,  $\frac{\partial I_B}{\partial I_C} = 0$

$$S = 1 + \beta_{dc} \quad \dots(5.40)$$

If  $\beta_{dc} = 100$  (say) then  $S = 101$ , means variation of  $I_C$  will be 101 times faster than  $I_{CO}$ . Such circuit may operate in the saturation region. Example is fixed bias.

## 5.10 Transistor Biasing

So far, we have discussed the transistor amplifier circuits using two voltage sources, one is connected in the input and other is connected in the output to operate the transistor in the normal mode. To make circuit simpler and economical, only one voltage source can be used. In the following circuits, only one power supply will be used for proper biasing of the transistor :

- Base bias or fixed bias
- Emitter feedback bias
- Collector feedback bias
- Voltage divider bias

### 5.10.1 Fixed Bias or Base Bias

Figure 5.29 shows the CE amplifier using base resistor  $R_B$  (several hundred  $k\Omega$ ), connected between base and positive terminal of supply for NPN transistor. Apply KVL in the input circuit :

$$V_{CC} = I_B R_B + V_{BE}$$

$$\text{or } I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \dots(5.41)$$

$$\text{Now consider stability factor } S = \frac{1 + \beta_{dc}}{1 - \beta_{dc} \left( \frac{\partial I_B}{\partial I_C} \right)}$$

Since expression for  $I_B$  shows that,  $I_B$  is independent of  $I_C$ .

$$\text{Therefore, } \frac{\partial I_B}{\partial I_C} = 0 \text{ and } S = 1 + \beta_{dc} \quad \dots(5.43)$$

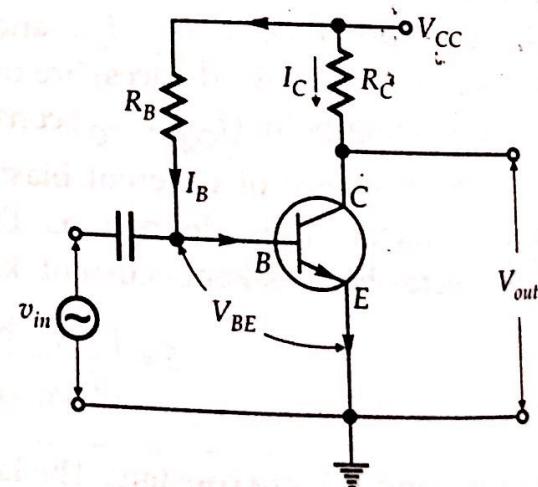


Figure 5.29 Fixed bias circuit

As current gain,  $\beta_{dc}$  is very large,  $S$  is also large. So the fixed bias circuit will be highly thermally unstable. That is why this circuit is seldomly used. The most remarkable feature of this circuit is simplicity.

**Example 5.13** From Fig. 5.30, determine collector current and collector to emitter voltage.

**Solution.** Given :  $V_{CC} = 6 \text{ V}$ ,  $R_B = 300 \text{ k}\Omega$ ,  $R_C = 2 \text{ k}\Omega$   
and  $\beta = 50$

(i) Apply KVL in the base circuit i.e.,

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{6 - 0.7}{300 \times 10^3} = 17.7 \mu\text{A}$$

$$\therefore I_C = \beta I_B = 50 \times 17.7 = 0.88 \text{ mA}$$

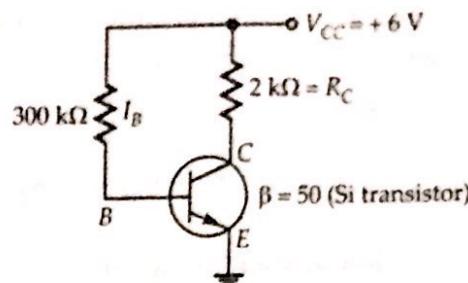


Figure 5.30 Fixed bias circuit

(ii) To get collector to emitter voltage apply KVL in the collector circuit (output)

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore V_{CE} = V_{CC} - I_C R_C = 6 - 0.88 \times 10^{-3} \times 2 \times 10^3 = 4.24 \text{ V.}$$

**Example 5.14** Draw the dc load line and locate the operating point  $Q$ , for fixed bias circuit shown in Fig. 5.31. What will be stability factor ( $V_{BE} = 0.7 \text{ V}$ )?

**Solution.** Given  $V_{CC} = 15 \text{ V}$ ,  $R_B = 820 \text{ k}\Omega$ ,  $R_C = 4.7 \text{ k}\Omega$   
and  $\beta = 120$

(i) d.c. load line

$$(a) I_C (\text{saturation}) = \frac{V_{CC}}{R_C} = \frac{15}{4.7 \times 10^3} = 3.2 \text{ mA}$$

$$(b) V_{CE} (\text{cut off}) = V_{CC} = 15 \text{ V}$$

$\therefore$  For dc load line two extreme points are (15 V, 0 mA)  
and B(0 V, 3.2 mA).

(ii) Operating point ( $Q$ ) i.e.,  $I_C(Q)$  and  $V_{CE}(Q)$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15 - 0.7}{820 \times 10^3} = 17.44 \mu\text{A}$$

$$\text{and } V_{CE}(Q) = V_{CC} - I_C R_C = V_{CC} - (\beta \cdot I_B) R_C \\ = 15 - 120 \times 17.44 \times 4.7 = 5.16 \text{ V}$$

$$\text{Thus } I_C(Q) = \beta I_B = 2.09 \text{ mA}, V_{CE}(Q) = 5.16 \text{ V}$$

(iii) Stability factor  $S = \beta + 1 = 121$ . Given circuit will  
be thermally unstable.

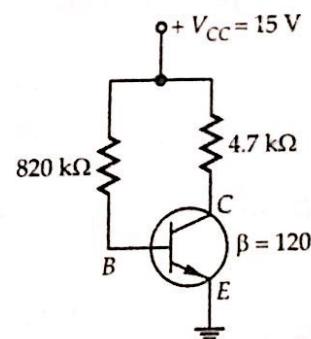


Figure 5.31

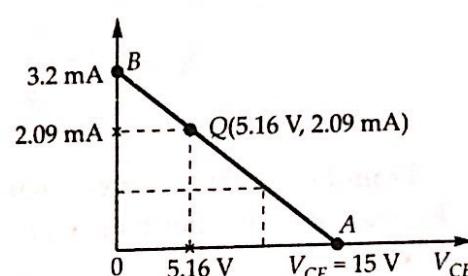


Figure 5.32

### 5.10.2 Emitter Feedback Bias

Figure 5.33 shows the emitter feedback bias circuit. The current in the  $R_E$  (feedback resistor) causes a voltage drop across it which is in the direction to compensate the changes in  $V_{BE}$ . Suppose collector current increases, this will increase the emitter voltage  $V_E$  which in turn decreases the base-to-emitter voltage,  $V_{BE}$  and consequently  $I_B$  decreases. Since  $I_C = \beta_{dc} I_B$ . Therefore, less collector current  $I_C$ . So  $I_C$  remains almost constant.  $R_E$  is common in input and output circuit. The circuit is termed as feedback because output current  $I_C$  produces a change in input current  $I_B$  through  $R_E$ .

$$\text{Here } I_E = I_C + I_B$$

$$\text{and } V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad (\text{KVL}) \quad \dots(5.44)$$

To find stability factor  $S$ ,  $\frac{\partial I_B}{\partial I_C}$  is required.

Differentiate current equation with respect to  $I_C$ ,

$$\frac{\partial I_E}{\partial I_C} = 1 + \frac{\partial I_B}{\partial I_C} \quad \dots(5.45)$$

Also differentiate voltage equation with respect to  $I_C$ ,

$$0 = \frac{\partial I_B}{\partial I_C} R_B + \frac{\partial I_E}{\partial I_C} R_E$$

On putting the value of  $\frac{\partial I_E}{\partial I_C}$ , we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E} \quad \dots(5.46)$$

$$\text{Therefore, } S = \frac{1 + \beta_{dc}}{1 - \beta_{dc} \left( \frac{\partial I_B}{\partial I_C} \right)} = \frac{1 + \beta_{dc}}{1 + \beta_{dc} \left( \frac{R_E}{R_B + R_E} \right)} << (1 + \beta_{dc}) \quad \dots(5.47)$$

In this arrangement, stability factor  $S$  is smaller than that of fixed bias. Hence, thermal stability of operating point will be enhanced. The stability factor ( $S$ ) can be reduced to 1, when ratio  $R_B / R_E$  is very very small compared to 1.

*Condition for  $R_E$  value :* Since  $I_E \approx I_C$

From voltage equation, we can write

$$I_C (\cong I_E) = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{\beta_{dc}}} \quad (\because I_C = \beta_{dc} I_B) \quad \dots(5.48)$$

From Eq. (5.48), it is clear that  $I_C$  depends upon  $\beta_{dc}$ . Therefore, to keep  $I_C$  independent of  $\beta_{dc}$ ,  $R_E$  should be greater than  $R_B / \beta_{dc}$  i.e.,

$$R_E >> \frac{R_B}{\beta_{dc}}$$

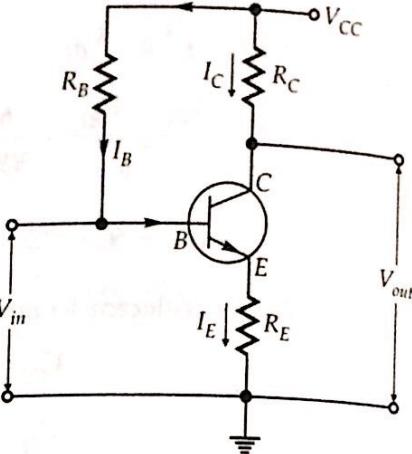


Figure 5.33 Emitter feedback bias circuit.

( $\because I_B \approx 0$ )

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**Example 5.15** For the emitter bias circuit as shown in Fig. 5.34, determine  $I_B$ ,  $I_C$ ,  $V_{CE}$ ,  $V_E$ ,  $V_B$ ,  $V_C$  and stability factor  $S$  ( $V_{BE} = 0.7$  V).

**Solution.** Given:  $V_{CC} = 20$  V,  $R_B = 430$  k $\Omega$ ,  $\beta = 50$  and  $R_E = 1$  k $\Omega$ .

(i)  $I_B$ : Apply KVL in the base (input) circuit,

$$I_B = \frac{V_{CC} - V_{BE} - I_E \cdot R_E}{R_B}$$

$$\text{where } I_E \approx I_C = \beta I_B, I_E = (1 + \beta) I_B$$

$$R_B I_B = V_{CC} - V_{BE} - (1 + \beta) I_B \cdot R_E$$

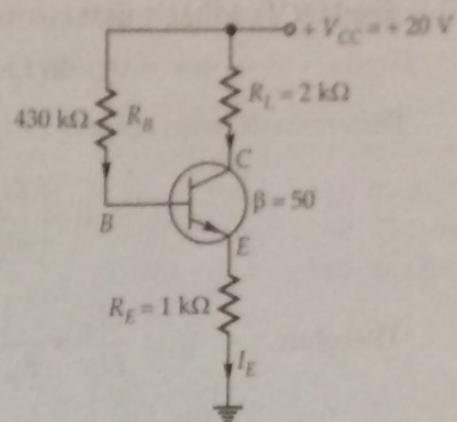


Figure 5.34

$$I_B = \frac{V_{CC} - V_{BE}}{(1 + \beta) R_E + R_B}$$

$$= \frac{20 - 0.7}{(1 + 50) \times 1 \times 10^3 + 430 \times 10^3} = 0.04 \text{ mA}$$

$$(ii) I_C = \beta R_B = 50 \times 0.04 = 2 \text{ mA}$$

(iii)  $V_{CE}$ : Apply KVL in the output circuit

$$V_{CC} = I_C R_C + V_{CE} + I_E \cdot R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (\because I_E \approx I_C)$$

$$= 20 - 2 \times 10^{-3} \times (2 + 1) \times 10^3 = 14 \text{ V}$$

$$(iv) V_E = I_E R_E \cong I_C R_E = 2 \times 10^{-3} \times 1 \times 10^3 = 2 \text{ V}$$

$$(v) V_B = V_{BE} + V_E = 0.7 + 2 = 2.7 \text{ V}$$

$$(vi) \text{Stability factor } S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_E + R_B} \right)} = \frac{1 + 50}{1 + 50 \left( \frac{1}{1 + 430} \right)} = 45.7$$

### 5.10.3 Collector Feedback Bias

A common emitter amplifier, in which base resistor is connected to collector terminal is shown in Fig. 5.35. This circuit is called collector feedback because output collector current  $I_C$  can cause the changes in base current  $I_B$  through feedback resistor  $R_B$ . When temperature increases,  $\beta_{dc}$  increases. This generates more collector current. As soon as collector current increases, collector to emitter voltage  $V_{CE}$  decreases. It means less voltage drop across  $R_B$ , causing less base current and in turn less collector current nullifies the effect of temperature.

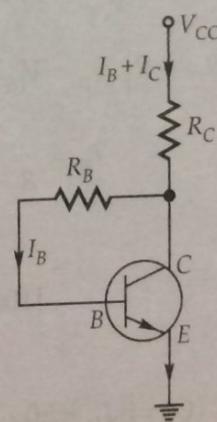


Figure 5.35 Collector feedback bias circuit.

Apply KVL in the input circuit,

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE} \quad \dots(5.49)$$

Differentiate with respect to  $I_C$ ,

$$0 = \left( \frac{\partial I_B}{\partial I_C} + 1 \right) R_C + \left( \frac{\partial I_B}{\partial I_C} \right) R_B$$

Therefore,

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_B + R_C}$$

Stability factor

$$S = \frac{1 + \beta_{dc}}{1 - \beta_{dc} \left( \frac{\partial I_B}{\partial I_C} \right)}$$

If we put the value of  $\frac{\partial I_B}{\partial I_C}$ , then

$$S = \frac{1 + \beta_{dc}}{1 + \frac{\beta_{dc} \cdot R_C}{R_B + R_C}} < 1 + \beta_{dc} \quad \dots(5.50)$$

So this circuit is more stable than fixed bias. Its stability can be improved by proper selection of  $R_B$  (small) and  $R_C$  (large). This circuit is not good for amplification though simpler and requires only two resistors.

**Example 5.16** In a collector feedback bias shown in Fig. 5.36, determine (i) position of Q-point and (ii) stability factor S.

**Solution.** Given :  $V_{CC} = 10 \text{ V}$ ,  $R_B = 100 \text{ k}\Omega$ ,  $R_C = 2 \text{ k}\Omega$ ,  $\beta = 50$  and  $V_{BE} = 0 \text{ V}$

(i) Apply KVL to base emitter circuit,

$$V_{CC} = I'_C R_C + I_B R_B + V_{BE}$$

$$\therefore V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$

$$((1+\beta)R_C + R_B)I_B = V_{CC} - V_{BE}$$

or

$$I_B = \frac{V_{CC}}{R_B + (1+\beta) \cdot R_C}$$

$$= \frac{10}{[100 + (1+50) \times 2] \times 10^3} = 49.5 \mu\text{A}$$

$$(ii) I_C(Q) = \beta I_B = 50 \times 49.5 \mu\text{A} = 2.475 \text{ mA}$$

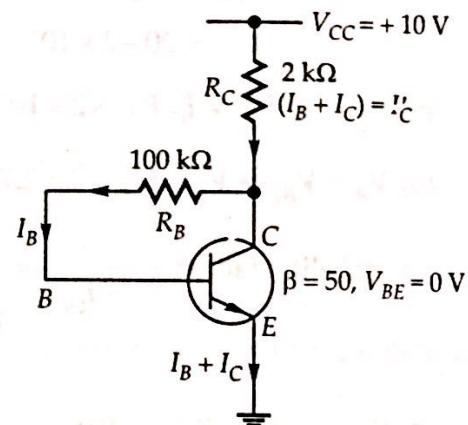


Figure 5.36

(iii)  $V_{CE}(Q)$ .

Apply KVL to collector-emitter circuit,

$$V_{CE} = V_{CC} - (I_C + I_B) \cdot R_C$$

$$= 10 - (2.475 + 0.0495) \times 10^{-3} \times 2 \times 10^3 = 4.95 \text{ V}$$

Therefore Q-point is (4.95 V, 2.475 mA).

$$(iv) \text{ Stability factor } S = \frac{1 + \beta}{1 + \beta \left( \frac{R_C}{R_C + R_B} \right)} = \frac{1 + 50}{1 + 50 \times \left( \frac{2}{2 + 100} \right)} = 25.75.$$

#### 5.10.4 Voltage Divider Bias or Self Bias

The voltage divider bias circuit is shown in Fig. 5.37. This is commonly used for biasing and stabilization of a transistor.  $R_1$  and  $R_2$  form the voltage divider, in which voltage across  $R_2$  provides the forward bias voltage to base-emitter junction. Resistor  $R_E$  is used for stabilization.

Suppose collector current increases due to change in temperature. This increases the current in  $R_E$  which increases the voltage drop across  $R_E$ . In this process,  $V_{BE}$  decreases, leading to decrease in  $I_B$ . Consequently  $I_C$  reduces and tends to its initial value.

From circuit

$$V_2 = \left( \frac{V_{CC}}{R_1 + R_2} \right) R_2 = V_{TH} \quad \dots(5.51)$$

$$\text{and } R_B = \left( \frac{R_1 R_2}{R_1 + R_2} \right) = R_{TH} \quad \dots(5.52)$$

This voltage is also known as Thevenin's voltage  $V_{TH}$  which can be obtained by applying Thevenin's theorem to the input circuit. Consider loop equation (KVL) around base circuit,

$$V_2 = V_{BE} + I_E R_E + I_B R_B$$

$$\text{or } V_2 = V_{BE} + (I_B + I_C) R_E + I_B R_B \quad \dots(5.53)$$

Differentiating with respect to  $I_C$ , we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_E + R_B} \quad \dots(5.54)$$

$$S = \frac{1 + \beta_{dc}}{1 + \beta_{dc} \left( \frac{R_E}{R_E + R_B} \right)}$$

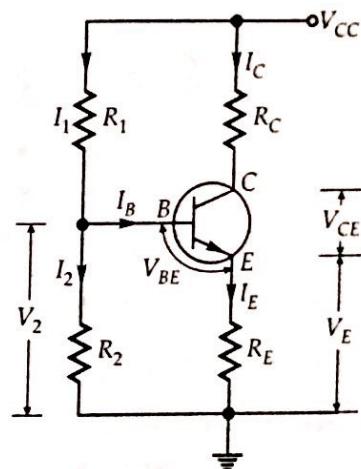
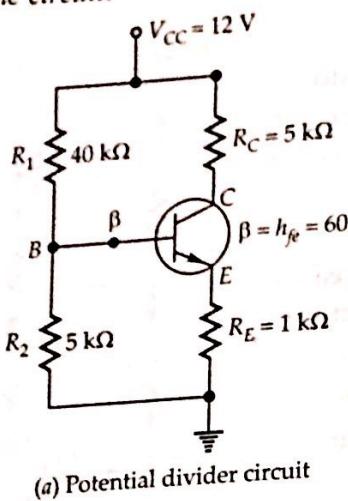


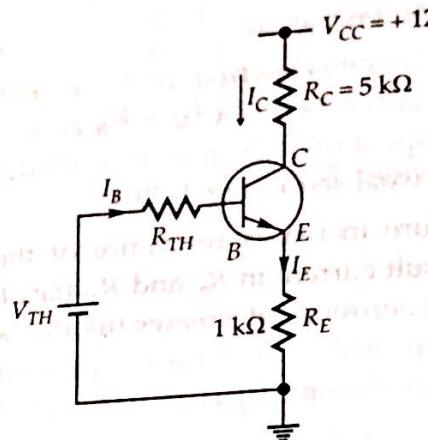
Figure 5.37 Voltage divider or self bias circuit.

Again we can say that  $S = 1$  if  $\frac{R_B}{R_E} \ll 1$ . As  $\frac{R_B}{R_E}$  increases,  $S$  keeps on increasing. When  $\frac{R_B}{R_E} \rightarrow \infty$ ,  $S \rightarrow 1 + \beta_{dc}$ . Here good stability is obtained at the cost of high  $R_E$ , less gain and more power dissipation. Inspite of all that it is most preferred biasing arrangement.

**Example 5.17** For Fig. 5.38, determine the operating point using Thevenin's theorem ( $V_{BE} = 0.3$  V). Also find  $S$  of the circuit.



(a) Potential divider circuit



(b) Thevenin's equivalent circuit

Figure 5.38 Thevenin's equivalent circuit.

**Solution.** Given :  $V_{CC} = 12$  V,  $R_1 = 40$  kΩ,  $R_Z = 5$  kΩ,  $R_C = 5$  kΩ,  $R_E = 1$  kΩ and  $\beta = 60$

Fig. 5.38(b) shows the Thevenin's equivalent circuit of Fig. 5.38(a) where

$$V_{TH} = \left( \frac{V_{CC}}{R_1 + R_2} \right) R_2 = \frac{12 \times 5}{(40+5)} = 1.3 \text{ V} \quad \text{and} \quad R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{40 \times 5}{40+5} = 4.44 \text{ k}\Omega$$

(i)  $I_B$ . Apply KVL to the base-emitter circuit

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E} = \frac{1.3 - 0.3}{4.44 + (1+60) \times 1 \times 10^3} = 15.28 \mu\text{A}$$

$$(ii) I_C (Q) = \beta I_B = 60 \times 15.28 \times 10^{-3} (\text{mA}) = 0.917 \text{ mA.}$$

(iii)  $V_{CE}(Q)$ . Apply KVL to collector-emitter circuit

$$V_{CE}(Q) = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C (R_C + R_E) \quad (\because I_C \approx I_E)$$

$$= 12 - 0.917 \times 10^{-3} (5+1) \times 10^3 = 6.45 \text{ V}$$

Therefore Q-point is (6.45 V, 0.917 mA)

$$(iv) S = \frac{1+\beta}{1+\beta \left( \frac{R_E}{R_E + R_{TH}} \right)} = \frac{1+60}{1+60 \left( \frac{1}{1+4.44} \right)} = 5.07 \quad (\text{Very stable})$$

## 5.11 Bias Compensation

The different biasing arrangements have been studied in section 5.10. Out of them, potential divider bias provides the best stability of transistor operation. In which negative feedback resistor  $R_E$  improves the stability at the cost of reduced gain. This drawback can be further improved by using temperature sensitive devices such as diodes, thermistors or resistors. This is known as bias compensation.

(i) **Thermistor compensation.** In this case, thermistor is used which has negative coefficient of resistance i.e., resistance decreases with temperature. The potential divider bias with a thermistor,  $R_T$  is visualised in Fig. 5.39.

If temperature increases resistance of thermistor,  $R_T$  decreases. As a result current in  $R_T$  and  $R_E$  (i.e.,  $I_E$ ) increases. More voltage drop across  $R_E$  decreases the  $V_{BE}$  which in turn decreases the  $I_B$  and consequently collector current reduces to maintain its original value. Thus any increase in temperature does not affect the collector current and Q-point remains fixed.

(ii) **Sensistor compensation.** Sensistors are resistors with positive coefficient of resistance i.e., their resistance increases with temperature. The sensistor compensation circuit is shown in Fig. 5.40. As temperature increases,  $R_S$  increases, causing increase in the resultant resistance  $\frac{R_1 R_S}{R_1 + R_S}$ . This decreases the voltage drop across  $R_2$ . So bias voltage at the base decreases and  $I_C$  decreases. Therefore increased  $I_C$  due to temperature is being compensated by sensistor.

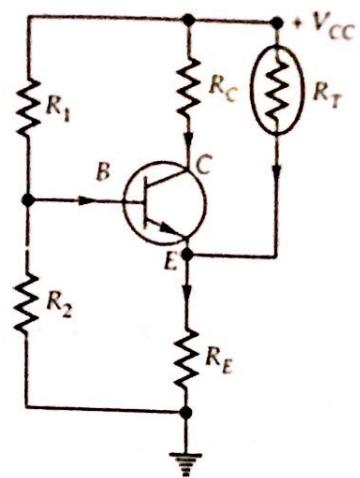


Figure 5.39 Thermistor compensation.

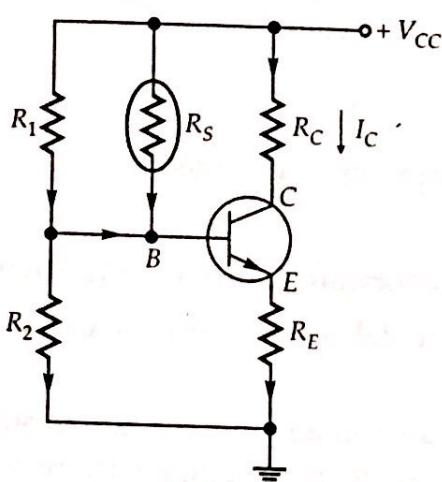


Figure 5.40 Sensistor compensation.

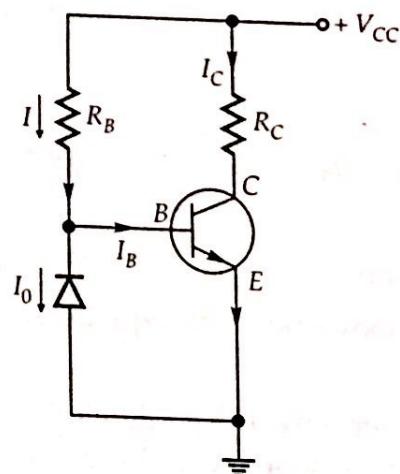


Figure 5.41 Diode compensation.

(iii) **Diode compensation.** Variations in leakage current  $I_{CO}$  with temperature can be compensated by a diode. When temperature increases, reverse saturation current of diode ( $I_0$ ) and transistor ( $I_{CO}$ ) increases at the same rate as shown in Fig. 5.41. Thus  $I$  and  $I_B$  increase at the same rate.

whereas input voltage and output current as dependent variables, given as follows :

$$v_i = f_1(i_i, v_0) \quad \text{and} \quad i_0 = f_2(i_i, v_0)$$

The positive directions of currents and voltages are shown in two-port network as shown in Fig. 5.42.

The network equations are :

$$v_i = h_i i_i + h_r v_0$$

$$i_0 = h_f i_i + h_0 v_0$$

where  $h_i$ ,  $h_r$ ,  $h_f$  and  $h_0$  are input impedance, reverse voltage gain, forward current gain and output admittance respectively. These **hybrid or h-parameters** can be defined as :

$$(i) h_i = h_{11} = \left( \frac{v_i}{i_i} \right)_{v_0=0} \quad (\text{ohms}) ; \text{output short circuited}$$

$$(ii) h_r = h_{12} = \left( \frac{v_i}{v_0} \right)_{i_i=0} \quad (\text{unitless}) ; \text{input open circuited}$$

$$(iii) h_f = h_{21} = \left( \frac{i_0}{i_i} \right)_{v_0=0} \quad (\text{unitless}) ; \text{output short circuited}$$

$$(iv) h_0 = h_{22} = \left( \frac{i_0}{v_0} \right)_{i_i=0} \quad (\text{Siemens or mhos}) ; \text{input open circuited}$$

where subscripts  $i = 11 = \text{input}$ ,  $0 = 22 = \text{output}$ ,  $f = 21 = \text{forward transfer}$ ,  $r = 12 = \text{reverse transfer}$ .

Using above network equations, equivalent model for a transistor can be drawn as in Fig. 5.43.

This general hybrid-parameter equivalent circuit contains input and output. In input, an impedance  $h_i$  is in series with the voltage source  $h_r v_0$  while in output, a current source  $h_f i_i$  is in parallel with an admittance  $h_0$ .

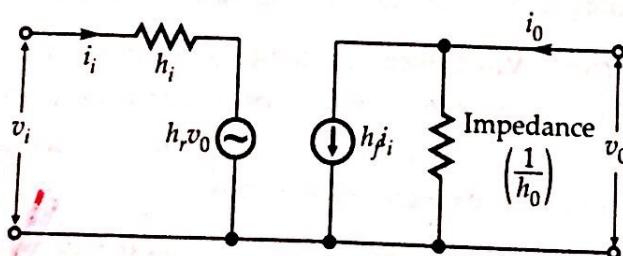


Figure 5.43 Equivalent circuit for a transistor in hybrid-parameter representation..

### 5.12.1 Analysis of a Transistor Amplifier Circuit using Hybrid $h$ -parameters

A transistor amplifier consists of a transistor, load resistor, bias supply and input alternating signal. Its two-port network is shown in Fig. 5.44.

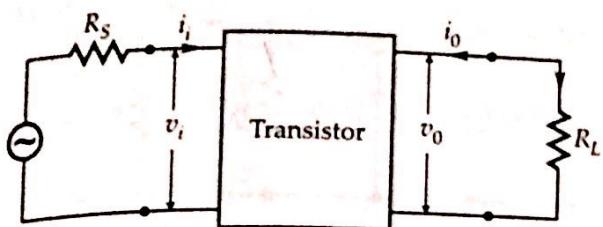


Figure 5.44 Basic amplifier circuit

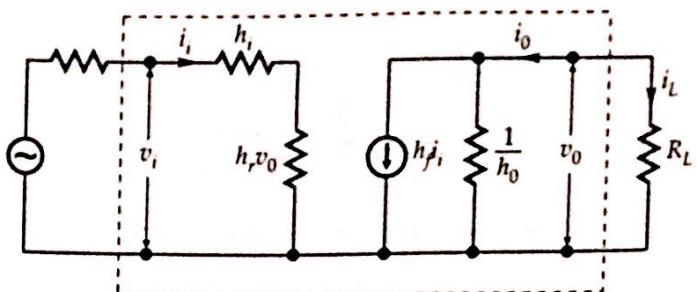


Figure 5.45 Hybrid model of amplifier circuit.

Its equivalent hybrid model is shown in Fig. 5.45.

where  $v_i = h_i i_i + h_r v_0$ ;  $i_0 = h_f i_i + h_0 v_0$  (Network equations)

$$(i) \text{ Current gain } (A_i) \quad A_i = \frac{i_L}{i_i} = \frac{-i_0}{i_i}$$

From second network equation

$$i_0 = h_f i_i + h_0 i_0 R_L \quad (\because v_0 = -i_0 R_L)$$

$$\therefore \frac{i_0}{i_i} = \frac{h_f}{1 + h_0 \cdot R_L}$$

$$\text{Therefore } A_i = -\frac{h_f}{1 + h_0 R_L} \quad \dots(5.55)$$

(ii) Input impedance ( $Z_i$ )

$$Z_i = \frac{v_i}{i_i} = \frac{h_i i_i + h_r v_0}{i_i} = h_i + h_r \frac{v_0}{i_i}$$

$$Z_i = h_i - h_r \frac{i_0 R_L}{i_i} \quad (\because v_0 = -i_0 R_L) \quad \dots(5.56)$$

$$Z_i = h_i + h_r A_i R_L \quad \left( \because A_i = -\frac{i_0}{i_i} \right) \quad \dots(5.56)$$

(iii) Voltage Gain ( $A_v$ )

$$A_v = \frac{v_0}{v_i} = \frac{-i_0 R_L}{v_i} \quad (\because v_0 = -i_0 R_L)$$

$$A_v = \frac{A_i i_i R_L}{v_i} \quad \left( \because A_i = -\frac{i_0}{i_i} \right) \quad \dots(5.57)$$

$$A_v = \frac{A_i R_L}{Z_i} \quad \left( \because Z_i = \frac{v_i}{i_i} \right) \quad \dots(5.57)$$

### 5.12.2 *h*-parameters Analysis of a Common-emitter Amplifier

Let us consider a CE amplifier circuit as shown in Fig. 5.46.

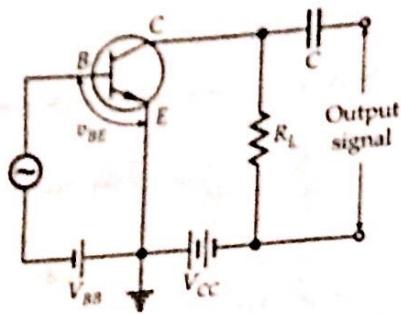


Figure 5.46 CE, PNP transistor amplifier.

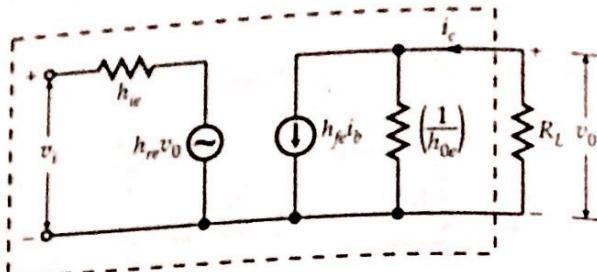


Figure 5.47 Equivalent model for CE amplifier.

The *h*-model for CE configuration is shown in Fig. 5.47, where dc bias sources have been omitted because *h*-model is drawn for alternating part only. Capacitor *C* is also neglected from the circuit because impedance is assumed to be zero over the given range of frequencies where amplifier operates.  $h_{re}$  is also neglected because most of the transistors give very small value ( $\sim 10^{-5}$ ). Finally  $h_{oe}$  is neglected as it is of the order of  $10^{-5}$  mho. Hence it has very large value of  $\frac{1}{h_{oe}}$  ( $\approx 100 \text{ k}\Omega$ ). Typically, load has value of  $5 \text{ k}\Omega$ . Therefore,  $\frac{1}{h_{oe}}$  can be treated as open circuit.

After considering the above assumptions, simplified equivalent circuit is shown in Fig. 5.48.

$$\text{From circuit } v_i = h_{ie} \cdot i_b$$

and

$$i_c = h_{fe} i_b$$

or

$$h_{fe} = \frac{i_c}{i_b}$$

Thus (i) current gain

$$A_{ie} = h_{fe} = \frac{i_c}{i_b} \quad \dots(5.58)$$

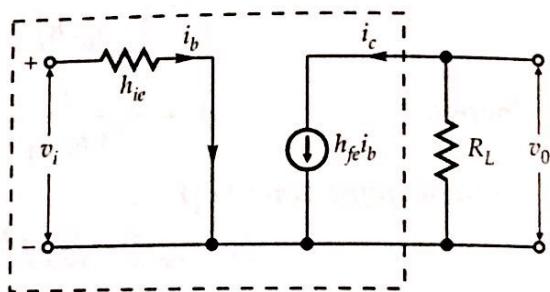


Figure 5.48 Simplified equivalent circuit for CE amplifier.

$$(ii) \text{ Voltage gain } A_{ve} = \frac{v_0}{v_{in}}$$

or

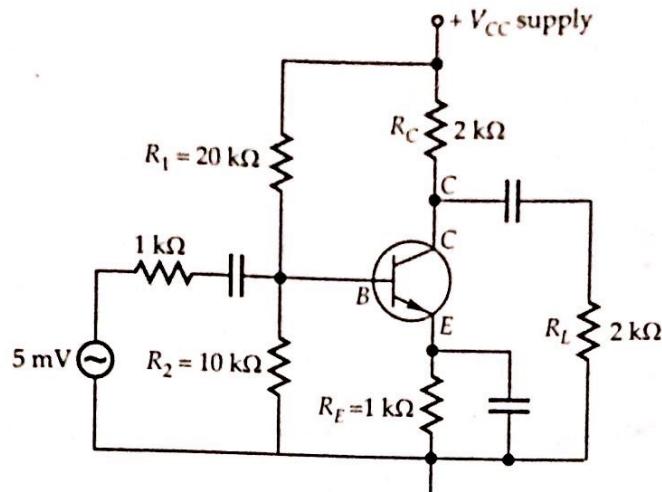
$$A_{ve} = \frac{-i_c R_L}{h_{ie} i_b} = \frac{-h_{fe} i_b R_L}{h_{ie} i_b} = \frac{-h_{fe}}{h_{ie}} R_L \quad \dots(5.59)$$

$$(iii) \text{ Power gain } A_{pe} = |\text{Current gain}| \times |\text{Voltage gain}|$$

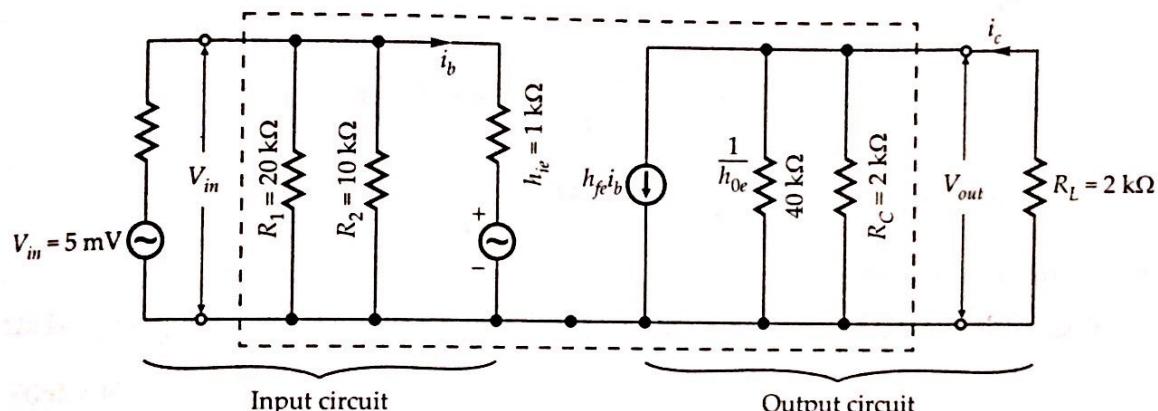
$$= \frac{h_{fe}^2}{h_{ie}} R_L \quad \dots(5.60)$$

In common-emitter amplifier, usually  $h_{fe}$  is large and  $h_{ie}$  is moderate. Therefore, current gain-voltage gain and power gain, all should be high.

**Example 5.18** Given  $h_{ie} = 1\text{k}\Omega$ ,  $h_{oe} = 2.5 \times 10^{-5}$ ,  $h_{fe} = 100$ , draw the h-parameter equivalent circuit of the amplifier shown in Fig. 5.49. Calculate the input impedance, output impedance, current gain and voltage gain.



(a) CE amplifier



(b) Hybrid equivalent circuit of CE amplifier

Figure 5.49

**Solution.** Given :  $h_{ie} = 1\text{k}\Omega$ ,  $h_{oe} = 2.5 \times 10^{-5}$ ,  $h_{fe} = 100$ ,  $R_1 = 20\text{k}\Omega$ ,  $R_2 = 10\text{k}\Omega$ ,  $R_E = 1\text{k}\Omega$ ,  $R_C = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$

(i) Input impedance ( $Z_i$ )

$$(Z_i) = h_{ie} || R_1 || R_2 = 1 || 20 || 10 = 0.87\text{k}\Omega$$

(ii) Output impedance ( $Z_0$ ),

$$Z_0 = \frac{1}{h_{oe}} || R_C = 40\text{k}\Omega || 2\text{k}\Omega = 1.9\text{k}\Omega$$

(iii) Current gain ( $A_i$ )

$$A_i = -\frac{h_{fe} R_B R_C}{(R_C + R_L)(R_B + Z_{in})} = \frac{-100 \times 6.667 \times 2}{(2+2) \times (6.667+1)} = -43.5$$

$$\left(\text{where } R_B = \frac{R_1 R_2}{R_1 + R_2} = 6.67\text{k}\Omega\right)$$

$$(iv) \text{ Voltage gain } (A_v) = \frac{-h_{fe}}{h_{ie}} \times R_{ac} = \frac{100}{1} \times 1.0 = -100.$$

(where  $R_{ac} = \frac{R_C \cdot R_L}{R_C + R_L}$ )

**Example 5.19** A CE amplifier is drawn by a voltage source of internal resistance  $R_S = 800\Omega$ , and the load impedance is a resistance  $R_L = 1k\Omega$ . The h parameters are  $h_{ie} = 1k\Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 50$ ,  $h_{oe} = 25 \mu A/V$ . Calculate current gain  $A_i$ , input resistance  $Z_{in}$ , output resistance  $Z_0$  and voltage gain  $A_v$  using exact and approximate analysis.

**Solution.** (a) Exact analysis :

$$(i) \text{ Current gain } (A_i) = \frac{-h_{fe}}{1 + h_{oe} R_L} = \frac{-50}{1 + 25 \times 10^{-6} \times 10^3} = -48.78$$

$$(ii) \text{ Input resistance } (Z_{in}) = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \frac{1}{R_L}} = 1000 - \frac{50 \times 2 \times 10^{-4}}{25 \times 10^{-7} + \frac{1}{1000}} = 990.24 \Omega$$

$$(iii) \text{ Voltage gain } (A_v) = A_i \frac{R_L}{R_i} = (-48.78) \times \frac{1000}{990.24} = -49.26$$

$$(iv) \text{ Output admittance } (Y_0) = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_S} = 1.94 \times 10^{-5} \text{ mho}$$

$$\text{Output resistance } (R_0) = \frac{1}{Y_0} = 51.42 \text{ k}\Omega$$

(b) Approximate analysis

$$(i) \text{ Current gain } (A_i) = -h_{fe} = -50$$

$$(ii) \text{ Input resistance } (R_{in}) = Z_{in} = h_{ie} = 1k\Omega$$

$$(iii) \text{ Output resistance } R_0 = \infty$$

$$(iv) \text{ Voltage gain } A_v = \frac{-h_{fe} R_L}{h_{ie}} = \frac{-50 \times 1000}{1000} = -50$$

Therefore to save the effort, we can analyze the circuit using approximate analysis method.

### 5.12.3 Hybrid Model for Common-Base Amplifier

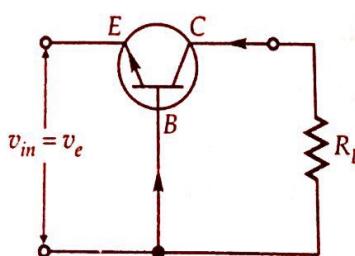


Figure 5.50 Common base amplifier.

Network equations are :

$$v_e = h_{ib} i_e + h_{rb} v_c$$

$$i_c = h_{fb} i_e + h_{ob} v_c$$

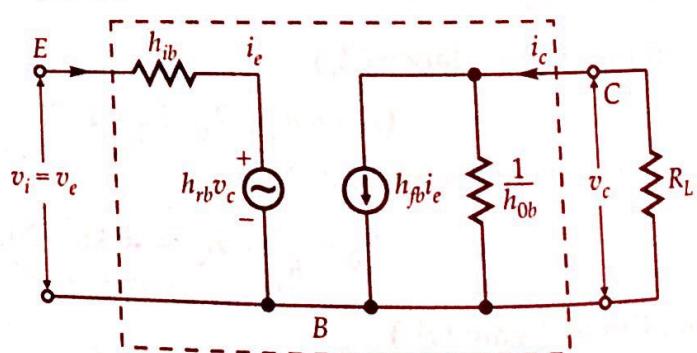


Figure 5.51 Hybrid equivalent circuit.

For most of the transistors,  $h_{rb} \approx 10^{-4}$  (very small) and  $\frac{1}{h_{ob}} \approx 100 \text{ k}\Omega$ , hence  $h_{rb} v_e$  (voltage generator) and shunt impedance  $\frac{1}{h_{ob}}$  can be omitted. Thus simplified circuit is shown in Fig. 5.52. Network equations become :

$$\left. \begin{array}{l} v_e = h_{ib} i_e \\ i_c = h_{fb} i_e \end{array} \right\}$$

(i) Current gain ( $A_i$ )

$$A_i = \frac{i_c}{i_e}$$

$$A_i = h_{fb} \quad \dots(5.61)$$

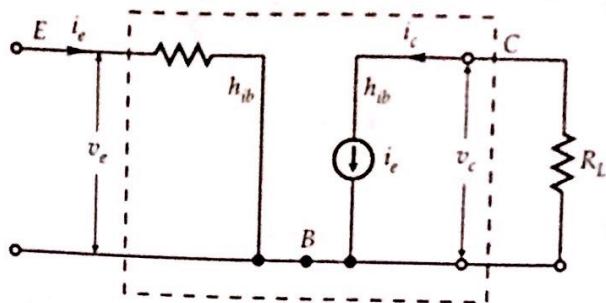


Figure 5.52 Simplified h-model.

(ii) Voltage gain ( $A_v$ )

$$A_v = \frac{v_c}{v_e} = \frac{-i_c R_L}{v_e}$$

$$(\because v_c = v_0 = -i_c R_L)$$

$$A_v = \frac{-i_e h_{fb} R_L}{h_{ib} i_e}$$

(From network equations)

$$A_v = \frac{-h_{fb}}{h_{ib}} R_L$$

...(5.62)

where  $\frac{h_{fb}}{h_{ib}} = \frac{i_c / i_e}{v_e / i_e} = \frac{i_c}{v_e} = \frac{i_c}{-v_b} = g_m$   $(\because v_e = v_e b = -v_{be} = -v_b)$

$g_m$  = transconductance, which is independent of transistor configuration.

(iii) Power gain ( $A_p$ ).

$$A_p = |A_i| |A_v| = \frac{h_{fb}^2 R_L}{h_{ib}}$$

In common base arrangement  $A_i \leq 1$ . Hence,

$$\text{Power gain } A_p \approx |A_v| = \frac{h_{fb}}{h_{ib}} R_L$$

$$A_p = g_m R_L \quad \dots(5.63)$$

#### 5.12.4 Hybrid Model for Common Collector Amplifier

Common collector amplifier circuit and its hybrid equivalent circuit are shown in Figs. 5.53 and 5.54 respectively. Here biasing has been ignored because in hybrid model it has no meaning.

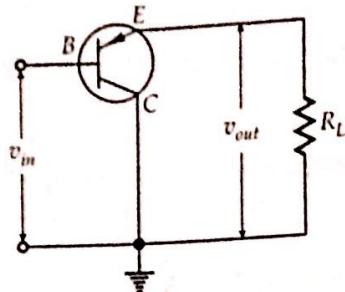


Figure 5.53 Common collector amplifier.

Basically CE and CC amplifier circuits are same except the position of load. In CE amplifier, load is connected at the collector while in CC, it is connected to the emitter. To get better understanding of hybrid model in this configuration, Fig. 5.53 can be redrawn as shown in Fig. 5.55.

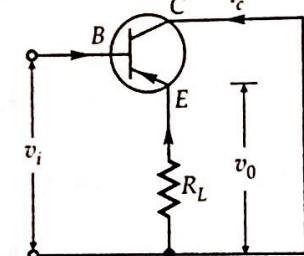


Figure 5.55 Redrawn common collector circuit.

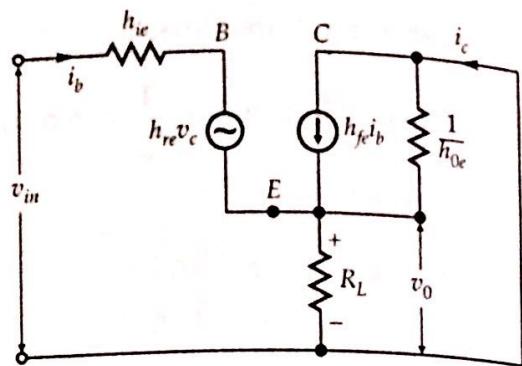


Figure 5.54 Hybrid equivalent circuit.

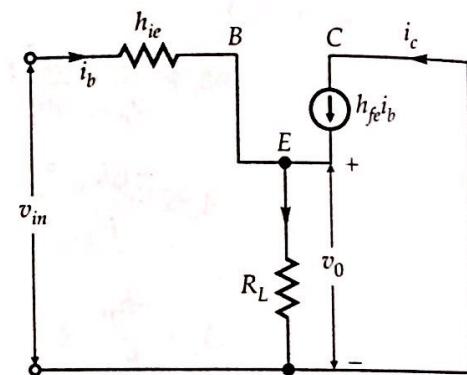


Figure 5.56 Simplified h-model.

Hybrid equivalent circuit as shown in Fig. 5.54, can be simplified by ignoring  $h_{re}v_c$  and  $\frac{1}{h_{oe}}$ .

Reasons are same as mentioned in the previous models. Thus, simplified circuit can be shown in Fig. 5.56.

$$\text{From circuit, } i_e = -(i_c + i_b) = -(1 + h_{fe})i_b \quad \dots(5.64)$$

$$v_i = h_{ie}i_b + (-i_e)R_L \quad (\because i_c = h_{fe}i_b) \quad \dots(5.65)$$

$$v_0 = -i_e R_L \quad \dots(5.66)$$

(i) Current gain ( $A_{ic}$ )

$$A_{ic} = \frac{i_e}{i_b} = -(1 + h_{fe}) \approx -h_{fe} \quad \dots(5.67)$$

(ii) Voltage gain ( $A_{vc}$ )

$$A_{vc} = \frac{v_0}{v_i} = \frac{-i_e R_L}{h_{ie}i_b - i_e R_L} = \frac{R_L}{h_{ie} \left( \frac{i_b}{-i_e} \right) + R_L} \quad \dots(5.68)$$

$$= \frac{R_L}{\left( \frac{h_{ie}}{1+h_{fe}} \right) + R_L}$$

 (from current gain,  $A_{ic}$ )

$$\therefore A_{vc} \approx \frac{R_L}{R_L + \left( \frac{h_{ie}}{h_{fe}} \right)}$$

... (5.69)

Since  $\frac{h_{fe}}{h_{ie}} = g_m$  = transconductance

(true for any transistor configurations)

$$\therefore A_{vc} = \frac{g_m R_L}{g_m R_L + 1} \leq 1$$

... (5.70)

 (iii) Power gain ( $A_{pc}$ ).

$$A_{pc} = |A_{vc}| \cdot |A_{ic}| = \frac{h_{fe} g_m R_L}{g_m R_L + 1}$$

... (5.71)

Here current gain is large, voltage gain is less than unity and power gain is also smaller than that of CE amplifier. Therefore it is good for current gain only. Main advantage of CC amplifier is that it has very high input impedance. So, it is used as impedance matching device between a source and low impedance load.

### 5.12.5 Comparison of CB, CE and CC Transistor Amplifiers

Brief comparison among CB, CE and CC transistor amplifier is given in Table 5.4.

Table 5.4 Comparison of various parameters of the three transistor amplifiers.

S.No.	Parameters	CB	CE	CC
1	Current gain	$\leq 1$	High	High
2	Voltage gain	High	High	$\leq 1$
3	Power gain	Moderate	Very high	Low
4	Input impedance	Low	Moderate	High
5	Output impedance	Very low	High	Low

## 5.13 Field Effect Transistor (FET)

A field effect transistor is a unipolar device in which current conduction is only by one polarity carrier (i.e., majority carrier) and conduction takes place in a channel of a semiconductor. Flow of current is controlled by electric field. FET can be categorized into two types i.e., (i) Junction field effect transistor

The FET has many advantages over BJT, as given below :

- (i) In BJT output current is controlled by input current. So named as current controlled device, while FET is voltage controlled device.
- (ii) The input to BJT amplifier involves a forward biased PN-junction with low resistance, while input to FET involves a reverse biased PN-junction with very high resistance ( $\approx 100 \text{ M}\Omega$ ).
- (iii) Thermally stable than BJT.
- (iv) Less noise than BJT.
- (v) FET can tolerate much level of radiation as it does not depend on minority carriers.

The main drawback of FET is relatively small gain bandwidth product.

### 5.13.1 Junction-Field Effect Transistor (JFET)

It can be of two kinds :

- (i) N-channel. It is made of N-type semiconductor.
- (ii) P-channel. It is made of P-type semiconductor.

Let us consider a N-channel semiconductor and its electrical equivalent circuit when connected by a voltage source as shown in Fig. 5.57.

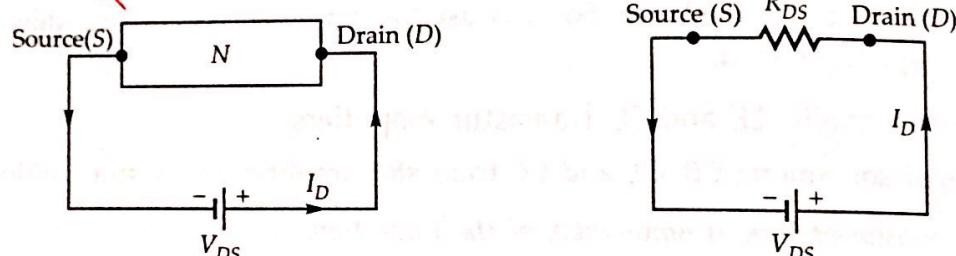


Figure 5.57 N-type semiconductor with its electrical equivalent circuit.

Here current flows from drain (D) to source (S) and majority carrier electrons will flow from S to D. Therefore, the terminal through which majority carriers (electrons in this case) enter the channel is called *source*, termed as S and terminal through which majority carrier leaves the channel is called *drain*, termed as D. If external voltage  $V_{DS}$  is increased, drain current,  $I_D$  will increase proportionally. To control this current  $I_D$  heavily doped P-type semiconductors are formed on both sides of N-type material. These impure regions are called *gates* G, usually connected together by the same potential. The gate is given a negative potential with respect to the source so that PN-junctions are reverse biased. The word *gate* is used because the voltage applied between gate and source,  $V_{GS}$  controls the channel width and hence the drain current  $I_D$ . The N-channel JFET structure is shown in Fig. 5.58.

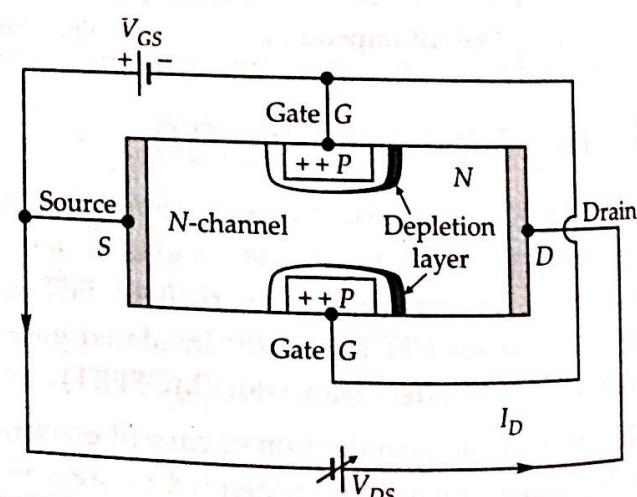


Figure 5.58 The structure of N-channel JFET.

The main operation of JFET depends on the formation of depletion layer at the reverse biased *PN*-junction *i.e.*, between *P*-type gate and *N*-type channel. The width of depletion region increases with the reverse biased. The potential at any point along the channel depends on the distance of that point from the drain. So the points nearer to the drain have higher potential than the points nearer to the source. Hence near to the drain, width of depletion layer will be larger and width of depletion layer decreases as we move towards the source. The flow of electrons from (non-conducting) regions. Therefore depletion width offers the resistance between drain and source. In extreme case channel may tend towards the closer. This situation is known as *pinch-off*. Practically complete pinch-off is impossible.

### 5.13.2 JFET Characteristics

An *N*-channel JFET with a reverse gate source,  $V_{GS}$  is shown in Fig. 5.59.

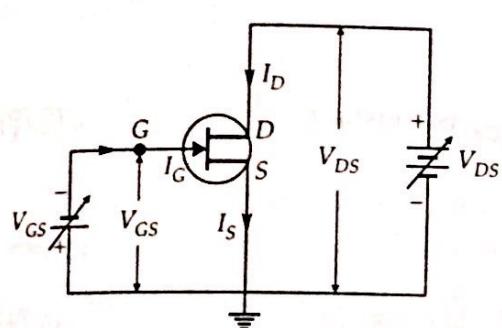


Figure 5.59 Conventional symbols used in JFET.

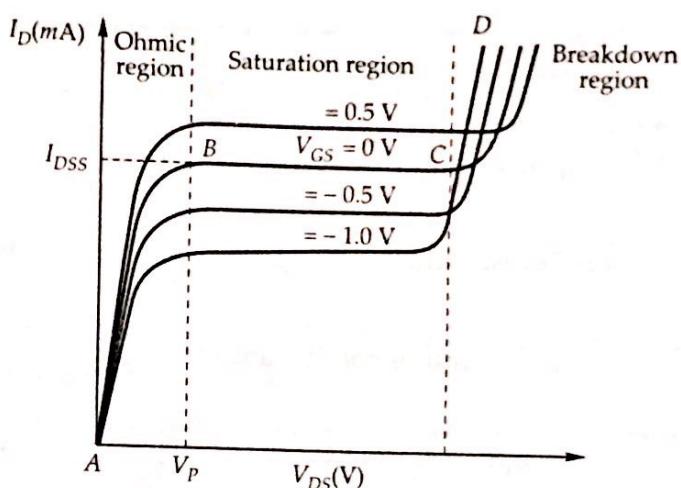


Figure 5.60 Drain characteristics of an *N*-channel JFET.

Drain characteristics of JFET ( $I_D$  vs.  $V_{DS}$ ) are plotted for different values of  $V_{GS}$  as shown in Fig. 5.60.

- Suppose  $V_{GS} = 0$  and  $V_{DS} = 0$ ,  $I_D$  becomes zero. In this case channel will remain open and behaves like simple semiconductor material because of no depletion region in the channel. As  $V_{DS}$  increases,  $I_D$  increases linearly (region AB). This region, AB is ohmic region with resistance,  $\frac{V_{DS}}{I_D}$ . It is useful in voltage variable resistor (VVR) or voltage dependent resistor (VDR).
- When  $V_{DS}$  reaches point  $V_P$ ,  $I_D$  becomes maximum and beyond that saturation or pinchoff region occurs where  $I_D$  becomes almost independent of  $V_{DS}$ . The reason for this is as follows : As  $V_{DS}$  increases, the effective cross-sectional area of the channel decreases, resulting in increase in the channel resistance. As a result,  $I_D$  maintains a constant value. This is shown by the region BC in Fig. 5.60.

occurs producing large  $I_D$ . This region is represented by CD, vertical current, known as *breakdown region*.

- (iv) Drain characteristic curve also shows that for any fixed value of  $V_{DS}$ ,  $I_D$  decreases with decrease of  $V_{GS}$  because channel width decreases as  $V_{GS}$  is made more negative. Hence less flow of carriers, produces less current.

### 5.13.3 JFET Parameters

Characteristic curve of JFET shows that  $I_D$  depends on  $V_{DS}$  and  $V_{GS}$ . So we can define some parameters relating to these variables as follows :

$$(i) \text{Drain resistance } (r_d) = \left( \frac{\partial V_{DS}}{\partial I_D} \right)_{V_{GS}} ; \quad \text{where } V_{GS} \text{ is constant} \quad \dots(5.72)$$

It has unit of resistance ( $\Omega$  or  $M\Omega$ ).

$$(ii) \text{Transconductance } (g_m) = \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} ; \quad \text{where } V_{DS} \text{ is constant.} \quad \dots(5.73)$$

It has unit of conductance (mho).

$$(iii) \text{Amplification factor } (\mu) = - \left( \frac{\partial V_{DS}}{\partial V_{GS}} \right)_{I_D} ; \quad \text{where } I_D \text{ is constant} \quad \dots(5.74)$$

where negative sign indicates that when  $V_{GS}$  is increased,  $V_{DS}$  should be decreased for a constant  $I_D$ . This is a unitless parameter.

The relationship among three parameters can be obtained as follows :

We have

$$\mu = \left( \frac{\partial V_{DS}}{\partial V_{GS}} \right)_{I_D}$$

Multiply and divide R.H.S. by  $\partial I_D$

$$\mu = \left( \frac{\partial V_{DS}}{\partial V_{GS}} \right) \times \frac{\partial I_D}{\partial I_D}$$

$$\mu = \left( \frac{\partial V_{DS}}{\partial I_D} \right) \times \left( \frac{\partial I_D}{\partial V_{GS}} \right)$$

$$\mu = r_d \times g_m \quad \dots(5.75)$$

Thus amplification factor = drain resistance  $\times$  transconductance.

### 5.13.4 Transconductance Curves

The transconductance curve of a JFET is a plot of output current,  $I_D$  versus input voltage,  $V_{GS}$  as shown in Fig. 5.61.

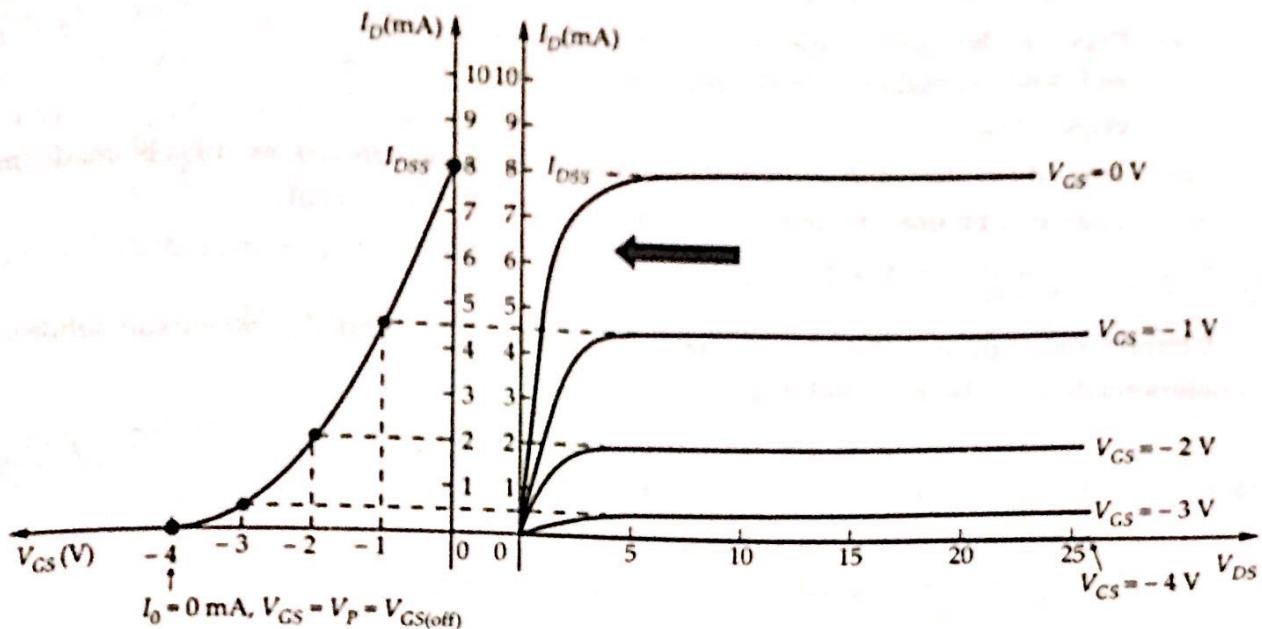


Figure 5.61 Transfer curve ( $I_D$  vs.  $V_{GS}$ ) obtained from the drain characteristics ( $I_D$  vs.  $V_{DS}$ ).

By reading the value of  $I_D$  and  $V_{GS}$  for a particular value of  $V_{DS}$ , the transconductance curve can be drawn. The transconductance curve is a part of parabola.

(i) Formula for saturation drain current  $I_{DS}$  is obtained from the transconductance curves as shown below :

$$I_{DS} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \quad \dots(5.76)$$

where  $I_{DS}$  is the saturation drain current ;  $I_{DSS}$  is the value of  $I_{DS}$  at  $V_{GS} = 0\text{ V}$

$V_P$  is pinch-off voltage  $= (V_{GS})_{off}$  ;  $V_{GS}$  is gate to source voltage.

(ii) Minimum value of  $V_{DS}$  for pinch off to happen at  $V_{GS}$  is :

$$V_{DS}(\min) = V_{GS} - V_P \quad \dots(5.77)$$

Data sheet provides only  $I_{DSS}$  and  $V_P = V_{GS(off)}$  value.

### 5.13.5 JFET Applications

It has several applications given below :

- (i) JFETs are used in cascade amplifiers in test and measuring devices, because of low level noise.
- (ii) They can be used in voltage variable resistor (VVR), because of variable resistance in ohmic region.

- (iii) They are used in low frequency amplifiers. (Hearing aid etc.), because of low coupling capacitor.
- (iv) They can be used in FM, TV receivers and many other communication devices, because of low modulation distortion.
- (v) They can be used as impedance matching device between high impedance source and low impedance load, because of high input impedance and low output impedance.
- (vi) They are preferred in computers and other integrated circuits, because of small sizes.
- (vii) They can be used in analog switches.
- (viii) They have very high power gain. Thus eliminating the requirement of driver stages.

*Example 5.20* For a N-channel JFET,  $I_{DSS} = 8.7 \text{ mA}$ ,  $V_p = -3 \text{ V}$ ,  $V_{GS} = -1 \text{ V}$ .

Calculate (i)  $I_{DS}$  (ii)  $g_m$  (iii)  $g_{m0}$ .

*Solution.* Given : Drain-source saturation current,  $I_{DSS} = 8.7 \text{ mA} = 0.0087 \text{ mA}$ , pinch off voltage,  $V_p = -3 \text{ V}$ , Gate-source voltage  $V_{GS} = -1 \text{ V}$ .

$$(i) I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2 = 0.0087 \left( 1 - \frac{1}{3} \right)^2 = 3.8667 \text{ mA}$$

$$(ii) \text{ Transconductance, } g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_p} \right)$$

where  $g_{m0}$  = transconductance at  $V_{GS} = 0$ , which is defined as :

$$g_{m0} = \frac{-2 I_{DSS}}{V_p} = \frac{-2 \times 8.7}{-3} = 5.8 \text{ mA/V}$$

$$\text{Therefore, } g_m = 5.8 \left( 1 - \frac{-1}{-3} \right) = 3.867 \text{ mA/V.}$$

## 5.14. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

**Construction.** The structure of *N*-channel enhancement type is provided in Fig. 5.62(a). Its circuit symbol is shown in Fig. 5.62(b). MOSFETs do not have continuous channel for conduction, which is shown by broken line in the circuit symbol.

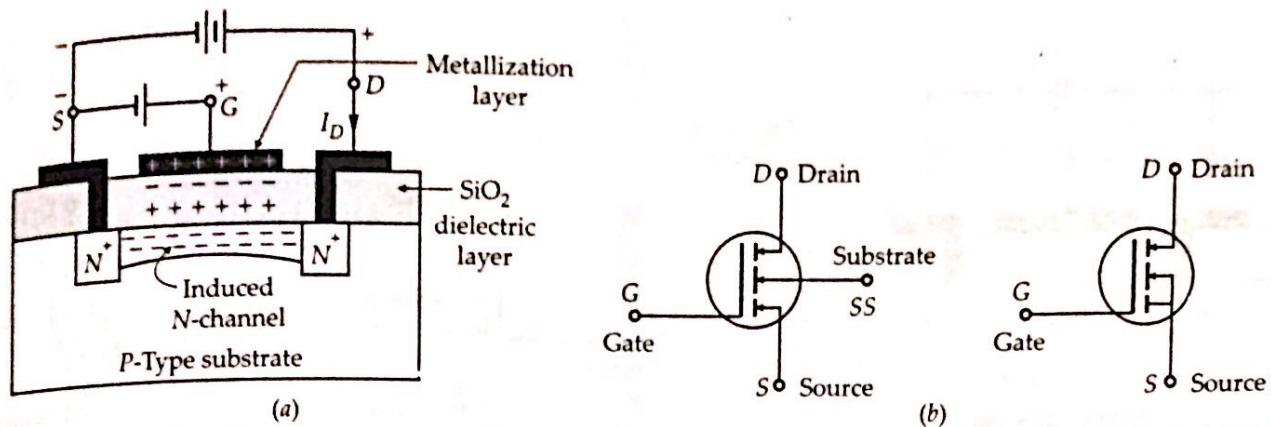


Figure 5.62 (a) Structure of enhancement MOSFET (b) circuit symbols.

A lightly doped *P*-type semiconductor is taken as a substrate and two highly doped *N*<sup>+</sup>-type regions are diffused in it. One *N*<sup>+</sup>-region is source *S* and other *N*<sup>+</sup>-region acts as drain *D*. These regions are separated by a small distance of approximately 1 mm. A thin layer of insulating material (*i.e.*,  $\text{SiO}_2$ ) is then deposited leaving only two holes for connections to the source and the drain. A thin layer of aluminium metal is now deposited over the  $\text{SiO}_2$ . This metallic layer acts as gate. The gate (*Al*), insulator ( $\text{SiO}_2$ ) and semiconductor channel together form a parallel plate capacitor, which replaces the *PN*-junction of the JFET. Insulating layer provides very high impedance to the input of the MOSFET. This value is of the order of  $10^{10}$ – $10^{15}$  ohms. An enhancement type MOSFET is suitable for switching application in digital circuits.

### Operation of MOSFET

Suppose  $V_{GS} = 0$ , a very small drain current will flow due to minority carriers present in the substrate of *P*-type. When positive voltage is applied at the gate with respect to source *i.e.*,  $V_{GS}$  is positive, an electric field is produced through the capacitor that draws minority carriers (electrons) from the substrate towards the region between source and drain forming channel of *N*-type material. In other words, positive potential at the gate induces opposite charges (electrons) between source and drain which acts as *N*-channel. Hence this channel is also known as *induced channel*. As a result conductivity increases and current flows through this channel. Therefore, drain current strongly increases with increase in gate to source ( $V_{GS}$ ) voltage as shown in Fig. 5.63.

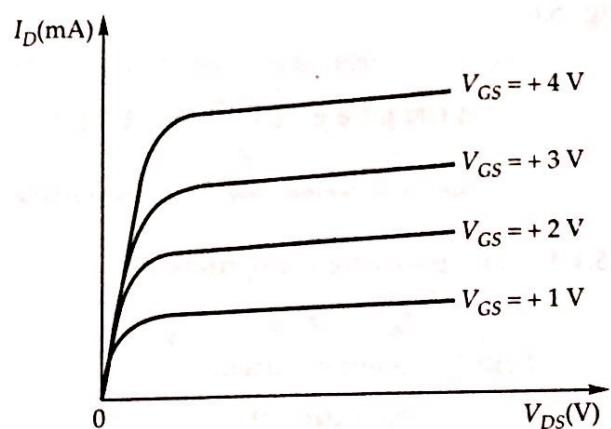


Figure 5.63 The drain characteristics of *N*-channel enhancement type.

### 5.14.2 Depletion Type MOSFET

The structure of an *N*-channel depletion type MOSFET is shown in Fig. 5.64(a) and its circuit symbol is shown in Fig. 5.64(b).

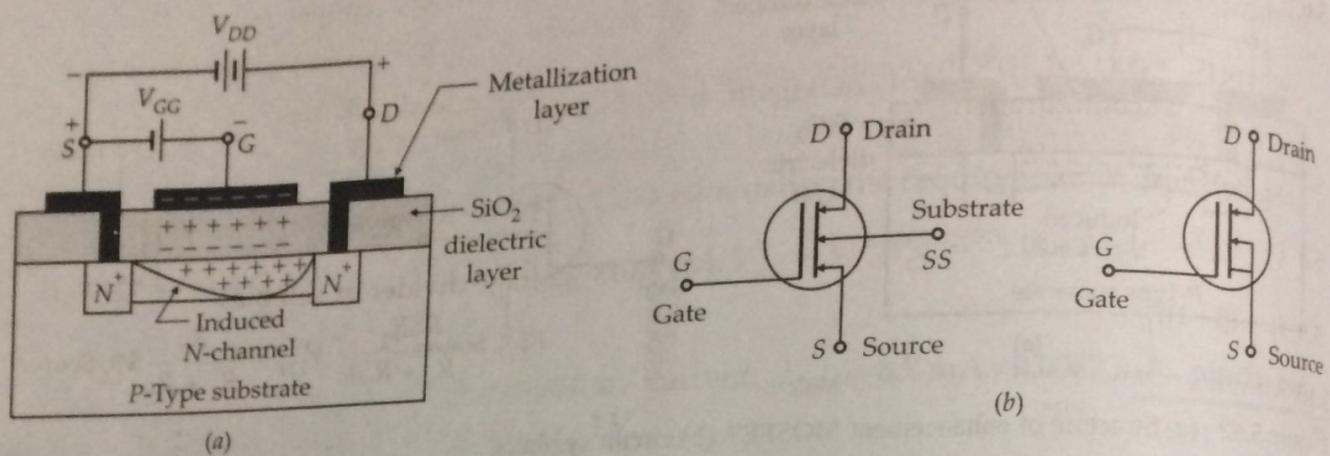


Figure 5.64 (a) Structure of depletion type MOSFET (b) Circuit symbol operation.

When  $V_{GS} = 0$ , a very small drain current flows due to minority carriers in the *P*-type substrate. When negative voltage is applied at the gate with respect to source,  $V_{GS}$  becomes positive, thus an electric field is produced which is perpendicular to the capacitor. In this process free carriers present in substrate (electrons in this case) are moved away from insulator-channel boundary. This creates a depletion layer at the channel. The width of depletion layer gradually increases from source to the drain because potential of the points near drain will be larger creating larger depletion width. This results in narrowing of the channel width and a pinch off situation will arise. In this condition, channel will be wedge shaped as shown in Fig. 5.64(a).

The drain characteristics are shown in Fig. 5.65.

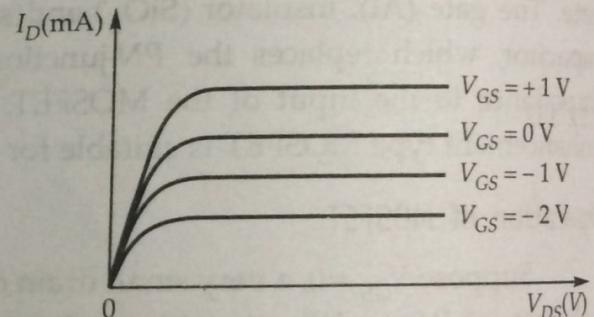


Figure 5.65 The drain characteristics of *N*-channel depletion type MOSFET

Formulae at a Glance

$$5.5 \alpha_{dc} = \frac{I_C}{I_E}$$

where  $\alpha_{dc}$  = current gain in common base configuration.

$$5.6 \beta_{dc} = \frac{I_C}{I_B}$$

where  $\beta_{dc}$  = current gain in common emitter configuration.

$$5.7 I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO} \quad (I_{CBO} \approx I_{CO})$$

$$5.8 I_C = \beta_{dc} I_E \quad (\because I_{CBO} = \text{negligible})$$

$$5.9 I_E = (\beta + 1) I_B$$

#### 5.10 Minimum power rating of a transistor

$$P_{\max} = V_{CE} I_C$$

where  $P_{\max}$  = It is the power which a transistor can withstand.

$$5.11 V_{BE} = 0.7 \text{ V (Si material)}$$

$$= 0.3 \text{ V (Ge material)}$$

where  $V_{BE}$  = cut-in voltage required to operate the diode in forward bias.

#### 5.12 Fixed bias

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \quad I_C = \beta I_B \approx I_E$$

$$S = \beta + 1$$

where  $S$  = stability factor of the circuit

$$= \left( \frac{\partial I_C}{\partial I_{CO}} \right)$$

and  $\beta = h_{fe}$   
= current gain of transistor.

#### 5.13 Emitter feedback bias

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_E}$$

$$S = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_E + R_B} \right)}$$

where  $V_{CC}$  = supply voltage

$V_{BE}$  = base-to-emitter voltage

$R_B$  = base resistor

$R_E$  = emitter resistor

$S$  = stability factor

$\beta$  = current gain of transistor.

#### 5.14 Collector feedback bias

$$S = \frac{1 + \beta}{1 + \frac{\beta R_C}{R_C + R_B}}$$

#### 5.15 Voltage divider or self bias

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}, \quad V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$

$$S = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_E + R_{TH}} \right)}$$

where

$R_1$  and  $R_2$  = potential divider resistances

$R_{TH}$  = Thevenin's equivalent resistance

$V_{TH}$  = Thevenin's voltage

$\beta$  = Current gain of transistor used.

#### 5.16 Stability factor $S$ is defined as,

$$S = \frac{\partial I_C}{\partial I_{CO}}$$

$$5.17 S = \frac{\partial I_C}{\partial \beta}, \quad S = \frac{\partial I_C}{\partial V_{BE}}$$

#### 5.18 For small signal transistor amplifier

$$(i) A_i = \frac{-h_f}{1 + h_0 R_L} \quad (ii) R_i = h_i + h_r A_i R_L$$

$$(iii) A_v = \frac{A_i R_L}{R_i}$$

$$(iv) Z_0 = \frac{1}{Y_0} \text{ where } Y_0 = h_0 - \frac{h_f h_r}{h_i + R_S}$$

where

$A_i$  = current gain of an amplifier

$R_i$  = input impedance of an amplifier

$A_v$  = voltage gain of an amplifier

$\chi_0$  = output admittance of an amplifier

$Z_0$  = output impedance of an amplifier

$h_f'$  = current gain of a transistor

$h_0$  = output admittance of a transistor

$h_t$  = reverse transfer voltage gain of

transistor

$R_L$  = load resistance

$R_S$  = source resistance.

5.19 For JFET and depletion type MOSFET

Shockley's equation:

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

$$\text{where } g_{m0} = \frac{-2I_{DSS}}{V_p} \text{ at } V_{GS} = 0$$

$g_{m0}$  = transconductance at  $V_{GS} = 0$ .

$I_{DSS}$  = saturation drain current at  $V_{GS} = 0$

$V_p$  = pinch off voltage.

$V_{GS}$  = gate to source voltage

$V_p$  = pinch-off voltage.

5.21 Transconductance,

$$g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_p} \right)$$

$$g_{m0} = \frac{-2I_{DSS}}{V_p} \text{ at } V_{GS} = 0$$

$g_{m0}$  = transconductance at  $V_{GS} = 0$ .

$I_{DSS}$  = saturation drain current at  $V_{GS} = 0$

$V_p$  = pinch off voltage.

$V_{GS}$  = gate to source voltage

$V_p$  = pinch-off voltage.

**Problem 5.2** Determine the values of  $I_E$ ,  $I_C$  of a transistor having  $\alpha = 0.98$  and  $I_{CBO} = 4\mu A$ . Base current  $I_B = 50\mu A$ .

**Solution.** Given :  $\alpha = 0.98$ ,  $I_{CBO} = 4\mu A$  and  $I_B = 50\mu A$

(i) Since we know that

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

$$\text{Amplification factor } (\mu) = - \left( \frac{\partial V_{DS}}{\partial V_{GS}} \right)_{I_D} = - \left( \frac{r_d}{r_s} \right)_{I_D} = r_d \times g_m$$

$$(ii) I_E = I_B + I_C = 0.05 + \frac{1 \times 0.004}{1 - 0.98} = 2.65 \text{ mA}$$

$$I_C = \left( \frac{\alpha}{1 - \alpha} \right) I_B + \left( \frac{1}{1 - \alpha} \right) I_{CBO} = \left( \frac{0.98}{1 - 0.98} \right) 0.05 + \frac{1 \times 0.004}{1 - 0.98} = 2.65 \text{ mA}$$

**Problem 5.3** In a transistor amplifier as shown in Fig 5.66(a),  $R_C = 8k\Omega$ ,  $R_L = 24k\Omega$  and  $V_{CC} = 24V$ . Draw the d.c. load line, determine the optimum operating point. Also draw the a.c. load line.

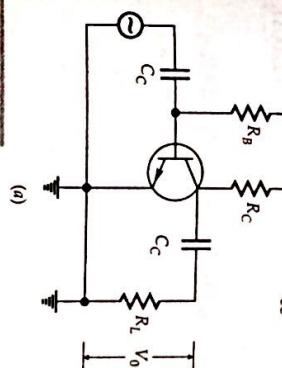


Figure 5.66

**Solution.** Given :  $R_C = 8k\Omega$ ,  $R_L = 24k\Omega$  and  $V_{CC} = 24V$

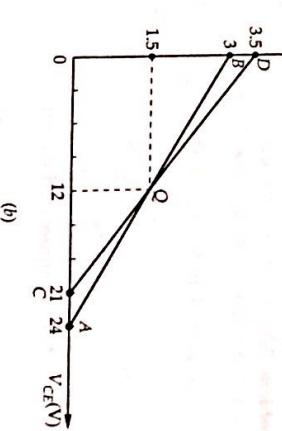
(a) (i)  $I_C$  (saturation), when  $V_{CE} = 0$ , is given by

$$I_C = \frac{V_{CC}}{R_C} = \frac{24}{8 \times 10^3} = 3mA \quad (\text{Point B})$$

(ii)  $V_{CE}$  (cut off), when  $I_C = 0$ , i.e.,  $V_{CE} = V_{CC} = 24V$  (Point A)

∴ dc load line is a line connecting two points A and B on the output characteristic curves.

(b) Optimum operating point: Midway of the load line AB provides the optimum or maximum operating point  $I_C(Q)$  and  $V_{CE}(Q)$ . In this case  $I_C(Q) = \frac{I_C}{2} = 1.5 \text{ mA}$  and  $V_{CE}(Q) = \frac{24}{2} = 12 \text{ V}$



(b)

**Solution.** Given :  $R_C = 8k\Omega$ ,  $R_L = 24k\Omega$  and  $V_{CC} = 24V$

(a) (i)  $I_C$  (saturation), when  $V_{CE} = 0$ , is given by

$$I_C = \frac{V_{CC}}{R_C} = \frac{24}{8 \times 10^3} = 3mA \quad (\text{Point B})$$

(ii)  $V_{CE}$  (cut off), when  $I_C = 0$ , i.e.,  $V_{CE} = V_{CC} = 24V$  (Point A)

∴ dc load line is a line connecting two points A and B on the output characteristic curves.

(b) Optimum operating point: Midway of the load line AB provides the optimum or maximum operating point  $I_C(Q)$  and  $V_{CE}(Q)$ . In this case  $I_C(Q) = \frac{I_C}{2} = 1.5 \text{ mA}$  and  $V_{CE}(Q) = \frac{24}{2} = 12 \text{ V}$

(c) ac load line.  $I_C$  (saturation) =  $I_C(Q) + \frac{V_{CE}(Q)}{R_{ac}} = 1.5 + \frac{12}{6 \times 10^3} = 3.5 \text{ mA}$  (Point D)

and

$$V_{CE} \text{ (cut off)} = V_{CE}(Q) + I_C(Q) \times R_{ac}$$

$$= 12 + (1.5) \times 10^{-3} \times 6 \times 10^3 = 21 \text{ V}$$

[∴  $R_{ac} = R_C \parallel R_L = \frac{R_C \cdot R_L}{R_C + R_L} = \frac{8 \times 24}{8 + 24} = 6 \text{ k}\Omega$ ]

$$(iv) I_{CEO} = \left( \frac{1}{1 - \alpha} \right) I_{CBO} = (1 + \beta) I_{CBO} = (1 + 99) \times 0.05 \text{ mA} = 5 \text{ mA.}$$

$$(v) I_E = I_B + I_C \therefore I_E = 0.05 + 5 = 5.05 \text{ mA}$$

$$(vi) I_{CEO} = \left( \frac{1}{1 - \alpha} \right) I_{CBO} = (1 + \beta) I_{CBO} = (1 + 99) \times 0.05 \text{ mA} = 5 \text{ mA.}$$

collector.

**Solution.** Given :  $\beta = 100$ ,  $V_{BE} = 0.7 \text{ V}$ ,  $I_C = 1 \text{ mA}$ ,  $V_{CC} = 5 \text{ V}$

$$(i) R_C = \frac{V_{CC} - V_C}{I_C} = \frac{15 - 5}{2 \times 10^{-3}} = 5 \text{ k}\Omega$$

(ii)  $V_{BE} = 0.7 \text{ but } V_B = 0 \text{ (as grounded)}$

Hence  $V_E = -0.7 \text{ V}$

∴ Voltage drop across

$$R_E = -0.7 - (-15) = 14.3 \text{ V}$$

$$\therefore R_E = \frac{14.3}{(I_E \approx I_C)} = \frac{14.3}{2 \times 10^{-3}} = 7.15 \text{ k}\Omega$$

Therefore, to design the circuit

$R_L = 5 \text{ k}\Omega$  and  $R_E = 7.15 \text{ k}\Omega$  would be used.

**Problem 5.10** Determine the  $I_C$  and  $V_{CE}$  for the voltage divider bias configuration of Fig. 5.69.

**Solution.** Given :  $V_{CC} = -18 \text{ V}$ ,  $R_1 = 47 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_C = 2.4 \text{ k}\Omega$  and  $R_E = 1.1 \text{ k}\Omega$ .

(i) From Fig. 5.69,

$$V_B = \left( \frac{V_{CC}}{R_1 + R_2} \right) R_2 = \frac{-18 \times 10}{47 + 10} = -3.16 \text{ V}$$

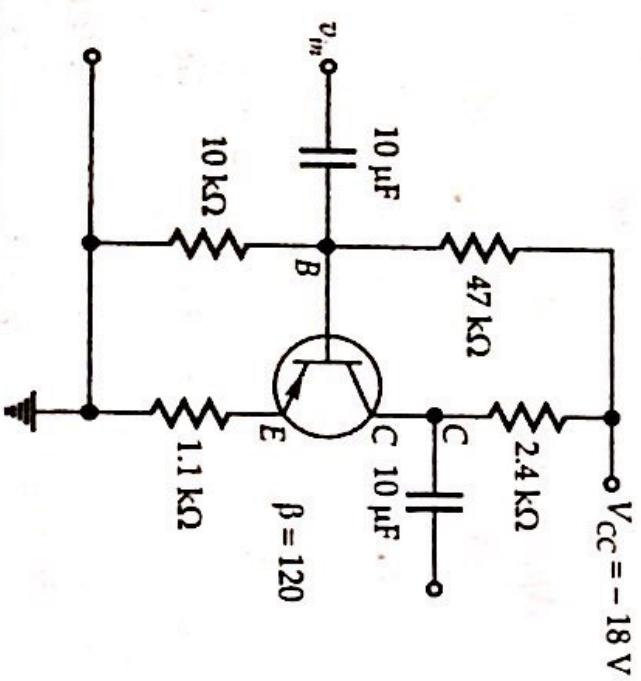


Figure 5.68

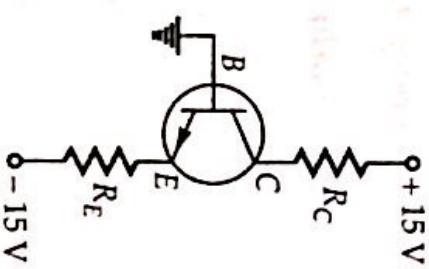


Figure 5.69

## Conceptual Questions

**5.1 Explain why  $I_{CRO}$  is greater than  $I_{CEO}$  in BJT.**

Ans. In a BJT,

$$I_F = I_C + I_R$$

and

$$I_C = \alpha I_E + I_{CEO} = \alpha(I_C + I_B) + I_{CEO} = \frac{\alpha I_B}{(1-\alpha)} + \frac{I_{CEO}}{(1-\alpha)}$$

When  $I_B = 0$ ,  $I_C = I_{CEO}$ ,

$$\text{i.e., } I_{CEO} = \frac{I_{CBO}}{1-\alpha}$$

since  $\alpha \leq 1 \Rightarrow I_{CEO} \gg I_{CBO}$ .

For example,  $\alpha = 0.99$ ,  $I_{CEO} = 100 I_{CBO}$ .

**5.2 What are  $\alpha$  and  $\beta$ ? How they are related to each other?**

Ans.  $\alpha$  is related to  $I_C$  and  $I_E$  i.e.,  $\alpha = \frac{I_C}{I_E}$ ,

$\beta$  is related to  $I_B$  and  $I_C$ . This is also known as dc current gain  $h_{FE}$  i.e.,  $\beta = \frac{I_C}{I_B}$

$$\beta = \frac{\alpha}{1-\alpha}$$

$\alpha$  is usually slightly less than unity.

**5.3 Why CE configuration is preferred in amplifier circuits?**

Ans. In this arrangement, current gain, voltage gain and power gain are quite high compared to CB and CC configurations.

**5.4 Why CC arrangement is called a voltage buffer? Does CC circuit same as emitter follower?**

Ans. CC configuration has very high input impedance and very low output impedance. That is why this configuration is placed between a high impedance source and low impedance source load. So CC arrangement is called as a voltage buffer. It is also known as impedance matching amplifier or emitter follower. (Here,  $A_v < 1$ ).

**5.5 What is early effect or base width modulation?** [IGSIPU, Dec. 2013 (5 marks)]

Ans. The modulation of the effective base width by the collector voltage is known as early effect. When collector voltage increases, width of depletion region at output junction diode increases and thus effective base width decreases.

**5.6 Explain why transistor action cannot be achieved by connecting two diodes back to back.**

Ans. Transistor action cannot be achieved by connecting two diodes back to back. It is not possible because in transistor the depletion layer formed in Emitter-Base junction and Collector-Base junction, are penetrable by both current carriers but in this case of two diodes both current carriers but

[IGSIPU, Nov. 2013 (2.5 marks)]