

VLSI

Integration :

- ① Compactness
- ② Less testing requirements at sys. level.
- ③ Less power consumption
- ④ Higher reliability
- ⑤ High speed
- ⑥ Low cost

CMOS digital IC - Kang
 CMOS VLSI design - Niel HE
 Digital IC - Reeby
 VLSI Tech - SM size

Evolution of VLSI

- ① Michael Faraday - 1833 (SC effect)
- ② Russel Ohl - 1940 (PN-JN effect)
- ③ John Bardeen - 1947 (Point contact transistor)
- ④ Jack Kilby - 1958 1st IC (Ge)
- ⑤ Robert Noyce - 1961 1st Monolithic IC
- ⑥ Gordon Moore - 1965

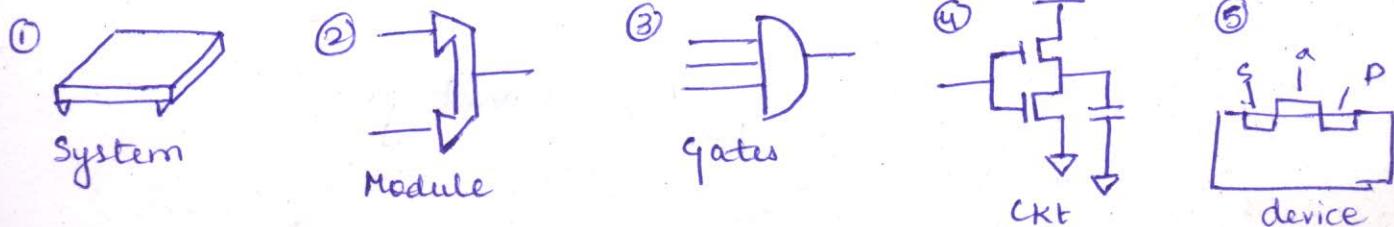
↳ No. of transistors doubles in 18 months Known as
 Moore's Law.

Integration Level (1 gate = 6 tr)

- | | |
|------|---------------------|
| SSI | - 10 gates / chip |
| MSI | - 1000 gates / chip |
| LSI | - 10,000 " " |
| VLSI | → 10,000 " " |

CMOS : Static power loss = 0

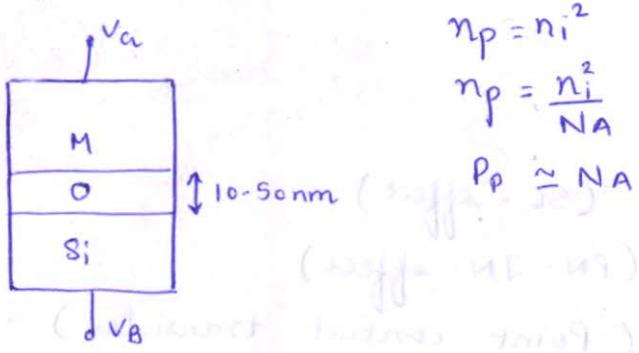
Abstraction



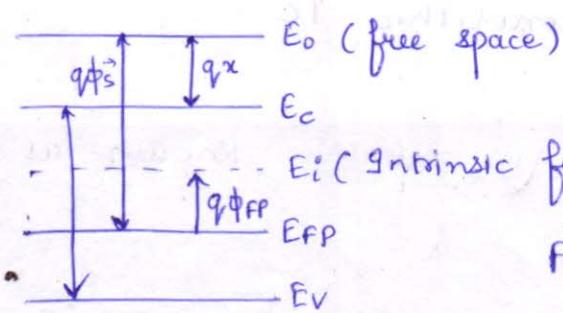
MOS \rightarrow config. is symmetric.
construction is easier.
static power dissipation is almost zero.

BJT \rightarrow config. is asymmetric.
const'n is difficult.

MOS Structure



Energy band diagram of P-Si



Fermi potential

$$\Phi_F = \frac{E_F - E_i}{q}$$

The energy required for an e^- to move from fermi level to free space is called work function ($q\phi_s$).

$$q\phi_s = q\chi + (E_C - E_F)$$

- Fermi potential at surface = surface potential ϕ_s .
 $\phi_s < \Phi_F$

$$P = n_i \exp \left(\frac{E_i - E_F}{kT} \right)$$

$$V_{FB} = \Phi_m - \phi_s$$

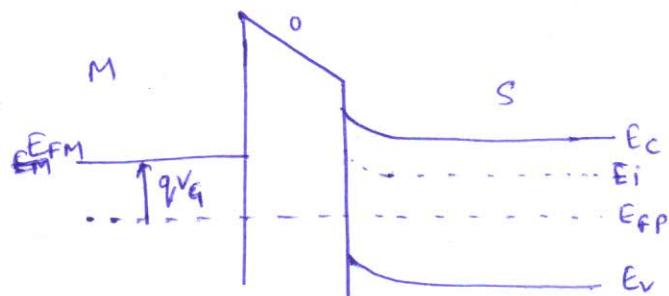
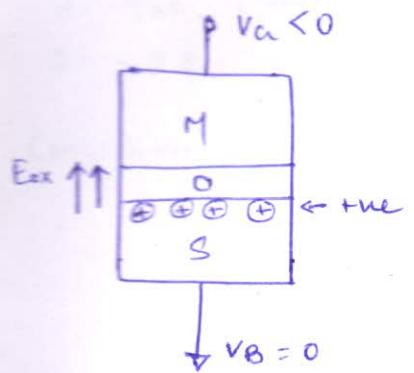
$$= q\Phi_m - q\phi_s$$

$$= 4.1 - 4.6 = -0.5 \text{ eV}$$

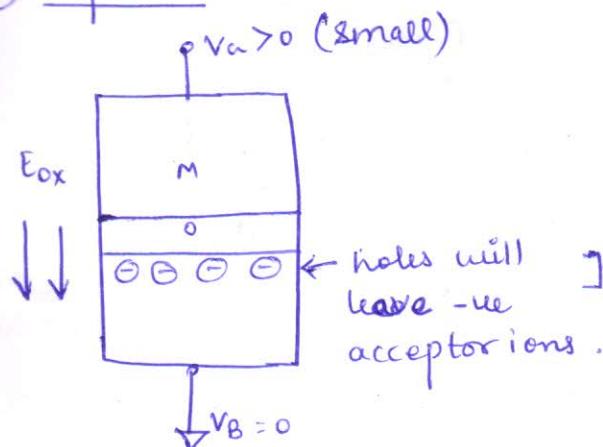
flat band voltage.

MOS under External Bias with gate as controlling parameter

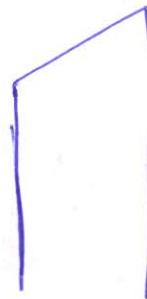
① Accumulation



② Depletion



█ depletion region (devoid of any mobile charges)



③ Inversion $V_a \gg 0$

$$\text{depletion region width: } x_d = \sqrt{\frac{2\epsilon_s |\phi_s - \phi_f|}{qN_A}}$$

$$(\text{charge density}) \quad Q = -qN_A x_d$$

$$Q = -\sqrt{2qN_A \epsilon_s |\phi_s - \phi_f|}$$

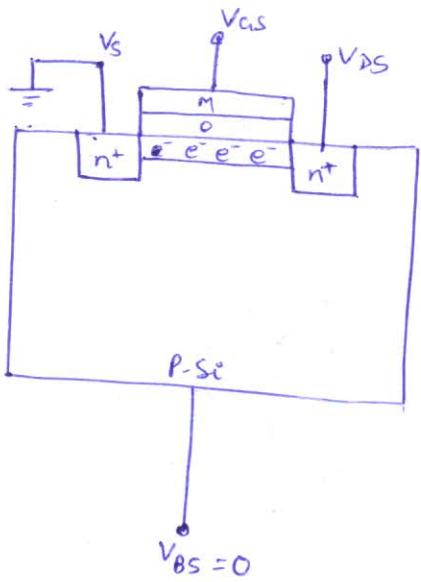


$$\boxed{\phi_s = -\phi_f}$$

No. of electrons will increase on surface but x_d remains the same.

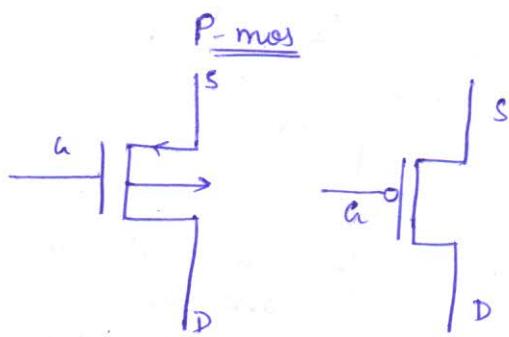
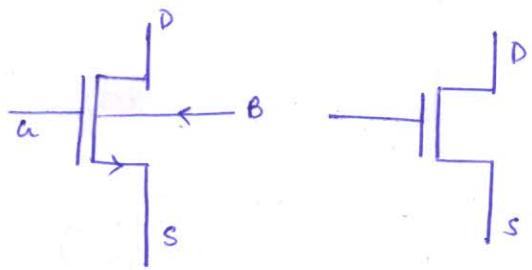
$$\text{Max depletion depth: } x_d = \sqrt{\frac{2\epsilon_s |2\phi_f|}{qN_A}}$$

MOSFET



NMOS : drain potential higher than source .
 enhancement type $V_{GS} > 0$
 depletion type $V_{GS} < 0$

N-mos



MOSFET Operation

Threshold voltage : V_{TO} depends upon the following :

1. ϕ_{AC} (work function b/w gate & channel)
2. $-2\phi_F$

Condition for inversion : $\phi_S = -\phi_F$

$$\begin{array}{c} \uparrow \quad \uparrow \\ \text{charge density} \quad \text{potential of bulk} \\ \downarrow \quad \downarrow \\ \text{potential of surface} \end{array}$$

3. $-\frac{\phi_{BO}}{C_{ox}}$ $\left\{ \begin{array}{l} \phi_{BO} = -\sqrt{2q_N A \epsilon_s | -2\phi_F | } \\ C_{ox} = \text{capacitance of oxide layer per unit area.} \end{array} \right. \quad \left\{ V_{SB} = 0 \right\}$

when $V_{SB} \neq 0 \Rightarrow \phi_B = -\sqrt{2q_N A \epsilon_s | -2\phi_F + V_{SB} | }$

4. Trap charges in oxide layer

$-\frac{\phi_{ox}}{C_{ox}}$ \leftarrow Fixed true charge density b/w oxide & silicon layer

$V_{TO} = \phi_{AC} - 2\phi_F - \frac{\phi_{BO}}{C_{ox}} - \frac{\phi_{ox}}{C_{ox}}$
 \downarrow
 $V_{SB}=0$

$V_T = \phi_{AC} - 2\phi_F - \frac{\phi_{BO}}{C_{ox}} - \frac{\phi_{ox}}{C_{ox}}$
 \uparrow
 $V_{SB} \neq 0$
 $= \phi_{AC} - 2\phi_F - \frac{\phi_{BO}}{C_{ox}} - \frac{\phi_{ox}}{C_{ox}} - \frac{(\phi_B - \phi_{BO})}{C_{ox}}$

$$\boxed{\frac{\phi_B - \phi_{BO}}{C_{ox}} = -\frac{\sqrt{2q_N A \epsilon_s | -2\phi_F + V_{SB} | } - \sqrt{| -2\phi_F | }}{C_{ox}}}$$

$$\boxed{V_T = V_{TO} + \gamma (\sqrt{| -2\phi_F + V_{SB} | } - \sqrt{| -2\phi_F | })}$$

where $\gamma = \frac{\sqrt{2q_N A \epsilon_s}}{C_{ox}}$ γ : body effect coefficient
or surface bias coefficient.

Note : For an n-channel MOSFET (nmos), the threshold ~~voltage~~ is increased by extra p-type impurities and is decreased by adding extra n-type impurities.

MOSFET OPERATION

① cut-off mode when $V_{DS} = 0$

② $V_{DS} > 0$ (small)

→ linear mode of operation

→ VCR : Voltage controlled resistor, because as voltage is ↑ed, current increases hence resistance decrease.

③ $V_{DS} = V_{DSat}$

→ depletion region increases

→ ~~pinch~~ of The surface will be pinched off.

④ $V_{DS} > V_{DSat}$

→ depletion layer channel will ~~not~~ collect toward source and effective channel length would gradually decrease.

I-V characteristic

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gradual channel approximation

① V_{TO} is constant in the entire system.

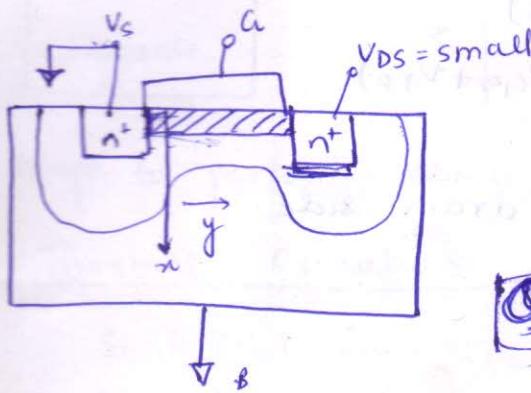
Assumptions: $V_{AS} > V_{TO}$

$$V_{AD} > V_{TO} \quad \text{--- (1)}$$

$$V_{AS} - V_{DS} > V_{TO} \quad \text{--- (2)}$$

$$\phi_I(y) = -C_{ox} (V_{AS} - V_{TO} - V_c(y))$$

gradual Channel Approximation



Linear Mode

E_y is dominant over E_x .

$$V_{AS} > V_{TO}$$

$$V_{AD} > V_{TO} \Rightarrow V_{AS} - V_{DS} > V_{TO}$$

$$\Rightarrow V_{DS} < V_{AS} - V_{TO}$$

$$I(y) = -C_{ox}(V_{AS} - V_{TO} - V_c(y))$$

channel voltage

Boundary Conditions

$$V_c(y=0) = V_S = 0$$

$$V_c(y=L) = V_{DS}$$

$$\text{now } I_D \text{ (drain current)} = V_d \times Q_I(y) \times W$$

$$\begin{aligned} &= \mu_n \times \frac{dV_c}{dy} \times -C_{ox}(V_{AS} - V_{TO} - V_c) \times W \\ &= \mu_n C_{ox} W (V_{AS} - V_{TO} - V_c) dV_c \end{aligned}$$

$$\Rightarrow I_D \cdot dy = \mu_n C_{ox} W (V_{AS} - V_{TO} - V_c) dV_c$$

Integrating from 0 to L

$$\int_0^L I_D \cdot dy = \mu_n C_{ox} W \int_0^{V_{DS}} (V_{AS} - V_{TO} - V_c) dV_c$$

$$\Rightarrow I_D \cdot L = \mu_n C_{ox} W \left[(V_{AS} - V_{TO} - \frac{V_{DS}^2}{2}) \right] \Big|_0^{V_{DS}}$$

$$\Rightarrow I_D = \frac{\mu_n C_{ox} W}{2L} \left[2(V_{AS} - V_{TO}) V_{DS} - V_{DS}^2 \right]$$

$$\Rightarrow I_D = \frac{K}{2} [2(V_{AS} - V_{TO}) V_{DS} - V_{DS}^2]$$

where K = transconductance parameter

$$K = \frac{\mu_n C_{ox} W}{L} \quad (\text{change in current by on change in voltage})$$

Saturation Mode

At Source $V_c(y)=0$

At drain $V_c(y)=V_{DS}$

Here V_{DS} is increased upto $V_{DS} = V_{AS} - V_{TO}$.

$$\begin{aligned} \text{now } Q_I(y) &= -C_{ox} (V_{AS} - V_{TO} - V_C(y)) \\ &= -C_{ox} (V_{AS} - V_{TO} - V_{DS}) \\ &= -C_{ox} (V_{AS} - V_{TO} - V_{DS} + V_{TO}) \\ &= 0 \end{aligned}$$

so, charge is nullified at the drain side.

$$I_{sat} = \frac{K}{2} (V_{AS} - V_{TO})^2$$

Cut-off Mode

~~$V_{AS} > V_{TO}$~~ $\Rightarrow I_D = 0$
 $\Rightarrow V_{AS} < V_{TO}$

N-mos

$$I_D = 0$$

Cut-off
 $V_{AS} < V_{TO}$

$$I_D = \frac{K}{2} [2(V_{AS} - V_{TO})V_{DS} - V_{DS}^2] \rightarrow \text{linear}$$

$V_{AS} > V_{TO}$ & $V_{DS} < V_{AS} - V_{TO}$

$$I_D = \frac{K}{2} (V_{AS} - V_{TO})^2 \rightarrow \text{saturation}$$

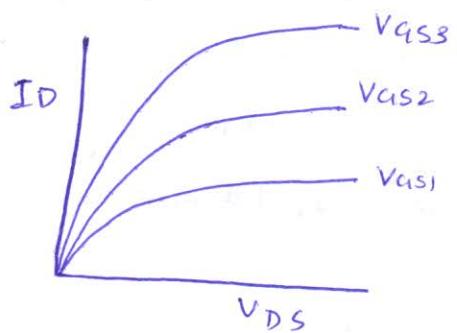
$V_{AS} \geq V_{TO}$
 $V_{DS} \geq V_{AS} - V_{TO}$

I_D is also dependent on V_{DS} even in the saturation region as in the ~~saturation~~, the width of channel decreases.

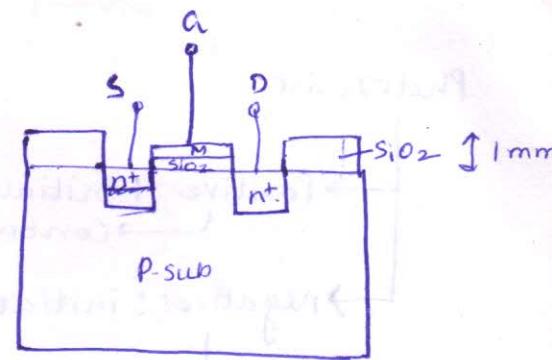
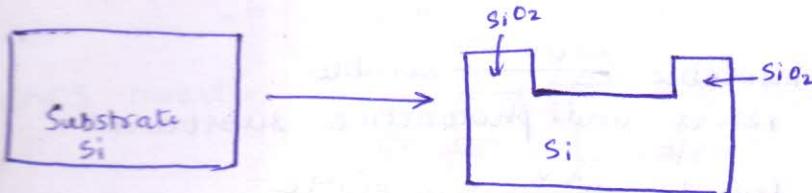
and $K \propto \frac{W}{L}$

$$\text{so } I_D = \frac{K}{2} (V_{AS} - V_{TO})^2 (1 + \lambda V_{DS})$$

where λ = channel length modulation coeff.

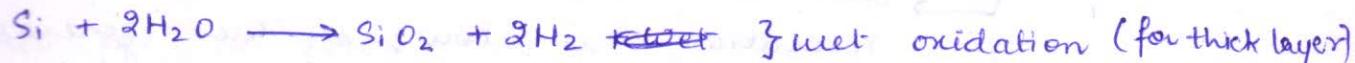


Fabrication of MOSFET

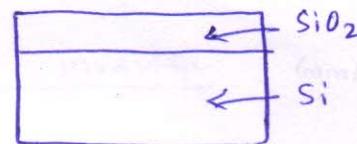


Steps to perform above functions :

① Thermal Oxidation

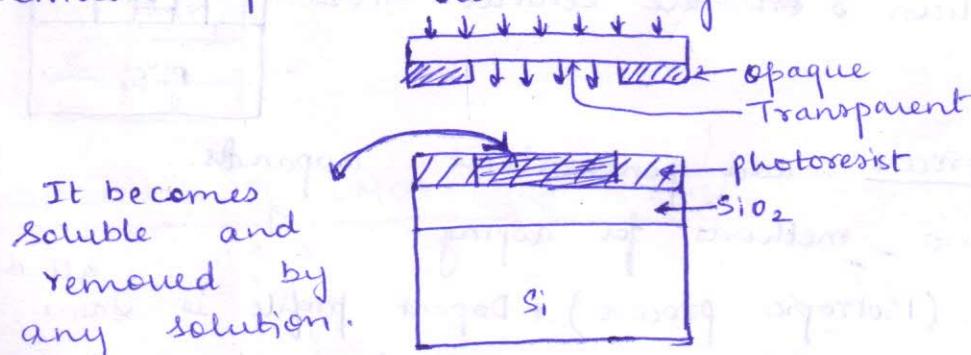


We'll use met oxidation as we require thick layer (1mm) and we get



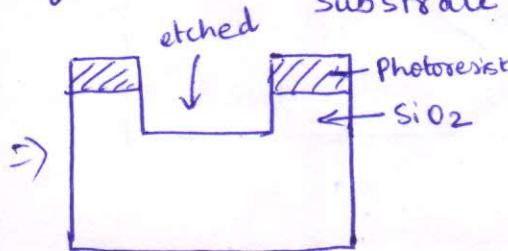
② Next we use Photoresist: light sensitive acid resistant polymer.

③ Then we do Lithography: transferring of a pattern to some surface. For lithography, we use photoresist and mask: premade patterns and UV rays.



④ Then remove the soluble photoresist with the help of any developer ~~solution~~ solution.

⑤ Next step is to do etching: selectively removing some part from the ~~substrate~~ Substrate with the help of ~~HCl~~. HF

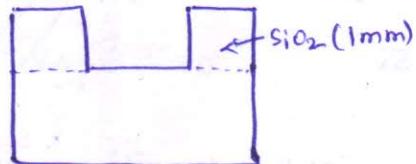


Photoresist

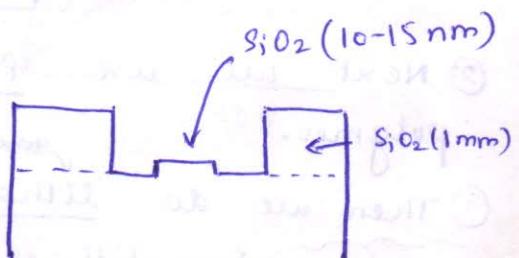
- Positive : initially insoluble \xrightarrow{UV} soluble
contains resins and photoactive substance
- negative : initially soluble \xrightarrow{UV} insoluble
contains polyisoprene and photoactive substance.
due to rubber, ~~it~~ it is swell hence resolution is low, so we generally use the photoresist. (low photolithographic resolution)

* n-mosfet preparation

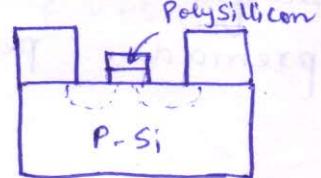
we have



- * grow thin layer of SiO_2 at centre (dry oxidation)



- * pattern polysilicon on the central SiO_2

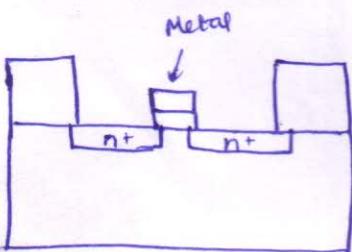


- * Self-aligned process : add pentavalent dopants.

There are two methods for doping

- Diffusion (Isotropic process) (Dopant profile is ^{all dir'} same in)
- Ion Implantation (Anisotropic process)

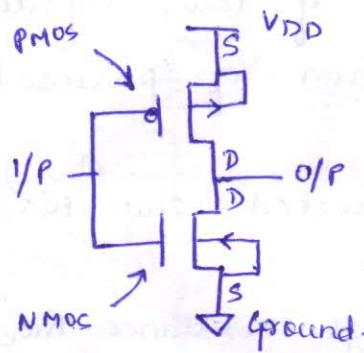
- Adv : • concentration is known & can be controlled
• used for adjusting threshold voltage
- Disad : • damage the lattice



Fabrication of CMOS Inverter

$1 \rightarrow V_{DD}$
 $0 \rightarrow \text{Ground}$

CMOS Inverter

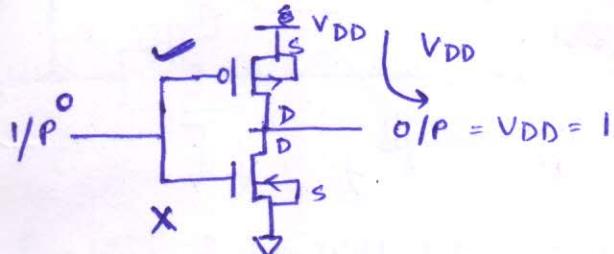


Higher pot. in nMOS : $\rightarrow D$

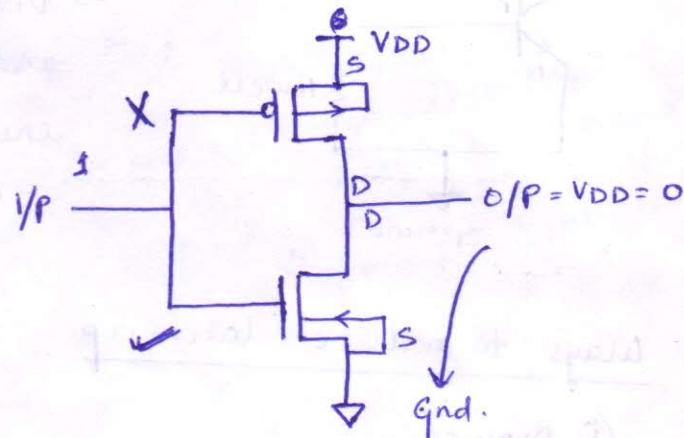
Higher pot. in PMOS : $\rightarrow S$.

Since we need $V_{SB} = 0$, we connect bulk to source in both pmos & nmos.

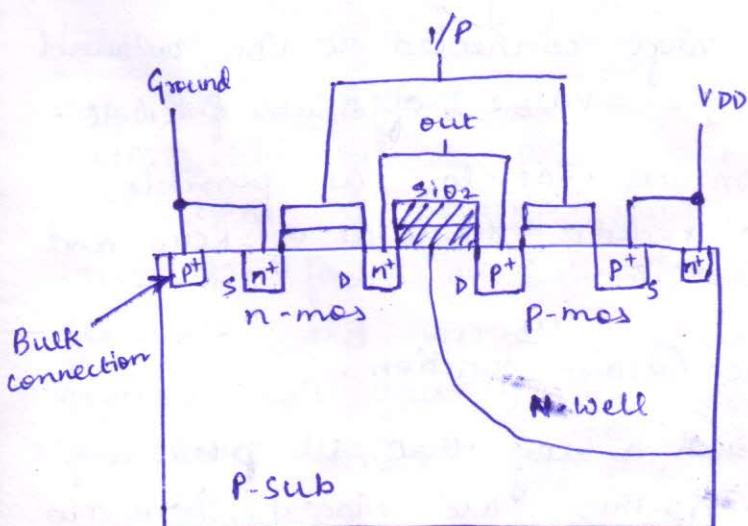
* Its working as an inverter



In	Out
0	1
1	0



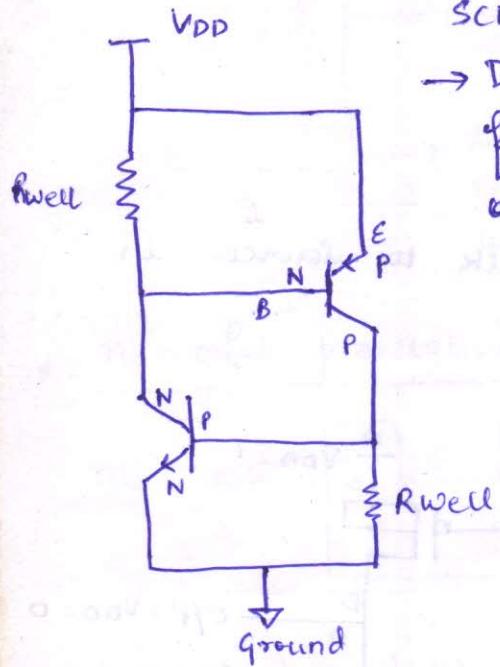
* Fabrications of CMOS using N-well



* Latch-up

Latch-up is the formation of low impedance path in CMOS ckt due to formation of parasitic BJTs. (n-p-n and p-n-p)

→ 2 BJTs connected end to end acts as an SCR.



→ Due to high resistance Rwell, V_{ceo} pot difference forms b/w B-E of p-n-p trans. which turns it on.

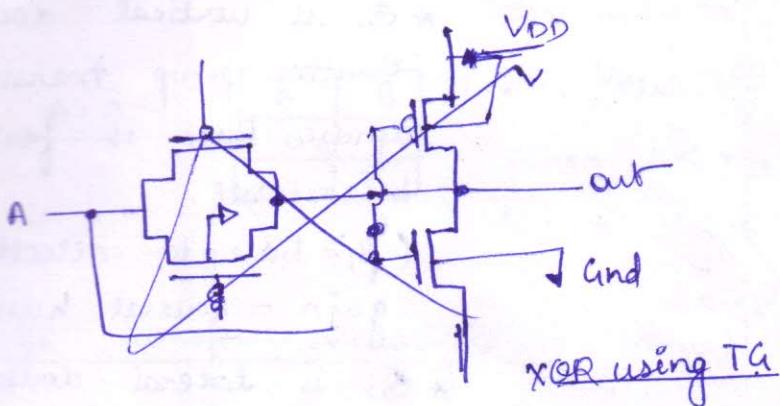
→ Then p-n-p in turns to turn on the n-p-n trans.

→ Direct path is formed b/w VDD and ground which results in energy loss.

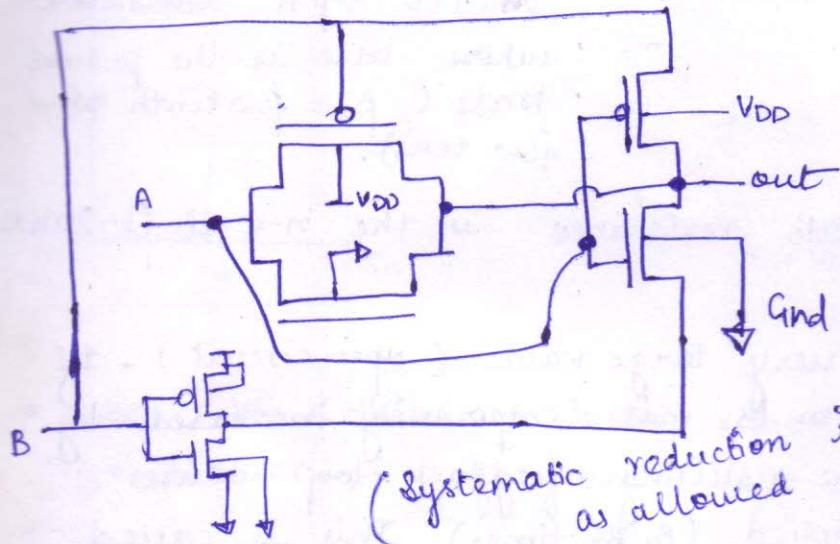
Ways to reduce latch-up

- ① Doping
- ② use of guard / band rings
- ③ Using Schottky source/drain contacts for reducing the minority carrier injection efficiency of BJT emitters.
- ④ Use P⁺ guardband rings connected to ground around NMOS transistor and N⁺ guardband rings connected to VDD around PMOS transistor to reduce the value of R_{sub} & R_{well}.
- ⑤ place substrate and well contacts as close as possible to the source connection to reduce the value of R_{sub} and R_{well}.
- ⑥ Avoid forward biasing of source/drain junction.
- ⑦ lay out n & p transistors in such a way that all p-MOS are placed closer to VDD and all n-MOS are placed closer to VSS and sufficient space is present b/w NMOS and PMOS.

Exp7:



XOR using TG



(Systematic reduction as allowed by the available technology)

size dimension
available technology
preserving
geometric ratio found
in larger devices

Scaling: The reduction in size and dimensions of a MOSFET is called scaling. It is done to achieve higher package density for VLSI technology.

Fig Two types of size reduction techniques

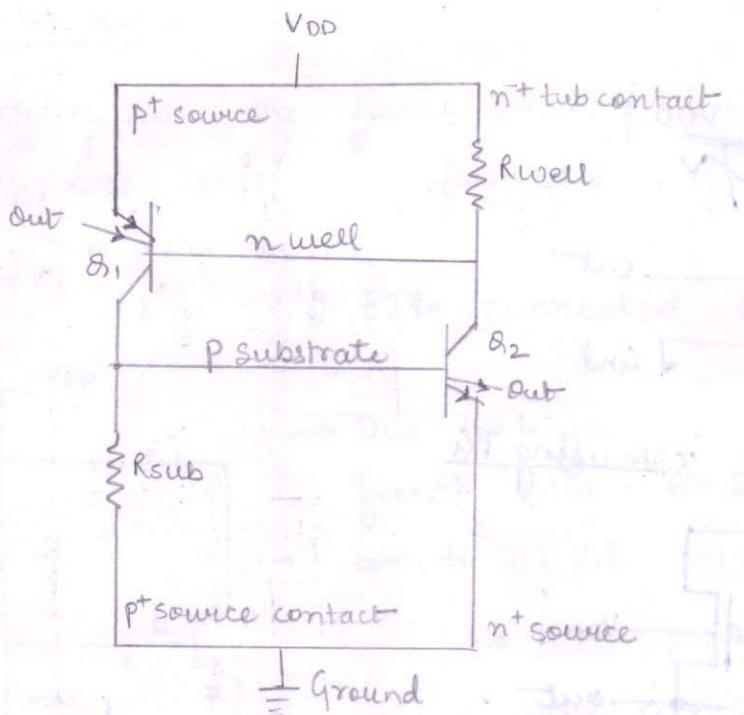
- ↳ Constant field (full-scaling)
- ↳ Constant voltage

Latch-up

Latch-up is defined as the generation of low impedance path in CMOS chips between power supply rail and ground rail due to interaction of parasitic p-n-p and n-p-n bipolar transistors.

These BJTs form a Silicon Controlled Rectifier (SCR) with positive feedback and virtually short circuits the power rail to ground rail thus causing excessive current leakage and even permanent device damage.

The latch-up susceptibility is inversely proportional to the product of doping concentration and square of the spacing.



* Q_1 is vertical double emitter p-n-p transistor whose base is formed by n-well.

(β_1 = base-to-collector gain = several hundred)

* Q_2 is lateral double emitter n-p-n transistor whose base is the p-substrate (β_2 = few tenth to few tens).

* R_{well} represents the parasitic resistance in the n-well (1-20k Ω)

Latch-Up Phenomena

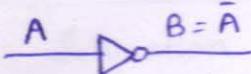
Assume R_{sub} , R_{well} to be very large value (open circuit). If the collector of either Q_1 or Q_2 is temporarily increased by any external triggering, the resulting feedback loop causes this current to be multiplied ($\beta_1 \beta_2$ times). This is called SCR triggering.

Once triggered, each transistor drives the other one with ~~to~~ the feedback thus a low impedance loop is sustained b/w power supply rail and ground rail. The condition satisfied for latch up is : $\beta_1 \beta_2 \geq 1$

Causes of Latchup

- * When I/P or O/P current swings far above VDD or far below VSS (ground) level, such disturbances can occur due to impedance mismatch.
- * Sudden transients in power or ground buses due to simultaneous switching of many drivers may turn BJT on.
- * leakage currents can cause large lateral current.
- * Radiation due to X-ray, cosmic ray may generate enough electron hole pair in both substrate and well regions of thus trigger the SCR.

MOS Inverter Characteristic



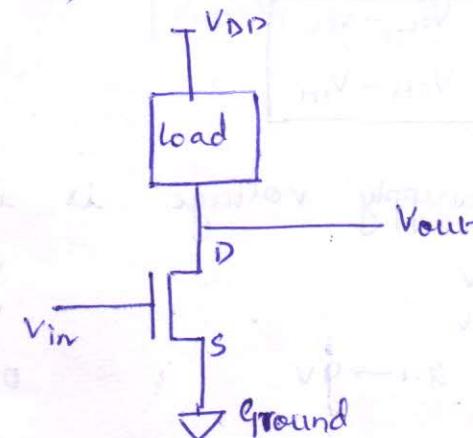
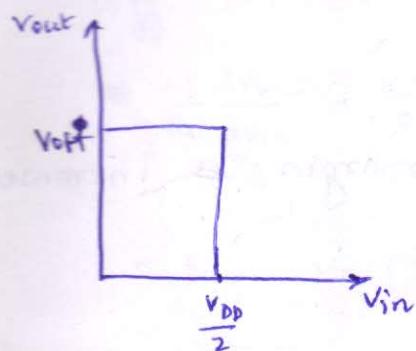
A	B
0	1
1	0

$V_{th} = \frac{V_{DD}}{2}$

when $0 < V_{in} < V_{th}$ $\xrightarrow{\text{O/P}} 0$

when $V_{th} < V_{in} < V_{DD}$ $\xrightarrow{\text{O/P}} 1$

Voltage transfer characteristics (ideal)



- When $V_{in} <$ threshold voltage for nmos
→ nmos is off and V_{out} is charged upto V_{DD}
- when $V_{in} >$ threshold voltage for nmos
→ nmos is on and V_{out} is discharged to ground.

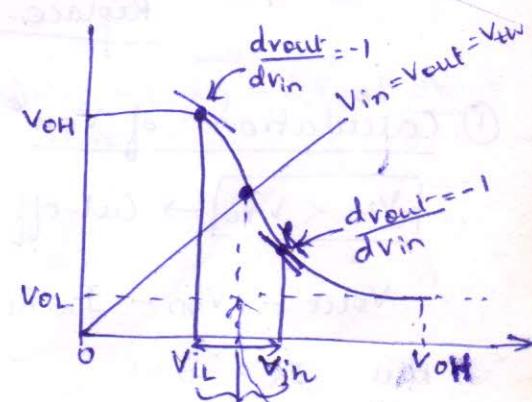
Voltage transfer characteristics (Real transistors)

V_{OH} = max O/P voltage when O/P level is at 1.

V_{OL} = min O/P voltage when O/P level is at 0.

V_{IL} = max I/P voltage which can be interpreted as logic 0.

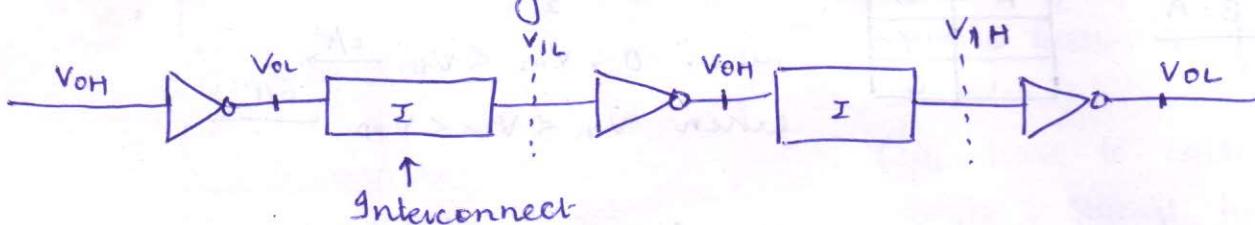
V_{IH} = min I/P voltage which can be interpreted as logic 1.



uncertain region
or transition region

Noise Margin

It is the max allowable noise that can be added to circuit without violating its characteristic.



$$\boxed{NM_L = V_{IL} - V_{OL}}$$

$$\boxed{NM_H = V_{OH} - V_{IH}}$$

When supply voltage is increased, noise margin increases.

$$V_{DD} = 4V$$

$$V_{th} = 2V$$

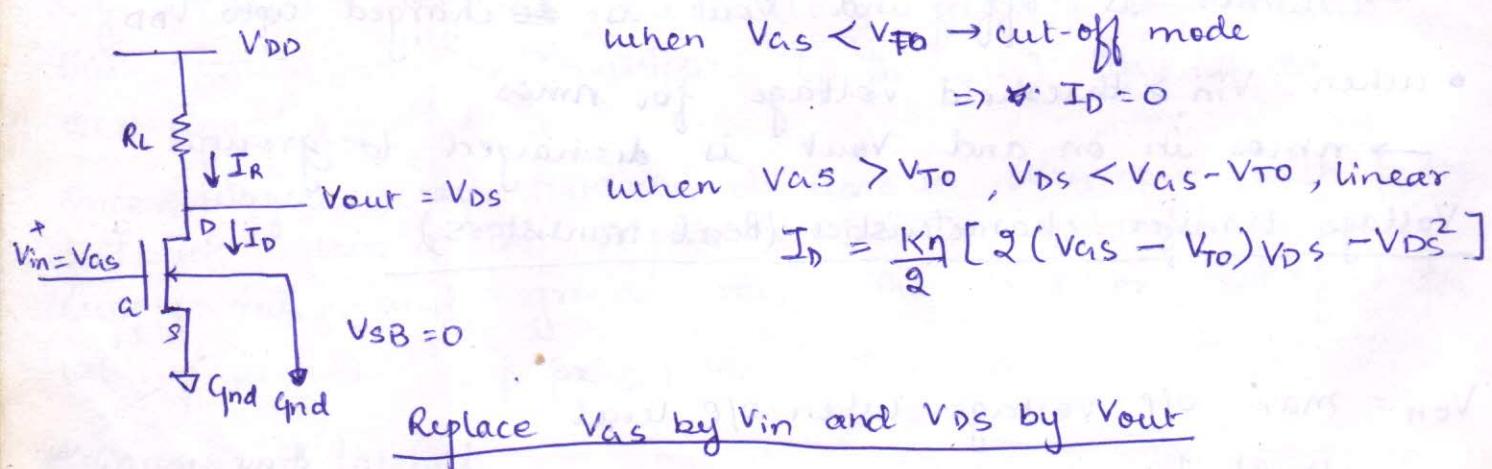
$$0 \rightarrow 1.3V \quad g. 1 \rightarrow 4V$$

$$V_{DD} = 6V$$

$$V_{th} = 3V$$

$$0 \rightarrow 2.9V$$

① Resistive Load Inverter



① Calculation of V_{OH} \leftarrow max O/P voltage (V_{out})

$$\boxed{V_{in} < V_{TO} \rightarrow \text{Cut-off}}$$

$$V_{out} = V_{DD} - I_R \cdot R_L$$

$$\text{But } I_R = I_D = 0 \Rightarrow V_{out} = V_{DD} = V_{OH}$$

② Calculation of V_{OL} \leftarrow V_{out}

$$\boxed{V_{in} = V_{OH} = V_{DD} \rightarrow \text{linear}}$$

$$I_R = I_D$$

$$\Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} [g(V_{in} - V_{TO})V_{out} - V_{out}^2]$$



$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{K_n}{2} [2(V_{DD} - V_{TO})V_{OL} - V_{OL}^2]$$

(3) Calculation of V_{IL} $\leftarrow V_{in}$

Saturation mode (V_P is low)

$$I_R = I_D(\text{sat})$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} [V_{in} - V_{TO}]^2$$

Diff. w.r.t V_{in}

$$\frac{-1}{R_L} \frac{dV_{out}}{dV_{in}} = \frac{K_n}{2} [V_{in} - V_{TO}]$$

↓
(-1) (V_{IL})

$$\frac{1}{R_L} = K_n (V_{IL} - V_{TO})$$

$$\frac{1}{K_n R_L} = V_{IL} - V_{TO}$$

$$V_{TO} + \frac{1}{K_n R_L} = V_{IL}$$

$$V_{IL} = V_{TO} + \frac{1}{K_n R_L}$$

↳ on solving

$$V_{OL} = V_{DD} - V_{TO} + \frac{1}{K_n R_L} -$$

$$(V_{DD} - V_{TO} + \frac{1}{K_n R_L})^2 - \frac{2V_{DD}}{K_n R_L}$$

(4) Calculation of V_{IH} $\leftarrow V_{in}$

Linear mode

$$I_R = I_D$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} [2(V_{in} - V_{TO})V_{out} - V_{out}^2] \quad \textcircled{1}$$

Diff. w.r.t V_{in}

$$-\frac{1}{R_L} \frac{dV_{out}}{dV_{in}} = \frac{K_n}{2} [2V_{in}V_{out} - 2((V_{in} - V_{TO}) \frac{dV_{out}}{dV_{in}} + \frac{V_{out}}{2}) - 2V_{out} \frac{dV_{out}}{dV_{in}}]$$

$$\text{Putting } \frac{dV_{out}}{dV_{in}} = -1$$

$$\Rightarrow \frac{1}{R_L} = \frac{K_n}{2} [-2(V_{in} - V_{TO}) + 2V_{out} + 2V_{out}]$$

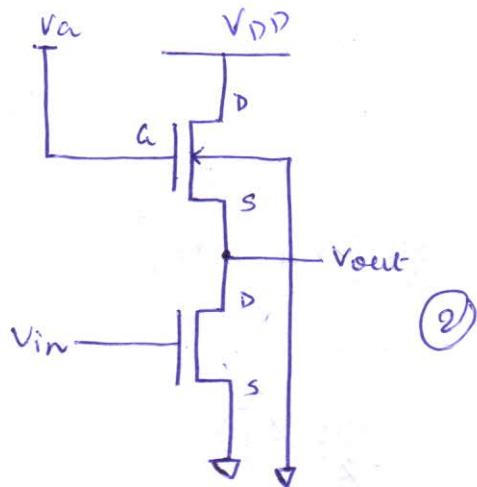
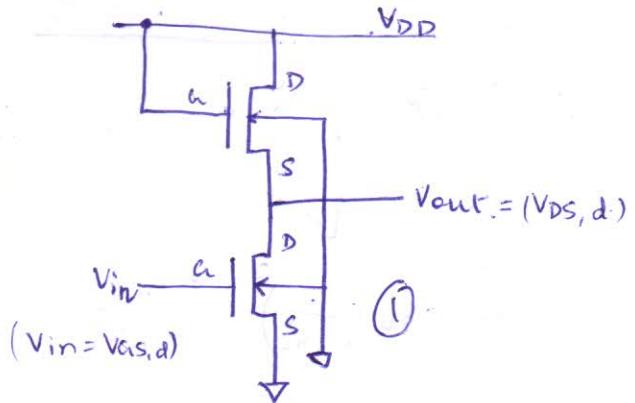
$$\Rightarrow \frac{1}{R_L} = K_n [V_{TO} - V_{in} + 2V_{out}]$$

Putting $V_{in} = V_{IH}$

$$\Rightarrow V_{IH} = 2V_{out} + V_{TO} - \frac{1}{K_n R_L} \quad \textcircled{2}$$

Solving $\textcircled{1}$ and $\textcircled{2}$ for V_{IH} : $V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{K_n R_L} - \frac{1}{K_n R_L}}$

Enhancement Load Inverter



enhancement transistor : channel is formed only when $V_{as} > V_{th}$
 depletion transistor : channel is already formed even when $V_{as} = 0$

①

Here $V_{as}(\text{load}) = V_{DS}(\text{load})$

- It will work in Saturation. $\{ V_{DS} > V_{as} - V_{TO} \}$

Drawback : It doesn't have strong 0's or 1's voltage.

When $I/P = 0$: driver in cut-off ; load in saturation

$$V_{out} = V_{DD} - V_{t, \text{load}}$$

(after charging upto above value, load will go to cut-off mode), as :

$$V_{as} = V_{DD} - V_{DD} + V_{t, \text{load}} \quad \{ \because V_{as} = V_a - V_s \}$$

$$\Rightarrow V_{as} = V_{t, \text{load}} \quad [\text{But we want } V_a > V_t]$$

②

$$\text{Here } \cancel{V_{t, \text{load}}} \quad V_a - V_t > V_{DD}$$

$$V_{as} > V_{DD} - V_{out}$$

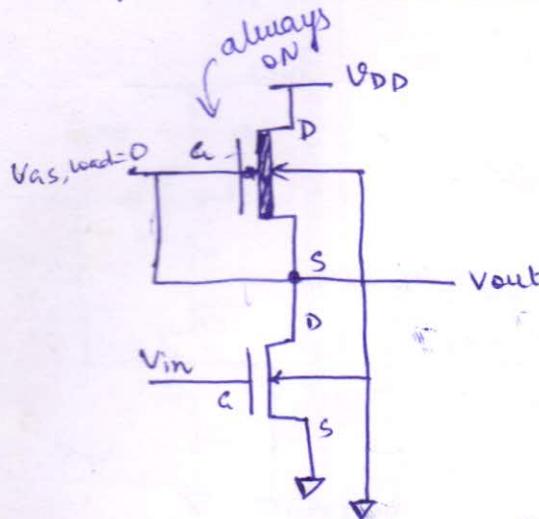
$$\text{now } V_{DS} = V_{DD} - V_{out}$$

$$\text{and } V_{as} = V_a - V_{out} - V_t$$

$$\Rightarrow V_{DS} < V_{as} - V_t \Rightarrow \text{linear}$$

But disadvantage : Two power supplies are needed \Rightarrow costly.

Depletion load Inverter



Here $V_{in} = V_{as,d}$

$$V_{out} = V_{DS,d}$$

$$V_{SB,d} = 0$$

$$V_{SB,l} \neq 0$$

$$V_{SB,l} = V_{out}$$

$$V_{th,l} = f(V_{out})$$

- Fabrication of enhancement type nmos of depletion type nmos is complex.
- Advantages: Sharp VTC transition, better noise margin, smaller layout area.

Load : Depletion type : $V_{t,load} < 0$

$$\text{linear} \rightarrow V_{DS} < V_{GS} - V_t$$

$$\Rightarrow V_{DD} - V_{out} < 0 - V_{t,load}$$

$$\Rightarrow V_{out} > V_{DD} + V_{t,load}$$

$$\text{Saturation} \rightarrow V_{DS} \geq V_{as} - V_t$$

$$\Rightarrow V_{DD} - V_{out} \geq 0 - V_{t,load}$$

$$\Rightarrow V_{out} \leq V_{DD} + V_{t,load}$$

Driver : Enhancement type : $V_{t,driver} > 0$

$$\text{linear} \rightarrow V_{DS} < V_{as} - V_t \quad ; \quad V_{in} \geq V_t$$

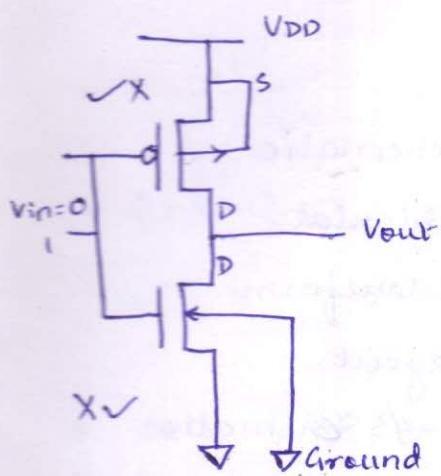
$$V_{out} < V_{in} - V_t$$

$$\text{Saturation} \rightarrow V_{out} \geq V_{in} - V_t \quad ; \quad V_{in} \geq V_t$$

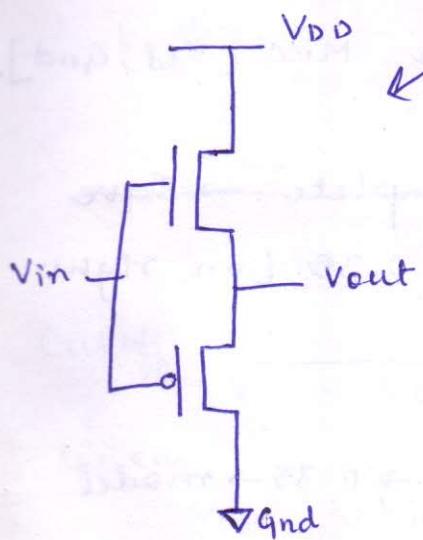
I/P	O/P	Driver op. region	load
V_{OL}	V_{OH}	cut-off	linear
V_{IL}	$\approx V_{OH}$	Saturation	linear
V_{IH}	$\approx V_{OL}$	linear	Sat.
V_{OH}	V_{OL}	linear	Sat.

Operating regions of nMOS depletion type load

CMOS inverter



- Advant:
- O/P \rightarrow is completely 1 when I/P is 0.
 - No direct path b/w VDD & ground.
 - Sharp V_{TC}
 - Steady state power = 0.



Buffer
(Bad Buffer)

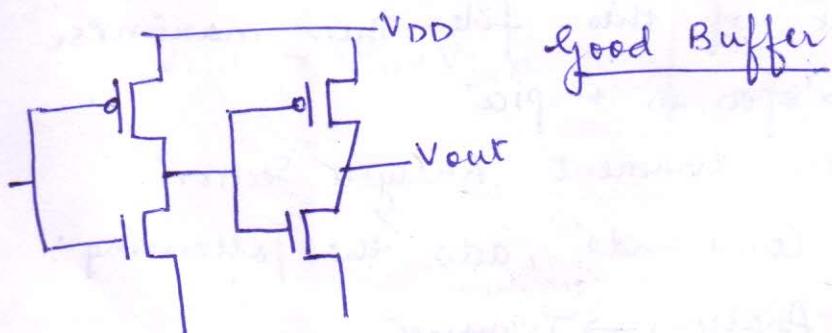
not used because always PMOS is used as pullup device and NMOS is used as pull-down device

Here $V_{out, max} \neq V_{DD}$

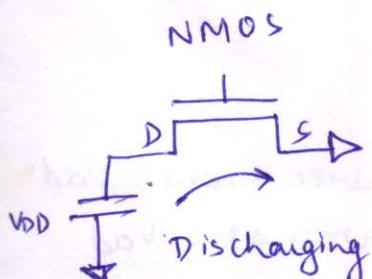
$$\hookrightarrow = V_{DD} - V_{t,n}$$

$V_{out, min} \neq 0$

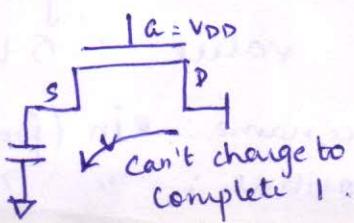
$$\hookrightarrow = V_{t,p}$$



good Buffer



NMOS
PMOS passes strong 1 \rightarrow load device
NMOS passes strong 0 \rightarrow driver device.



$I_A = V_{DD}$
Can't change to complete 1.

CMOS inverter

Derivation of critical parameters

$$V_{AS,n} = V_{in} \quad V_{AS,p} = V_{in} - V_{DD} = -(V_{DD} - V_{in})$$

$$V_{DS,n} = V_{out} \quad V_{DS,p} = V_{out} - V_{DD} = -(V_{DD} - V_{out})$$

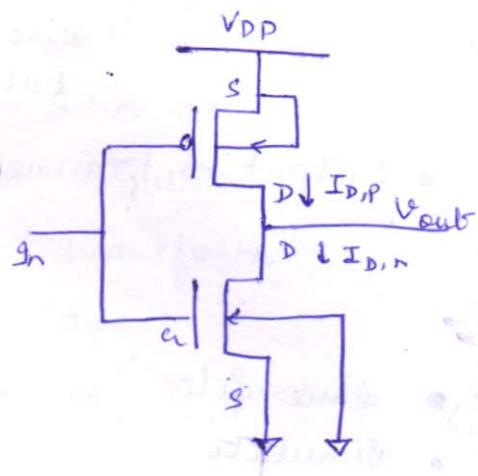
when $V_{in} < V_{t,n} \rightarrow \text{NMOS cut-off}$

$V_{in} > V_{DD} + V_{t,p} \rightarrow \text{PMOS cut-off.}$

$$V_{AS,n} > V_{t,n}$$

$$V_{AS,p} < V_{t,p}$$

$$V_{in} = V_{DD} + V_{t,p} \rightarrow V_{AS,p} = \frac{V_{DD} + V_{t,p} - V_{DD}}{V_{t,p}}$$



① V_{OH} when $V_{in} < V_{t,n} \Rightarrow \text{NMOS} \rightarrow \text{cut-off}$ and $I_{D,n} = 0$

$$\text{KCL} = I_{D,p} = I_{D,n} = 0$$

$$V_{OH} = V_{out} = V_{DD} \quad \boxed{V_{DS,p} = 0 \text{ as } I_{D,p}=0}$$

② V_{OL} when $V_{in} > V_{DD} + V_{t,p} \rightarrow \text{PMOS cutoff} \Rightarrow I_{D,p} = 0$

$$\Rightarrow I_{D,n} = 0 \rightarrow V_{DS,n} = 0 \quad \text{i.e.,} \quad \boxed{V_{out} = V_{OL} = 0}$$

NMOS

- Cutoff $\rightarrow V_{in} < V_{TO,n}$
- linear $\rightarrow V_{DS} < V_{AS,n} - V_{t,n}$
- $\Rightarrow \boxed{V_{out} < V_{in} - V_{t,n}}$

Saturation $\rightarrow \boxed{V_{out} \geq V_{in} - V_{t,n}}$

PMOS

linear $\rightarrow V_{DS,p} > V_{AS,p} - V_{t,p}$

$$\Rightarrow V_{out} - V_{PB} \geq V_{in} - V_{PB} - V_{t,p}$$

$$\Rightarrow \boxed{V_{out} > V_{in} - V_{t,p}}$$

Saturation $\rightarrow \boxed{V_{out} \leq V_{in} - V_{t,p}}$

Cut-off $= V_{in} > V_{TO,p} + V_{DD}$

I/P Voltage	O/P Voltage	N-MOS	PMOS
$< V_{t,n}$	V_{OH}	Cut-off	not linear
V_{IL}	$\approx V_{OH}$	Sat	Linear
V_{th}	V_{th}	Sat	Sat
V_{IH}	$\approx V_{OL}$	Linear	Sat.
$> V_{DD} + V_{t,p}$	V_{OL}	Linear	not Cut-off

② V_{th} ; NMOS in Sat, PMOS in Sat.

$$\text{Here } V_{in} = V_{out} = V_{th}$$

$$I_{D,n \text{ sat}} = I_{D,p \text{ sat}}$$

$$\Rightarrow \frac{K_n}{2} (V_{as,n} - V_{t,n})^2 = \frac{K_p}{2} (V_{as,p} - V_{t,p})^2$$

$$\Rightarrow \frac{K_n}{2} (V_{in} - V_{t,n})^2 = K_p (- (V_{DD} - V_{in}) - V_{t,p})^2$$

$$\Rightarrow K_n (V_{in} - V_{t,n})^2 = K_p (- V_{DD} - V_{in} + V_{t,p})^2 \quad \text{--- (1)}$$

$$\Rightarrow (V_{in} - V_{t,n}) = \sqrt{\frac{K_p}{K_n}} (V_{DD} - V_{in} + V_{t,p})$$

$$\Rightarrow V_{in} \left(1 + \sqrt{\frac{1}{K_p}} \right) = \sqrt{\frac{1}{K_p}} (V_{DD} - V_{t,p}) + V_{t,n}$$

$$\Rightarrow \boxed{\frac{V_{in} - V_{t,n}}{V_{th}} = \frac{V_{DD} - V_{t,p}}{1 + \sqrt{\frac{1}{K_p}}}}$$

transconductance parameter
 $\frac{K_n}{K_p} = K_T$

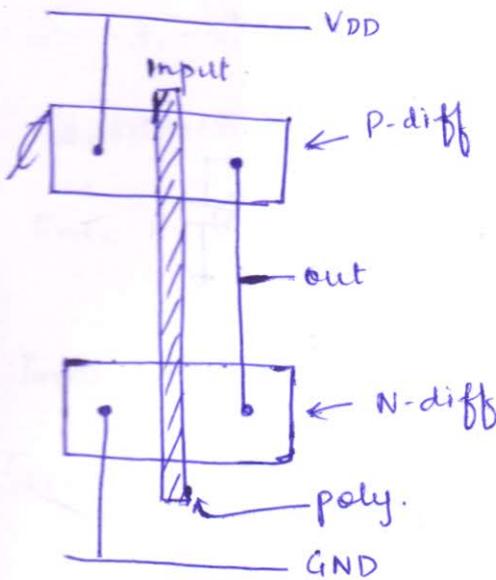
Design of symmetric and ideal Inv $V_{th} = \frac{V_{DD}}{2}$

$$\text{From eq (1)} \quad \frac{K_n}{K_p} = \frac{(V_{DD} - V_{in} + V_{t,p})^2}{(V_{in} - V_{t,n})^2} \quad \text{and}$$

• symmetrical means $V_{t,n} = |V_{t,p}|$

• Replace V_{in} by V_{th}

$$\frac{K_n}{K_p} = \frac{(0.5 V_{DD} + V_{t,p})^2}{(0.5 V_{DD} - V_{t,n})^2} = 1 \quad \left\{ \begin{array}{l} V_{t,p} = -V_{t,n} \end{array} \right.$$



Rectangle \rightarrow p & n diff

- \rightarrow contact

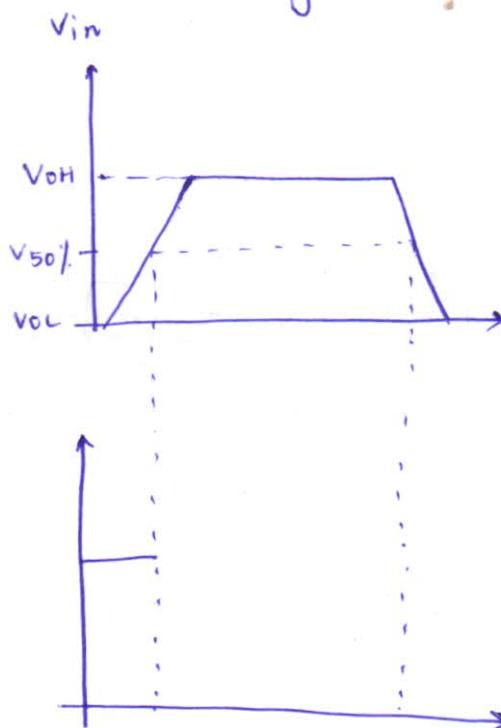
Stripped line \rightarrow poly

Solid line \rightarrow metal.

Assignment 1 : Mosfet Scaling & Small Geometry Effect
 Assignment 2 : Mosfet capacitances. (Derivation) } Ch-3
 Definition

Switching characteristics : MOS inverter

10 Feb 15 (Tue)



Fall time : Time required by the O/P to fall from 90% to 10%.

Rise time : Time required by the O/P to rise from 10% to 90%.

$$V_{50\%} = V_{OL} + \frac{1}{2} (V_{OH} - V_{OL})$$

$$= \frac{V_{OH} + V_{OL}}{2}$$

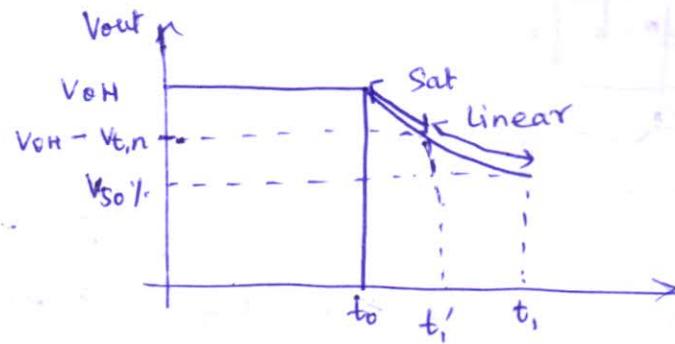
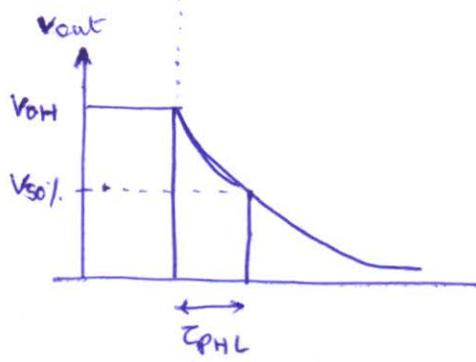
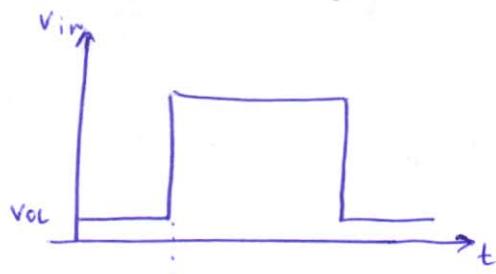
$$V_{90\%} = V_{OL} + 0.9 (V_{OH} - V_{OL})$$

$$V_{10\%} = V_{OL} + 0.1 (V_{OH} - V_{OL})$$

avg. propagation delay T_p =

$$T_p = \frac{T_{PHL} + T_{PLH}}{2}$$

Calculation of Prop. delay τ_{PHL}



$$C_{load} \frac{dV_{out}}{dt} = i_C = i_{D,P} - i_{D,N}$$

τ_{PHL} occurs when O/P turns 1 \Rightarrow P-cut-off and capacitor discharging

$$i_{D,P} \approx 0$$

$$C_{load} \frac{dV_{out}}{dt} = -i_{D,N}$$

$$\int dt = -C_{load} \int \frac{dV_{out}}{(i_{D,N})}$$

① Sat (from t_0 to t'_1)

$$\int_{t_0}^{t'_1} dt = -C_{load} \int_{V_{OH}}^{\frac{V_{OH}-V_{t,n}}{2}} \frac{dV_{out}}{\frac{K_n}{2} (V_{OH}-V_{t,n})^2}$$

$$\Rightarrow t'_1 - t_0 = -\frac{2C_{load}}{K_n(V_{OH}-V_{t,n})} [-V_{t,n}]$$

$$\Rightarrow \boxed{t'_1 - t_0 = \frac{2C_{load}V_{t,n}}{K_n(V_{OH}-V_{t,n})}} \quad \text{--- ①}$$

② linear

$$\int_{t'_1}^{t_1} dt = -2C_{load} \int_{V_{SOH}}^{\frac{V_{OH}-V_{t,n}}{2}} \frac{dV_{out}}{\frac{K_n}{2} [2(V_{OH}-V_{t,n})V_{out} - V_{out}^2]}$$

Sat (nmos)

$$V_{DS} \geq V_{GS} - V_{t,n}$$

$$\Rightarrow V_{out} \geq V_{OH} - V_{t,n}$$

linear: $\boxed{V_{out} < V_{OH} - V_{t,n}}$

$$I_{D,SAT} = \frac{K_n}{2} (V_{AS}-V_{t,n})^2$$

$$\Rightarrow t_i - t'_i$$

Subtracting eq② from ①

$$T_{PHL} = t_i - t_o = \frac{C_{load}}{K_n(V_{DD} - V_{t,n})} \left[\frac{2V_{t,n}}{V_{DD} - V_{t,n}} + \ln \left(\frac{4(V_{DD} - V_{t,n}) - 1}{V_{DD}} \right) \right]$$

Similarly

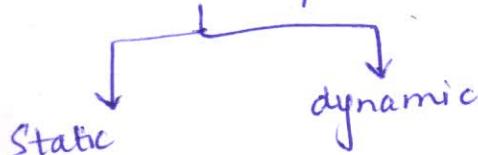
$$T_{PLH} = \frac{C_{load}}{K_p(V_{DD} - |V_{t,p}|)} \left[\frac{2|V_{t,p}|}{V_{DD} - |V_{t,p}|} + \ln \left(\frac{4(V_{DD} - |V_{t,p}|) - 1}{V_{DD}} \right) \right]$$

If delays are given (T_{PHL} , T_{PLH} etc) and $\frac{w}{L}$ is asked:

$$\text{use } K_n = M_n C_{ox} \left(\frac{w}{L} \right)_n$$

$$\left(\frac{w}{L} \right)_n = \frac{C_{load}}{M_n C_{ox} T_{PHL} (V_{DD} - V_{t,n})} \left[\frac{2V_{t,n}}{V_{DD} - V_{t,n}} + \ln \left(\frac{4(V_{DD} - V_{t,n}) - 1}{V_{DD}} \right) \right]$$

Power dissipation



Static : When $V_{in}=0$ and load is already charged, so [in CMOS] no pot. diff b/w V_{DD} and load, so no current flows. So static dissipation here is zero.

- Static
 - Sub-threshold
 - leakage
 - Tunelling

Static power dissipation ;
 $P_{static} = I_{static} V_{DD}$.

Sub-threshold : distⁿ b/w drain and source is so small that there is no requirement of channel for conduction and current flows if there is pot. diff b/w source and drain.

Dynamic: Occurs when circuit switches (1 to 0 or 0 to 1) of switching.
Let the frequency be f_{sw} .

over one cycle total charge $Q = CV_{DD}$
over interval $T = T f_{sw}$

$$\begin{aligned} \text{Pavg} &= \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} dt \\ &= \frac{V_{DD}}{T} \int_0^T i_{DD}(t) \cdot dt \\ &= \frac{V_{DD}}{T} [C V_{DD} t] \Big|_0^T \\ &= C V_{DD}^2 f_{sw} \end{aligned}$$

Dynamic power dissipation total := Switching P.D + short circuiting P.D.

2, 3, 5, 6th part.

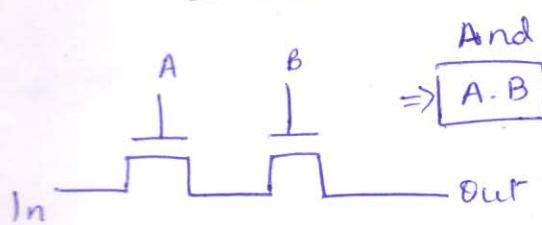
$$q = CV$$

$$\begin{aligned} \text{Pavg} &= \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} dt \\ &= \frac{V_{DD}}{T} \int_0^T i_{DD}(t) dt \\ &= \frac{V_{DD}}{T} \int_0^T C V_{DD} dt \\ &= \frac{V_{DD}}{T} [CV_{DD} t] \Big|_0^T \\ &= C V_{DD}^2 f_{sw} \end{aligned}$$

#6

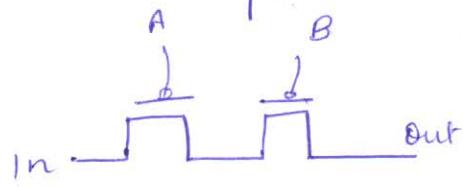
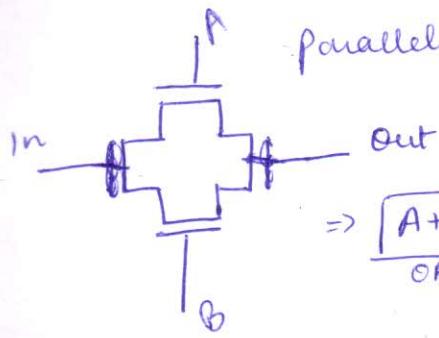
Combinational ckts (Kang Ch-7)

Ex:-

NMOS SeriesPMOS

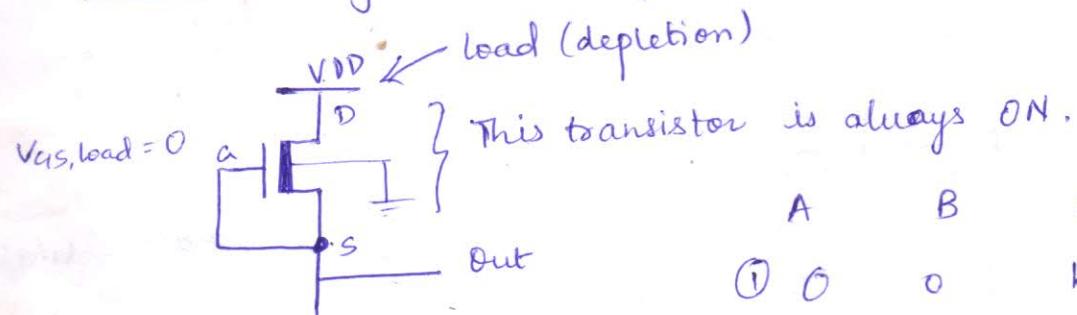
Parallel

$$\text{NAND} = \overline{\overline{A} + \overline{B}} = \overline{AB}$$



Series

$$\text{Nor} = \overline{\overline{A} \cdot \overline{B}} = \overline{A+B}$$

#2 1/P NOR gate with depletion load (No. of transistors = N+1)

	A	B	out
①	0	0	high
②	0	1	low
③	1	0	low
④	1	1	lower

Truth table for NOR gate.

- $\underline{V_{OH}} = V_{DD}$

- $\underline{V_{OL}}$ ($V_{in} = V_{OH}$)

N-MOS

Sat :- $V_{DS} \geq V_{GS} - V_t$

$$\Rightarrow V_{DD} - V_{out} \geq 0 - V_{t, \text{load}}$$

$$\Rightarrow V_{out} \leq V_{DD} + V_{t, \text{load}}$$

using general formula
of V_{OL} of depletion load
inverter.

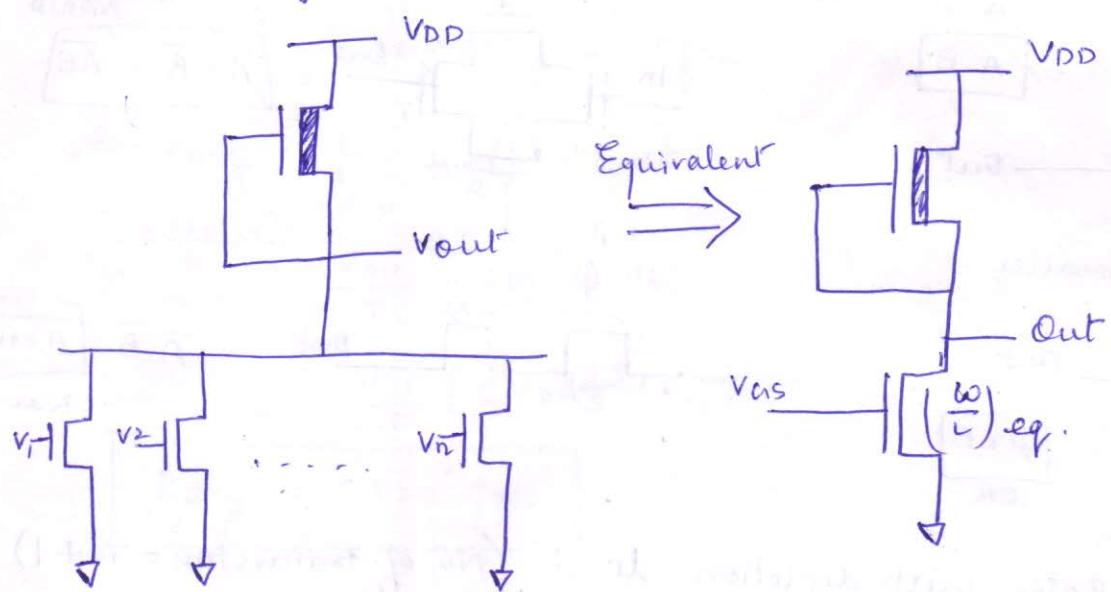
$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \frac{K_{load}}{K_{d,A}} (V_{t, \text{load}})^2}$$

} for case ②
A=0 B=1

for case 3 replace K_d, A with K_d, B

for case 4 replace K_d, A with $K_d, A + K_d, B$.

N-1/P NOR gate



If $V_1 = V_2 = \dots = V_n = V_{AS}$, above ckt will act as inverter.

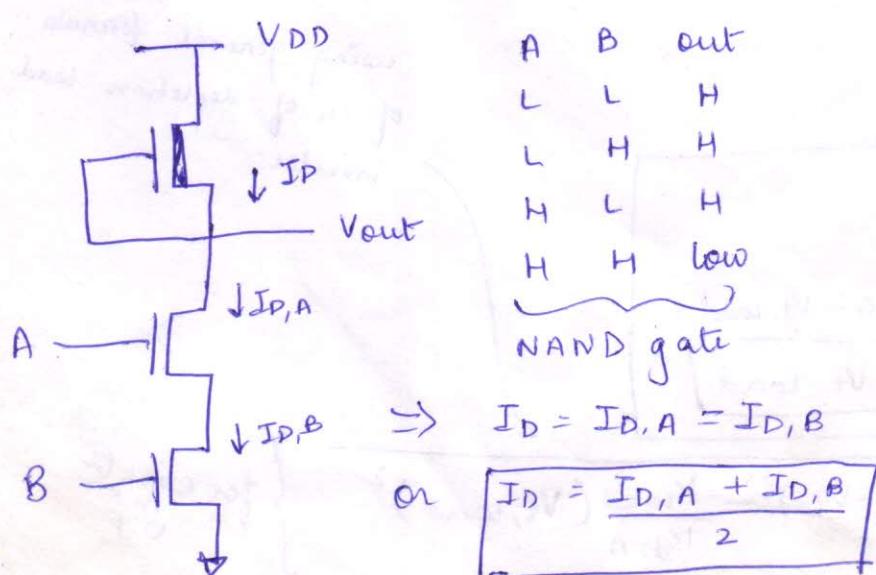
$$I_D = \sum_{K(on)} I_{D,K} = \frac{\mu n C_{ox}}{2} \left[\sum_{K(on)} \left(\frac{w}{L} \right)_K \right] (V_{AS} - V_t)^2 \quad \text{sat.}$$

$$= \frac{\mu n C_{ox}}{2} \left[\sum_{K(on)} \left(\frac{w}{L} \right)_K \right] (2(V_{AS} - V_t)V_{DS} - V_{DS}^2) \quad \text{linear}$$

$$\left(\frac{w}{L} \right)_{eq} = \sum_{K(on)} \left(\frac{w}{L} \right)_K$$

NMOS transistors are parallel
 $\Rightarrow \left(\frac{w}{L} \right)_{eq}$ = sum of individual.

N-1/P NAND gate



A	B	out
L	L	H
L	H	H
H	L	H
H	H	low

$$I_D = I_{D,A} = I_{D,B}$$

\Rightarrow

$$\boxed{I_D = \frac{I_{D,A} + I_{D,B}}{2}}$$

$$I_{D,A} + I_{D,A}$$

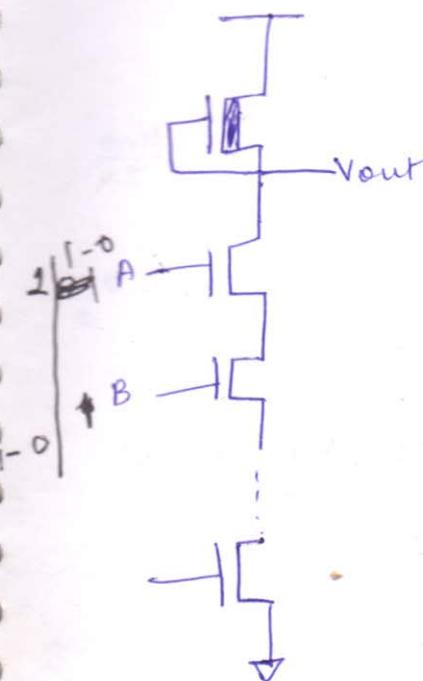
$$I_D = \frac{I_{D,A} + I_{D,A}}{2}$$

$$I_D = \frac{K_d}{4} [2(V_{AS} - V_{TO})V_{DS} - V_{DS}^2]$$

$$K_{eq} = \frac{K_d}{2}$$

When transistors are connected in series

N-1/P Nand gate



$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\sum K_{(on)} \left(\frac{W}{L}\right)_K} = \frac{1}{n} \times \left(\frac{W}{L}\right) \quad \text{if } \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \dots = \left(\frac{W}{L}\right)_n$$

Transient response

Case ①

$$A \rightarrow V_{OH} \uparrow (1)$$

$$B \rightarrow V_{OH} \text{ to } V_{OL} \downarrow$$

{ More delay
would occur }

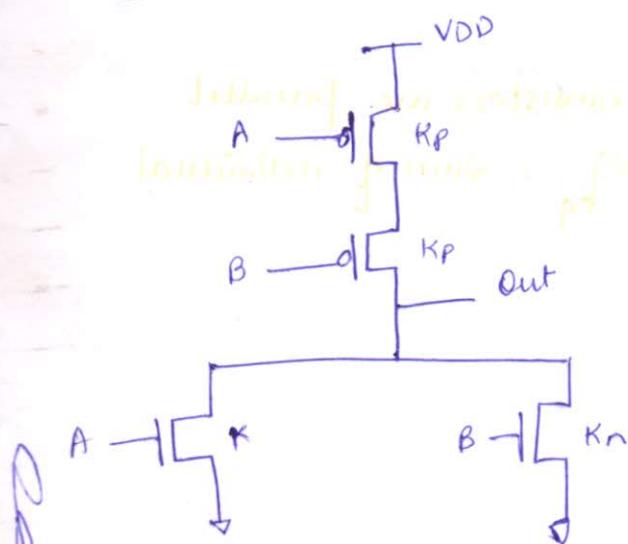
Case ②

$$A \rightarrow V_{OH} \text{ to } V_{OL}$$

$$B \rightarrow V_{OH}$$

{ less delay/no
delay would occur }

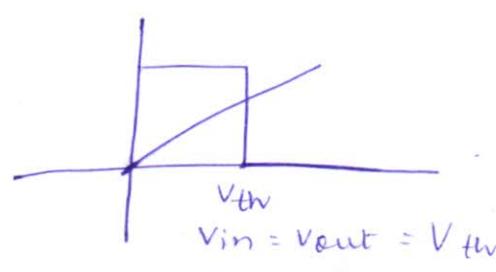
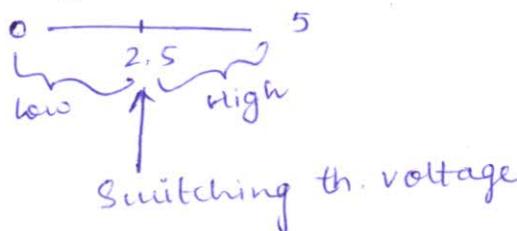
2/P 2 1/P CMOS NOR gate (no. of transistors = 2n)



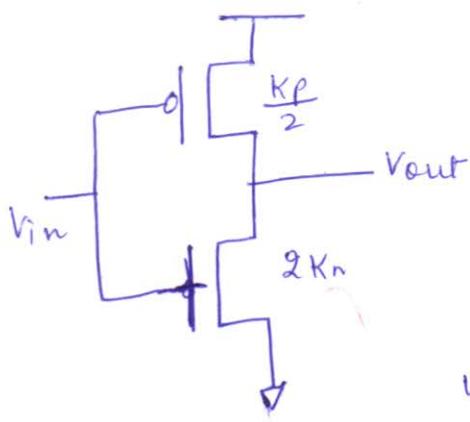
A	B	out
0	0	1
0	1	0
1	0	0
1	1	0

$$K_n = \frac{W}{L}$$

Switching threshold voltage



Equivalent ckt

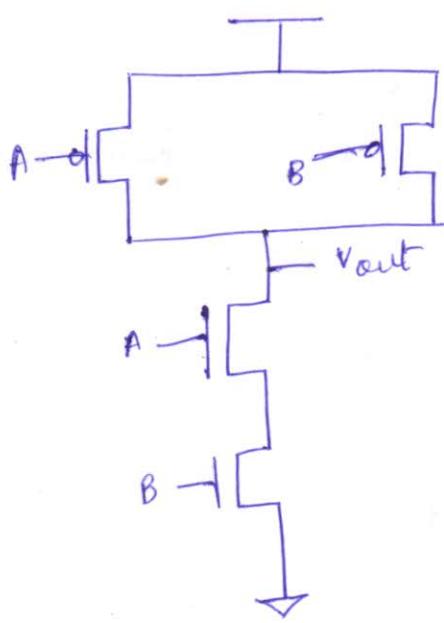


$$V_{th(1NR)} = \frac{V_{T,n} + \sqrt{\frac{K_p}{K_n}} (V_{DD} - |V_{t,p}|)}{1 + \sqrt{\frac{K_p}{4K_n}}}$$

$$= \frac{V_{T,n} + \sqrt{\frac{K_p}{4K_n}} (V_{DD} - |V_{t,p}|)}{1 + \sqrt{\frac{K_p}{4K_n}}}$$

when $K_p = 4K_n$ and $|V_{t,p}| = V_{t,n}$; $V_{th} = \frac{V_{DD}}{2}$

2 input NAND



Here ~~$\frac{2K_p}{2}$~~ , $\frac{2K_n}{2}$

$$V_{th(NAND)} = \frac{V_{T,n} + \sqrt{\frac{4K_p}{K_n}} (V_{DD} - |V_{t,p}|)}{1 + \sqrt{\frac{4K_p}{K_n}}}$$

$$\frac{2K_p}{2} = \frac{2K_n}{2}$$

Parallel (NMOS), Series (PMOS)

$$\left(\frac{w}{l}\right)_{eq} = \sum_{K(on)} \left(\frac{w}{l}\right)_k$$

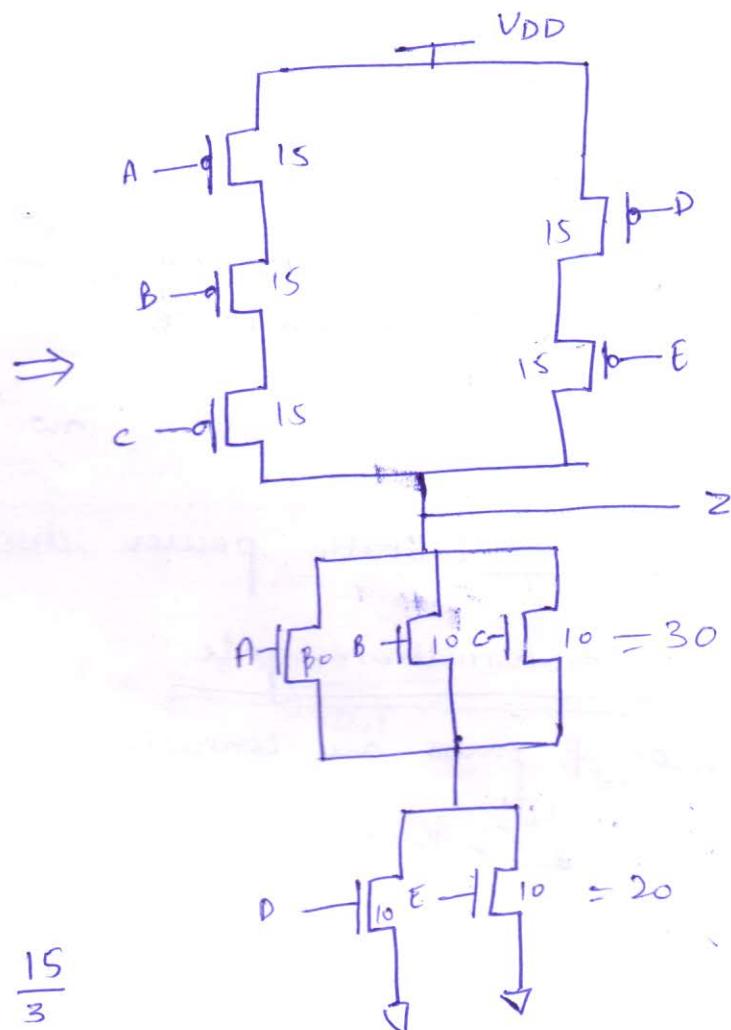
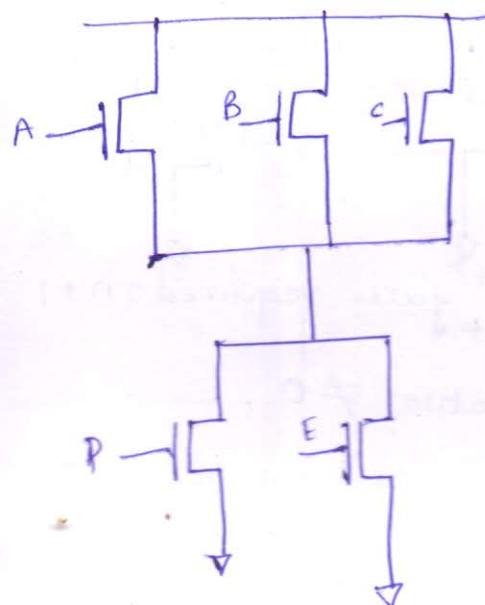
Series (NMOS), Parallel (PMOS)

$$\left(\frac{w}{l}\right)_{eq} = \frac{1}{\sum_{K(on)} \left(\frac{1}{\left(\frac{w}{l}\right)_k}\right)}$$

Q Implement $Z = \overline{(A+B+C)(D+E)}$ using CMOS logic and draw its equivalent ckt if $(\frac{W}{L})_P = 15$ & pmos f $(\frac{W}{L})_N = 10$ & nmos.

80

$$(A+B+C)(D+E)$$



$\frac{W}{L}$ of PMOS NMOS PMOS

A, B, C are parallel

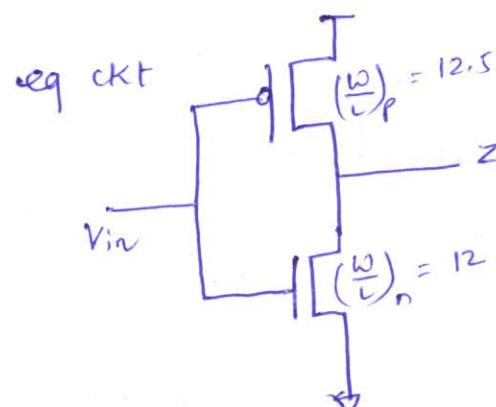
$$\frac{W}{L_{eq}} = \frac{A, B, C}{D, E} \rightarrow \frac{15}{3}$$

$$D, E \rightarrow \frac{15}{2}$$

$$\text{Sum} = \frac{15}{3} + \frac{15}{2} = 12.5 = \left(\frac{W}{L}\right)_P$$

NMOS

$$\frac{1}{\frac{1}{30} + \frac{1}{20}} = \frac{60}{5} = 12 = \left(\frac{W}{L}\right)_N$$



Pseudo-NMOS

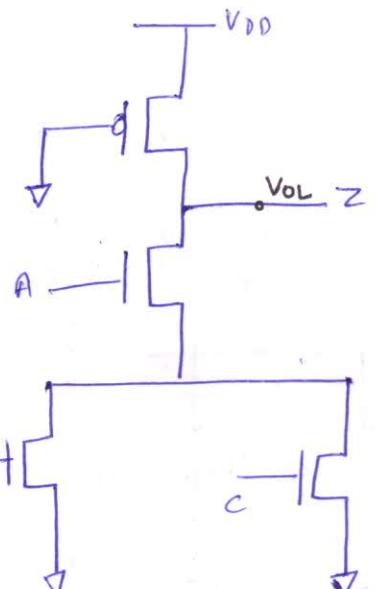
$$Z = \overline{A(B+C)}$$

→ also called ratioed logic because low voltage (V_{OL}) depends on the ~~no.~~ ratio of PMOS and NMOS.

→ V_{OL} can be controlled by controlling transconductance of PMOS & NMOS

$$I_D \propto \frac{W}{L}$$

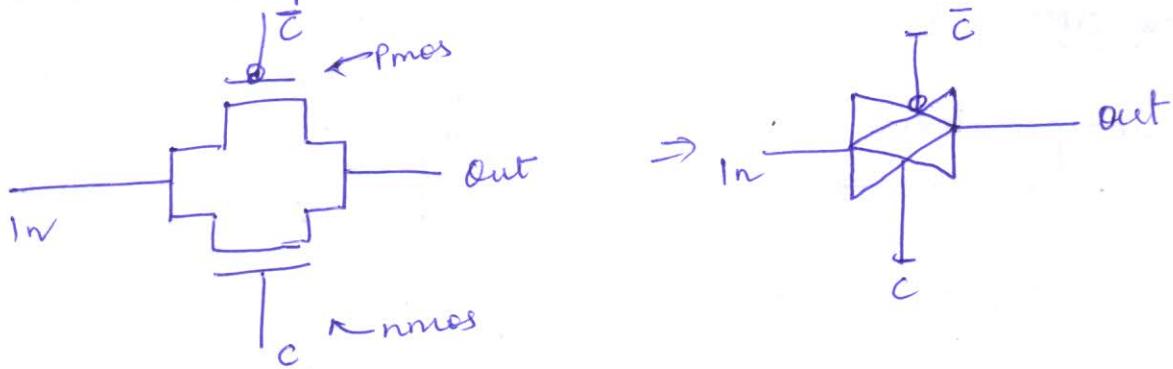
→ Disadvantage: Static power dissipation $\neq 0$.



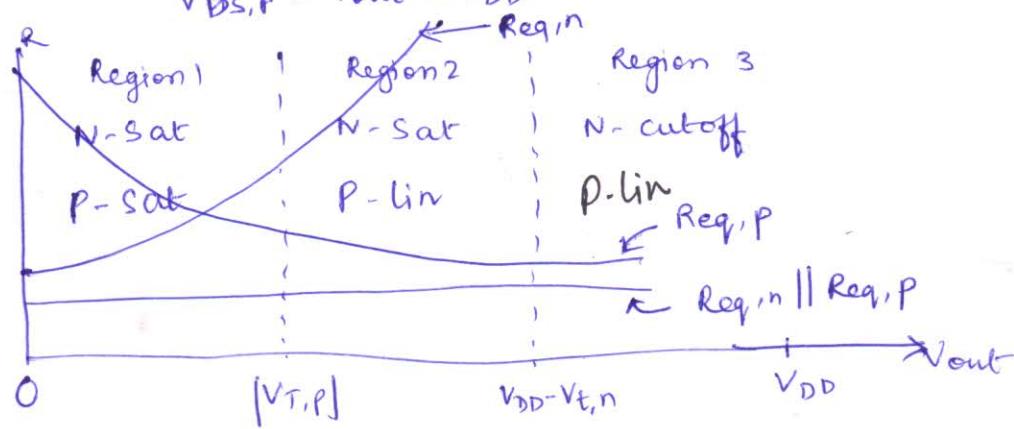
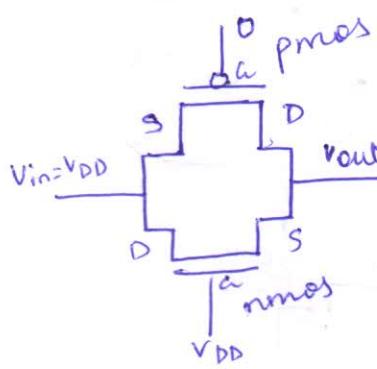
no. of gates required: $n+1$

CMOS transmission gate

→ NMOS & PMOS are connected in parallel.



Derivation



$$V_{AS,n} = V_{DD} - V_{out}$$

$$V_{DS,n} = V_{DD} - V_{out}$$

$$V_{AS,p} = -V_{DD}$$

$$V_{DS,p} = V_{out} - V_{DD}$$

Region 3

N-cut off

P-Lin

Req, P

$\approx Req, n \parallel Req, P$

V_{out}

NMOS

[Sat: $V_{DS} \geq V_{GS} - V_{t,n}$; lin: $V_{DS} \leq V_{GS} - V_t$]

$$V_{out} = V_{DD} - V_{t,n}$$

$$V_{GS,n} = V_{DD} - V_{DD} + V_{t,n} = V_{t,n}$$

PMOS

Sat: $V_{DS} \leq V_{GS} - V_{t,p}$

$$V_{out} - V_{DD} \quad -V_{DD} + 1$$

o

$$R1: 0.5 - 5 \quad -5+ \\ -4.5 < -4 \Rightarrow \text{Sat.}$$

$$R2: 2-5 \quad -5+ \\ -3 > -4 \Rightarrow \text{lin}$$

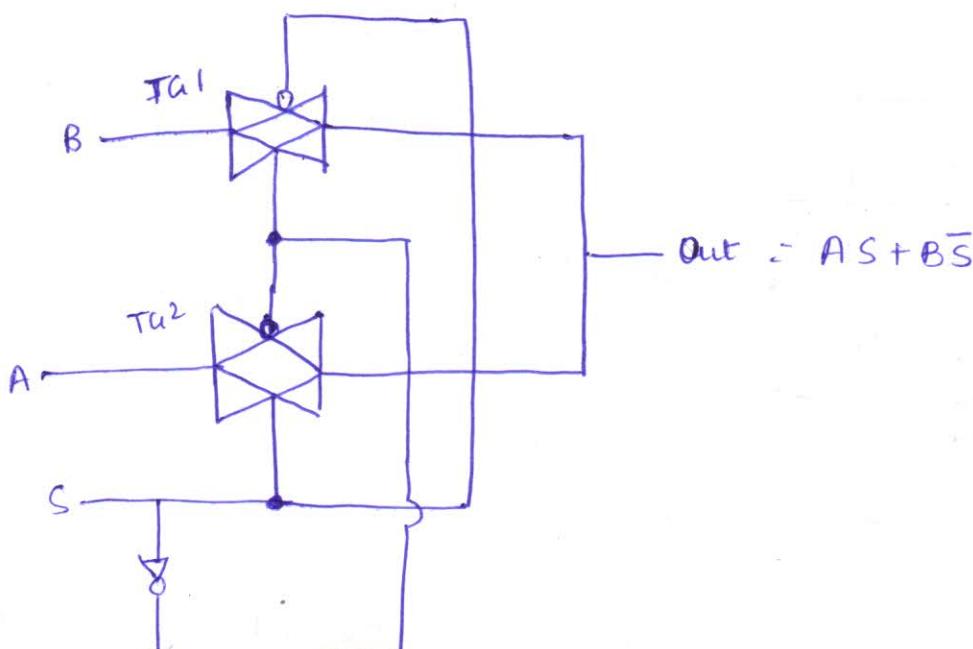
(let $V_{t,p} = -1$)
 $V_{DD} = 5V$)

$$I = I_{SD,p} + I_{DS,n}$$

$$\text{Req.}_n = \frac{V_{DD} - V_{out}}{I_{DS,n}}$$

$$\text{Req.}_p = \frac{V_{DD} - V_{out}}{I_{SD,p}}$$

2:1 MUX using TA



$S=1 \Rightarrow$ TG1 off, TG2 on $\Rightarrow \text{out} = A$

$S=0 \Rightarrow$ TG1 on, TG2 off $\Rightarrow \text{out} = B$

2 I/P XOR gate using CMOS

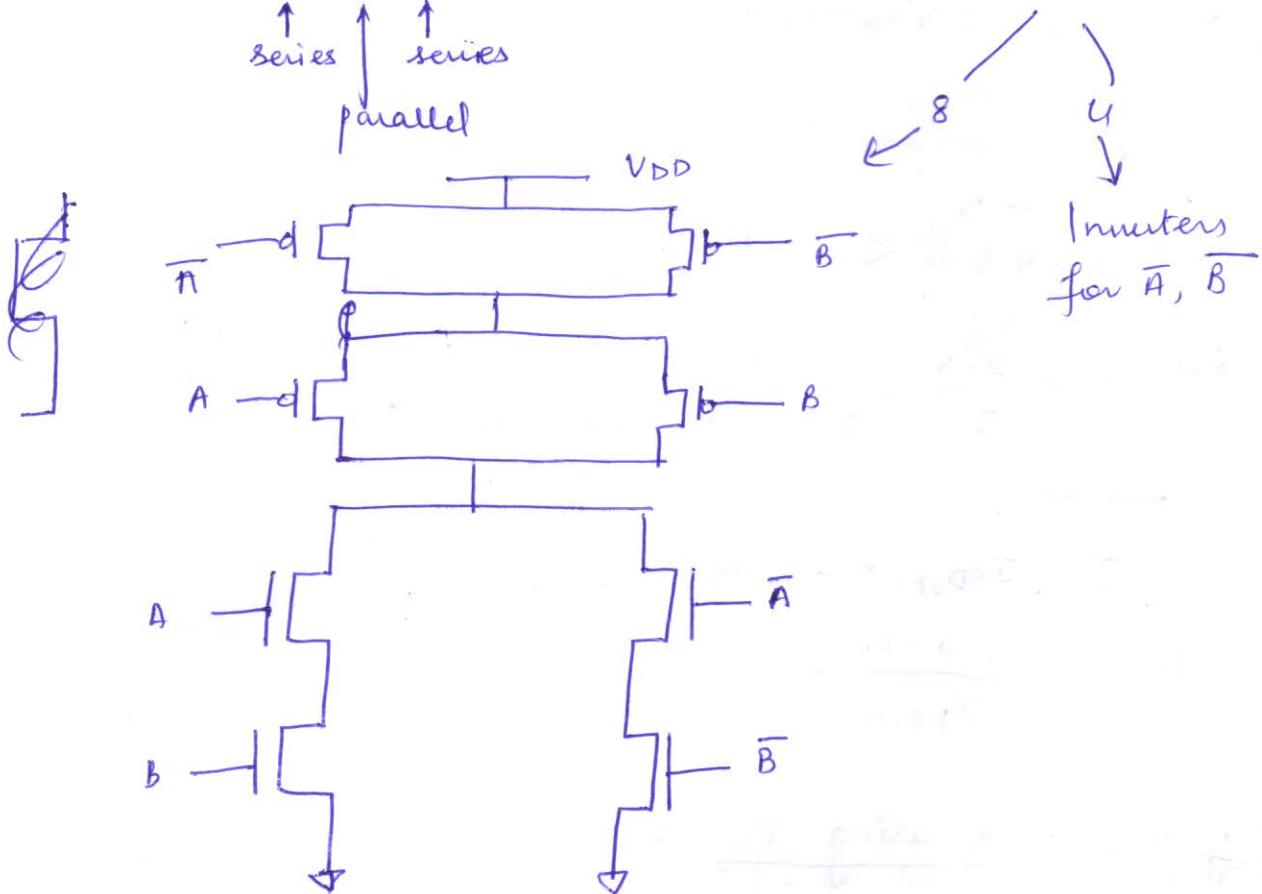
$A \oplus B$

$$Y = AB + \bar{A}\bar{B} \quad \bar{A}\bar{B} + A\bar{B}$$

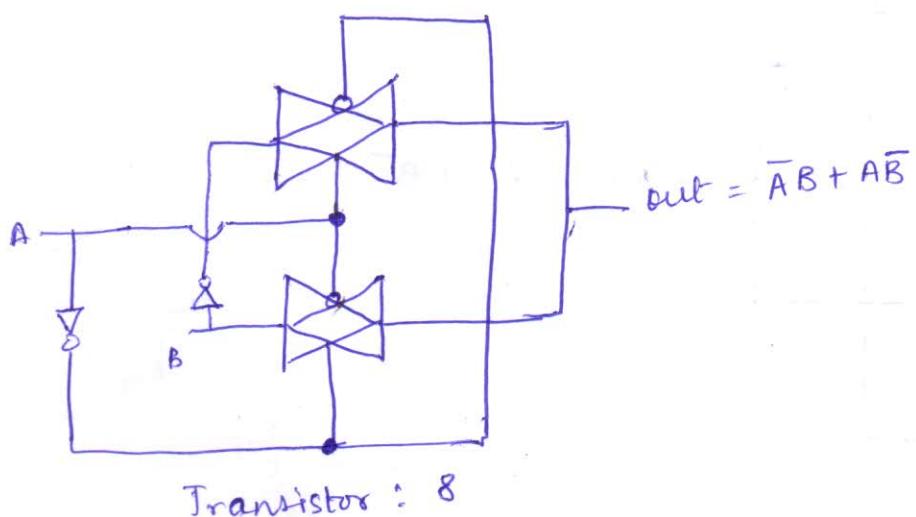
Driver : $Y = AB + \bar{A}\bar{B}$

↑ Series ↑ Series
↑ parallel

Total transistors : 12

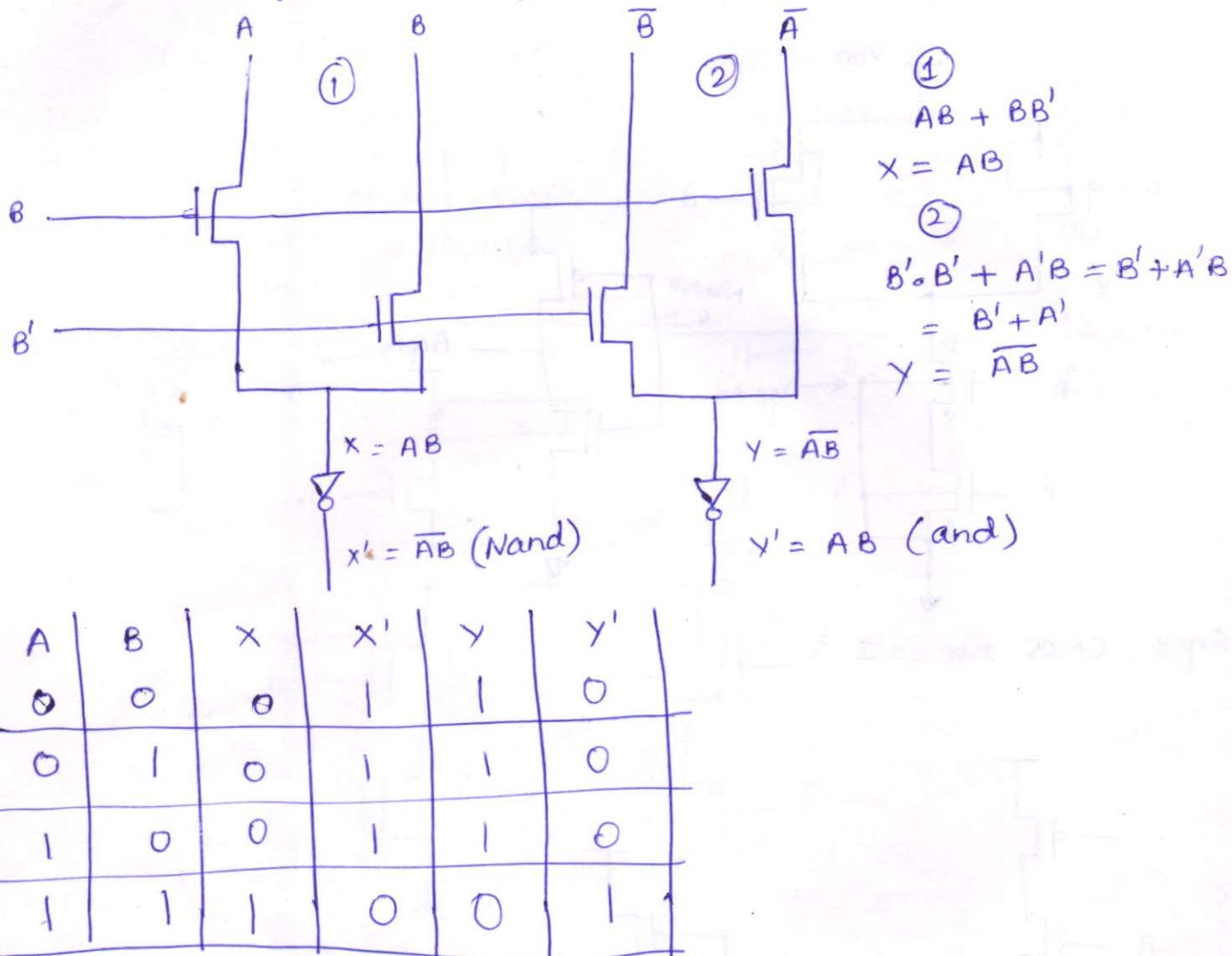


Using TG.



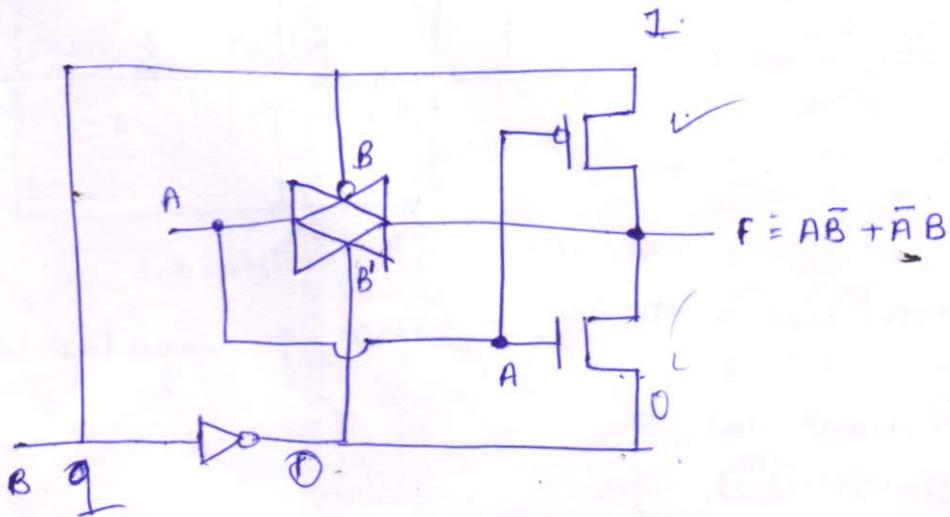
- Advantage of CMOS TG :
- ① passes strong 1's & 0's : ideal switch
 - ② low resistance & independent of O/P
 - ③ less transistors required.

Complementary Pass to logic transistor logic (CPL)



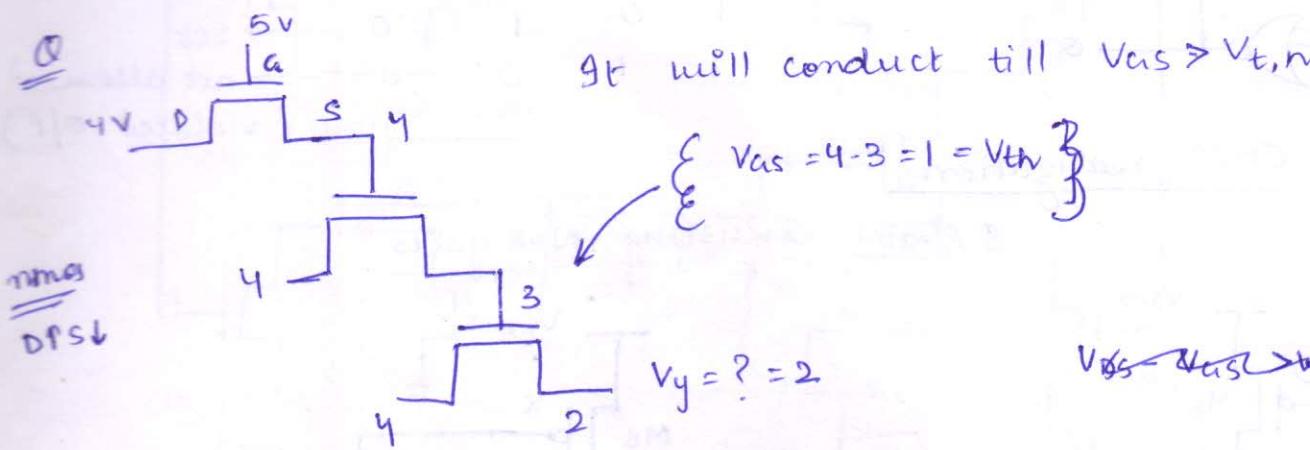
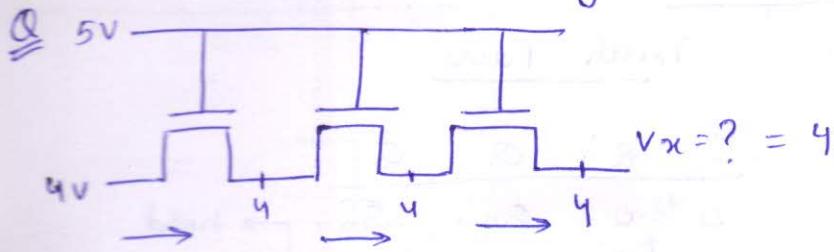
If \bar{B} and B of the gates 1/p are interchanged, the same circuit will give NOR as X' and OR as Y' .

XOR using TA (6 transistors used)

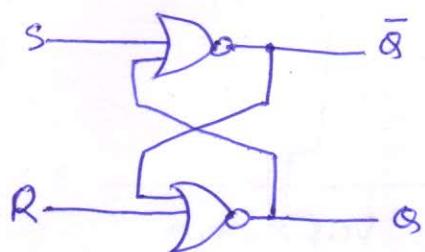


A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

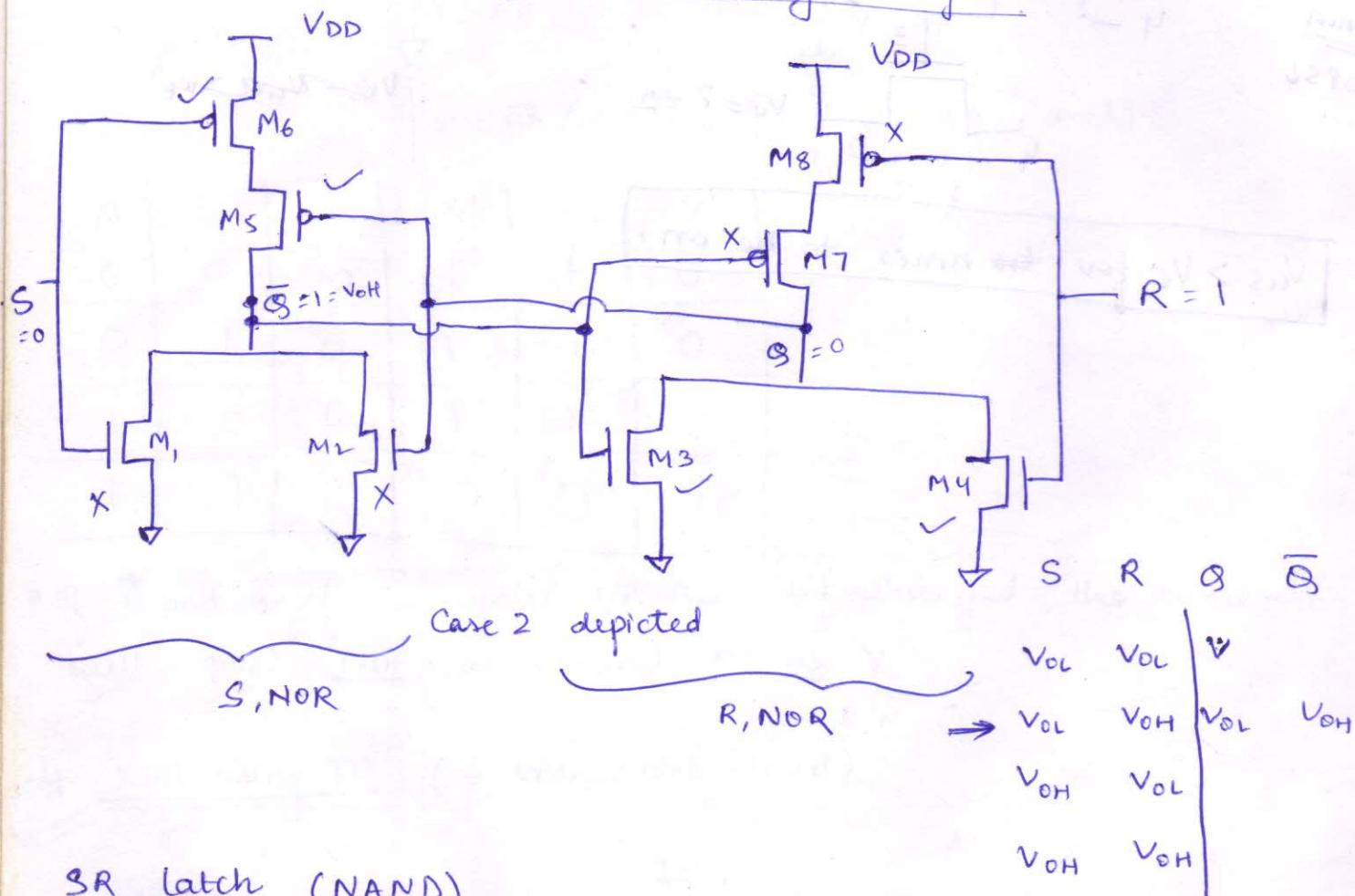
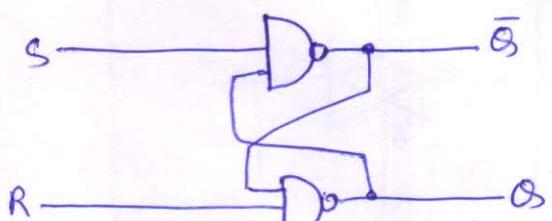
$A\bar{B} + \bar{A}B$



$V_{as} > V_t$ for nmos to be on.

Sequential circuitsSR Latch (NOR)Truth Table

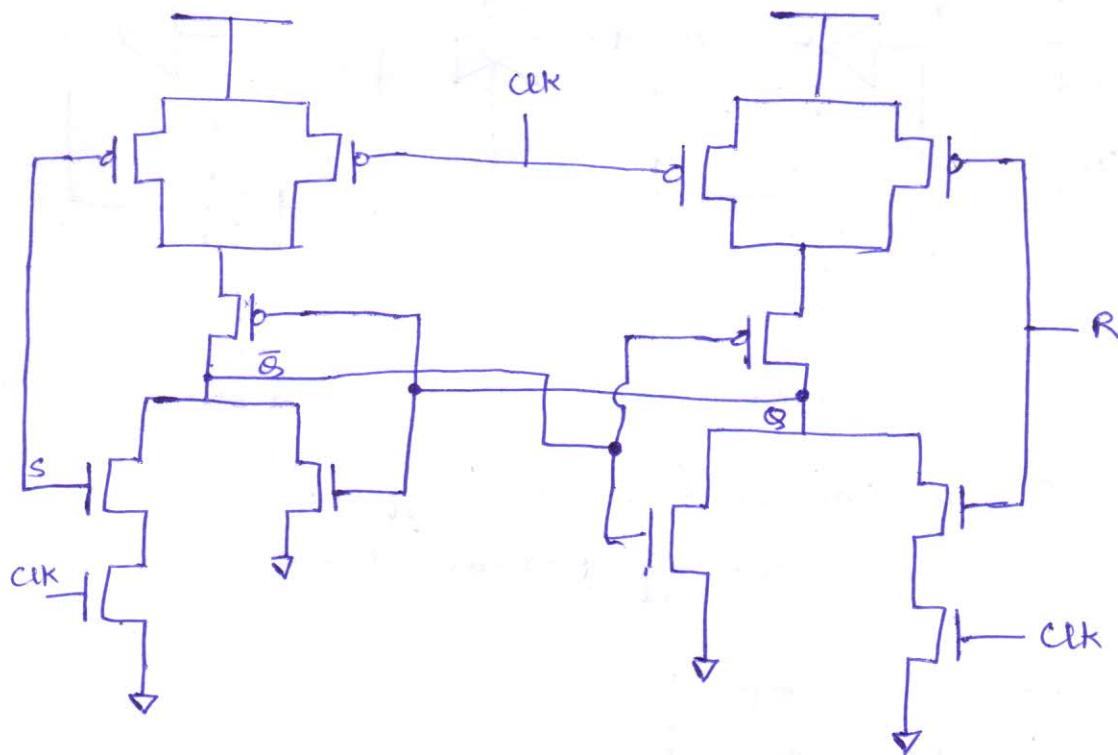
S	R	Q	\bar{Q}	
0	0	Q_{n-1}	\bar{Q}_{n-1}	→ hold
0	1	0	1	→ Reset
1	0	1	0	→ Set
1	1	0	0	→ not allowed (violated O/P)

CMOS realizationS, R latch consisting NOR gatesSR latch (NAND)

S	R	Q	\bar{Q}
0	0	1	1 ← not allowed
0	1	1	0 ← Set
1	0	0	1 ← Reset
1	1	Q_{n-1}	\bar{Q}_{n-1}

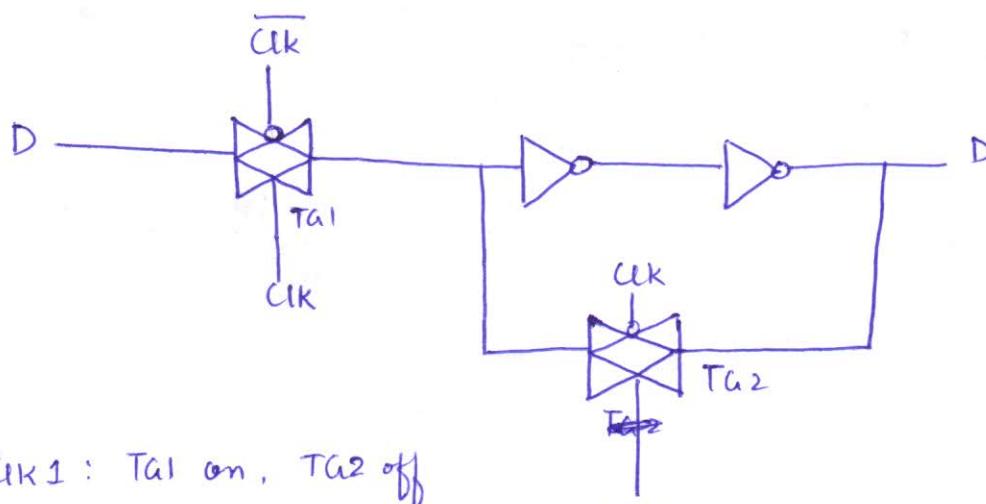
- To make above ckts synchronous, we place 2 'and' gates before S & R I/P in SR(NOR) [Active high] and we place 2 'or' gate before S & R in SR(NAND) [Active low]

CMOS realisation of SR, NOR synchronous



D-Latch

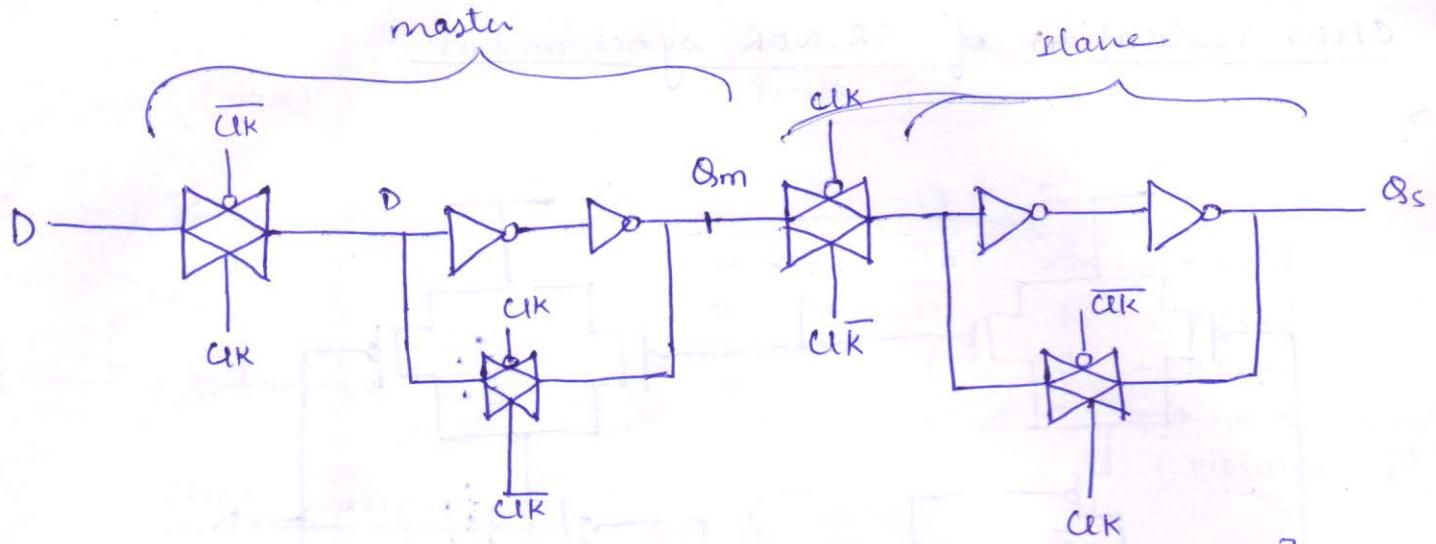
($\text{CLK} = 1 \rightarrow \text{out} = D$
 $\text{CLK} = 0 \rightarrow \text{out} = \text{hold}$)



CLK1 : TG1 on, TG2 off

CLK0 : TG1 off, TG2 on

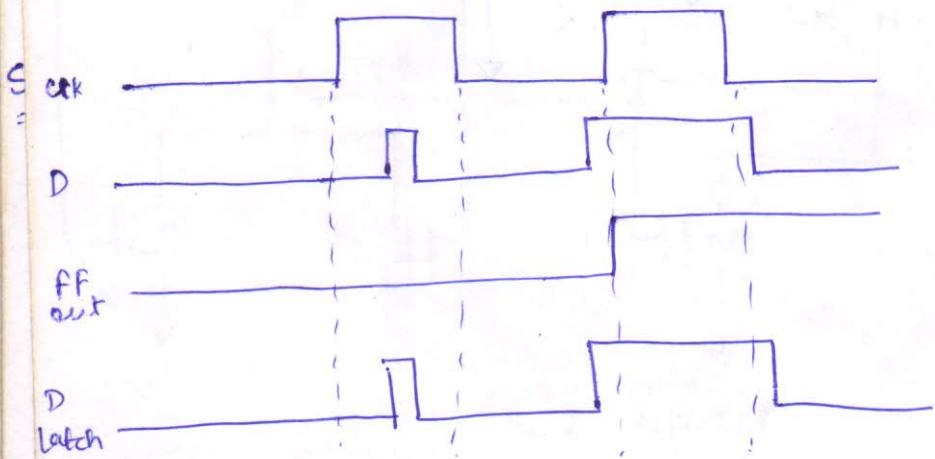
Advantage : no voltage leakage when $D=1$ and $\text{CLK}=0$.



Case 1 [edge triggered, master-slave configuration]

$CK=1$; $Q_m=D$; master on, slave off

$CK=0$; $Q_s = Q_m$; master off, slave on

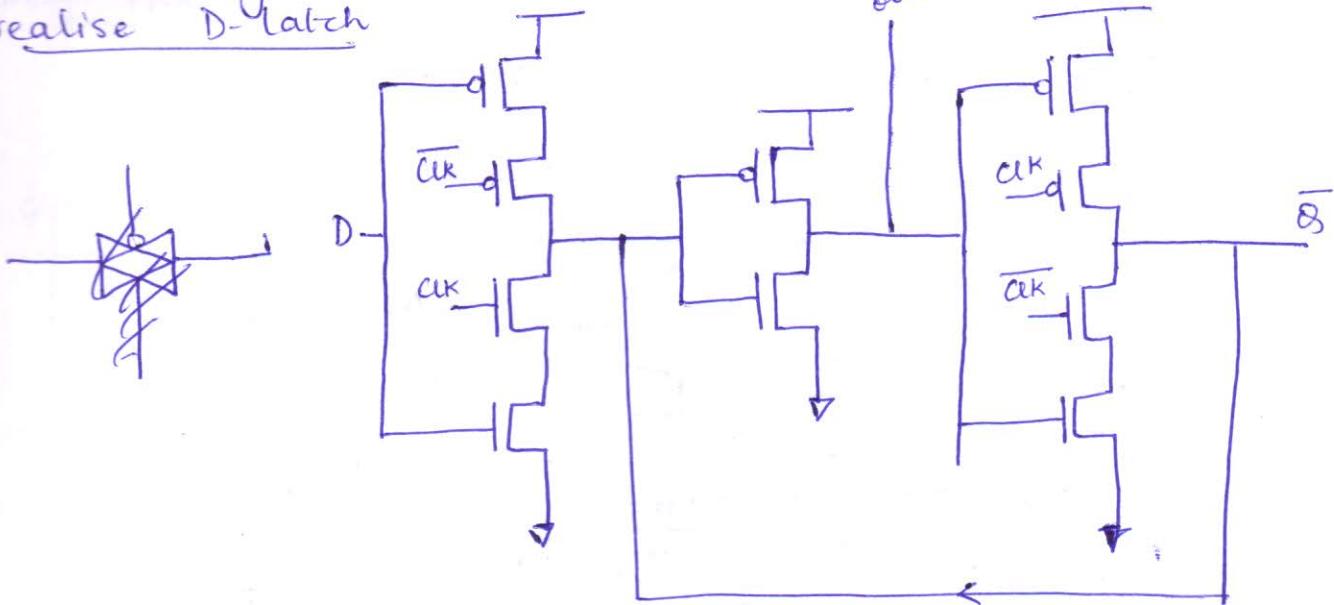


#

18 March 2015

18 March

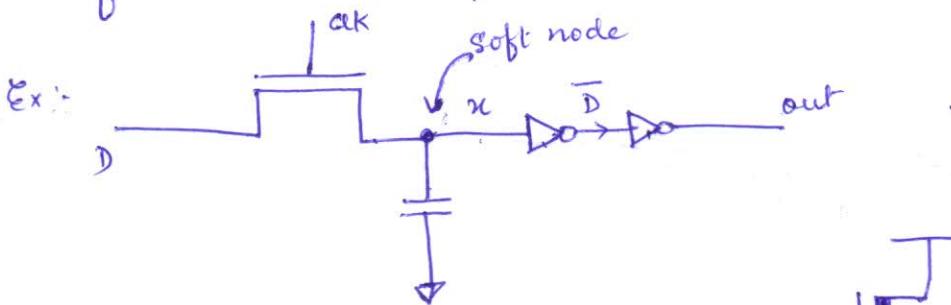
Another way to
realise D-latch



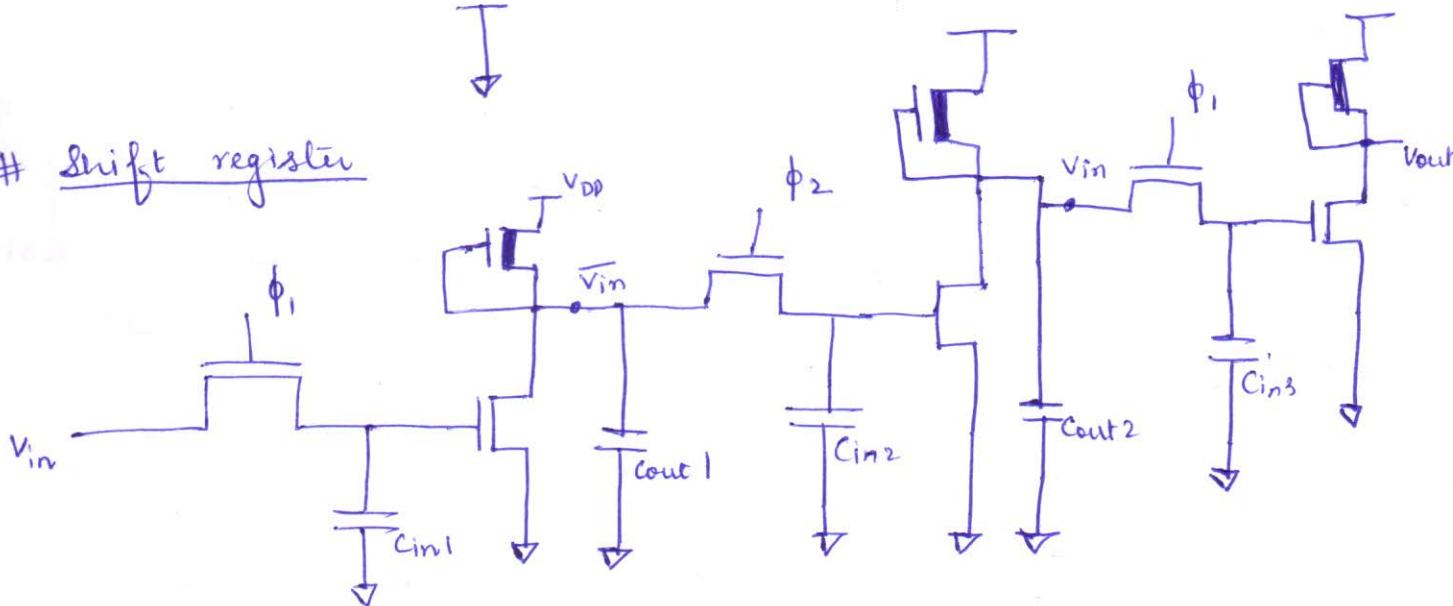
Chapter 9: Dynamic Logic (Kang Ch-9)

O/P depends upon the charge capacity of parasitic capacitor.

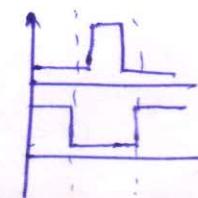
→ No. of transistors required is ~~the~~ less than in static logic.



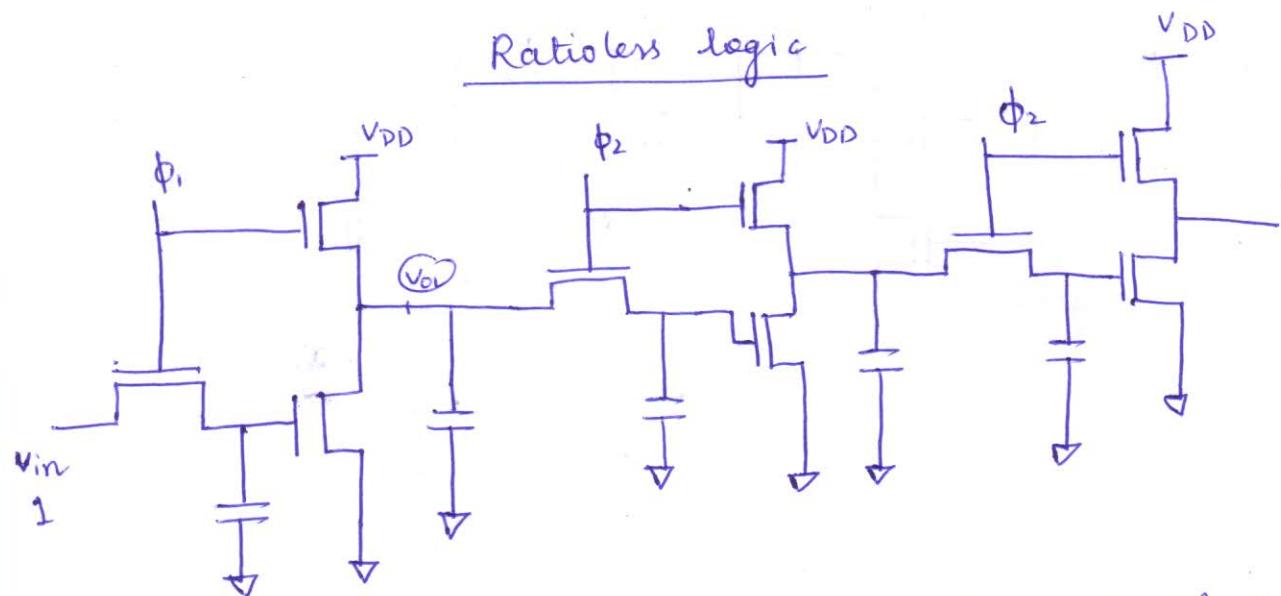
Shift register



where ϕ_1 , and ϕ_2 are non overlapping clock sig



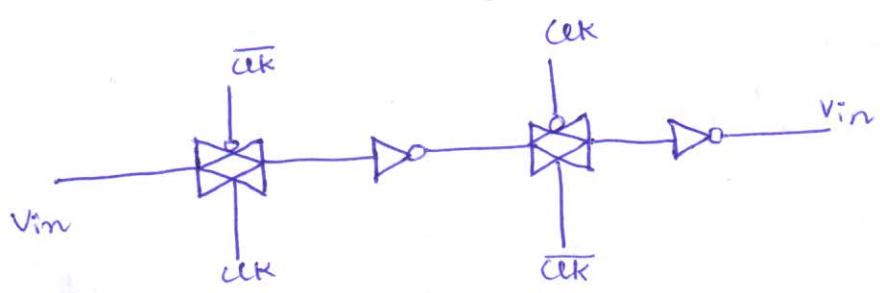
→ we can also use enhancement type load instead of depletion type but it has a disadvantage : can't park strong H_1 , o/p is then ratioed logic.



now V_{OL} is not depending upon the ratio of 2 transistors.

19 March 2015

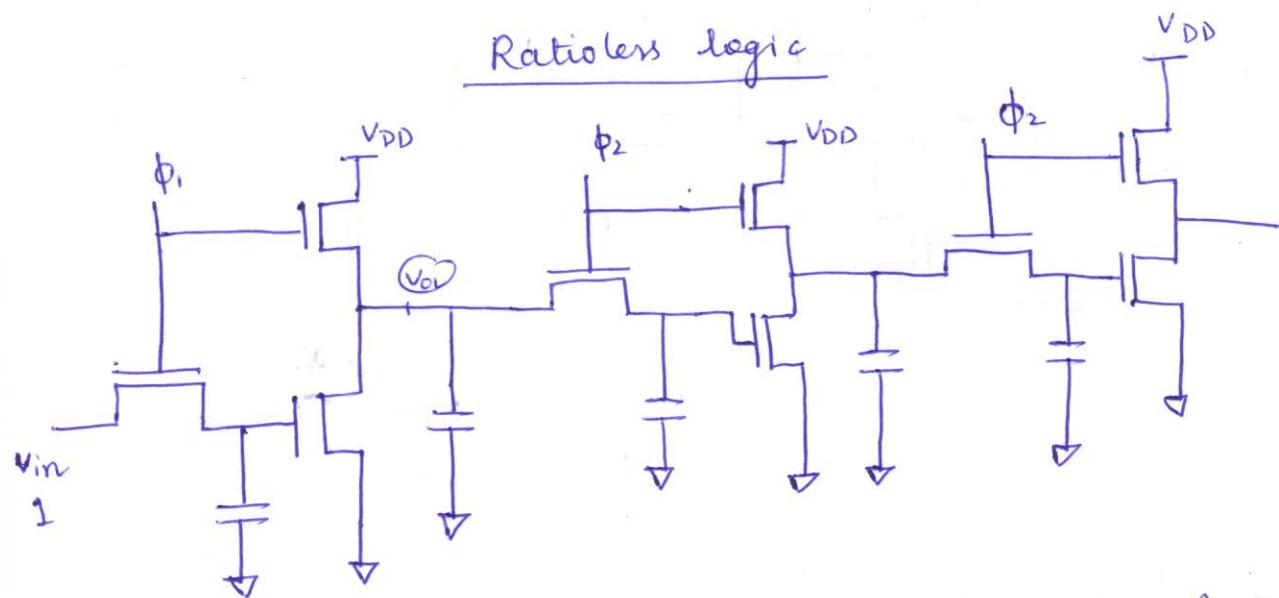
shift register (using TA)



- Advantage :- less resistance, so it passes V_{in} fastly.
- Disadvantage :- clk and $cclk$ overlaps sometime somewhat.



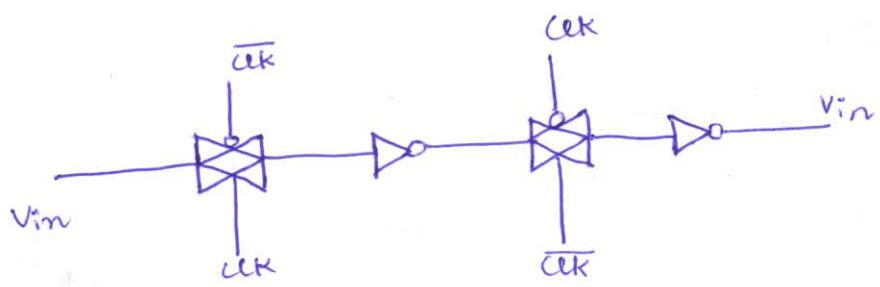
→ we can also use enhancement type load instead of depletion type but it has a disadvantage : can't pack strong O/L , o/p is then ratioed logic.



now V_{OL} is not depending upon the ratio of 2 transistors.

19 March 2015

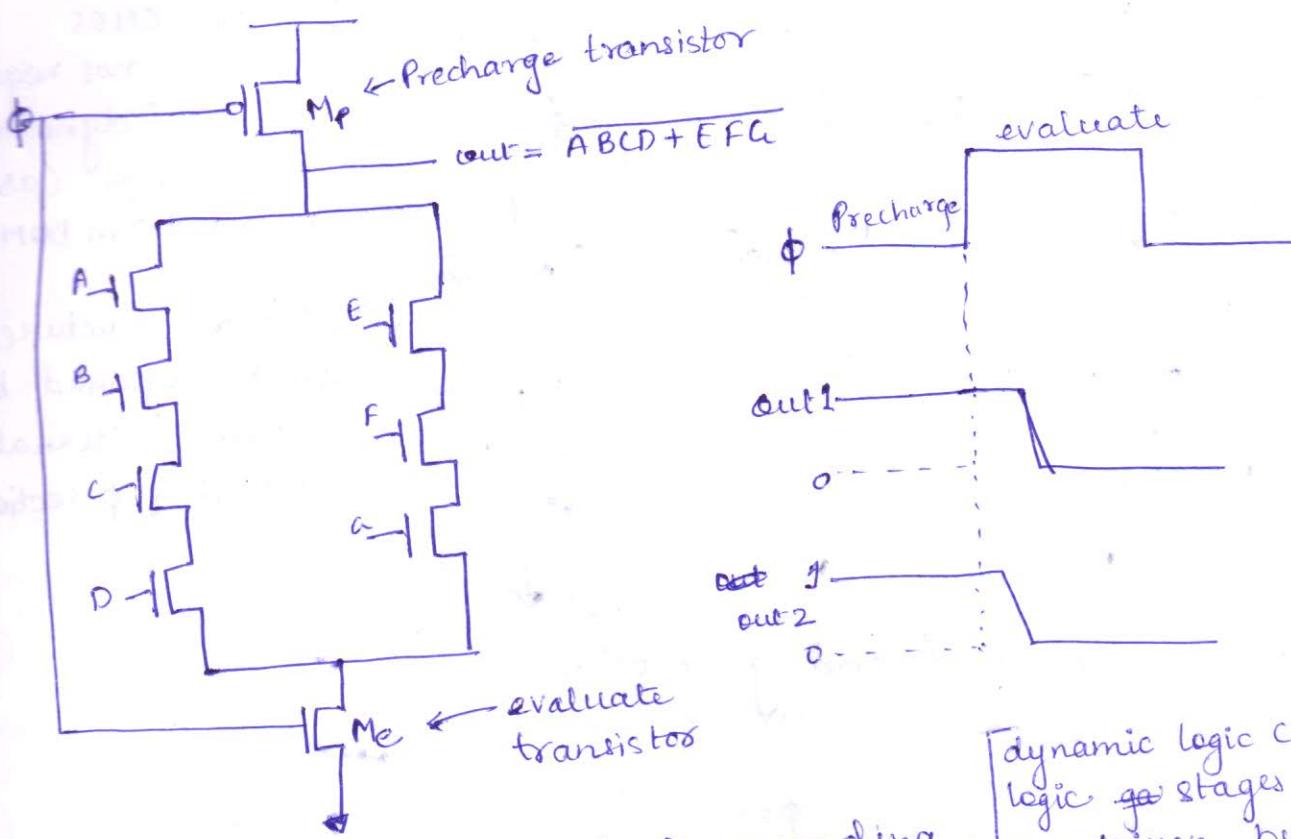
shift register (using TA)



- Advantage :- less resistance, so it passes V_{in} fastly.
- Disadvantage :- CLK and CCLK overlaps sometime somewhat.



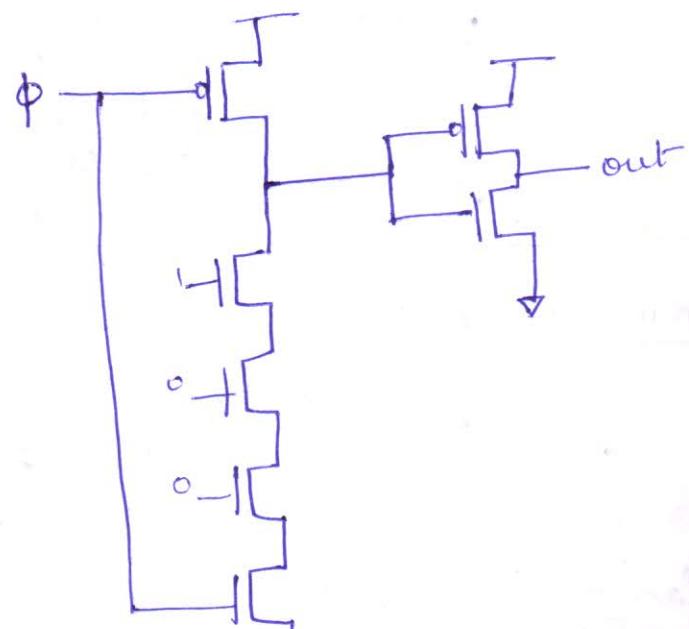
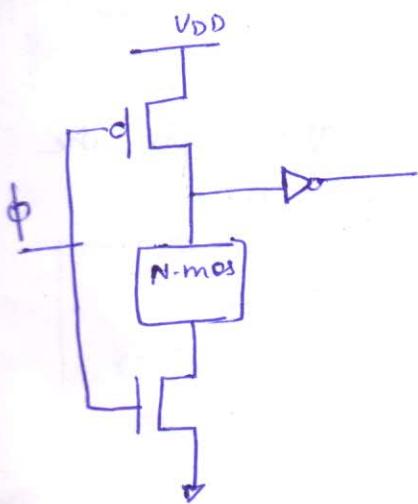
Dynamic CMOS Logic (Precharge Evaluate logic)



• Disadv: \rightarrow It is unable to do cascading.

dynamic logic CMOS logic goes stages which are driven by the same clk, can't be cascaded

Domino logic (Evaluation of 2nd stage place after c/k)

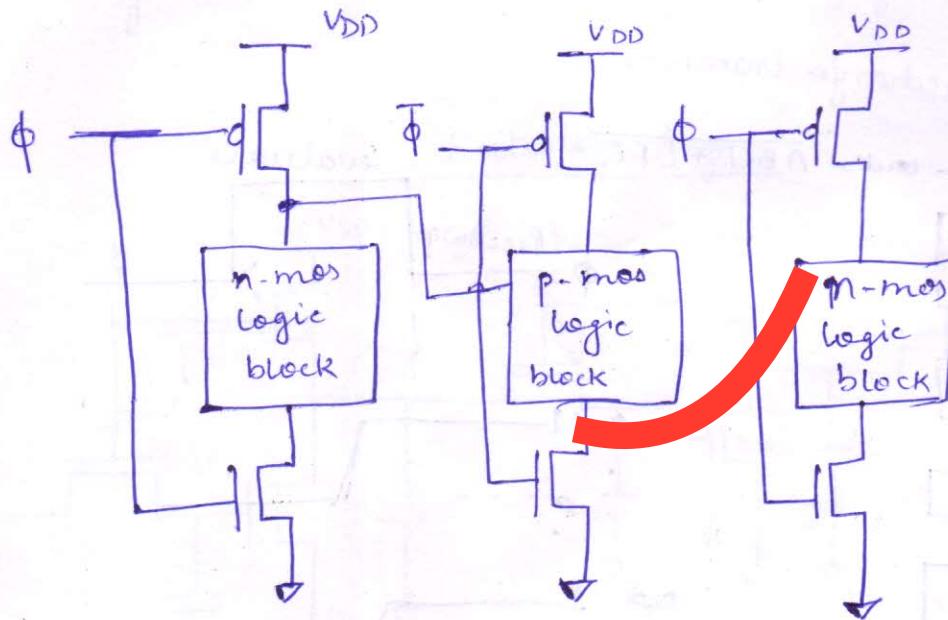


disadv: • It is used to cascade non-inverting blocks only.

• Charge sharing:

Solution:— Use a weak pull-up ~~transistor~~ (pmos)

NORA logic (NP Domino Logic)

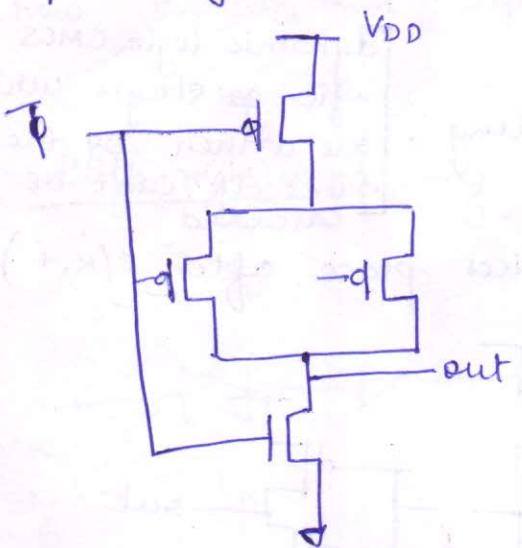


Advantage

① Static CMOS inverter not required at each dynamic O/P stage (as required in DOMINO)

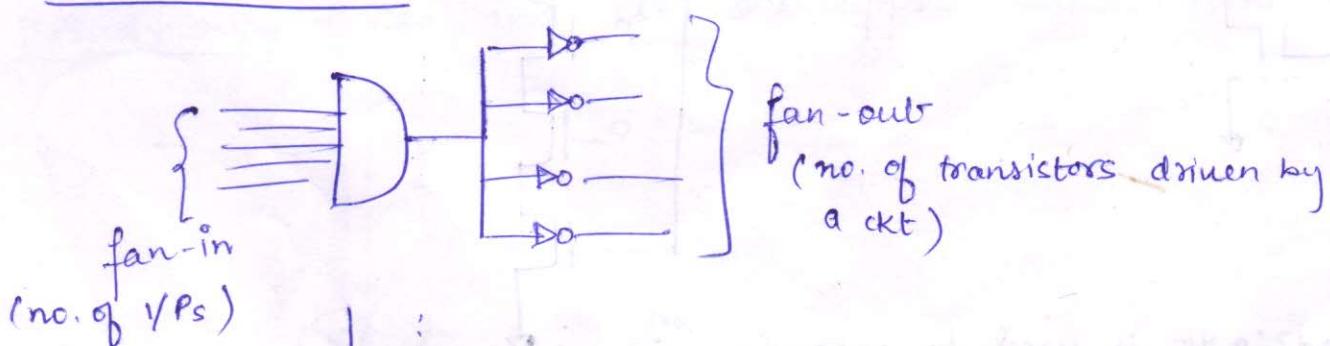
② Pipeline structure can be obtained by cascading alternating ϕ section & $\bar{\phi}$ section

p-mos logic block (nand gate using PMOS)

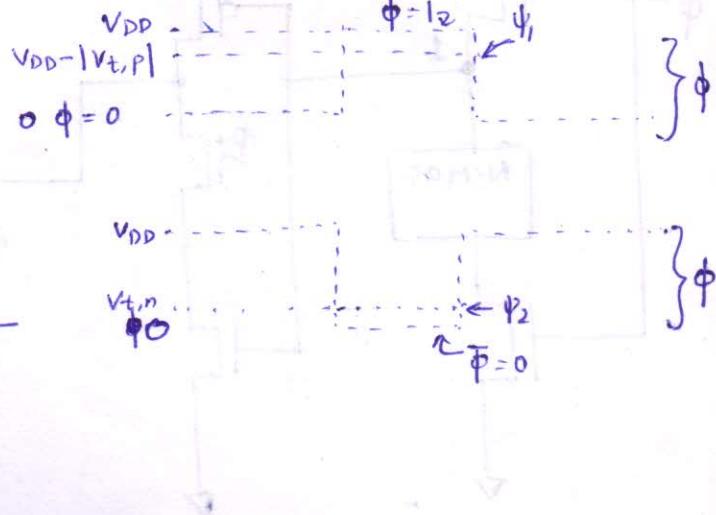
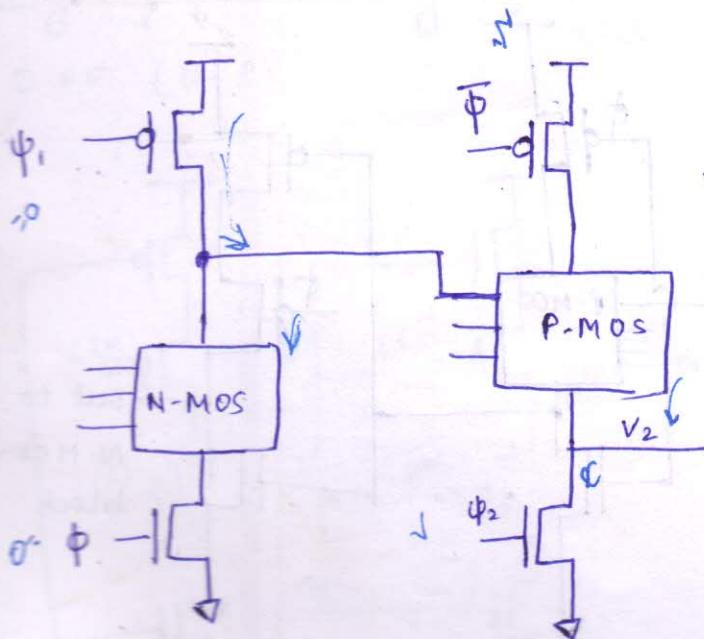


$\phi = 0, \bar{\phi} = 1 \Rightarrow$ out \rightarrow Pre discharge
 $\phi = 1, \bar{\phi} = 0 \Rightarrow$ out \rightarrow
 $\phi = 0, \bar{\phi} = 1$
 \Rightarrow nmos block $\&$ pmos block precharge & predischarge
 $\phi = 1, \bar{\phi} = 0$
 \Rightarrow all stages evaluate one after the other, in a domino fashion.

Fan in - Fan out



Zipper CMOS circuit

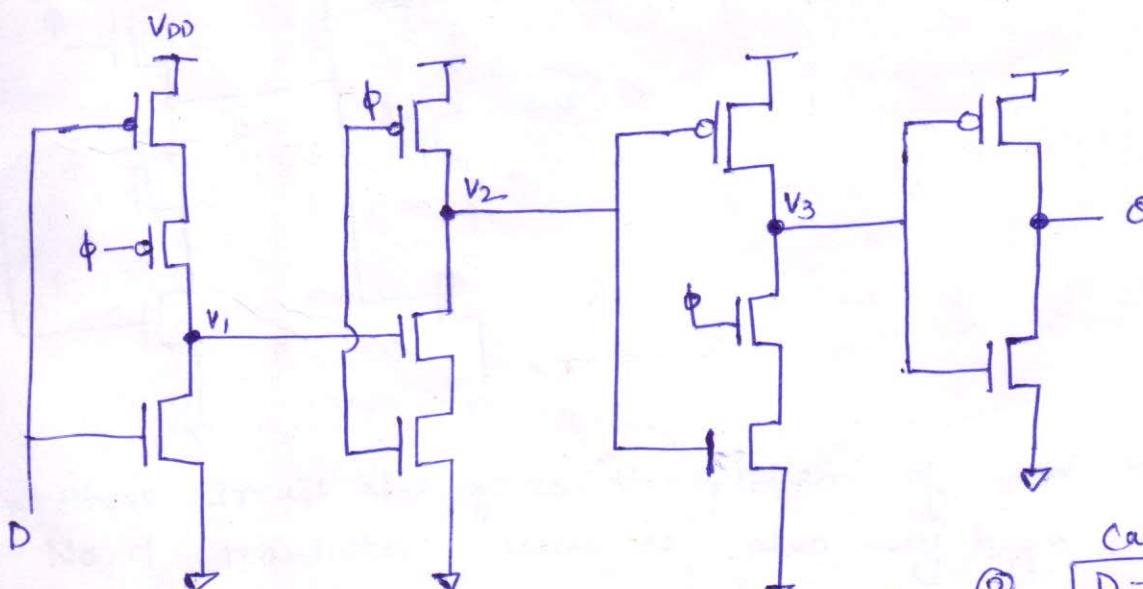


- ① when $\Phi \neq 0, \Phi_1 = 0 \rightarrow$ NMOS \rightarrow Precharging
 $\bar{\Phi} = V_{DD}, \Phi_2 = V_{DD} \rightarrow$ PMOS \rightarrow Predischarging

- ② when $\Phi = 1, \Phi_1 = V_{DD} - |V_{t,P}|$
 $\Phi = 0, \Phi_2 = V_{t,n}$

Cascaded evaluation

* Imp
True single phase clock (TSPC) edge triggered D-FF
[Transistors used = 11]



Cases 1 $D = 1$

① $\Phi = 0$

$\Phi = 1$

V₁

V₂

V₃

Q

②

Case 2
D = 0

②

Case 2
D = 0

V₁

V₂

V₃

Q

V₁

V₂

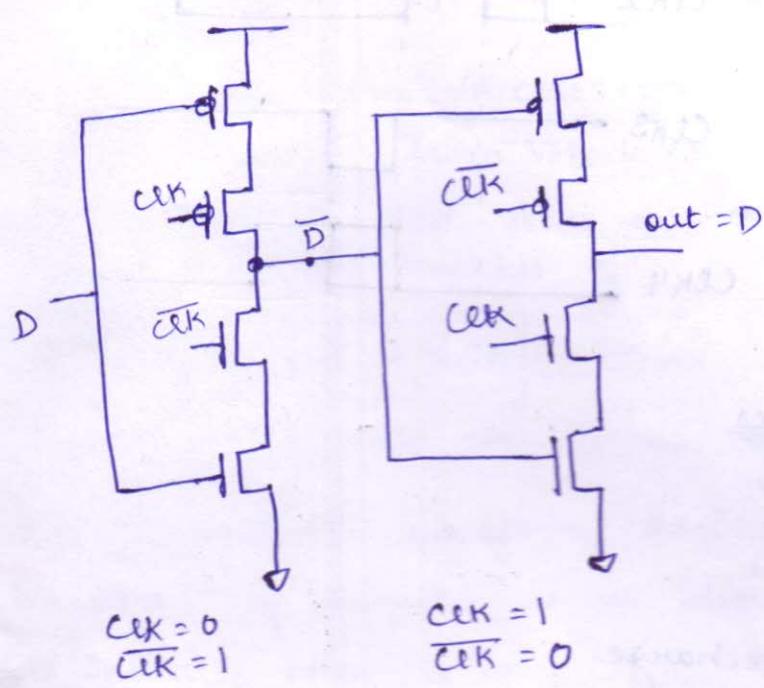
V₃

Q

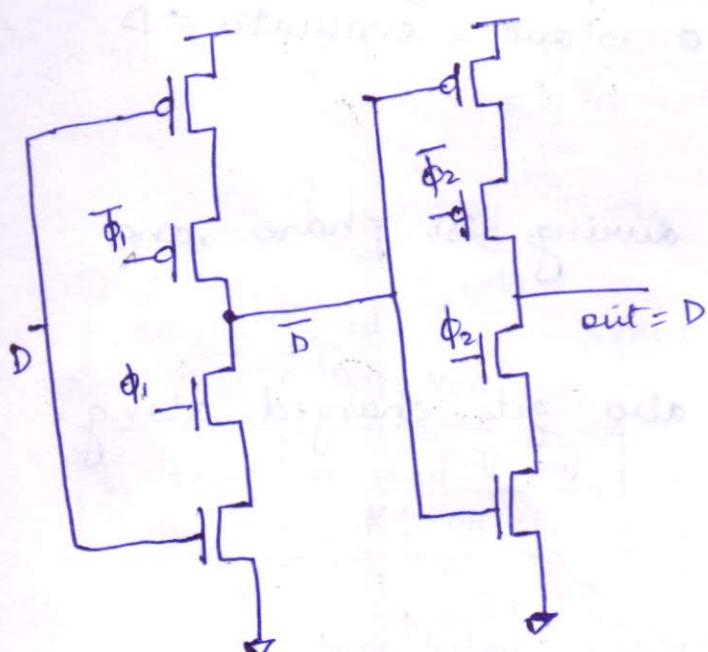
23 April

Single phase clocking

D-FF (0-1)

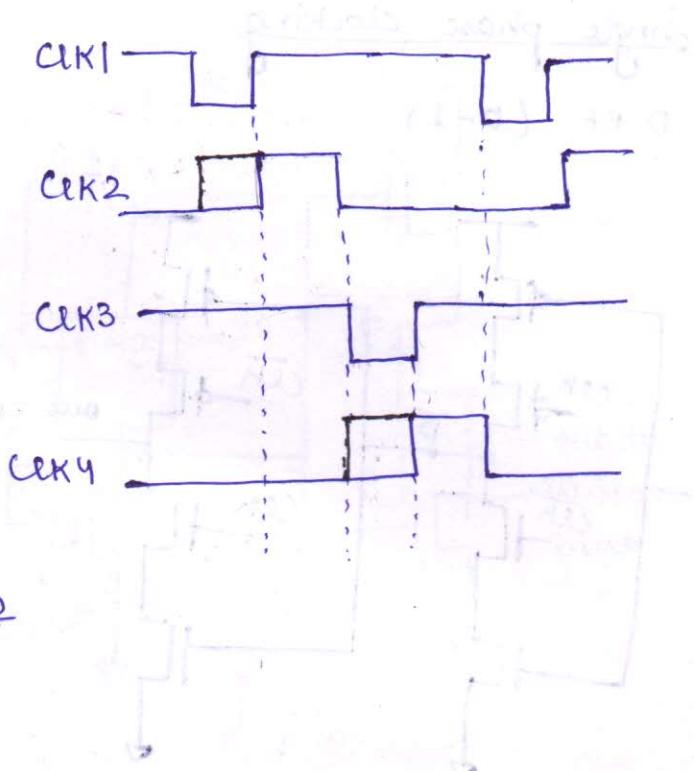
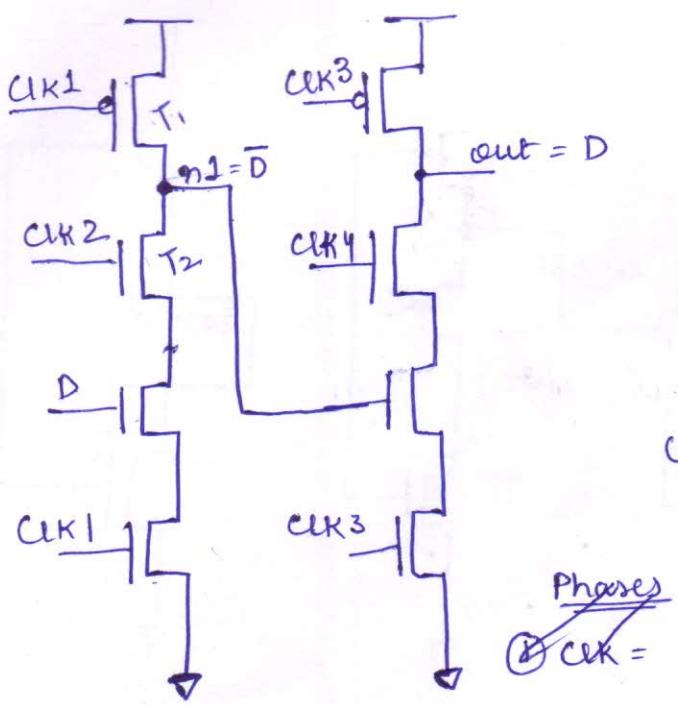


Two-phase clocking



- Above circuit also faces the problem of clock skew.
- No. of transistors used is also very high : 12.
- To overcome above disadvantage we use 4-phase clocking.

Four Phase Clocking



Phases

- ① $\text{CK}_1 = 0, \text{CK}_2 = 0 \Rightarrow n_1 = \text{precharge}$
- ② $\text{CK}_2 = 1, \text{CK}_1 = 1 \Rightarrow n_1 = \text{evaluation } (\bar{D})$
- ③ $\text{CK}_3 = 0, \text{CK}_1 = 1, \text{CK}_2 = 0, \text{out} = \text{precharge}$
- ④ $\text{CK}_3 = \text{CK}_4 = 1, \text{CK}_1 = 1, \text{CK}_2 = 0 \Rightarrow \text{out} = \text{evaluate } = D$

Drawback: charge sharing

Solution: To keep $\text{CK}_1 = \text{CK}_2 = 1$ during 1st phase, and similarly $\text{CK}_3 = 0, \text{CK}_4 = 1$.

so during precharge phase T_2 also gets charged along with T_1 .

Calculation of Delay Time (T_{PHL}) for CMOS inverter

Delay Time can be obtained by solving the state eqⁿ of the O/P node in the time domain

$$C_{load} \frac{dV_{out}}{dt} = i_{D,P} - i_{D,n} \quad (\text{fig 1})$$

Consider the rising I/P case: ~~case~~
as V_{in} switches from V_{OL} to V_{OH}
nMOS turns on and start discharging and pMOS switches off

$$\Rightarrow C_{load} \frac{dV_{out}}{dt} = -i_{D,n} \quad \text{--- ①}$$

and the equivalent circuit is as shown in fig 2

The I/P and O/P waveform during this high-to-low transition of Output is as shown in fig 3.

(1) Initially nmos is in saturation,

$$i_{D,n} = \frac{K}{2} (V_{DS} - V_{T,n})^2$$

$$= \frac{K}{2} (V_{OH} - V_{T,n})^2$$

$$\text{for } V_{OH} - V_{T,n} < V_{out} < V_{OH}$$

Using eq ① finding $t'_1 - t_0$

$$\int_{t_0}^{t'_1} dt = - \frac{C_{load}}{i_{D,n}} \int_{V_{OH}}^{V_{OH} - V_{T,n}} \frac{dV_{out}}{V_{OH}}$$

$$\Rightarrow t'_1 - t_0 = \frac{2C_{load} V_{T,n}}{K (V_{OH} - V_{T,n})^2} \quad \text{--- eq ②}$$

(2) When O/P drops below $V_{OH} - V_{T,n}$ ~~then~~ nMOS Starts working in linear region

$$i_{D,n} = \frac{K}{2} [2(V_{DS} - V_{T,n}) V_{DS} - V_{DS}^2]$$

$$i_{D,n} = \frac{K}{2} [2(V_{OH} - V_{T,n}) V_{out} - V_{out}^2]$$

$$\star V_{out} < V_{OH} - V_{T,n}$$

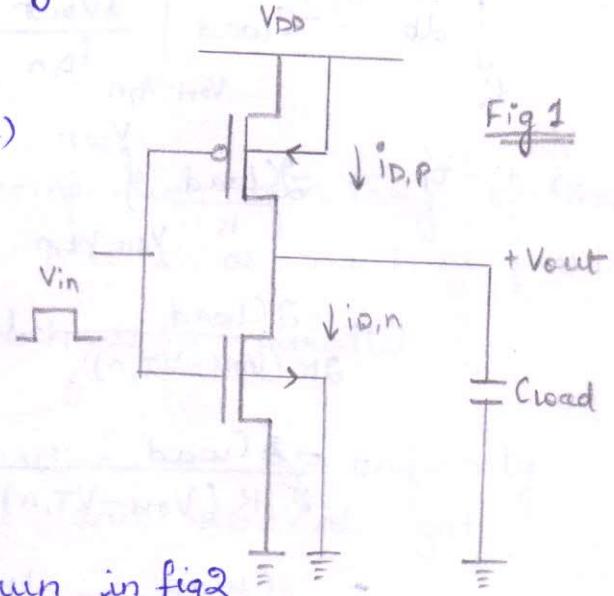


Fig 1

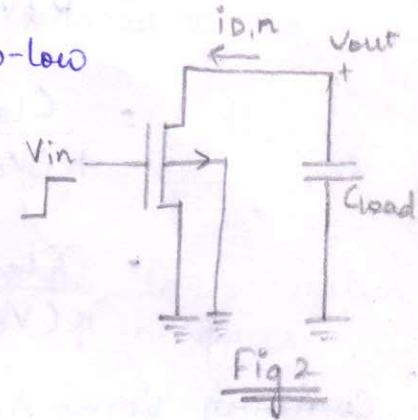


Fig 2

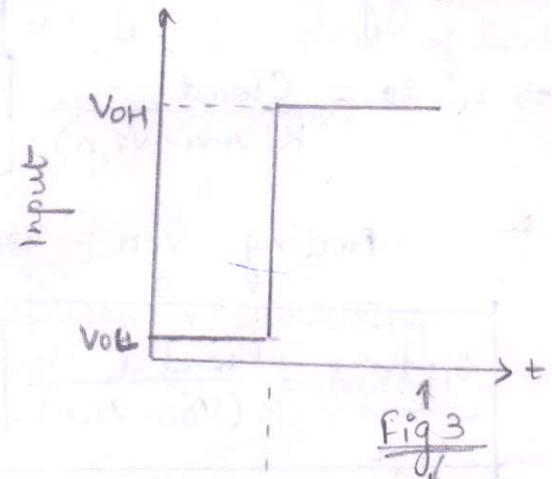
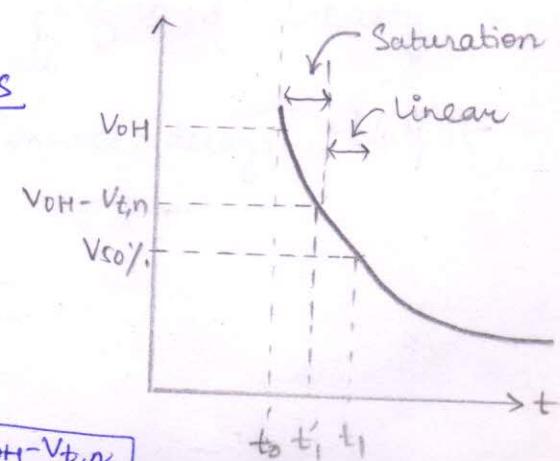


Fig 3



using eq 1 to find out $t_1 - t'$

$$\int_{t'}^{t_1} dt = -C_{load} \int_{V_{OH}-V_{T,n}}^{V_{SO}\%} \frac{dV_{out}}{i_{D,n}}$$

$$\Rightarrow t_1 - t' = \frac{-2C_{load}}{K} \int_{V_{OH}-V_{T,n}}^{V_{SO}\%} \frac{dV_{out}}{[2(V_{OH}-V_{T,n})V_{out} - V_{out}^2]}$$

$$= \frac{-2C_{load}}{2K(V_{OH}-V_{T,n})} \ln \left[\frac{V_{out}}{2(V_{OH}-V_{T,n}) - V_{out}} \right]_{V_{OH}-V_{T,n}}^{V_{SO}\%}$$

$$= \frac{-2C_{load}}{K(V_{OH}-V_{T,n})} \ln \left[\frac{V_{SO}\%}{2(V_{OH}-V_{T,n}) - V_{SO}\%} \right]$$

$$= \frac{C_{load}}{K(V_{OH}-V_{T,n})} \ln \left[\frac{2(V_{OH}-V_{T,n}) - V_{SO}\%}{V_{SO}\%} \right]$$

$$= \frac{C_{load}}{K(V_{OH}-V_{T,n})} \ln \left[\frac{2(V_{OH}-V_{T,n})}{V_{SO}\%} - 1 \right]$$

$$= \frac{C_{load}}{K(V_{OH}-V_{T,n})} \ln \left[\frac{4(V_{OH}-V_{T,n})}{(V_{OH}+V_{OL})} - 1 \right] \quad \text{--- eq ③}$$

Combining eq ② + eq ③ to get $t_1 - t_0$

$$\Rightarrow t_1 - t_0 = \frac{C_{load}}{K(V_{OH}-V_{T,n})} \left[\ln \left(\frac{4(V_{OH}-V_{T,n})}{(V_{OH}+V_{OL})} - 1 \right) + \frac{2V_{T,n}}{V_{OH}-V_{T,n}} \right]$$

Putting $V_{OH} = V_{DD}$ and $V_{OL} = 0$

$$\boxed{t_1 - t_0 = \frac{C_{load}}{K(V_{DD}-V_{T,n})} \left[\ln \left(\frac{4(V_{DD}-V_{T,n})}{V_{DD}} - 1 \right) + \frac{2V_{T,n}}{V_{DD}-V_{T,n}} \right]}$$

Concept of Regularity, Modularity and Locality

→ These concepts are required to be used to simplify a hierarchical design.

Regularity

- It means that the hierarchical decomposition of a large system should in simple and similar blocks as much as possible.
- Ex:- design of array structures such as a parallel multiplication array.
- It can exist at any level of abstraction. For ex:- uniformly sized transistors at transistor level and identical gate structures at gate level.
- It reduces the no. of different modules that need to be designed and verified.

Modularity

- It means that various blocks which makes up the large system must have clear and well-defined functions & interfaces.
- So, that each block may be designed independently of each other since there is no ambiguity about functions of each.
- It enables the parallelisation of the design process.

Locality

- It ensures that the connections are between neighbouring blocks/modules, avoiding the need of long distance connections as much as possible.
- Time-critical operations should be performed locally, without the need of distant signals.
- It is important to avoid long interconnect delays.

VLSI Design Styles

Gate Array Design (metal mask design and processing is used).

→ It has two steps manufacturing:

① first phase is based on generic masks (standard masks).

It results in an array of uncommitted transistors on each GA chip.

② Second phase is the customization, which is done by defining the metal interconnects between the transistors of the array.

→ It has a turn around time of a few days to few weeks.

→ GA ~~platforms~~ allow dedicated areas called channels for intercell routing b/w rows and columns of MOS transistors.

The availability of these routing channels simplify the interconnections.

→ Interconnection patterns can be stored in a library, which can later be used.

→ Chip utilization factor (used chip area divided by total chip area) is higher than FPCB; high chip speed.

Standard Cell Based Design

→ It requires development of a full custom mask set.

→ All of the commonly used logic cells are developed, characterised and stored in a Standard Cell library. A typical library may contain few hundreds cells such as : inverter, flip-flop, adder, latch etc.

→ The power and ground rails typically run parallel to the upper and ~~lower~~ lower boundaries of the cell.

→ Generally N-MOS transistors are located close to the ground rail and P-MOS transistors are located close to the power rail.

→ If a no. of cells must share the same I/P and/or O/P, sigs, a common sig must ~~be~~ can be incorporated into standard cells based chip layout.

Measurement of MOSFET parameters

→ Model parameters to be measured :

- Transconductance parameters : K_p, K_n
- Zero bias threshold voltage : V_{TO}
- Channel length mod. coefficient: λ
- Substrate bias coefficient : γ

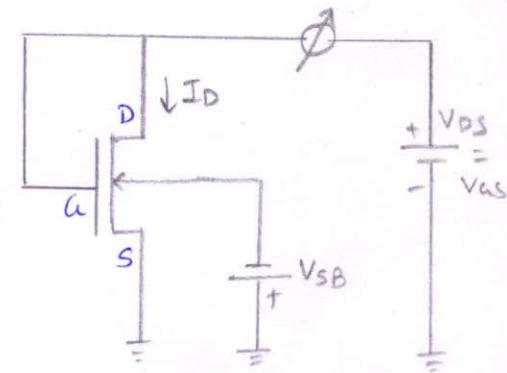
① Consider Setup 1

- $V_{SB} = \text{constant}$ and I_D is measured for different values of V_{AS}
- Since $V_{DS} = V_{AS}$, nMOS operates in saturation

$$I_D(\text{sat}) = \frac{K_n}{2} (V_{AS} - V_{TO})^2$$

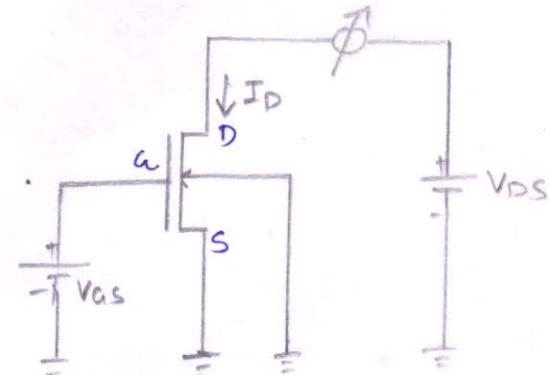
$$\Rightarrow \sqrt{I_D} = \sqrt{\frac{K_n}{2}} (V_{AS} - V_{TO})$$

- If now $\sqrt{I_D}$ is plotted against V_{AS} , slope will give $\sqrt{\frac{K_n}{2}}$ and Voltage-axis intercept of resulting curve will give V_{TO} and γ .
 → V_{FO} will be given by the extrapolation of $V_{SB}=0$ curve.
 → γ will be calculated by $\gamma = \frac{V_T(V_{SB}) - V_{TO}}{\sqrt{2\phi_F + V_{SB}}} - \sqrt{2\phi_F}$



② Consider setup 2

- V_{AS} is kept $V_{TO} + 1$.
- V_{DS} is chosen sufficiently large ($V_{DS} > V_{AS} - V_{TO}$) so that nMOS operates in saturation.
- I_D is measured for two diff V_{DS} values : $V_{DS1} \neq V_{DS2}$



$$I_D(\text{sat}) = \frac{K_n}{2} (V_{AS} - V_{TO})^2 (1 + \lambda V_{DS})$$

$$\Rightarrow \frac{I_{D1}}{I_{D2}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}$$

This relation can be used to calculate the value of λ .