

**Ans. (i) Variable threshold CMOS circuit**

One of the efficient methods to reduce power consumption is to use low supply voltage and low threshold voltage without losing speed performance. But increase in the lower threshold voltage devices leads to increased sub-threshold leakage and hence more standby power consumption.

**Variable Threshold CMOS (VTCMOS)** devices are one solution to this problem. In VTCMOS technique threshold voltage of the low threshold devices are varied by applying variable substrate bias voltage from a control circuitry. VTCMOS technique is very effective technique to reduce the power consumption with some drawbacks related to manufacturing of these devices. VTCMOS requires either twin well or triple well technology to achieve different substrate bias voltage levels at different parts of the IC.

**(ii) Multi-threshold CMOS (MTCMOS)** is a variation of CMOS chip technology which has transistors with multiple threshold voltages ( $V_{th}$ ) in order to optimize delay or power. The  $V_{th}$  of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Low  $V_{th}$  devices switch faster, and are therefore useful on critical delay paths to minimize clock period. The penalty is that low  $V_{th}$  devices have substantially higher static leakage power. High  $V_{th}$  devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high  $V_{th}$  devices reduce static leakage by 10 times compared with low  $V_{th}$  devices.

One method of creating devices with multiple threshold voltages is to apply different bias voltages ( $V_b$ ) to the base or bulk terminal of the transistors. Other methods involve dopant concentration in the channel region beneath the gate oxide. A common method of fabricating multi-threshold CMOS involves simply adding additional photolithography and ion implantation steps. For a given fabrication process, the  $V_{th}$  is adjusted by altering the concentration of dopant atoms in the channel region beneath the gate oxide.

**Q. 9. Short note:**

(a) **MOSFET Scaling.**

**Ans. MOSFET SCALING**

- Reduction in size of an MOS chip by reducing the dimensions of MOSFETs and interconnects.

• Reduction is symmetric and preserves geometric ratios which are important to the functioning of the chip. Ideally, allows design reuse.

• Assume that  $S$  is the scaling factor. Then a transistor with original dimensions of  $L$  and  $W$  becomes a transistor with dimensions  $L/S$  and  $W/S$ .

Typical values of  $S$ : 1.4 to 1.5 per biennium.

**Two major forms of scaling**

- Full scaling (constant-field scaling)** – All dimensions are scaled by  $S$  and the supply voltage and other voltages are so scaled.
- Constant-voltage scaling** – The voltages are not scaled and, in some cases, dimensions associated with voltage are not scaled.

Year Channel

Year	Channel
1980	5.00 $\mu$
1998	0.25 $\mu$
2000	0.18 $\mu$
2002	0.13 $\mu$
2003	0.09 $\mu$

**Q. 9. (b) Concept of regularity, Modularity and Locality.**

**Ans. Refer Q.1. (c) of End Term Examination 2017.**

## FIRST TERM EXAMINATION [FEB. 2019]

### SIXTH SEMESTER [B.TECH]

### VLSI DESIGN [ETEC-308]

**M.M. : 30**

**Time : 1.30 hrs.**

**Note :- Attempt Q. No. 1 which is compulsory and any two more questions from remaining.**

**Q.1. (a) What do you understand by pseudo nMOS logic?**

**Ans.** The inverter that uses a p-device pull-up or load that has its gate permanently grounded. An n-device pull-down or driver is NMOS technology and is thus called 'pseudo-pMOS'. The circuit is used in a variety of CMOS logic circuits. In this, PMOS for most of equivalent to use of a depletion load is NMOS technology and is thus called 'pseudo-pMOS'. The circuit is used in a variety of CMOS logic circuits. In this, PMOS for most of the time will be linear region. So resistance is low and hence RC time constant is low.

**Q.1. (b) Draw the layout of CMOS inverter.**

**Ans.** Refer question no.1.(b) of End Term 2018. (Page No. 7-2018)

**Q.1. (c) Discuss the latch-up problem in contrast to CMOS inverter.**

**Ans.** A latch-up is a type of short circuit which can occur in an integrated circuit (IC). More specifically it is the inadvertent creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disrupts proper functioning of the part, possibly even leading to its destruction due to overcurrent. A power cycle is required to correct this situation.

**Q.1. (d) Derive the expression of dynamic power dissipation of a CMOS inverter.**

**Ans.** On many integrated circuits, several thousand gates exist and hence this power dissipation can be large. It is for this reason that the input voltage to a CMOS circuit must not be held at  $V_{dd}/2$ . When the inputs are switching the power dissipated is called dynamic power dissipation. However, as long as the input signals have a fast rise and fall time then this form of dynamic power dissipation is called dynamic power dissipation of MOS?

**Q.1. (e) What are the narrow channel effects in MOS?**

**Ans.** The main cause of dynamic power dissipation, however, in a CMOS circuit is due to the charge and discharge of capacitance at each gate output. The dynamic power dissipation of a CMOS gate is therefore dependent upon the number of times a capacitor is charged and discharged. Hence as the frequency of switching increases so the dynamic power dissipation increases. The dynamic power dissipation for a CMOS gate is equal to

$$P_{dynamic} = C_L \times V_{DD}^2 \times f$$

**Q.2. (a) Design the schematic of nMOS load inverter and explain its working with the help of VTC. Mark all important points on VTC and discuss the mode of operation of driver and load at each point.**

**Ans. Depletion-load nMOS inverter:** The circuit diagram of the depletion-load inverter circuit is shown in Fig. (a), and a simplified view of the circuit consisting of a nonlinear load resistor and a non-ideal switch (driver) is shown in fig. (b)

ment equations for  $V_{out} = f(V_{in})$ . Figure shows the VTC of a typical depletion-load inverter with  $k_{n,driver} = k_{n,load}$ .

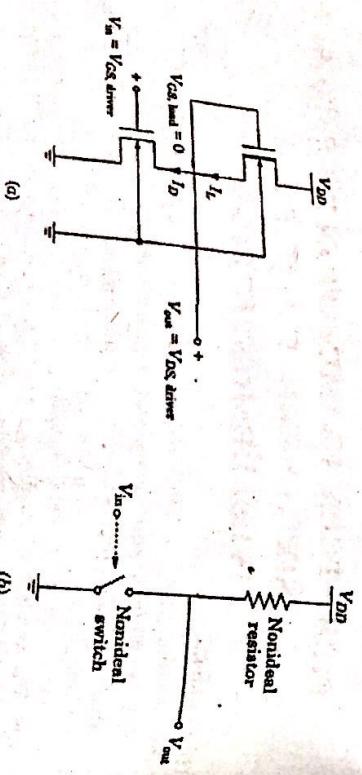


Fig : (a) Inverter circuit with depletion-type nMOS load. (b) Simplified equivalent circuit consisting a nonlinear load resistor and a non-ideal switch controlled by the input.

- The load is a depletion-type nMOS transistor so its threshold voltage is less than zero i.e.,  $V_{T,load} < 0$ . The driver device is an enhancement-type transistor so its threshold voltage is a positive quantity i.e., with  $V_{T,driver} > 0$ .

The gate and the source nodes of the load transistor are connected so that,  $V_{GS,load} = 0$  and  $V_{GS,load} > V_{T,load}$ . So that the load device always has a conducting channel regardless of the input and output voltage levels.

- Both the driver transistor and the load transistor are built on the same p-type substrate, which is connected to the ground. So the source-to-substrate voltage of the load device is equal to output voltage ( $V_{SB,load} = V_{out}$ ). The threshold voltage is also function of source-to-substrate voltage ( $V_{out}$ ) and given by

$$V_{T,load} = V_{T,0,load} + \gamma(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|})$$

The operating mode of the load transistor is determined by ( $V_{GS} = 0$ ).

- In saturation region (i.e., when  $V_{out} < V_{DD} + V_{T,load}$ ), the load current is given by

$$I_{D,load} = \frac{k_n,load}{2} [V_{GS,load} - V_{T,load}]^2$$

$$I_{D,load} = \frac{k_n,load}{2} [-V_{T,load}(V_{out})]^2 = \frac{k_n,load}{2} |V_{T,load}(V_{out})|^2$$

- In linear region (i.e., when  $V_{out} > V_{DD} + V_{T,load}$ ), the load current is given by

$$I_{D,load} = \frac{k_n,load}{2} [2(V_{GS,load} - V_{T,load})V_{DS,load} - V_{DS,load}^2]$$

$$I_{D,load} = \frac{k_n,load}{2} [2|V_{T,load}(V_{out})|(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2]$$

- The voltage transfer characteristic (VTC) of this inverter can be constructed by setting  $I_{D,driver} = I_{D,load}$ ,  $V_{GS,driver} = V_{in}$  and  $V_{DS,driver} = V_{out}$ , and by solving the corresponding

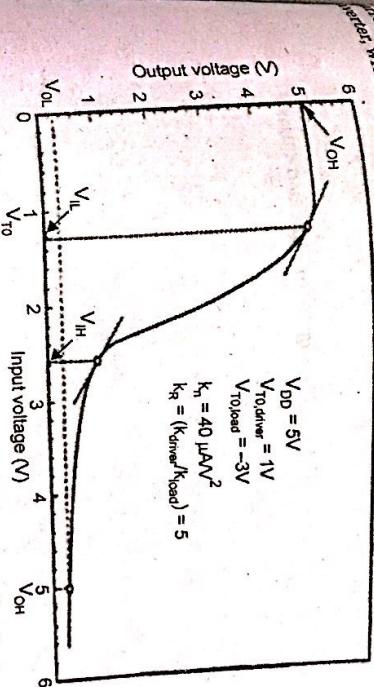


Fig. Typical VTC of a depletion-load inverter circuit.

Q.2. (b) Derive the expression of current of a MOS transistor for linear and saturation mode.

Ans. Linearity Region:

$$I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}$$

Saturation Region:

$$I_D = \mu C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2$$

1. Linear Region :

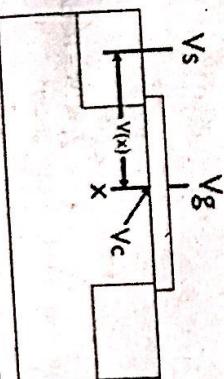


Fig. Concentration Contours in Linear Region.  
A uniform narrow channel exists.

$$V_G - V_S = V_G - V_C + V_C - V_S$$

$$V_G - V_S = V_{GS}$$

$$V_G - V_C = V_{GC}$$

$$V_C - V_S = V(x)$$

$$V_{GS} = V_{GC} + V(x) \text{ or } V_{GS} - V(x) = V_{GC}$$

$$Q_T(x) = V_{GC} C_{ox} = (V_{GS} - V(x)) C_{ox}$$

$$Q_T(x) = Q(x)_{\text{mobile}} + Q(x)_{\text{depletion}}$$

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## Sixth Semester, VLSI Design

$$\begin{aligned} Q(x)_{\text{mobile}} &= \text{mobile electron charge in channel at } x \\ Q(x)_{\text{mobile}} &= [V_{GS} - V(x) - V_{TH}]C_{ox} \end{aligned}$$

Use mobile charge to get current:

$$J_n = q\mu nE + qD_n \frac{dn}{dx} = q\mu nE \quad (\text{no diffusion current in the channel}) \quad (5)$$

$$qn(x) = Q(x)_{\text{mobile}} = Q_m(x)$$

$$J_n = Q_m(x)\mu E, \text{ but } E = -\frac{dV}{dx}$$

$$J_n = -Q_m(x)\mu \frac{dV}{dx}, \text{ substitute for } Q_m(x)$$

Separate variables and neglect (-) sign. Consider only the magnitude.

$$J_n dx = \mu C_{ox} [(V_{GS} - V(x)) - V_{TH}] \frac{dV}{dx}$$

Due to continuity,  $J_n$  = constant (no hole current or no generation, recombination)Integrating from source to drain or from  $x = 0$  to  $x = L$ , where  $L$  = gate length:

$$J_n \int_0^L dx = \mu C_{ox} \int_{V(0)}^{V(L)} [(V_{GS} - V_{TH}) - V(x)] dV$$

$$V(L) = V_{DS}, V(0) = 0$$

$$J_n \int_0^L dx = \mu C_{ox} \int_0^{V_{DS}} [(V_{GS} - V_{TH}) - V(x)] dV$$

$$J_n L = \mu C_{ox} \left[ (V_{GS} - V_{TH})V - \frac{V^2}{2} \right]_{0}^{V_{DS}}$$

$$J_n = \frac{\mu C_{ox}}{L} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

 $J_n$  for channel is Amp/cm since  $Q_m$  = Charge/cm<sup>2</sup> $I_D$  for Linear Region:

$$I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- 2. Saturation Region :** When  $V_{DS} \geq (V_{GS} - V_{TH})$  channel pinches off. This means that the channel current near the drain spreads out and the channel near drain can be approximated as the depletion region. After this occurs, at  $V_{DS} = (V_{GS} - V_{TH})$ , if you make  $V_{DS}$  larger, the current  $I_D$  does not change (to zero approximation). This is because any additional  $V_{DS}$  you add will get dropped across the depletion region and won't change the current  $I_D$ .
- So for  $V_{DS} > (V_{GS} - V_{TH})$  we find  $I_D$  by setting  $V_{DS} = (V_{GS} - V_{TH})$  substituting into the linear equation.

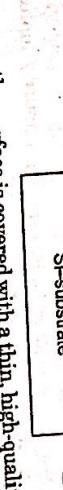
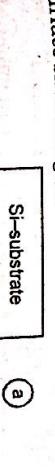
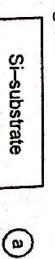
$$I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{TH})(V_{GS} - V_{TH}) - \frac{(V_{GS} - V_{TH})^2}{2} \right]$$

$$I_D = \mu C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2$$

for Saturation Region:

- Q.3 Attempt all parts  
**Q.3.(a) With the help of proper diagram discuss the nMOS fabrication steps.**

**Fabrication Steps:** The process starts with the oxidation of the silicon substrate in fig (a) in which a relatively thick silicon dioxide layer, also called field oxide is created on the surface shown in fig (b)



Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the Gate oxide of the MOS transistor Fig. (d). Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created Fig. (c).

- After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates Fig. (f)
- On top of the thin oxide layer, a layer of polyilicon is deposited Fig. (e)
- Thin oxide  
SiO<sub>2</sub>(oxide)  
Thin oxide  
Polysilicon  
Thin oxide  
SiO<sub>2</sub>(oxide)  
Si-substrate  
Thin oxide  
Polysilicon  
Thin oxide  
SiO<sub>2</sub>(oxide)  
Si-substrate

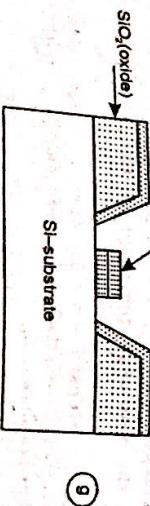
*Sixth Semester, 1972-1973*

The thin gate oxide over the source and drain regions exposes the bare silicon surface on which the source and drain juctions are to be formed FIG. (C).

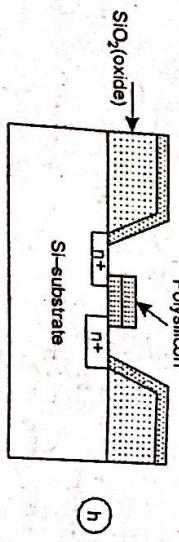
**Q.3. (b)** Design the run CMOS logic circuit for the Boolean function  $Z = A(BC + D) + \overline{E}$ . Find the equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming  $(WL)_p = 10$  for all pMOS and  $(WL)_n = 15$  for all nMOS.

$$Z = \frac{A(BC + D) + E}{F}$$

$$Z = A(BC + D) + E$$

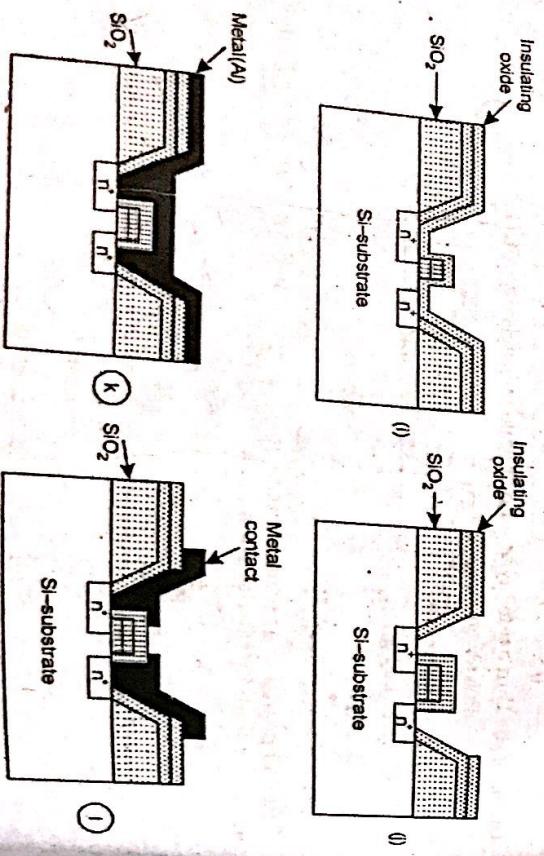


The entire silicon surface is then coated with a high concentration of impurities either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping). Fig. (2) shows that the doping penetrates.



The exposed areas on the silicon surface, ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity.

Once the source and drain regions are completed, the entire surfaces is again covered with an insulating layer of  $\text{SiO}_2$  (Fig. (f)). The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions Fig. (f). The surface is covered with evaporated aluminium which will form the interconnects Fig. (g). Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface Fig. (l).



We have also given that,  $\left(\frac{W}{L}\right)_p = 10$  for all pMOS and  $\left(\frac{W}{L}\right)_n = 15$  for all nMOS.

To obtain  $\left(\frac{W}{L}\right)_{n, \text{eon.}}$ , the transistor B and C are in series

$$C_{eq.} = \frac{C_1 \times C_2}{C_1 + C_2} = \frac{15 \times 15}{15 + 15} = 7.5$$

This equivalent is in parallel with transistor D

$$C_{eq.} = \frac{22.5 \times 15}{22.5 + 15} = 9$$

Now this equivalent and transistor A are in. 23.5 x 15

The equivalent and transistor E are in parallel

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## Sixth Semester, VLSI Design

$$\left(\frac{W}{L}\right)_{n,eq} = 9 + 15 = 24$$

To obtain  $\left(\frac{W}{L}\right)_{p,eq}$   
The capacitor B and C are in parallel.

This equivalent and A are in series

$$C_{eq} = \frac{20 \times 10}{30} = \frac{20}{3}$$

This equivalent and A are in parallel

$$C_{eq} = \frac{20}{3} + 10 = \frac{50}{3}$$

Now this equivalent and E are in series

$$\left(\frac{W}{L}\right)_{p,eq} = \frac{\frac{50}{3} \times 10}{\frac{50}{3} + 10} = \frac{50}{8} = 6.25$$

- Q.4. Attempt all parts  
 Q.4. (a) Design a 4 : 1 multiplexer circuit using CMOS transmission gates and explain its working.  
 Ans.

Q.4. (b) What do you understand by a pass transistor? Discuss the mode of operation of a pass transistor when we pass a "0" and "1" through it. Define rise time and fall time.

Ans. Refer Q.4.(b) of Mid Term Examination 2018, (Page No. 5-2018)

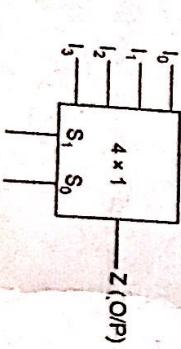
(5)



Fig.A TG posed CMOS implementation of 4:1 MUX

Truth table of  $4 \times 1$  MUX is shown below

$S_1$	$S_0$	Z(Output)
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$



## END TERM EXAMINATION [MAY, 2019]

### SIXTH SEMESTER [B.TECH]

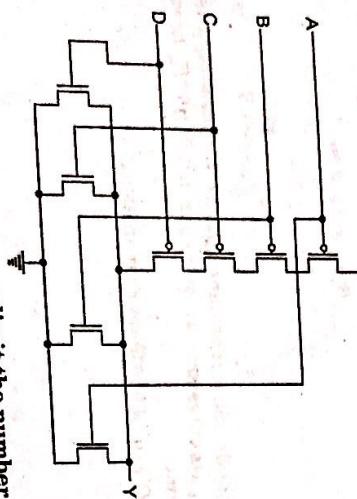
### VLSI DESIGN [ETEC-308]

M.M.: 75

Time : 3 hrs.

**Note :-** Attempt five questions in all including Q. no. 1 which is compulsory. Select one question from each unit. Assume missing data if any.

**Q.1. (a) Sketch of transistor level schematic of a CMOS 4-input NOR gate. (5)**  
**Ans.** The transistor level schematic of a CMOS 4-input NOR gate is shown below.



**Q.1. (b) Does the body effect of a process limit the number of transistors that can be placed in series in a CMOS gate at low frequencies. (5)**

**Ans.** No. Any number of transistors may be placed in series, although the delay increases with the square of the number of series transistors.

**Q.1. (c) What is Latch up in CMOS? Explain. (5)**

**Ans.** Latch-up is defined as the generation of a low-impedance path in CMOS chips between the power supply rail and the ground rail due to interaction of parasitic pnp and npn bipolar transistors. The latch-up is inversely proportional to the product of the substrate doping level and the square of the spacing.

**Prevention of Latch-up:**

- Reduce the gains of BJTs by lowering the minority carrier lifetime through gold doping of the substrate.

• Use  $p^+$  guardband rings connected to ground around nMOS transistors and  $n^+$  guard ring connected to  $V_{DD}$  around pMOS transistors to reduce  $R_w$  and  $R_{Sub}$  and to capture injected minority carrier before they reach the base of the parasitic BJTs.

• Place substrate and well contacts as close as possible to the source connections of MOS transistors to reduce the values of  $R_w$  and  $R_{Sub}$ .

• Use minimum area p-wells.

• Source diffusion regions of pMOS transistors should be placed so that they lie along equipotential lines when currents flow between  $V_{DD}$  and p-wells.

• Avoid the forward biasing of source/drain junctions.

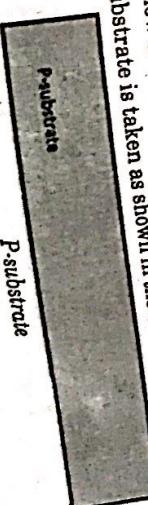
- Q.2. (a) Compare the relative merits of three forms of pull-up for an inverter circuit. What is the best choice for realization in (i) NMOS technology? (ii) CMOS technology? (5)**
- Ans.** CMOS stands for Complementary Metal-Oxide-Semiconductor. On the other hand, NMOS is a metal oxide semiconductor or MOS or MOSFET (metal-oxide-semiconductor field effect transistor). These are two logic families, where CMOS uses both PMOS and MOS transistors for design and NMOS uses only FETs for design. CMOS is chosen over NMOS for embedded system design. Because, CMOS propagates both logic 0 and 1, whereas NMOS propagates only logic 1 that is  $V_{DD}$ . The output after passing through one, the NMOS gate would be  $V_{DD} - V$ . Therefore, CMOS technology is preferred.
- In CMOS logic gates, a set of n-type MOSFETs is positioned in a pull-down network between the low-voltage power supply rail and the output. Instead of the load resistor between the high-voltage rail and the output. Therefore, if both transistors have their gates connected to the same input, the p-type MOSFET will be on when the n-type MOSFET is off, and vice-versa.
- CMOS and NMOS both inspired by the growth in digital technologies, that are used to construct the integrate circuits. Both CMOS and NMOS are used in many digital logic circuits and functions, static RAM and microprocessors. These are used as data converters and image sensors for analog circuits, and also used in Trans-receptors for many modes of telephone communication. While both CMOS and NMOS have the same function as transistors for both analog and digital circuits, but many people still choose CMOS technology to the latter for its many advantages.
- As compared to the NMOS, the CMOS technology is top in quality. Especially, when it comes to its features like low-static power utilization and noise resistance, CMOS technology conserves energy and it does not produce heat. Though costly, a lot of people prefer the CMOS technology used by the CMOS black market to fabricate the technology used by the BiCMOS.

**Q.2. (b) Briefly describe n-well BiCMOS fabrication process steps with suitable diagram. (4)**

**Ans.** BiCMOS Logic: It is a complex processing technology that provides NMOS and PMOS technologies amalgamated each other with the advantages of having very low power consumption bipolar technology and high speed over CMOS technology. MOSFETs grant high input impedance logic gates and bipolar transistors provide high current gain.

**Steps for BiCMOS Fabrication:** The BiCMOS fabrication combines the process of fabrication of BJT and CMOS, but merely variation is a realization of the base. The following steps show the BiCMOS fabrication process.

**Step 1: P-Substrate** is taken as shown in the below figure





**Step 3:** A small opening is made on the oxide layer.



*Opening is made on the oxide layer.*

**Step 4:** N-type impurities are heavily doped through the opening.

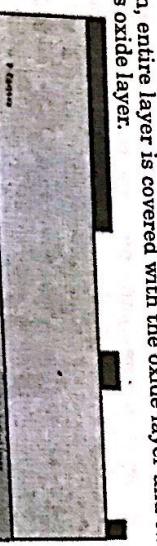


*N-type impurities are heavily doped through the opening.*

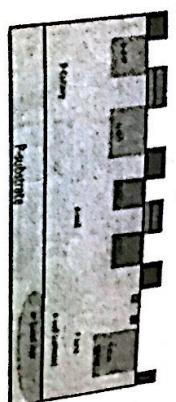
**Step 5:** The P-Epitaxy layer is grown on the entire surface.



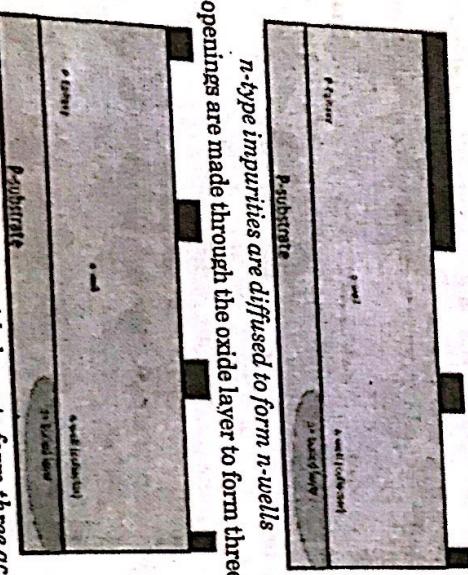
**Step 6:** Again, entire layer is covered with the oxide layer and two openings are made through this oxide layer.



**Step 7:** From the openings made through oxide layer n-type impurities are diffused to form n-wells.



**Step 8:** Three openings are made through the oxide layer to form three active devices.

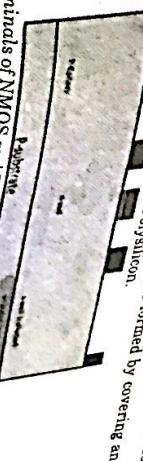


**n-type impurities are diffused to form n-wells.**

**Three openings are made through the oxide layer to form three active devices.**

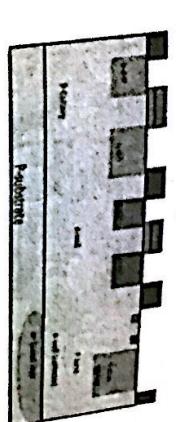
**Step 9:** The gate terminals of NMOS and PMOS are formed with Thinox and PolySilicon.

**Step 10:** The P-impurities are added to form the base terminal of BJT and for contact purpose N-type impurities are doped into the N-well collector.



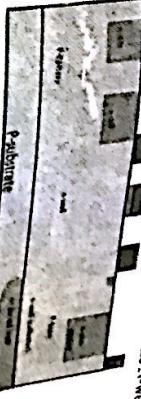
**The gate terminals of NMOS and PMOS are formed with Thinox and PolySilicon.**

**N-type impurities are added to form the base terminal of BJT and for contact purpose N-type impurities are doped into the N-well collector.**



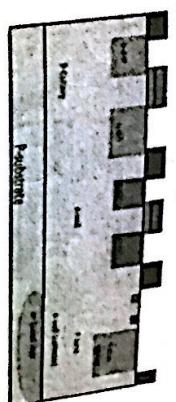
P-impurities are added to form source and drain regions of PMOS.

**Step 11:** To form source and drain regions of PMOS and to make contact in P-base region the P-type impurities are heavily doped.



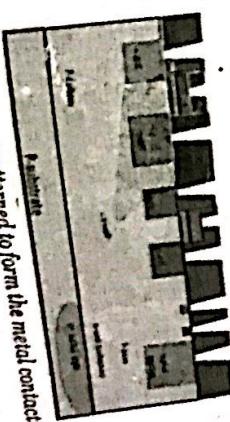
**P-type impurities are heavily doped to form source and drain regions of PMOS.**

**Step 12:** Then the entire surface is covered with the thick oxide layer.



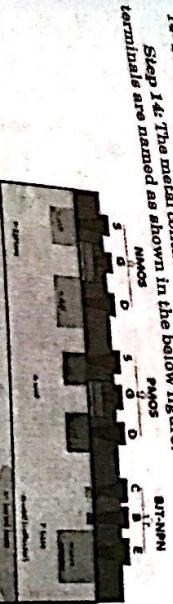
**Entire surface is covered with the thick oxide layer.**

**Step 13:** Through the thick oxide layer the cuts are patterned to form the metal contacts.

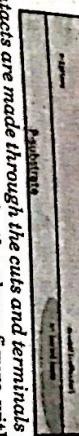


**The cuts are patterned to form the metal contacts.**

(d) From the given logic function of 3:2 Priority encoder, the transistor level schematic is shown below



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Step 14: The metal contacts are made through the cuts made on oxide layer and the terminals are named as shown in the below figure.



Metal contacts are made through the cuts and terminals are named.  
The fabrication of BICMOS is shown in the above figure with a combination of NMOS, PMOS and BJT. In the fabrication process some layers are used such as channel stop implant, thick layer oxidation and guard rings.

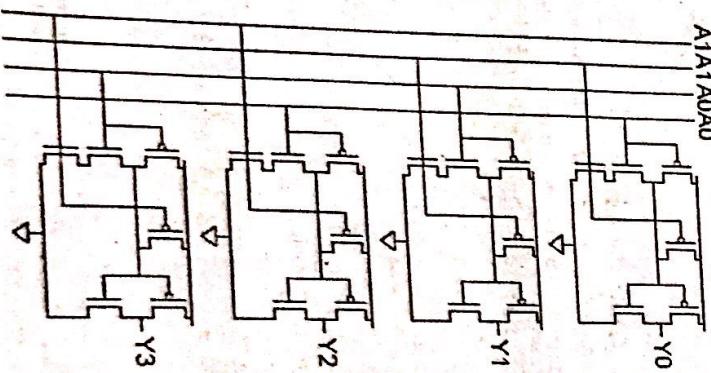
OR

Q.3. (a) Sketch transistor level schematics for the following logic functions. You may assume you have both true and complementary versions of the inputs suitable

$$(i) \text{A } 2:4 \text{ decoder defined by } Y_0 = \bar{A}_0 \bar{A}_1; \quad Y_1 = A_0 \bar{A}_1 \\ Y_2 = \bar{A}_0 A_1; \quad Y_3 = A_0 A_1$$

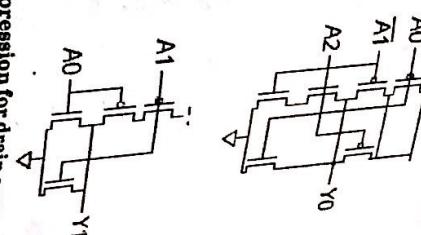
$$(ii) \text{A } 3:2 \text{ Priority encoder defined by} \\ Y_0 = \bar{A}_0 \cdot (A_1 + \bar{A}_2); \quad Y_1 = \bar{A}_0 \cdot \bar{A}_1$$

Ans. (i) From the given logic function of 2:4 decoder, the transistor level schematic is shown below



Q.3. (b) Derive an expression for drain current in an NMOS transistor and discuss in detail the effect of channel length modulation.

Ans. To understand drain current in n-channel MOSFET, Let us consider geometry of the surface inversion layer (channel region).



Boundary conditions for the channel voltage  $V_c$  are:

$$V_c(y=0) = V_s = 0 \quad \dots(1)$$

$$V_c(y=L) = V_{DS}$$

Also it is assumed that the entire channel region between the source and the drain is inverted as

$$V_{GS} \geq V_{IO} \quad \dots(2)$$

$$V_{GD} = V_{GS} - V_{DS} \geq V_{IO}$$

Let  $Q(y)$  be the total mobile electron charge in the surface inversion layer. This can be expressed as

$$Q(y) = -C_{ox}[V_{GS} - V_c(y) - V_{IO}] \quad \dots(3)$$

Now consider incremental resistance  $dR$  can be expressed as

$$dR = \frac{-dy}{W \mu_n Q(y)} \quad \dots(4)$$



$$\text{NMOS area} = W \cdot L_n \quad (\because L = L_n = L_p)$$

$$\text{CMOS area} = W_n L_n + L_p \cdot W_p$$

$$\text{CMOS area} = L^2 \left[ \frac{W_n}{L_n} + \frac{W_p}{L_p} \right] = L^2 \left[ \frac{W_n}{L_n} + \frac{W_p}{L_p} \right] \quad (\because L = L_n = L_p)$$

Summarizing that CMOS transistor are directly proportional to  $(n + P)$ , we can call this method of estimating area as proxy method.

- For transistors sizing issues, we have two situations (cases).



Then equivalent  $\frac{W}{L}$  i.e.,

$$\left( \frac{W}{L} \right)_{\text{equivalent}} = \left( \frac{W}{L} \right)_1 + \left( \frac{W}{L} \right)_2 + \left( \frac{W}{L} \right)_3 + \dots + \left( \frac{W}{L} \right)_n$$

**Case II:** When various similar transistors are

connected in series Fig.

**Q.5. (b) Suppose  $V_{DD} = 1.2V$  and  $V_t = 0.4V$ . Determine  $V_{out}$  in following. Neglect the body effect.**

- $V_{in} = 0V$
- $V_{in} = 0.6V$
- $V_{in} = 0.9V$
- $V_{in} = 1.2V$

**Ans.** We have given that

$$V_{DD} = 1.2V \quad \text{and} \quad V_t = 0.4V$$



**Q.6. (a) What are the non ideal effects in dynamic logic?**

**Ans.** Non-ideal effects in dynamic logic are given as follows:

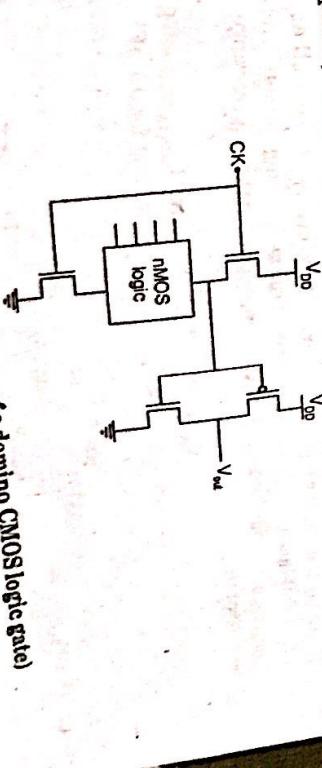
- Charge Leakage:** The operation of a dynamic MOS Logic Explain. (7.5) of the output value on a capacitor. If the dynamic storage current. However, this charge gradually leaks away due to leakage ideally remain at the precharged state of  $V_{DD}$  during the evaluation phase. Eventually resulting in a malfunctioning of the gate.
- Charge Sharing:** Another important concern of the gate. This is the impact of charge sharing. During the precharge phase, the output node is precharged to  $V_{DD}$ . Assume that all inputs are set to 0 during precharge, and that the capacitance  $C_o$  of the output node may couple capacitively and destroy the state of the floating node. A wire routed over a dynamic node may couple capacitively and destroy the state of the floating node. Another equally important form of capacitive coupling is the back-gate effect. Assume further that input B remains at 0 during evaluation. Input A makes a 0 to 1 transition, turning transistor M<sub>1</sub> on. The charge stored originally on capacitor  $C_1$  is redistributed over  $C_1$  and  $C_2$ . This causes a drop in the output voltage, which cannot be recovered due to the dynamic nature of the circuit.

**Q.6. (b) Explain the operation of Domino Logic.**

**Ans. Domino CMOS logic:** A domino logic module consists of an n-type dynamic logic block followed by a static inverter. The generalized circuit diagram of a domino CMOS logic gate shown in fig. The addition of the inverter allows us to operate a number of such structures in cascade, as explained below.

- When  $CK = 0$  (pre-charge phase), the output node of the dynamic CMOS stage is pre-charged to a high logic level, and the output of the CMOS inverter (buffer) becomes low.
- When the clock signal rises at the beginning of the evaluation phase ( $CK = 1$ ), there are two possibilities: The output node of the dynamic CMOS stage is either discharged to a low level through the nMOS circuitry (1 to 0 transitions), or it remains high. So, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1.

- $V_{in} = 0V$   
When  $V_{in} = 0V$  Then  $V_{in} < V_t \therefore V_{out} = 0$
- $V_{in} = 0.6V$   
When  $V_{in} = 0.6V$  Then  $V_{in} > V_t \therefore V_{out} = 0.6V$
- $V_{in} = 0.9V$   
When  $V_{in} = 0.9V$  Then  $V_{in} > V_t \therefore V_{out} = 2|V_{tp}| = 0.8V$
- $V_{in} = 1.2V$   
When  $V_{in} = 1.2V$  Then  $V_{in} > V_t \therefore V_{out} = V_{DD} - V_{in} = 1.2 - 0.4 = 0.8V$



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Domino CMOS has the following properties:

- Since each dynamic gate has a static inverter logic can be implemented.
- Very high speeds can be achieved.
- Allow a significant reduction in the number of transistors required to realize any complex boolean function.

**Q.7.(a) Design clocked SR latch and DFF with CMOS.**

Ans.

OR

(7.5)

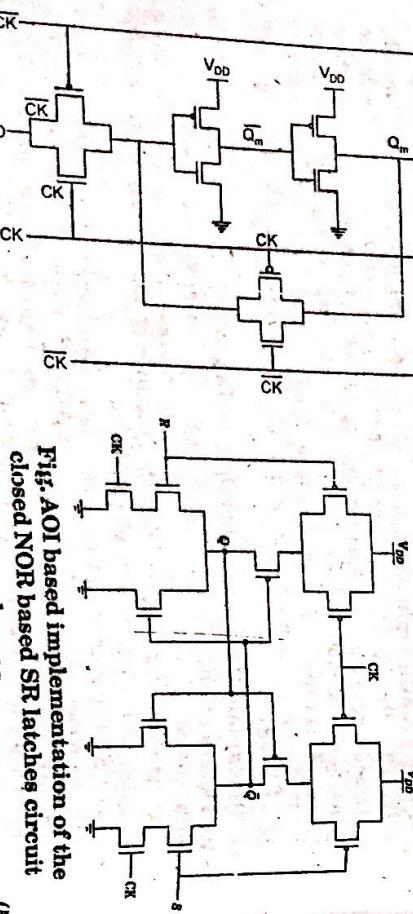


Fig. AOI based implementation of the closed NOR based SR latches circuit

(5)

**Q.7. (b) Discuss different clock distribution schemes.**

**Ans. Clock Distribution:** The clock distribution is a very serious problem in sequential logic circuits i.e., synchronous or asynchronous circuits. If one counts up all the capacitance in the registers in a large CMOS design, it may well add up to over a

1000 pF. If this has to be driven in a small time and at a high repetition rate, the peak transient current and average dynamic current can be in the ampere range. For example, we can consider:

$$V_{DD} = 5 \text{ V}; \quad T_{clock} = 10 \text{ nsec}; \quad T_{rise/fall} = 1 \text{ nsec}$$

$$C_{\text{register}} = 2000 \text{ pF} (20 \text{ K register bits for } 0.1 \text{ pF})$$

$$I_{peak} = C \frac{dV}{dt}$$

$$I_{peak} = \frac{2000 \times 10^{-12} \times 5}{1 \times 10^{-9}} = 10 \text{ Ampere}$$

Two types of designs are used for CAD tools. Two types of designs are used for CAD tools.

(i) **Front-End design:** Front-End design is the process of creating the logic source from logic source for design.

(ii) **Back-End design:** Back-End design is the process of creating the physical source from logic source for design.

**Q.8.(b) Concept of regularity, modularity, and locality.**

**Ans. Concepts of Regularity, Modularity, and Locality**

The hierarchical design approach reduces the design complexity by dividing the large system into several sub-modules. Usually, other design concepts and design approaches are also needed to simplify the process. Regularity means that the hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. A good example of regularity is the design of array structures consisting of identical cells such as a parallel multiplication array. Regularity can exist at all levels of abstraction. For example, at the transistor level, uniformly sized transistors simplify the design and at the logic level, identical gate structures can be used. If the designer has a small library of well-characterized basic building blocks, a number of different functions can be constructed by using this principle. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

Modularity in design means that the various functional blocks which make up the larger system must have well-defined functions and interfaces. Modularity allows that each block or module can be designed relatively independently from each other, since there is no ambiguity about the function and the signal interface of these blocks. All of the blocks can be combined with ease at the end of the design process, to form the large system. The concept of modularity enables the parallelization of the design process. The well-defined functionality and signal interface also allow the use of generic modules in various designs.

By defining well-characterized interfaces for each module in the system, we effectively ensure that the internals of each module become unimportant to the exterior modules. Internal details remain at the local level. The concept of locality also ensures that connections are mostly between neighboring modules, avoiding long interconnect delays. Time-critical operations should be performed.

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Locally, without the need to access distant modules or signals. Sometimes, the replication of some logic in distant location may solve this problem in large system architectures.

### Q.8.(c) Low Power design concepts using CMOS Technology.

**Ans.** The VLSI low power design problems can be broadly classified into two analysis and optimization.

Analysis problems are concerned about the accurate estimation of the power circuitry dissipation at different phases of the design process. Analysis techniques differ in their accuracy and efficiency. The accuracy of analysis depends on the availability of design information. Analysis techniques also serve as the foundation for design optimization.

Optimization is the process of generating the best design given an optimization goal, without violating design specifications. An automatic design optimization algorithm requires a fast analysis engine to evaluate the merits of the design choices. Manual optimization also depends a reliable analysis tool to provide accurate estimation of power dissipation.

A decision to apply a particular low-power technique often involves trade off from different sources putting in various directions.

- Major criteria to be considered are the impact to the circuit delay, which affects the Performance and throughput of the chip, and the chip area, which directly translates to manufacturing costs.

### NEEDS FOR LOW POWER VLSI CHIPS

• As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation.

- A need for low power VLSI chips arises from various evolution forces of integration circuits.

• The requirements for low power consumption must be met along with equally demanding goals of high chip density and high throughput.

- The need for low-power design is also becoming a major issue in high performance digital systems, such as DSPs, microprocessors and other applications.

• High Performance computing system characterized by large power dissipation also drives the low power needs.

- Power dissipation has a direct impact on the packaging cost of the chip and the cooling cost of the system.

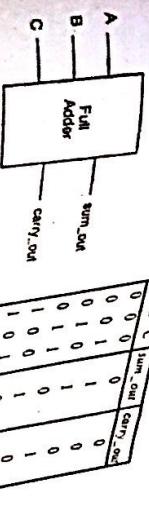
• Another major demand for low power chips and systems comes from environmental concerns. Computers are the fastest-growing electricity loads in the commercial sector. Since electricity generation is a major source of air pollution, inefficiency energy usage in computing equipment indirectly contributes to environmental pollution.

- Device characteristics (e.g., threshold voltage), device geometries and interconnect proper are significant factors in lowering the power consumption. Circuit level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clock strategies can be used to reduce power dissipation at the transistor level.

• The power consumed by the system can be reduced by a proper selection of the data processing algorithms, specifically to minimize the number of switching events for a given task.

### Q.9. Explain Adder design using CMOS.

**Ans.** We start our design by considering the Boolean description of the binary adder circuit. Let A and B represent the two input variables (addend bits), and let C represent



Full Adder				
A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The sum and carry\_out signals can be found as the following two combinational Boolean functions of the three input variables, A, B, and C.

$$\text{carry\_out} = AB + AC + BC$$

Note that instead of realizing the two functions independently, we use the carry\_out signal to generate the sum output, since the output can also be expressed as

$$\text{sum\_out} = ABC + (A + B + C) \text{carry\_out}$$

This implementation ultimately reduces the circuit complexity and hence, saves chip area. Also, we identify two separate sub-networks consisting of several gates (highlighted with dashed boxes) that will be utilized for the transistor-level realization of the full-adder circuit.

Initially, we will design all nMOS and pMOS transistors with a (W/L) ratio of (90 nm/50 nm), which is the minimum transistor size allowed in this particular technology. This initial sizing of transistors, which is obviously not an optimum solution, may be changed later depending on the performance characteristics of the adder circuit. Choosing minimum-size transistors in the initial design stage usually provides a simple, first cut verification of the circuit functionality.

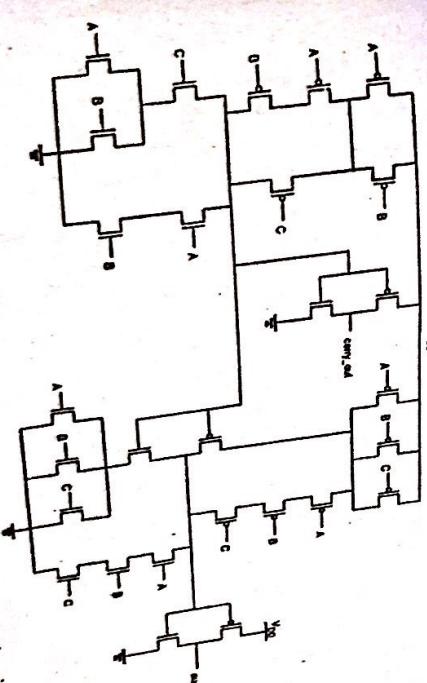


Fig. Transistor-level schematic of the 1-bit full adder circuit.