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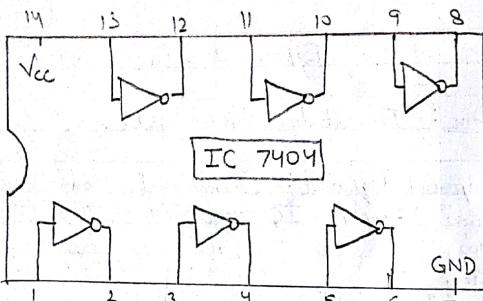
Experiment 1(a)

- Aim: To study basic gates.
- Equipment Required: Breadboard, connecting wires, power supply, IC 7400, 7404, 7408, 7432, 7486, 7402.
- Theory
A logic gate is an electronic circuit which makes logical decisions. The most common logic gates are - OR, AND, NOT, NAND and NOR. NAND & NOR gates are called as Universal Gates. Exclusive-NOR & Exclusive-NOR (XOR & XNOR) gates can be constructed using basic logic gates.

1. AND Gate (IC 7408)

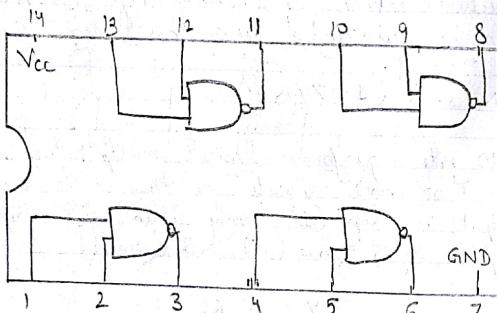
AND gate performs logical multiplication. It has two or more inputs & a single output. The output is high (1) only when all inputs are high. It is low (0) otherwise.

$Y = A \cdot B$		
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1



NOT Gate

$$A \rightarrow \text{NOT} \rightarrow Y = \bar{A}$$



NAND Gate

$$A \quad B \rightarrow \text{NAND} \rightarrow Y = A \cdot B$$

2.

OR Gate (IC 7432)

The OR gate performs logical addition. It consists of two or more inputs & only one output. The output is low (0) when all the inputs are low and high (1) otherwise.

$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3.

NOT Gate (IC 7404)

NOT gate performs the logical function called inversion. The purpose of this gate is to convert one logic level into the opposite logic level. It has one input & one output.

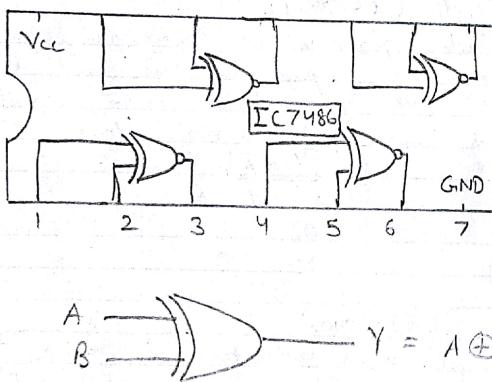
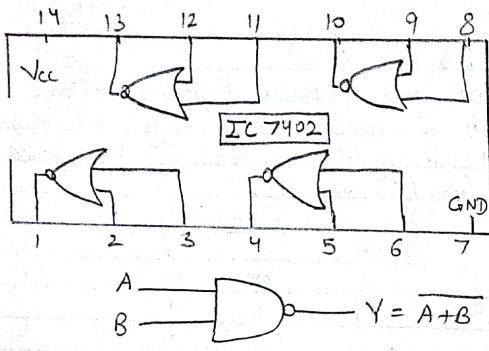
$$Y = \bar{A}$$

A	Y = \bar{A}
0	1
1	0

4.

NAND Gate (IC 7400)

NAND gate is a contraction of the NOT-AND gate. It has two or more inputs & one output. When all the inputs are high, output is low. If any one/ both inputs are low, output is high.



Ex - OR Gate

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$Y = A \cdot B$		
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR Gate (IC 7402)
NOR is a contraction of NOT - OR gates. It has two or more inputs, and one output. The output is high only when all the inputs are low. If any one or both the inputs are high, then the output is low.

A	B	$Y = A + B$
0	0	1
0	1	0
1	0	0
1	1	0

6. X - OR Gate (IC 7486)
X - OR gate is one having two or more inputs & one output. The output of a two input X-OR gate assumes as high if one & only one input is high.

$$Y = A \oplus B = \overline{AB} + A\overline{B}$$

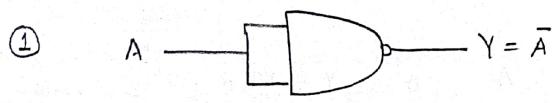
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Procedure

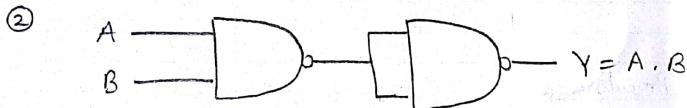
1. The required ICs were tested on the IC tester.
2. Connections made as per diagram.
3. Truth tables of the basic gates were verified.

Result

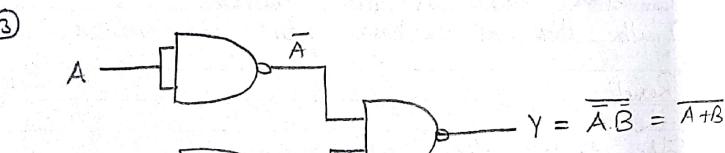
The truth tables of corresponding gates is verified.



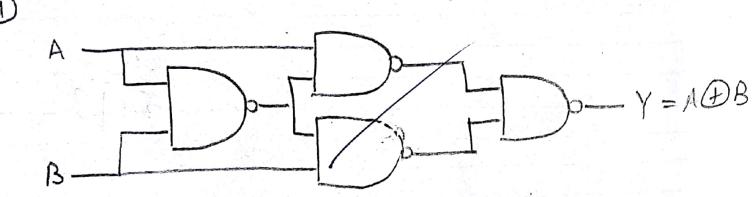
NOT Using NAND



AND Using NAND



OR Using NAND



XOR Using NAND

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Experiment - 1 (b)

- Aim : To implement universal gates using Basic Gates.

- Equipment Required : Breadboard, connecting wires, power supply, IC - 7400 & 7402.

Theory

NOT, AND, OR gates are called basic gates because we can make different gates like NAND & NOR gates but these are universal gates go by using any of them, we can make any logic circuit.

1. NOT using NAND

By short circuiting the input of NAND, we get NOT gate.

2. AND using NAND

We require 2 NAND gates to form AND gate.

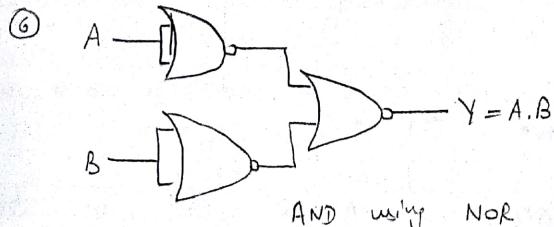
3. OR using NAND

The logic is, we use 2 NAND gates in parallel and one NAND gate in series with them.

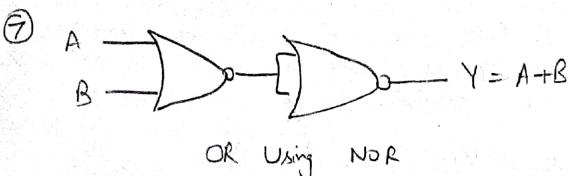
4. XOR using NAND



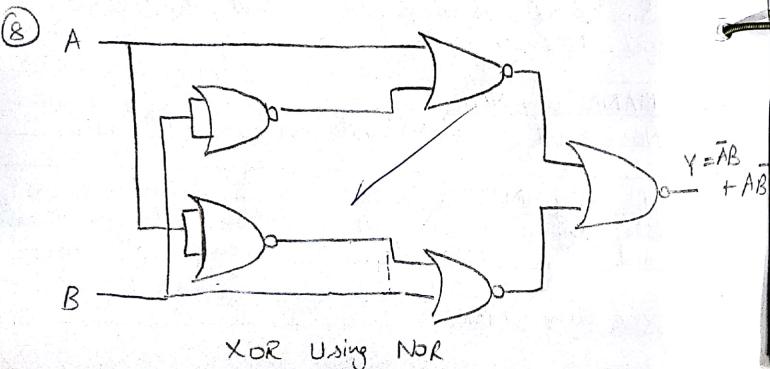
NOT using NOR Gate



AND using NOR



OR Using NOR



XOR Using NOR

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A design is more acceptable when it has less number of hardware & is simpler, so we use 4 NAND gates from XOR.

5. NOT using NOR

By short circuiting the input of NOR gate, we get NOT gate. If A is short circuited, then A is output.

6. AND using NOR

The circuit is made of 2 short circuited NOR gates in parallel & again connected with NOR gates.

7. OR using NOR

This circuit is drawn using NOR gate in series with a short circuited NOR gate.

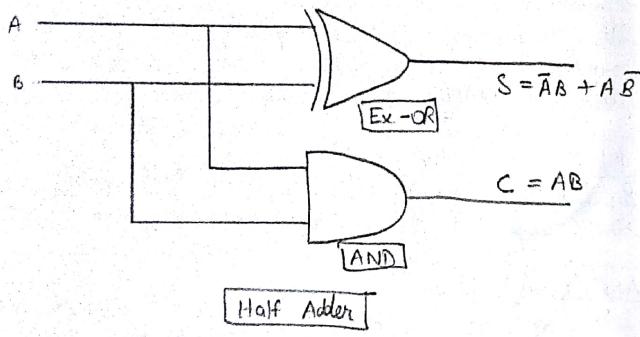
8. XOR using NOR : We use 5 XOR gates to form a NOR

- Procedure : Connections & logical inputs are done as per circuit diagrams.

Precautions

- All connections should be tight & accurate.
- Power Supply should be switched off after the exp.

- Result : Verified truth table for gates using Universal gates.



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Experiment - 2

- AIM : (a) Design half adder using basic gates.
(b) Design full adder using basic gates.
- Equipment Required : Breadboard, wires, power supply, IC - 7408, 7486, 7432.

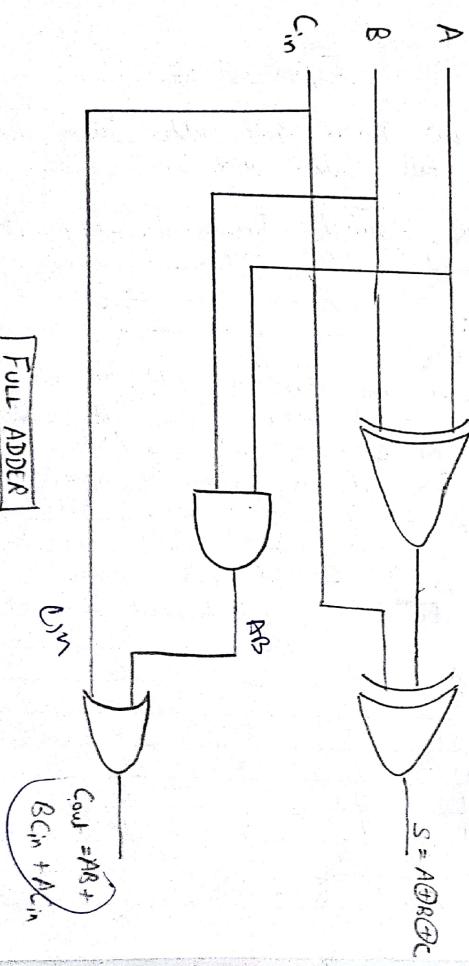
Theory : Half Adder

This means we have to add two bits with the possibility of a carry. The half adder circuit consists of Ex-OR gate and AND gate. The output of Ex-OR gate is called the 'sum' and the output of AND gate is called 'carry'. The AND gate produce a high output only when both inputs are high. The Ex-OR gate produces a high output if either output input, but not both are high.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = \bar{A}B + A\bar{B} = A \oplus B \quad C = A \cdot B$$

FULL ADDER



Full Adder

A half-adder has only two inputs & there is no provision to add a carry coming from the lower order bits when multi-bit addition is performed. For this purpose, a full-adder is designed.

A full adder is a combinational circuit that performs the arithmetic sum of three input bits & produces a sum of three input bits output and a carry.

The output of Ex-OR gate is called Sum(S) & output of OR gate is called Carry(C_{out}). When 2 or more inputs A, B & C is high, full adder will generate a carry. Also, when number of high A, B & C_{in} input arrives the Ex-OR gate produces a high output.

A	B	C _{in}	Sum(S)	Carry(C _{out})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = A \oplus B \oplus C$$

$$C_{out} = AB + BC_{in} + AC_{in}$$

Procedure

- 1. Connections were made as per diagrams.
- 2. Truth tables of half adder & full adder were verified.

Precautions

- 1. All connections should be tight & accurate.
- 2. Power supply should be switched off after the exp.

Result

Truth tables of half adder & full adder were verified.

Experiment 3

- Aim : Design half & full subtractor using logic gates.
- Equipment Required : Breadboard, wires, power supply, IC 7408, 7486, 7404, 7432.

Theory

Half Subtractor

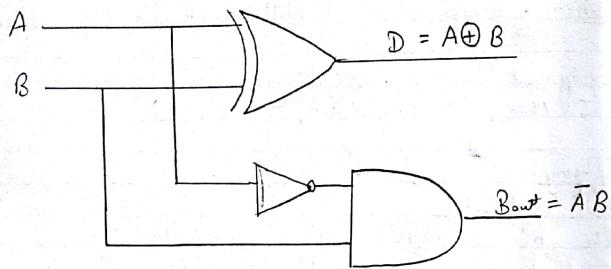
The half-subtractor is a combinational circuit which is used to perform subtraction of 2 bits. It has 2 inputs & 2 outputs. The outputs are difference & borrow. The difference can be applied using XOR gate, borrow output can be implemented using AND gate & an inverter.

<u>A</u>	<u>B</u>	<u>D (Difference)</u>	<u>Bout (Borrow)</u>
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$D = \overline{A} \overline{B} + A \overline{B}$$

$$= A \oplus B$$

$$B_{out} = \overline{A} B$$



Half Subtractor

• Full Subtractor

A full subtractor is a combinational circuit that performs subtraction involving 3 bits, namely minuend bit, subtrahend bit and the borrow from the previous stage. It has three inputs & three outputs. The full subtractor is a combination of XOR, AND, OR, NOT gates. The two half subtractors put together can give a full subtractor.

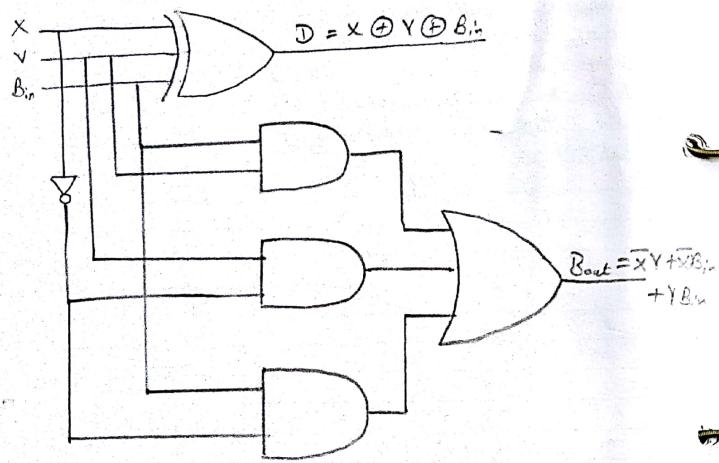
X	Y	B _{in}	D	B _{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = X \oplus Y \oplus B_{in}$$

$$B_{out} = \overline{X}Y + \overline{X}B_{in} + YB_{in}$$

• Procedure

Connections were done as per the circuit diagrams. Logical inputs were given as per circuit diagrams. Output was observed & truth table verified.



Full Subtractor

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Precautions

All connections should be done according to circuit diagram.

All connections should be tight & accurate.

Power supply should be switched OFF after the experiment.

Result

Truth tables of half subtractor & full subtractor were verified.

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Experiment 4

- Aim: To design a magnitude comparator.
- Equipment: Breadboard, connecting wires, power supply, IC 7486, 7404 & 7432.

Theory

A magnitude comparator is a combinational circuit that compares the magnitude of two nos. & generates one of the following outputs:

1. $A = B$
2. $A > B$
3. $A < B$

Ans

To implement the magnitude comparator, the Ex-Nor & AND gates are used. The property of Ex-Nor gate can be used to find whether the two binary digits are equal or not and the AND gates are used to find whether a binary digit is less than / greater than another bit.

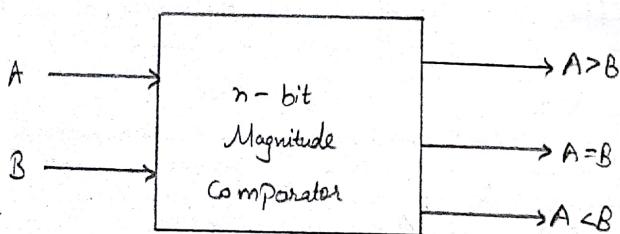
- 1-Bit Comparator

$$A_0 \oplus B_0 \quad (A_0 = B_0)$$

$$\overline{A_0} \overline{B_0} \quad (A_0 > B_0)$$

$$\overline{A_0} B_0 \quad (A_0 < B_0)$$

- 2-Bit Comparator



Block Diagram of
n-bit Magnitude Comparator



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2-bit magnitude comparator compares the numbers each having two bits (A_1, A_0) & (B_1, B_0) .

INPUT				OUTPUT		
A	A_0	B_1	B_0	$A > B$	$A = B$	$A < B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	0	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	0	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

1. $A_1 B_1 + A_0 B_0$ ($A_1 \oplus B_1$) for $(A > B)$
2. $(A_1 \oplus B_1) (A_0 \oplus B_0)$ ($A_0 \oplus B_0$) for $(A = B)$
3. $\bar{A}_1 B_1 + \bar{A}_0 B_0$ ($A_1 \oplus B_1$) for $(A < B)$

Procedure-

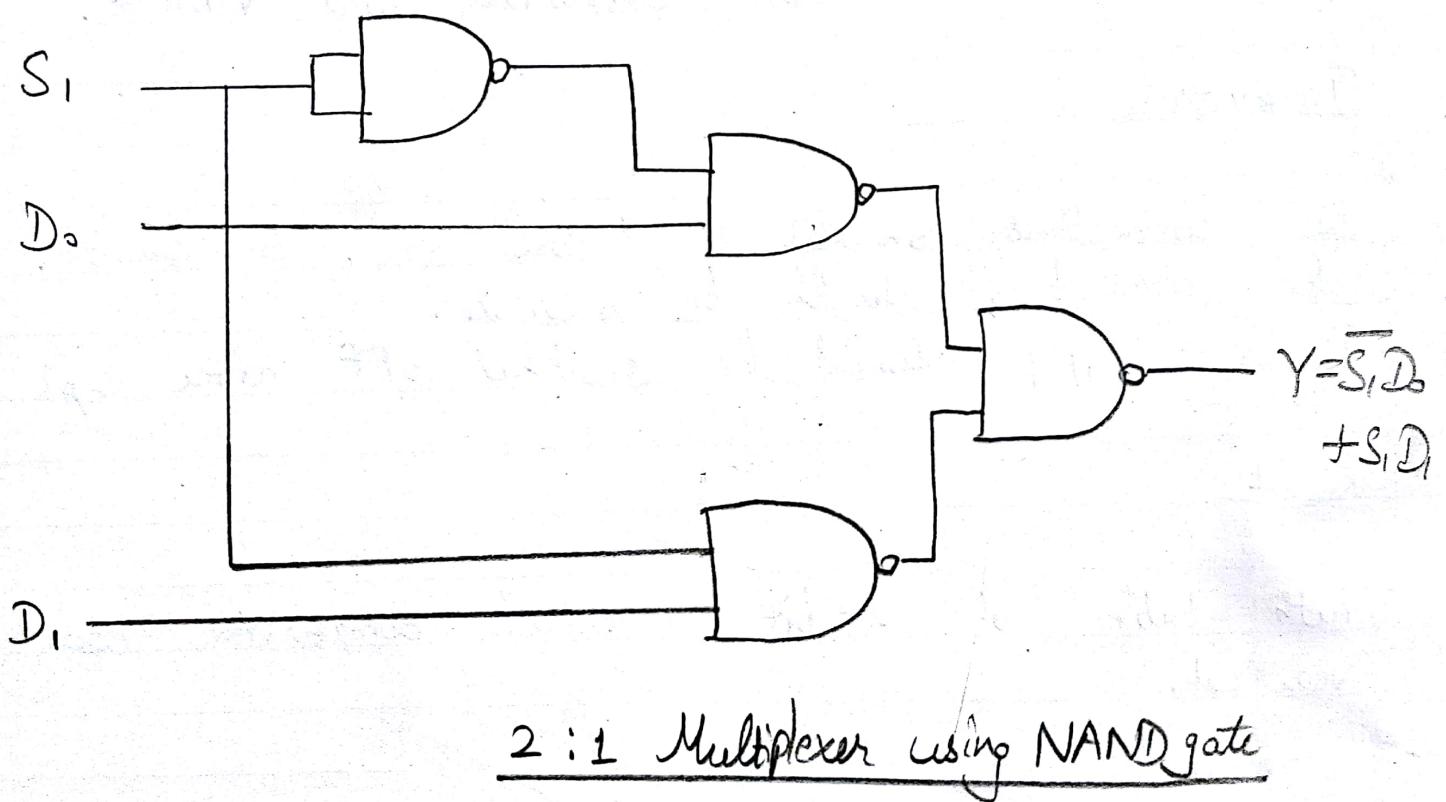
- 1. Connections were done as per circuit diagram.
- 2. Truth table of 2 bit comparator was verified.

Precautions

- 1. All connections should be done acc. to circuit.
- 2. All connections should be accurate.
- 3. Power supply should be switched off after expt.

Result

Truth table of 2-bit magnitude comparator was verified.



2 : 1 Multiplexer using NAND gate

Experiment 5

- aim: Design a multiplexer using NAND gate.
- Equipment: Breadboard, connecting wires, power supply.
- Theory
A digital multiplexer (MUX) is a combinational circuit that selects digital information from several sources & transmits the selected information on a single output line.
A MUX is also called a data selector since it selects one of many inputs & steers the information to the output.

The Mux has many data input lines & a single output line. The selector of a particular input line is controlled by a set of selection lines. If the number of n input lines is equal to 2^m , then m select lines are required to select from n input lines.

2:1 Multiplexers

It has 2 input lines -
Since $2^1 = 2$, 1 select line is needed to select output.

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Data Select Input (S_1)	Output Y
0	D_0
1	D_1

$$Y = D_0 \bar{S}_1 + D_1 S_1$$

• Procedure

1. Connections were done as per circuit diag.
2. Truth table of 2:1 Mux was verified.

• Precautions

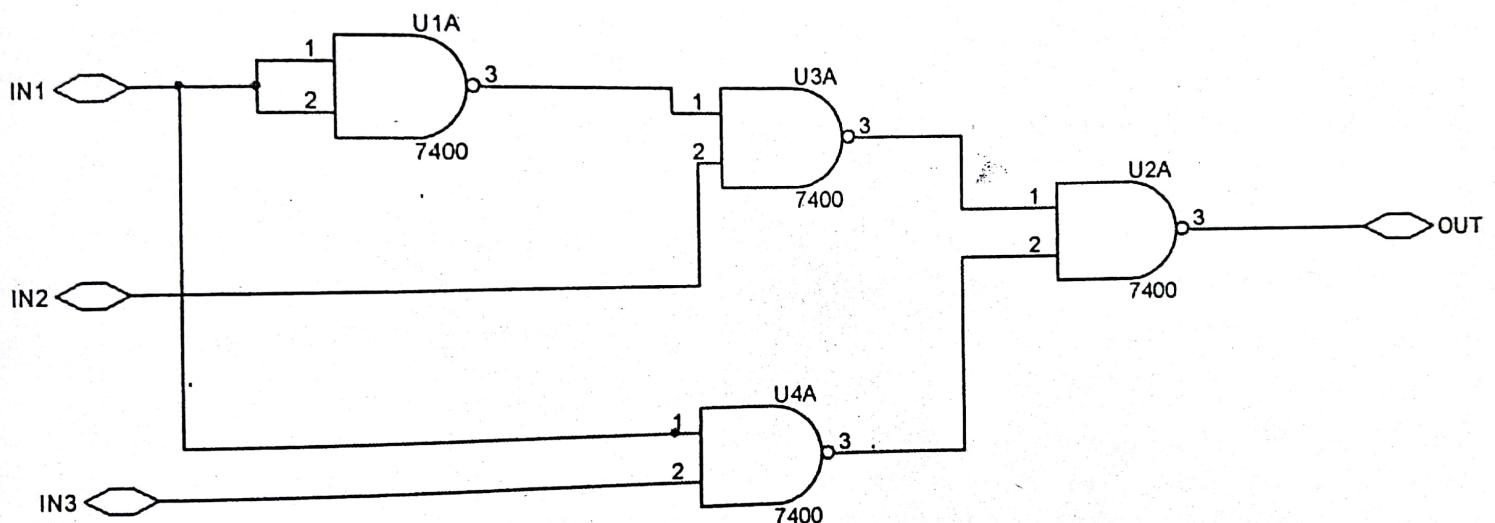
1. All connections should be tight & accurate
2. Power supply should be switched OFF after the experiment.

• Result

Truth table of 2:1 Mux was verified.

Ans

2:1 MULTIPLEXER USING NAND



Experiment 6

- Aim: Design SR flip flop using NAND gates.
- Equipment: Breadboard, connecting wires, power supply IC 7400.

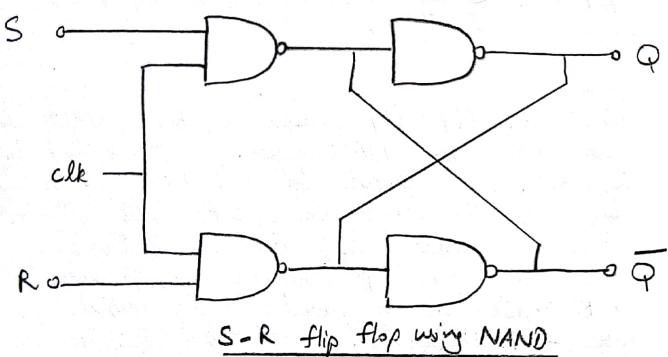
Theory

The S-R flip-flop consists of basic NAND latch and two other NAND gates. If the clock input is low, the output of both NAND gates is high & the changes in S & R inputs will not affect the output (Q) of the flip flop.

When the clock input becomes HIGH, the value at S & R inputs will be passed to the output of the first 2 NAND gates, & the output (Q) of the flip flop will change acc. to the changes in S & R inputs.

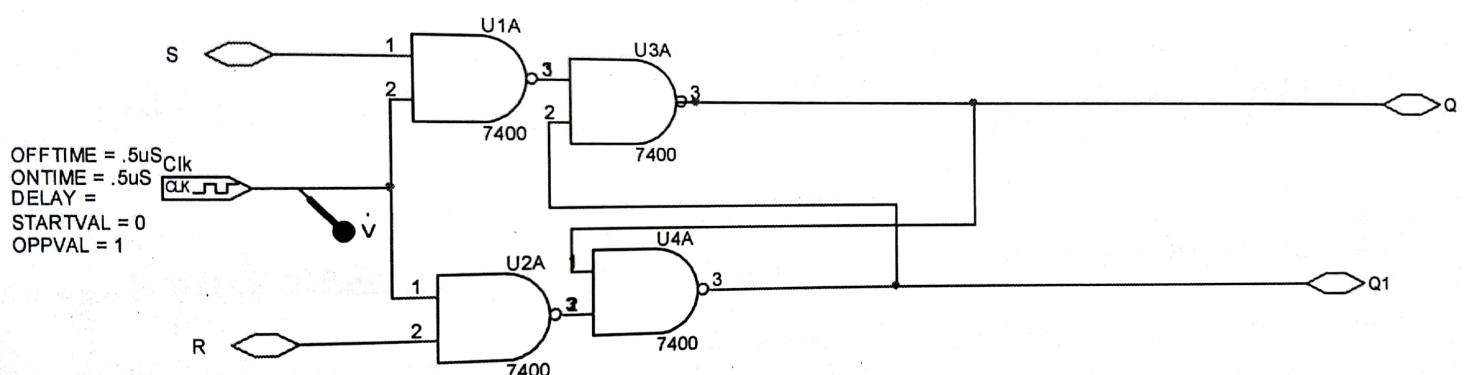
INPUTS		OUTPUTS		ACTION
S	R	Q_{n+1}	Q_n	
0	0	Q_n	Q_n	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	?	?	Not allowed

The outputs have been found out assuming the clock to be HIGH.



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<ul style="list-style-type: none"> • <u>Procedure</u> 	<ol style="list-style-type: none"> 1. Connect NAND gate ICs to perform SR flip flop connections. 2. Verify the truth table.
<ul style="list-style-type: none"> • <u>Precautions</u> 	<ol style="list-style-type: none"> 1. All connections should be acc. to circuit diag. 2. Power supply should be turned off after the expt.
<ul style="list-style-type: none"> • <u>Result</u> 	<p>SR flip flop has been designed & its truth table verified.</p> <p style="text-align: right;">WV</p>

SR-flipflop



Experiment - 7

- Aim: Design JK flip flop using NAND gate.
- Equipment: Breadboard, wires, power supply, IC-7400.

Theory:

J-K flip-flop has characteristics similar to that of an SR flip-flop. In addition, the uncertain condition of S-R flip-flop ($S=R=1$) is permitted in it.

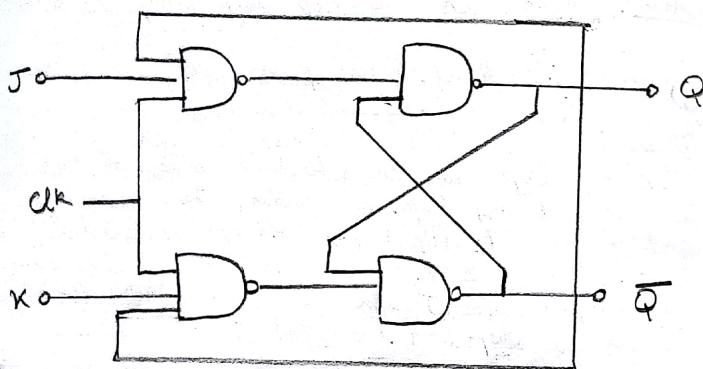
Data inputs are J & K which are AND with \bar{Q} & Q respectively such that -

$$S = J \cdot \bar{Q}$$

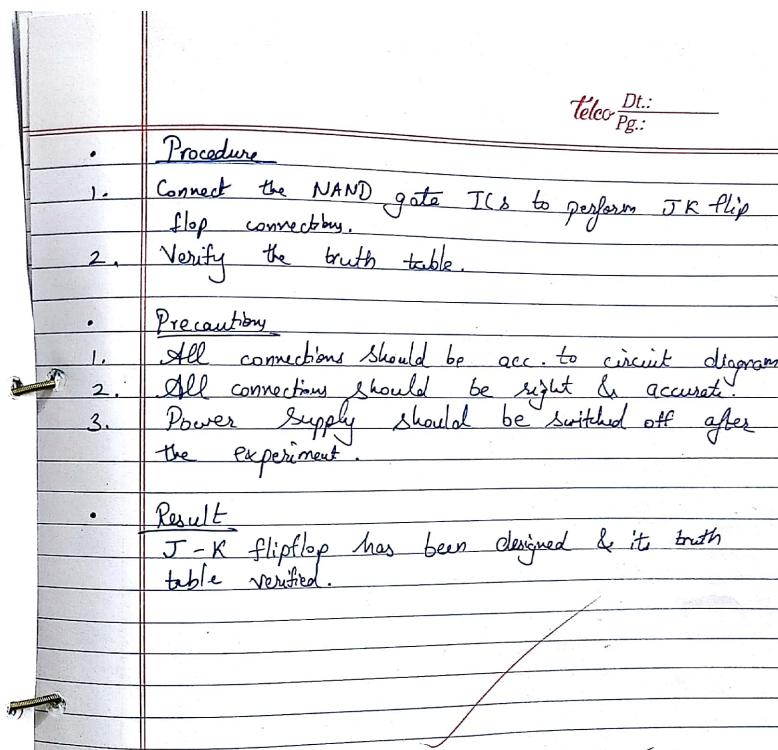
$$R = K \cdot Q$$

Inputs J & K behave like inputs S & R to set & reset the flip flop resp. When $J=K=1$, the flip flop output toggles, i.e. switches to its complement state; if $Q=0$ it switches to $Q=1$ & vice-versa.

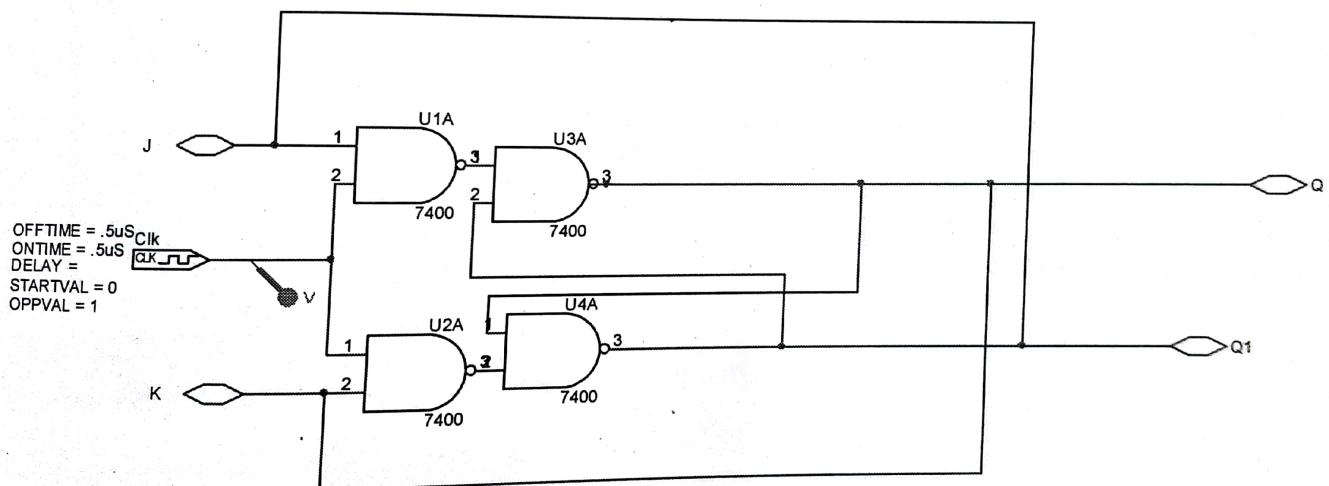
Clock	Input		Output Q_{n+1}	Action
	J	K		
X	0	0	Q_n	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	\bar{Q}_n	Toggle



JK flip flop using NAND



JK-flipflop



Experiment 8

- Aim: To design a binary to gray converter.
- Equipments: Breadboard, connecting wires, 74LS86 Quad 2 EXOR gate
- Theory

The conversion from one code to another is common in digital systems. Sometimes the output of a system is used as the input to other systems. Code converter is a circuit that makes two systems compatible even though each uses different binary code. There are four inputs & outputs. Gray code is a non-weighted code.

- Binary to Gray code conversion:

1. MSB Gray Code = MSB Binary Code

2. From left to right, add each adjacent pair of binary code bits to get next gray code bit.

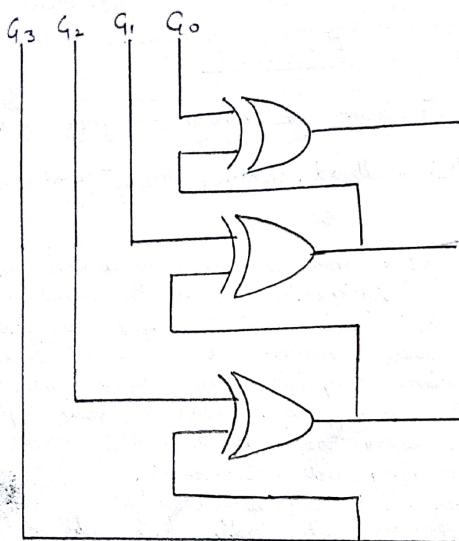
Discard other.

E.g. Consider the decimal no. 68.

$$(68)_{10} = (1000100)_2$$

$$\text{Binary code} = 1000100$$

$$\text{Gray code} = 1100110$$



Binary to Gray Converter

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Decimal	Binary Code (I/p)	Gray Code (O/p)
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0

Procedure
Using the derived expression, implement binary to gray code converter using logic gates & verify its function table.

Precaution

- All connections should be correct.
- Switch off power supply after expt.

Result
We implemented & designed binary to gray code converter & verified its truth table.

Experiment 9

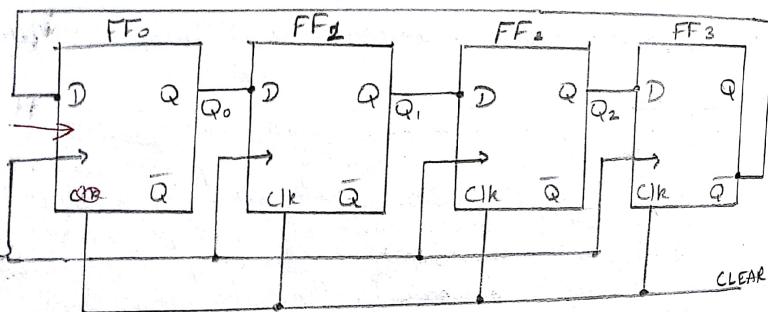
- Aim: To design a shift register using D flip flop.
- Equipment: Breadboard, connecting wires, D flip flop, NAND gates.

Theory

A shift register is an n-bit register with provision for shifting its stored data by one position at each clock pulse. The logical configuration of a shift register consists of a chain of flip flops connected in cascade, with the output of one flip flop connected to the input of next flip flop. All flip flops receive a common clock pulse which causes the shift from one stage to next. The basic type of shift registers are: Serial In - Serial Out, Parallel in - serial out, serial in - parallel out, parallel in - parallel out. Bidirectional shift registers

Clock Pulse	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0

Diagram



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Procedure

Connect the two IC 7474 D flip flop to perform its function. Verify the truth table.

Precaution

- All connections should be acc. to diagram.
- Turn off power when not in use.

Result

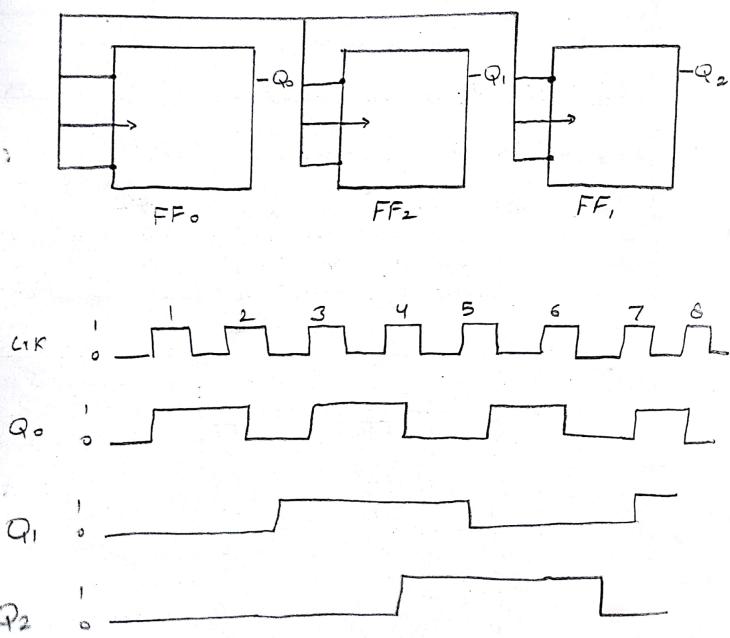
Shift register using D-flip flop has been designed & its truth table verified.

Experiment 10

- Aim : To design an asynchronous counter using JK FF.
- Equipments : Breadboard, wires, IC 7473, JK FF.
- Theory : Asynchronous counter is a sequential circuit that is used to count the no. of clock input signal. The output of one flip flop is given as clock pulse to another FF, so it is called a serial counter.

Truth Table

FF ₂	FF ₁	FF ₀
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



Procedure	
1.	Connect the two IC 7473 JK flip flop & perform its function on breadboard, and software.
2.	Verify truth table.
Precaution	
1.	All connections should be accurate.
2.	Turn off the circuit after performing.
Result	
<p>An asynchronous (ripple) counter using JK flip flop has been designed & verified.</p> <p style="text-align: right;">(Signature)</p>	