Mahatma Gandhi Mission's College of Engineering and Technology
Kamothe,Navi Mumbai

MAHATMA GANDHI MISSION

Department of Computer Engineering

Course Code: CSC405 **Course Name: Microprocessor**

Assignment No. 1

Class: SE **AY: 2021-22**

Q.No	Question
Q1.Justify Your Answers	
	(a) CX register is used as a default counter in case of string and loop instructions..
	(b) If MN/MX is low the 8086 operates in MAX mode.
	(c) The 1 MB byte of memory can be divided into 64 kbyte segment.
	(d) In 8086 microprocessor , the address bus is 16 bit wide
	(e) 8086 Microprocessor supports 2 modes of operation.
Q2. Choose Correct Options	
	(a) In a segment if offset is a 16-bit number, then the maximum possible locations are_____. a) 1 KB b) 64 bytes c) 64 KB d) 1 MB
	(b) In which T-state does the CPU sends the address to memory or I/O and the ALE signal for demultiplexing. A.T1 B.T2 C.T3 D.T4
	(c) In 8086 microprocessor the following has the highest priority among all type interrupts. a) NMI b) DIV 0 c) TYPE 255 d) OVER FLOW
	(d) 8088 microprocessor differs with 8086 microprocessor in a) Data width on the output b) Address capability c) Support of coprocessor d) Support of MAX / MIN mode
	(e) In 8086 the overflow flag is set when a) The sum is more than 16 bits b) Signed numbers go out of their range after an arithmetic operation c) Carry and sign flags are set d) During subtraction
Q3. State whether the following statements are true or false (Give Reasons)	
	(a) In 8086 microprocessor one of the following statements is not true. a) Coprocessor is interfaced in MAX mode b) Coprocessor is interfaced in MIN mode c) I/O can be interfaced in MAX / MIN mode d) Supports pipelining .
	(b)EU takes care of all the address and data transfers on the buses.(True/False)
	(c) 8086 has 6 active flags. (True/False)
Q4. Name the following or define or design the following	
	(a) Write the main function of EU and BIU. Ans: Main function of EU is to execute instructions that have already been fetched by the BIU. Main function of BIU is to fetch instructions , read data from memory and I/O ports, writes data to memory and I/O ports.
	(b) Name the Programming model of 8086 processor. Ans: X-86 family of advanced microprocessors is the programming model of 8086 processor.
	(c) How to find physical address in 8086(starting address of code segment is 248A H and offset in IP address is 4114H)?

Ans: 248A H

4114 H

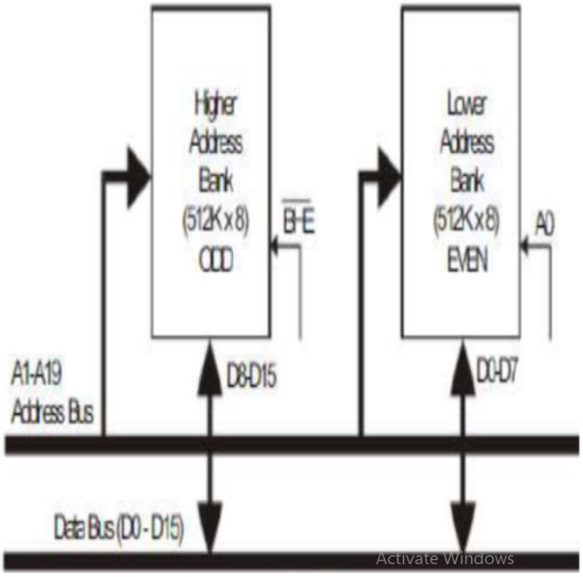
FEI5G

Q5. Answer the following questions in brief (20 to 30 words)

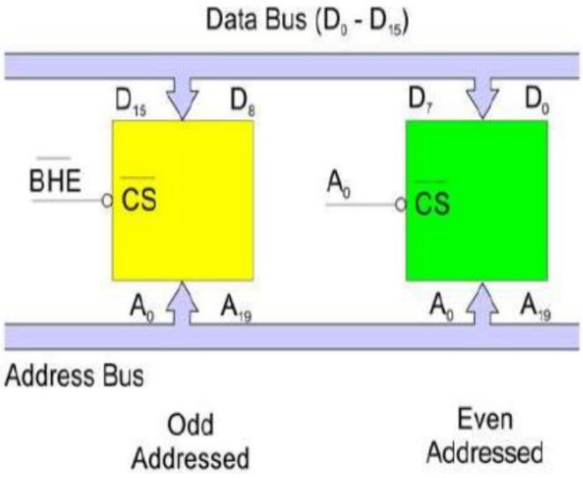
(a) Justify how memory bank is used in 8086 microprocessor.

Ans:

- The **8086** has 20-bit address bus, so it can address **2^20 or 10,48,576** addresses.
- Each address represents a stored byte.
- To make it possible to read or write a word with one machine cycle, the **memory** for an **8086** is set up in to **2 banks** of up to **5,24,288** bytes each.



- **Memory IC's:** Byte oriented
- **Word:** Stored by two consecutive memory location for **LSB** and **MSB**
- **Address of Word:** Address of **LSB**
- **Bank 0:** $A_0 = 0 \Rightarrow$ Even Address Memory Bank
- **Bank 1:** $\overline{BHE} = 0 \Rightarrow$ Odd Address Memory Bank



(b) Try to find out the advantages of segmented memory with reference to the 8086 microprocessor.

Ans: The main advantages of segmentation are as follows:

- It provides a powerful memory management mechanism.
- Data related or stack related operations can be performed in different segments.
- Code related operation can be done in separate code segments.
- It allows to processes to easily share data.
- It allows to extend the address ability of the processor, i.e. segmentation allows the use of 16 bit registers to give an addressing capability of 1 Megabytes. Without segmentation, it would require 20 bit registers.
- It is possible to enhance the memory size of code data or stack segments beyond 64 KB by allotting more than one segment for each area.

(c) Justify with your answer What happens when 8086 mp receives DMA request on RQ/GT_0 & RQ/GT_1 pins simultaneously.

Ans: In the maximum mode, the 8086 is operated by strapping the MN/MX pin to ground. The pins that have a function in maximum mode are as given follows. • S2, S1 & S0:- The states bits indicate the function of current cycle. These signals are normally decoded by the 8288. • LOCK: - The LOCK output is used to look peripheral off the system. This pin is activated by using LOCK prefix on any instruction. • RQ/GT0 & RQ/GT1:- The request/grant pins request DMA during the maximum mode operations of 8086. These lines are bi-directional and are used to request and grant a DMA operation. • QS1 & QS0:- The queue states bit show the states of the internal instruction queue in 8086.

S2	S1	S0	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive state

. Q6. Answer the following questions in brief (50 to 70 words)

(a) Draw and explain in detail Maximum and minimum mode configuration of 8086?

Ans: Minimum Mode 8086 System

The microprocessor 8086 is operated in minimum mode by strapping its MN/MX pin to logic 1.

In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.

The remaining components in the system are latches, trans receivers, clock generator, memory and I/O devices.

Latches are generally buffered output D-type flip-flops like 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.

Minimum Mode Configuration For 8086

Trans receivers are the bidirectional buffers and sometimes they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals. They are controlled by two signals namely, DEN and DT/R.

The DEN signal indicates the direction of data, i.e. from or to the processor.

The system contains memory for the monitor and users program storage. Usually, EPROM are used for monitor storage, while RAM for users program storage. A system may contain I/O devices.

The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

The read cycle begins in T1 with the assertion of address latch enable (ALE) signal and also

M / IO signal. During the negative going edge of this signal, the valid address is latched on the local bus.

The BHE and A0 signals address low, high or both bytes. From T1 to T4, the M/IO signal indicates a memory or I/O operation.

At T2, the address is removed from the local bus and is sent to the output. The bus is then tristate. The read (RD) control signal is also activated in T2.

The read (RD) signal causes the address device to enable its data bus drivers. After RD goes low, the valid data is available on the data bus.

The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tristate its bus drivers.

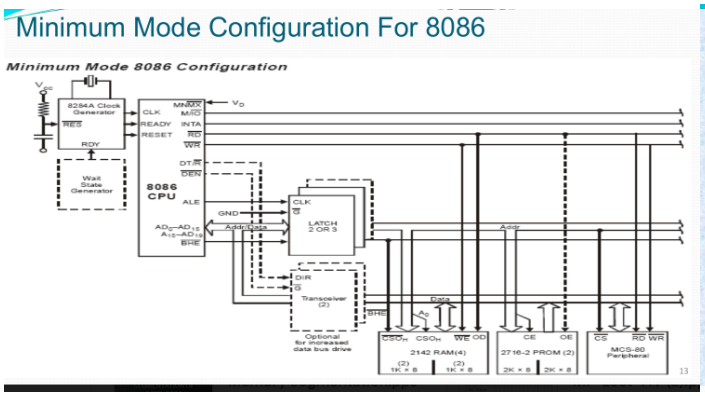
A write cycle also begins with the assertion of ALE and the emission of the address.

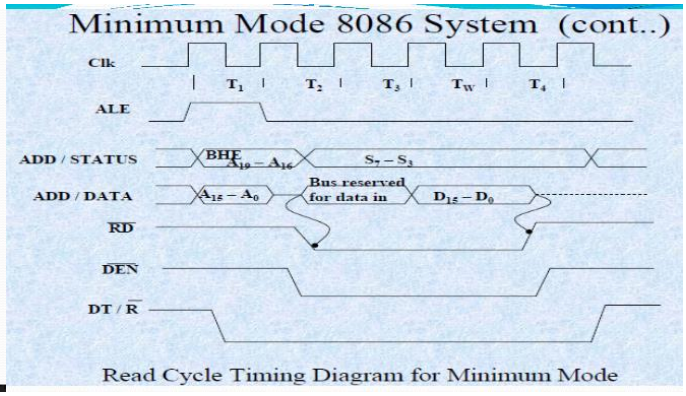
The M/IO signal is again asserted to indicate a memory or I/O operation. In T2, after sending the address in T1, the processor sends the data to be written to the addressed location.

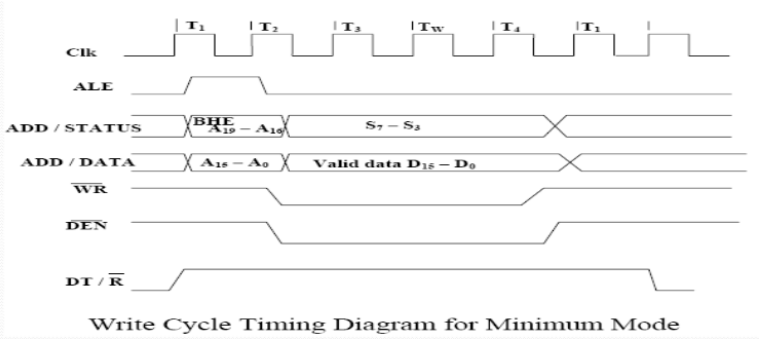
The data remains on the bus until middle of T4 state. The WR becomes active at the beginning of T2 (unlike RD is somewhat delayed in T2 to provide time for floating).

The BHE and A0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.

The M/IO, RD and WR signals indicate the type of data transfer as specified in table below.







Maximum Mode 8086 System

In the maximum mode, the 8086 is operated by strapping the MN/MX pin to ground.

In this mode, the processor derives the status signal S2, S1, S0.

Another chip called bus controller derives the control signal using this status information .

In the maximum mode, there may be more than one microprocessor in the system configuration. The components in the system are same as in the minimum mode system.

The basic function of the bus controller chip IC8288, is to derive control signals like RD and WR (for memory and I/O devices), DEN, DT/R, ALE etc. using the information by the processor on the status lines.

The bus controller chip has input lines S2, S1, S0 and CLK. These inputs to 8288 are driven by CPU.

It derives the outputs ALE, DEN, DT/R, MRDC, MWTC, AMWC, IORC, IOWC and AIOWC. The AEN, IOB and CEN pins are especially useful for multiprocessor systems.

AEN and IOB are generally grounded. CEN pin is usually tied to +5V. The significance of the MCE/PDEN output depends upon the status of the IOB pin.

INTA pin used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.

IORC, IOWC are I/O read command and I/O write command signals respectively .

These signals enable an IO interface to read or write the data from or to the address port.

The MRDC, MWTC are memory read command and memory write command signals respectively and may be used as memory read or write signals.

All these command signals instructs the memory to accept or send data from or to the bus.

Here the only difference between in timing diagram between minimum mode and maximum mode is the status signals used and the available control and advanced command signals.

R0, S1, S2 are set at the beginning of bus cycle.8288 bus controller will output a pulse as on the ALE and apply a required signal to its DT / R pin during T1.

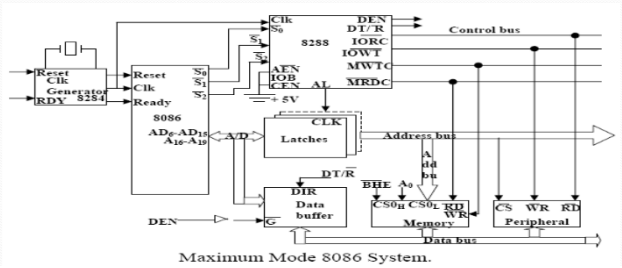
In T2, 8288 will set DEN=1 thus enabling transceivers, and for an input it will activate MRDC or IORC. These signals are activated until T4.

For an output, the AMWC or AIOWC is activated from T2 to T4 and MWTC or IOWC is activated from T3 to T4.

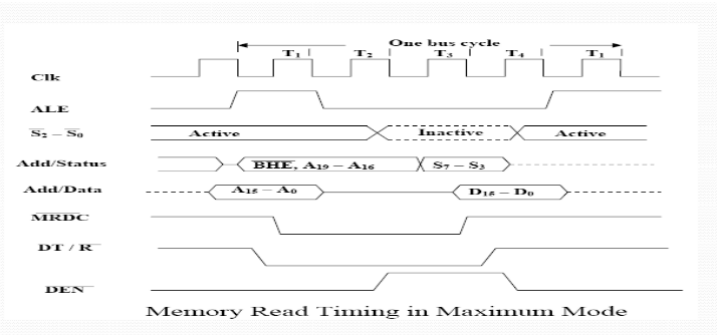
The status bit S0 to S2 remains active until T3 and become passive during T3 and T4.

If reader input is not activated before T3, wait state will be inserted between T3 and T4.

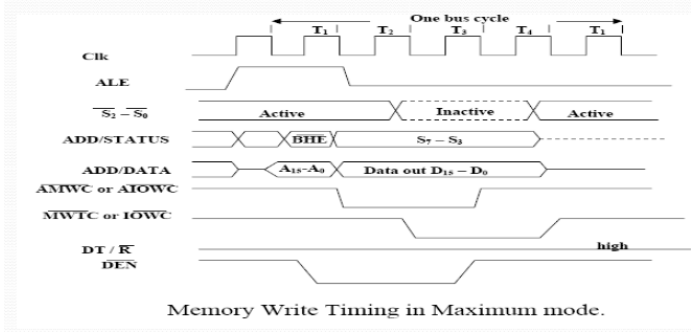
Maximum Mode Configuration For 8086



Maximum Mode 8086 System.



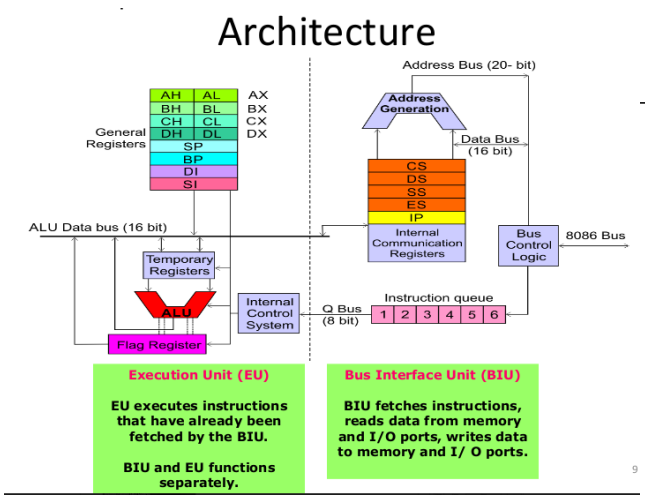
Memory Read Timing in Maximum Mode

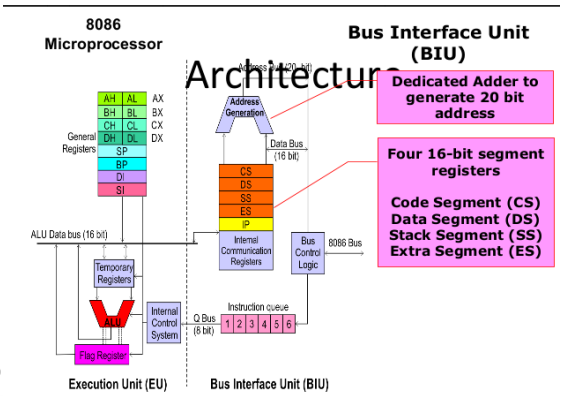


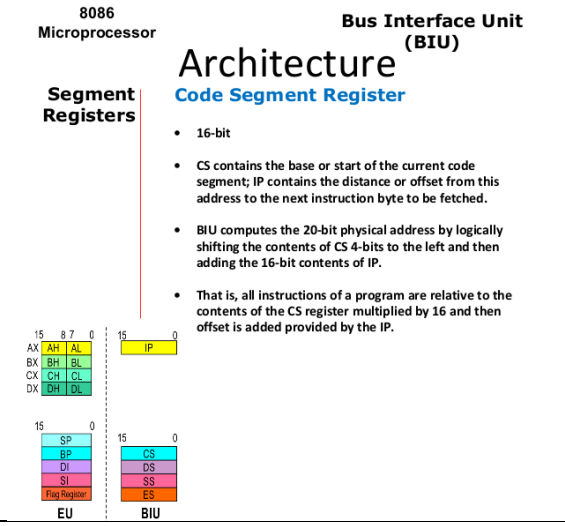
Memory Write Timing in Maximum mode.

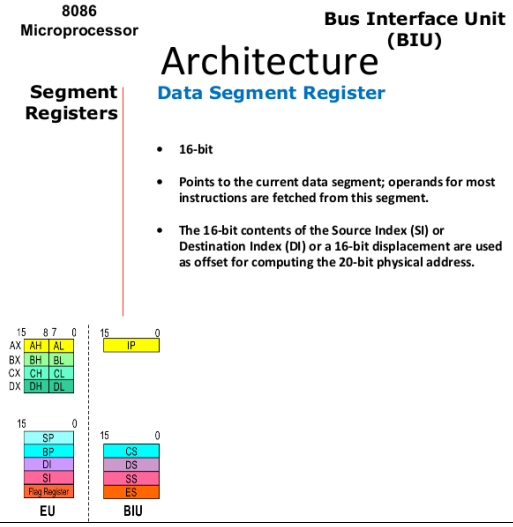
(b) Draw and explain the architecture of 8086 .

Ans:









8086 Microprocessor

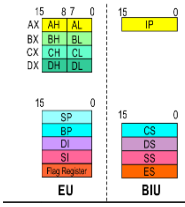
Bus Interface Unit (BIU)

Architecture

Segment Registers

Stack Segment Register

- 16-bit
- Points to the current stack.
- The 20-bit physical stack address is calculated from the Stack Segment (SS) and the Stack Pointer (SP) for stack instructions such as PUSH and POP.
- In based addressing mode, the 20-bit physical stack address is calculated from the Stack segment (SS) and the Base Pointer (BP).



8086 Microprocessor

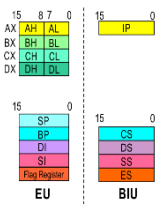
Bus Interface Unit (BIU)

Architecture

Segment Registers

Extra Segment Register

- 16-bit
- Points to the extra segment in which data (in excess of 64K pointed to by the DS) is stored.
- String instructions use the ES and DI to determine the 20-bit physical address for the destination.



8086 Microprocessor

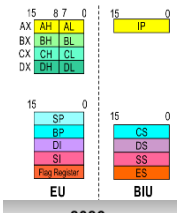
Bus Interface Unit (BIU)

Architecture

Segment Registers

Instruction Pointer

- 16-bit
- Always points to the next instruction to be executed within the currently executing code segment.
- So, this register contains the 16-bit offset address pointing to the next instruction code within the 64Kb of the code segment area.
- Its content is automatically incremented as the execution of the next instruction takes place.



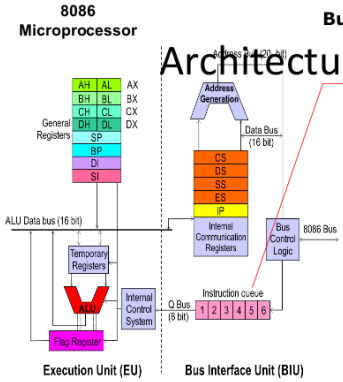
8086 Microprocessor

Bus Interface Unit (BIU)

Architecture

Instruction queue

- A group of First-In-First-Out (FIFO) in which up to 6 bytes of instruction code are pre fetched from the memory ahead of time.
- This is done in order to speed up the execution by overlapping instruction fetch with execution.
- This mechanism is known as pipelining.



8086 Microprocessor

Execution Unit (EU)

Architecture

EU decodes and executes instructions.

A decoder in the EU control system translates

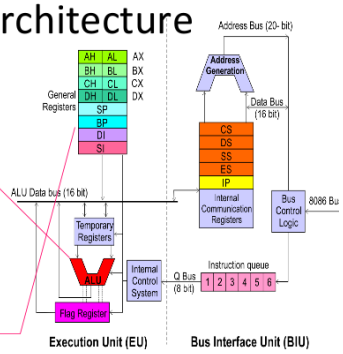
16-bit ALU for performing arithmetic and logic operation

Four general purpose registers(AX, BX, CX, DX);

Pointer registers (Stack Pointer, Base Pointer);

and

Index registers (Source Index, Destination Index) each of 16-bits



Some of the 16 bit registers can be used as two 8 bit registers as :

AX can be used as AH and AL
BX can be used as BH and BL
CX can be used as CH and CL

8086 Microprocessor

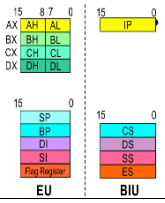
Execution Unit (EU)

Architecture

EU Registers

Accumulator Register (AX)

- Consists of two 8-bit registers AL and AH, which can be combined together and used as a 16-bit register AX.
- AL in this case contains the low order byte of the word, and AH contains the high-order byte.
- The I/O instructions use the AX or AL for inputting / outputting 16 or 8 bit data to or from an I/O port.
- Multiplication and Division instructions also use the AX or AL.



8086 Microprocessor

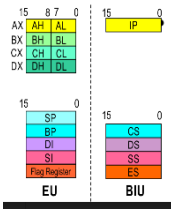
Execution Unit (EU)

Architecture

EU Registers

Base Register (BX)

- Consists of two 8-bit registers BL and BH, which can be combined together and used as a 16-bit register BX.
- BL in this case contains the low-order byte of the word, and BH contains the high-order byte.
- This is the only general purpose register whose contents can be used for addressing the 8086 memory.
- All memory references utilizing this register content for addressing use DS as the default segment register.



8086 Microprocessor

Execution Unit (EU)

Architecture

EU Registers

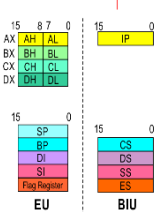
Counter Register (CX)

- Consists of two 8-bit registers CL and CH, which can be combined together and used as a 16-bit register CX.
- When combined, CL register contains the low order byte of the word, and CH contains the high-order byte.
- Instructions such as SHIFT, ROTATE and LOOP use the contents of CX as a counter.

Example:

The instruction LOOP START automatically decrements CX by 1 without affecting flags and will check if [CX] = 0.

If it is zero, 8086 executes the next instruction; otherwise the 8086 branches to the label START.



8086 Microprocessor

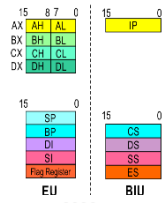
Execution Unit (EU)

Architecture

EU Registers

Data Register (DX)

- Consists of two 8-bit registers DL and DH, which can be combined together and used as a 16-bit register DX.
- When combined, DL register contains the low order byte of the word, and DH contains the high-order byte.
- Used to hold the high 16-bit result (data) in 16 X 16 multiplication or the high 16-bit dividend (data) before a 32 ÷ 16 division and the 16-bit reminder after division.



8086 Microprocessor

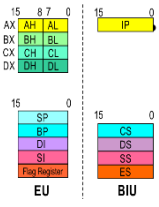
Execution Unit (EU)

Architecture

EU Registers

Stack Pointer (SP) and Base Pointer (BP)

- SP and BP are used to access data in the stack segment.
- SP is used as an offset from the current SS during execution of instructions that involve the stack segment in the external memory.
- SP contents are automatically updated (incremented/ decremented) due to execution of a POP or PUSH instruction.
- BP contains an offset address in the current SS, which is used by instructions utilizing the based addressing mode.



8086 Microprocessor

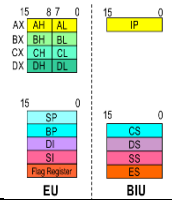
Execution Unit (EU)

Architecture

EU Registers

Source Index (SI) and Destination Index (DI)

- Used in indexed addressing.
- Instructions that process data strings use the SI and DI registers together with DS and ES respectively in order to distinguish between the source and destination addresses.



8086 Microprocessor

Execution Unit (EU)

Architecture

EU Registers

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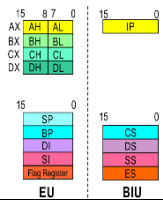
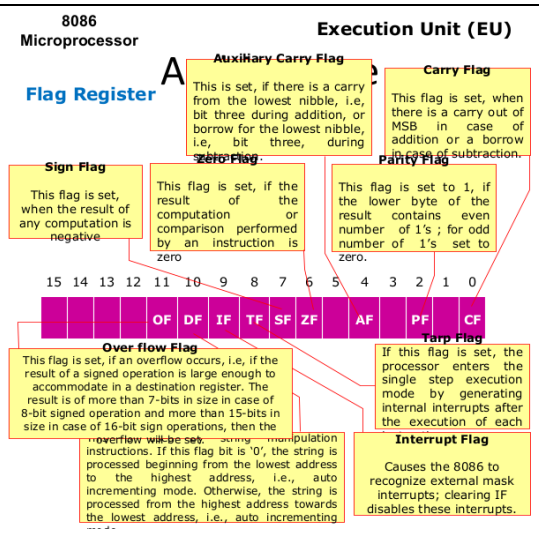
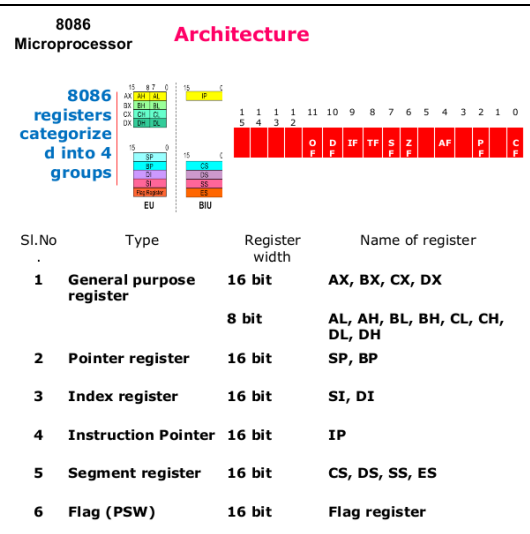






Sl.No.	Type	Register width	Name of register
1	General purpose register	16 bit	AX, BX, CX, DX
		8 bit	AL, AH, BL, BH, CL, CH, DL, DH
2	Pointer register	16 bit	SP, BP
3	Index register	16 bit	SI, DI
4	Instruction Pointer	16 bit	IP
5	Segment register	16 bit	CS, DS, SS, ES
6	Flag (PSW)	16 bit	Flag register

(c) Draw and Explain memory read and memory write machine cycle timing diagrams in minimum and maximum mode of 8086.?

Ans: The timing diagram for read operation in minimum mode is shown in fig below:

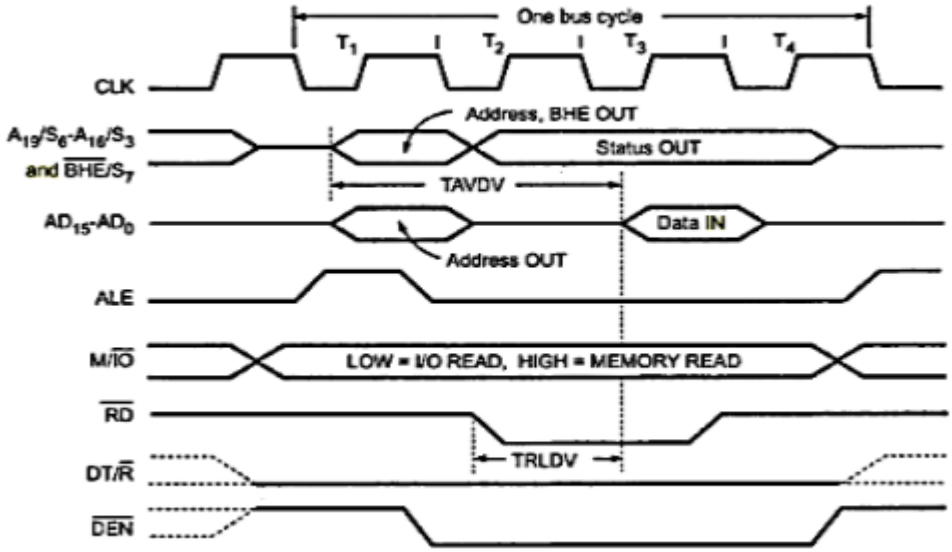


Fig. 7.13 (a) Input (read operation)

These are explained in steps.

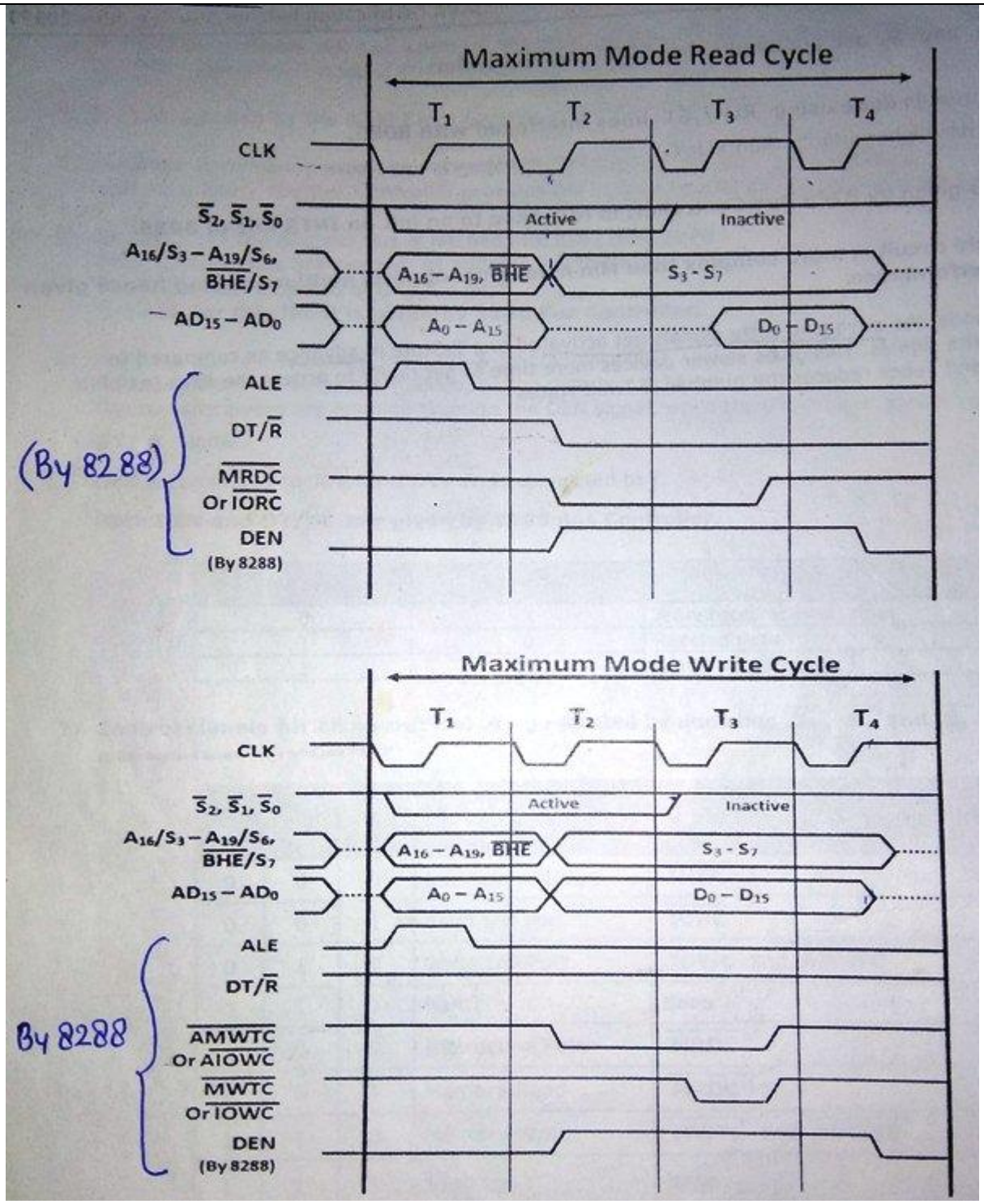
1. When processor is ready to initiate the bus cycle, it applies a pulse to ALE during T1. Before the falling edge of ALE, the address, BHE, M/IO, DEN and DT/R must be stable i.e. DEN = high and DT/R = 0 for input or DT/R = 1 for output.
2. At the trailing edge of ALE, ICs 74LS373 or 8282 latches the address.
3. During T2 the address signals are disabled and S3-S7 ale available on AD16/S3-AD19/S6 and BHE/S7. Also DEN is lowered to enable transceiver.
4. In case of input operation, RD is activated during T2 and AD° to AD15 go in high impedance preparing for input.
5. If memory or I/O interface can perform the transfer immediately; there are no wait states and data is output on the bus during T3.
6. After the data is accepted by the processor, RD is raised high at the beginning of T4.
7. Upon detecting this transition during T.4, the memory or I/O device will disable its data signals.

8. For an output operation, processor applies WR = 0 and then the data on the data bus during T2.
9. In T4, WR is raised high and data signals are disabled.
10. For either input or output operation, DEN is raised during 14 to disable the transceiver. Also M/I0 is set according to the next transfer at this time or during next T1 state. Thus length of bus cycle in 8086 is four clock cycle. If the bus is to be inactive after completion of bus cycle, then the gap between the successive cycles is filled by ideal state clock cycles.

When the memory or I/O device is not able to respond quickly during transfer, wait states (Tw) are inserted between T3 and T4 by disabling the READY input of the 8086. The bus activity during wait state is same as during T3.

The timing diagram for write operation in minimum mode is shown in fig above:

- When processor is ready to initiate the bus cycle, it applies a pulse to ALE during T1. Before the falling edge of ALE, the address, BHE, M/IO, DEN and DT/R must be stable i.e. DEN = high and DT/R = 0 for input or DT/R = 1 for output.
- At the trailing edge of ALE, ICs 74LS373 or 8282 latches the address.
- During T2 the address signals are disabled and S3-S7 ale available on AD16/S3-AD19/S6 and BHE/S7. Also DEN is lowered to enable transceiver.
- In case of input operation, RD is activated during T2 and AD° to AD15 go in high impedance preparing for input.
- If memory or I/O interface can perform the transfer immediately; there are no wait states and data is output on the bus during T3.
- After the data is accepted by the processor, RD is raised high at the beginning of T4. Upon detecting this transition during T.4, the memory or I/O device will disable its data signals. For an output operation, processor applies WR = 0 and then the data on the data bus during T2. In T4, WR is raised high and data signals are disabled.
- For either input or output operation, DEN is raised during 14 to disable the transceiver. Also M/I0 is set according to the next transfer at this time or during next T1 state. Thus length of bus cycle in 8086 is four clock cycle.
- If the bus is to be inactive after completion of bus cycle, then the gap between the successive cycles is filled by ideal state clock cycles.
- When the memory or I/O device is not able to respond quickly during transfer, wait states (Tw) are inserted between T3 and T4 by disabling the READY.



- It is a multiprocessor mode. Along with 8086, there can be other processors like 8087 and 8089 in the circuit. Here MN/¯MX is connected to ground itself.
- Since, there are multiple processors; ALE for the latch is given by 8288 bus controller. Instead of 8086 control signals are generated by bus controller 8288 using special decoding of status pins ¯(S0,) ¯(S1,) ¯S2.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State (What the µP wants to do)	8288 Active Output (What Control signal should 8288 generate)
0	0	0	Int. Acknowledge	$\overline{\text{INTA}}$
0	0	1	Read I/O Port	$\overline{\text{IORC}}$
0	1	0	Write I/O Port	$\overline{\text{IOWC}}$ and $\overline{\text{AIOWC}}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{\text{MRDC}}$
1	0	1	Memory Read	$\overline{\text{MRDC}}$
1	1	0	Memory Write	$\overline{\text{MWTC}}$ and $\overline{\text{AMWTC}}$
1	1	1	Inactive	None

- Since 8288 independently generates control signals, it needs a CLK from 8284 clock generator.

Q7. Think and Answer

(a) Why is the 8086 Queue only six byte long?

Ans: This is because the longest instruction in the instruction set of **8086** is **six byte long**. Hence with a **six byte long queue** it is possible to pre-fetch even the longest instruction in the main program.

(b) Justify the memory segmentation in Intel 8086 processor with its advantage and disadvantages.

Ans: **Segmentation** is the process in which the main memory of the computer is logically divided into different segments and each segment has its own base address. It is basically used to enhance the speed of execution of the computer system, so that the processor is able to fetch and execute the data from the memory easily and fast.

Need for Segmentation –

The Bus Interface Unit (BIU) contains four 16 bit special purpose registers (mentioned below) called as Segment Registers.

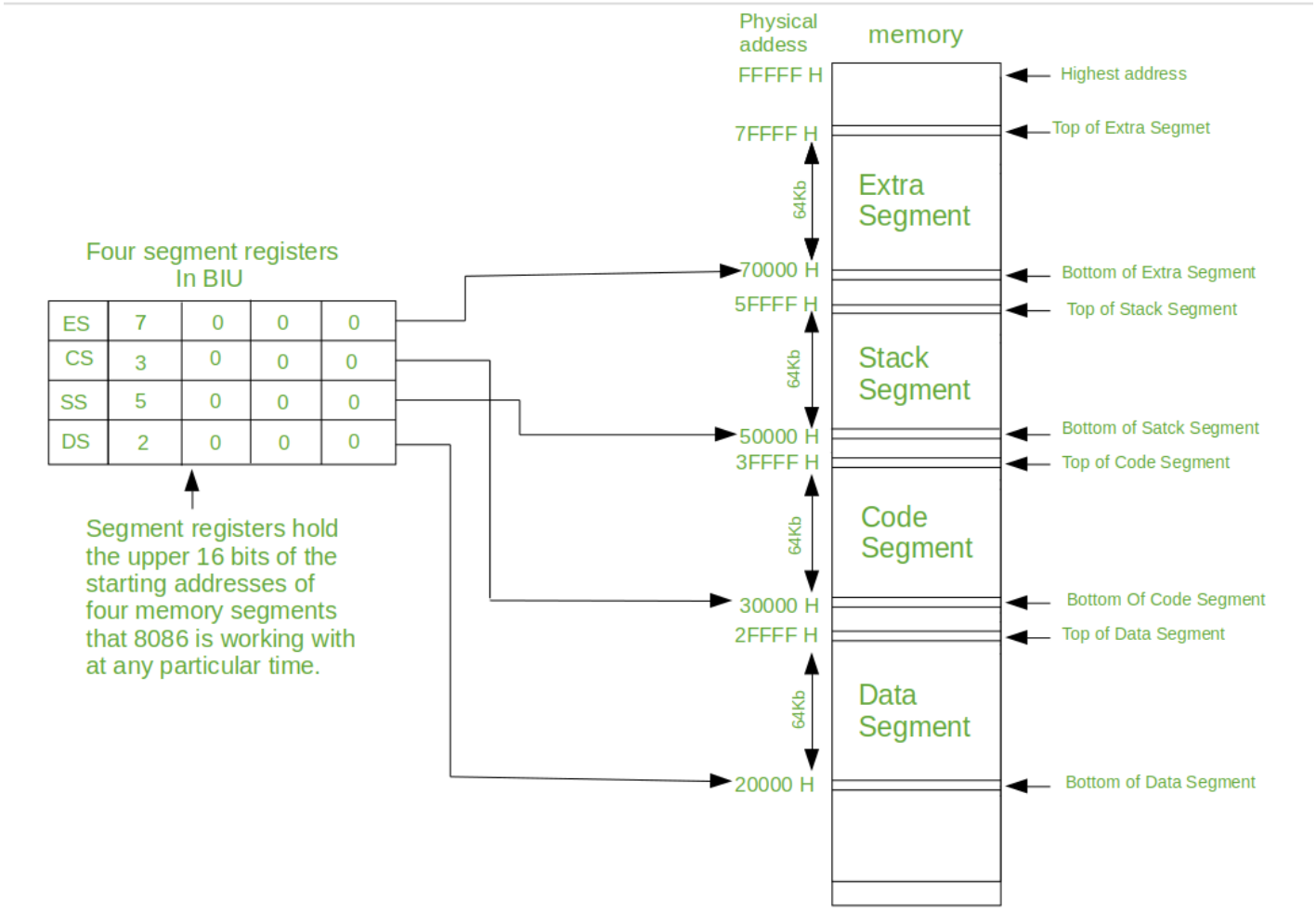
- **Code segment register (CS):** is used for addressing memory location in the code segment of the memory, where the executable program is stored.
- **Data segment register (DS):** points to the data segment of the memory where the data is stored.
- **Extra Segment Register (ES):** also refers to a segment in the memory which is another data segment in the memory.
- **Stack Segment Register (SS):** is used for addressing stack segment of the memory. The stack segment is that segment of memory which is used to store stack data.

The number of address lines in 8086 is 20, 8086 BIU will send 20bit address, so as to access one of the 1MB memory locations. The four segment registers actually contain the upper 16 bits of the starting addresses of the four memory segments of 64 KB each with which the 8086 is working at that instant of time. A segment is a logical unit of memory

that may be up to 64 kilobytes long. Each segment is made up of contiguous memory locations. It is an independent, separately addressable unit. Starting address will always be changing. It will not be fixed.

Note that the 8086 does not work the whole 1MB memory at any given time. However, it works only with four 64KB segments within the whole 1MB memory.

Below is the one way of positioning four 64 kilobyte segments within the 1M byte memory space of an 8086.



Types Of Segmentation –

1. **Overlapping Segment –** A segment starts at a particular address and its maximum size can go up to 64kilobytes. But if another segment starts along with this 64kilobytes location of the first segment, then the two are said to be *Overlapping Segment*.
2. **Non-Overlapped Segment –** A segment starts at a particular address and its maximum size can go up to 64kilobytes. But if another segment starts before this 64kilobytes location of the first segment, then the two segments are said to be *Non-Overlapped Segment*.

Rules of Segmentation Segmentation process follows some rules as follows:

- The starting address of a segment should be such that it can be evenly divided by 16.

- Minimum size of a segment can be 16 bytes and the maximum can be 64 kB.

Segment	Offset Registers	Function
CS	IP	Address of the next instruction
DS	BX, DI, SI	Address of data
SS	SP, BP	Address in the stack
ES	BX, DI, SI	Address of destination data (for string operations)

Advantages of the Segmentation The main advantages of segmentation are as follows:

- It provides a powerful memory management mechanism.
- Data related or stack related operations can be performed in different segments.
- Code related operation can be done in separate code segments.
- It allows to processes to easily share data.
- It allows to extend the address ability of the processor, i.e. segmentation allows the use of 16 bit registers to give an addressing capability of 1 Megabytes. Without segmentation, it would require 20 bit registers.
- It is possible to enhance the memory size of code data or stack segments beyond 64 KB by allotting more than one segment for each area.

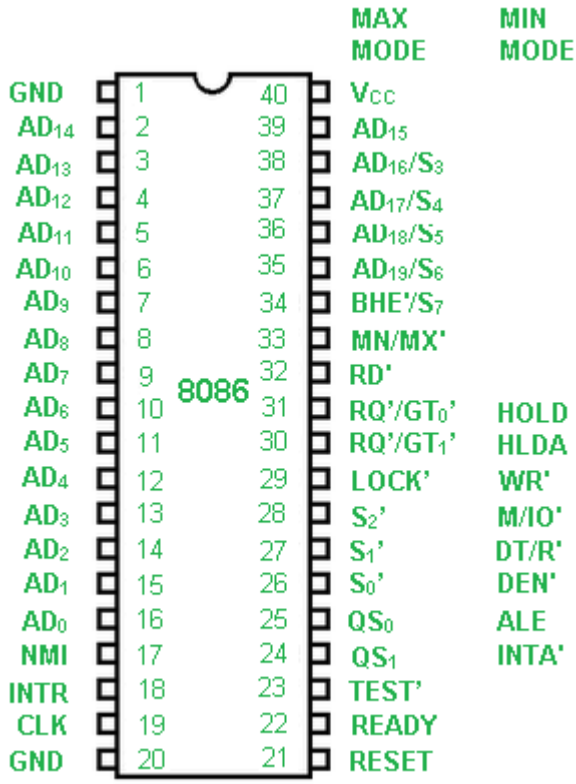
Disadvantages of Memory Segmentation

- It is a costly technique as compared to the other one.
- External fragmentation is there in it.
- Since there is a variably sized partition. So, it is difficult to allocate memory to them.

Q8. **My Ideas**

(a) Design the real time application using of microprocessor 8086 new hardware required to generate clock and reset the signal.

Ans: Pin diagram of 8086 microprocessor is as given below:



Intel 8086 is a 16-bit HMOS microprocessor. It is available in 40 pin DIP chip. It uses a 5V DC supply for its operation. The 8086 uses 20-line address bus. It has a 16-line data bus. The 20 lines of the address bus operate in multiplexed mode. The 16-low order address bus lines have been multiplexed with data and 4 high-order address bus lines have been multiplexed with status signals.

AD0-AD15 : Address/Data bus. These are low order address bus. They are multiplexed with data. When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A0-A15. When data are transmitted over AD lines the symbol D is used in place of AD, for example D0-D7, D8-D15 or D0-D15.
A16-A19 : High order address bus. These are multiplexed with status signals.
S2, S1, S0 : Status pins. These pins are active during T4, T1 and T2 states and is returned to passive state (1,1,1 during T3 or Tw (when ready is inactive). These are used by the 8288 bus controller for generating all the memory and I/O operation) access control signals. Any change in S2, S1, S0 during T4 indicates the beginning of a bus cycle.

S2	S1	S0	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port

0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive state

A16/S3, A17/S4, A18/S5, A19/S6 : The specified address lines are multiplexed with corresponding status signals.

A17/S4	A16/S3	Function
0	0	Extra segment access
0	1	Stack segment access
1	0	Code segment access
1	1	Data segment access

BHE'/S7 : Bus High Enable/Status. During T1 it is low. It is used to enable data onto the most significant half of data bus, D8-D15. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S7. S7 signal is available during T2, T3 and T4.
RD': This is used for read operation. It is an output signal. It is active when low.
READY : This is the acknowledgement from the memory or slow device that they have completed the data transfer. The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the microprocessor. The signal is active high(1).
INTR : Interrupt Request. This is triggered input. This is sampled during the last clock cycles of each instruction for determining the availability of the request. If any interrupt request is found pending, the processor enters the interrupt acknowledge cycle. This can be internally masked after resulting the interrupt enable flag. This signal is active high(1) and has been synchronized internally.
NMI : Non maskable interrupt. This is an edge triggered input which results in a type II interrupt. A subroutine is then vectored through an interrupt vector lookup table which is located in the system memory. NMI is non-maskable internally by software. A transition made from low(0) to high(1) initiates the interrupt at the end of the current instruction. This input has been synchronized internally.

INTA : Interrupt acknowledge. It is active low(0) during T2, T3 and Tw of each interrupt acknowledge cycle.
MN/MX' : Minimum/Maximum. This pin signal indicates what mode the processor will operate in.
RQ'/GT1′, RQ'/GT0′ : Request/Grant. These pins are used by local bus masters used to force the microprocessor to release the local bus at the end of the microprocessor's current bus cycle. Each of the pin is bi-directional. RQ'/GT0′ have higher priority than RQ'/GT1′.
LOCK' : Its an active low pin. It indicates that other system bus masters have not been allowed to gain control of the system bus while LOCK' is active low(0). The LOCK signal will be active until the completion of the next instruction.
TEST' : This examined by a 'WAIT' instruction. If the TEST pin goes low(0), execution will continue, else the processor remains in an idle state. The input is internally synchronized during each of the clock cycle on leading edge of the clock.
CLK : Clock Input. The clock input provides the basic timing for processing operation and bus control activity. Its an asymmetric square wave with a 33% duty cycle.
RESET : This pin requires the microprocessor to terminate its present activity immediately. The signal must be active high(1) for at least four clock cycles.
Vcc : Power Supply(+5V D.C.)
GND : Ground
QS1,QS0 : Queue Status. These signals indicate the status of the internal 8086 instruction queue according to the table shown below

QS1	QS0	Status
0	0	No operation
0	1	First byte of op code from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

DT/R : Data Transmit/Receive. This pin is required in minimum systems, that want to use an 8286 or 8287 data bus transceiver. The direction of data flow is controlled through the transceiver.
DEN : Data enable. This pin is provided as an output enable for the 8286/8287 in a minimum system which uses transceiver. DEN is active low(0) during each memory and input-output access and for INTA cycles.
HOLD/HOLDA : HOLD indicates that another master has been requesting a local bus .This is an active high(1). The microprocessor receiving the HOLD request will issue HLDA (high) as an acknowledgement in the middle of a T4 or T1 clock cycle.
ALE : Address Latch Enable. ALE is provided by the microprocessor to latch the address into the 8282 or 8283 address latch. It is an active high(1) pulse during T1 of any bus

	cycle. ALE signal is never floated, is always integer.