Mahatma Gandhi Mission's College of Engineering and Technology
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MAHATMA GANDHI MISSION

Department of Computer Engineering

Course Code: CSC405 **Course Name: Microprocessor**

Assignment No.3

Class: SE **AY: 2021-22**

Q. No	Question
Q1.Justify Your Answers	
	(a) The interrupt for which the processor has the highest priority among all the external interrupts is NMI.
	(b) The 8259 operates in master and slave mode.
	(c) The NMI stand for Non-maskable Interrupt.
	(d) At the end of ISR, the instruction should be RET.
	(e) The 8259 PIC known as Programmable Interrupt Controller.
Q2. Choose Correct Options	
	1. In 8257 (DMA), each of the four channels has a) a pair of two 8-bit registers b) a pair of two 16-bit registers c) one 16-bit register d) one 8-bit register
	2. In the I/O mode, the 8255 ports work as a) reset pins b) set pins c) programmable I/O ports d) only output port
	3. In control word register, if SC1=0 and SC0=1, then the counter selected is a) counter 0 b) counter 1 c) counter 2 d) none
	4. Once the ICW1 is loaded, then the initialization procedure involves a) edge sense circuit is reset b) IMR is cleared c) slave mode address is set to 7 d) all of the mentioned
	5. The register that stores the bits required to mask the interrupt inputs is a) In-service register b) Priority resolver c) Interrupt Mask register
Q3. State whether the following statements are true or false (Give Reasons)	
	a. When the PS(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a buffer enable (T/F).
	(b) The automatic rotation is used in the applications where all the interrupting devices are of equal priority.(T/F)
	c) Whenever a large memory is required in a microcomputer system, the memory subsystem is generally designed using Dynamic RAM.(T/F)
Q4. Name the following or define or design the following	
	(a) Write the main function of IRR and ISR.

Ans: **Interrupt request register (IRR) –**
It stores all the interrupt level which are requesting for Interrupt services.
Interrupt service register (ISR) –
It stores the interrupt level which are currently being executed.

(b) Name the interrupt in 8086 processor and give Example For Non-maskable Interrupts..

Ans: The interrupt in 8086 processor is Trap. Common examples of non-maskable interrupt include types of **internal system chipset errors, memory corruption problems, parity errors** and **high-level errors needing immediate attention**. In a sense, a non-maskable interrupt is a way to prioritize certain signals within the operating system.

(c) Design 8086 based system in Minimum mode system for following requirements:

A)

I) 128 KB ROM using 32KB X 8 memory device

II) 512 KB ROM using 64KB X 8 memory device?

B)

I) 64 KB ROM using 32KB X 8 memory device

II) 64 KB EPROM using IC27128?

Q5. Answer the following questions in brief (20 to 30 words)

(a) Justify Which interrupt has highest priority in 8086.

Ans: *NMI (Non Maskable Interrupt)* – It is a single pin non maskable hardware interrupt which cannot be disabled. It is the highest priority interrupt in 8086 microprocessor. After its execution, this interrupt generates a TYPE 2 interrupt. IP is loaded from word location 00008 H and CS is loaded from the word location 0000A H.

(b) Try to find out The Differences Between The Nmi And Intr

Ans: **The characteristics of NMI are as follows:**

- They are also known as the non-maskable types.

- They are always give higher priorities over the INTR.

- The interrupt is edge triggered specifically Low to High transition.

- In order to function they must remain high for at least 2 cycles of CLK.

- These interrupts do not send out any form of acknowledgements.

The characteristics of INTR are:

- They are also known as the maskable types of interrupts.

- They have a lower priority as compared to NMI.

- These interrupts are level triggered and not edge triggered.

- These interrupts do not support latching and must remain high till the CPU acknowledges them to do so.

(c) Justify with your answer how DMA Operations are Performed?

Ans: Then how does Direct Memory Access work? Standard Direct Memory Access (also called third-party DMA) adopts a DMA controller. The DMA controller can produce memory addresses and launch memory read or write cycles. It covers multiple hardware registers that can be read and written by the CPU.

These registers consist of a memory address register, a byte count register, and one or more control registers. Depending on the features provided by the Direct Memory Access controller, these control registers can appoint some combination of source, destination, transfer direction (read from or write to I/O device), size of the transfer unit, and/or the number of bytes to transfer in one burst.

To perform input, output, or memory-to-memory operations, the host processor initializes the DMA controller with the number of words to transfer and the memory address to use. Then the CPU commands the peripheral device to begin data transfer.

Then the Direct Memory Access controller offers addresses and read/write control lines to the system memory. Each time a byte of data is prepared to be transferred between the peripheral device and the memory, the DMA controller increments its internal address register until a complete data block is transferred.

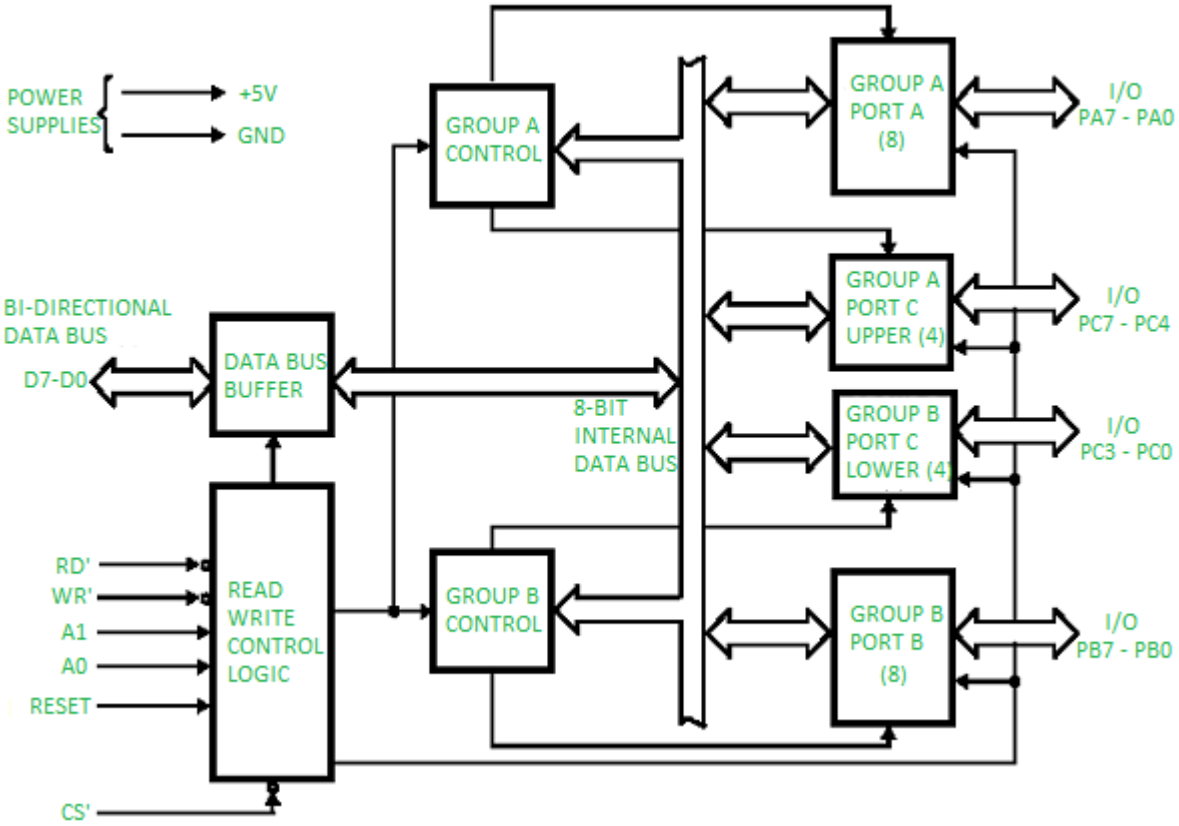
. Q6. Answer the following questions in brief (50 to 70 words)

(a) Draw and Explain the block diagram of 8255 PPI with control word formats.

Ans: PPI 8255 is a general purpose programmable I/O device designed to interface the CPU with its outside world such as ADC, DAC, keyboard etc. We can program it according to the given condition. It can be used with almost any microprocessor.

It consists of three 8-bit bidirectional I/O ports i.e. PORT A, PORT B and PORT C. We can assign different ports as input or output functions.

Block diagram –



It consists of 40 pins and operates in +5V regulated power supply. Port C is further divided into two 4-bit ports i.e. port C lower and port C upper and port C can work in either BSR (bit set rest) mode or in mode 0 of input-output mode of 8255. Port B can work in either mode 0 or in mode 1 of input-output mode. Port A can work either in mode 0, mode 1 or mode 2 of input-output mode.

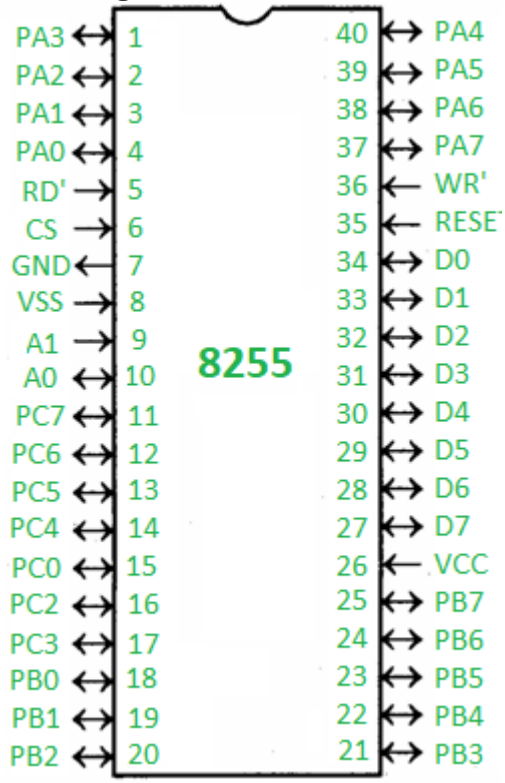
It has two control groups, control group A and control group B. Control group A consist of port A and port C upper. Control group B consists of port C lower and port B.

Depending upon the value if CS', A1 and A0 we can select different ports in different modes as input-output function or BSR. This is done by writing a suitable word in control register (control word D0-D7).

CS'	A1	A0	Selection	Address
0	0	0	PORT A	80 H
0	0	1	PORT B	81 H
0	1	0	PORT C	82 H
0	1	1	Control Register	83 H

1	X	X	No Seletion	X

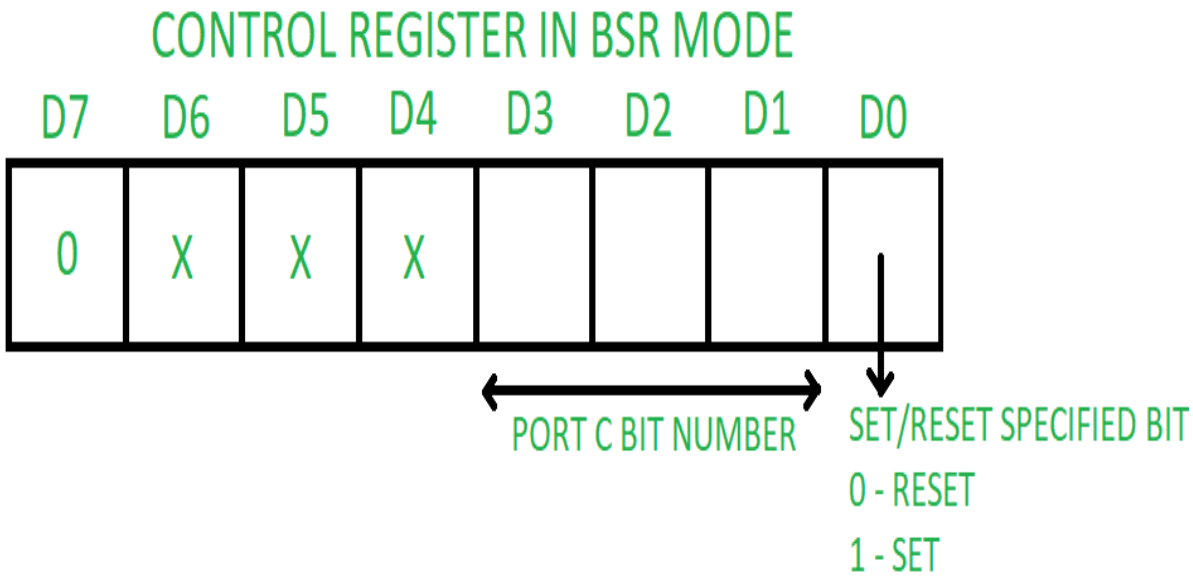
Pin diagram –



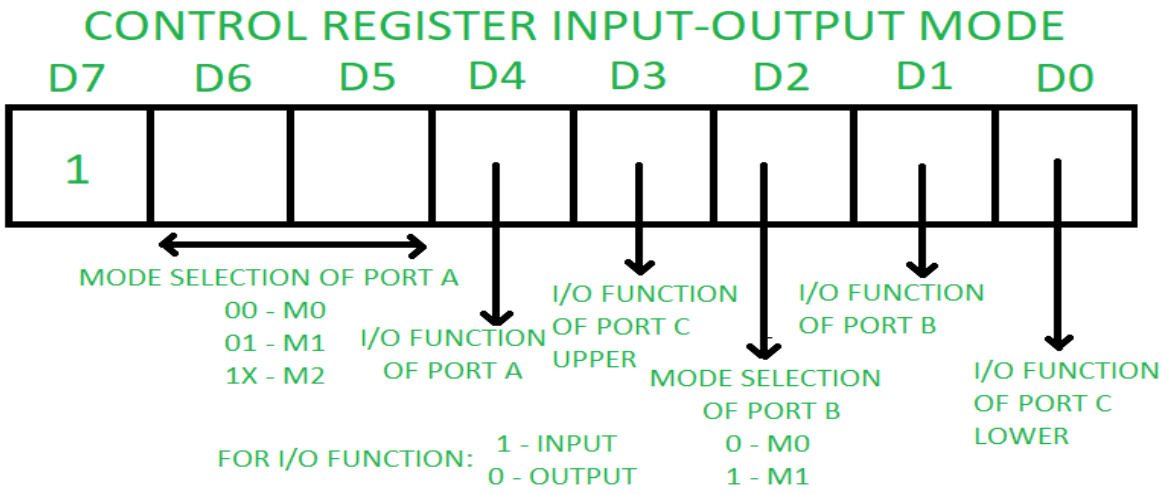
- **PA0 – PA7 –** Pins of port A
- **PB0 – PB7 –** Pins of port B
- **PC0 – PC7 –** Pins of port C
- **D0 – D7 –** Data pins for the transfer of data
- **RESET –** Reset input
- **RD' –** Read input
- **WR' –** Write input
- **CS' –** Chip select
- **A1 and A0 –** Address pins

Operating modes –

1. **Bit set reset (BSR) mode –**
   If MSB of control word (D7) is 0, PPI works in BSR mode. In this mode only port C bits are used for set or reset.



2. **Input-Output mode –**
   If MSB of control word (D7) is 1, PPI works in input-output mode. This is further divided into three modes:

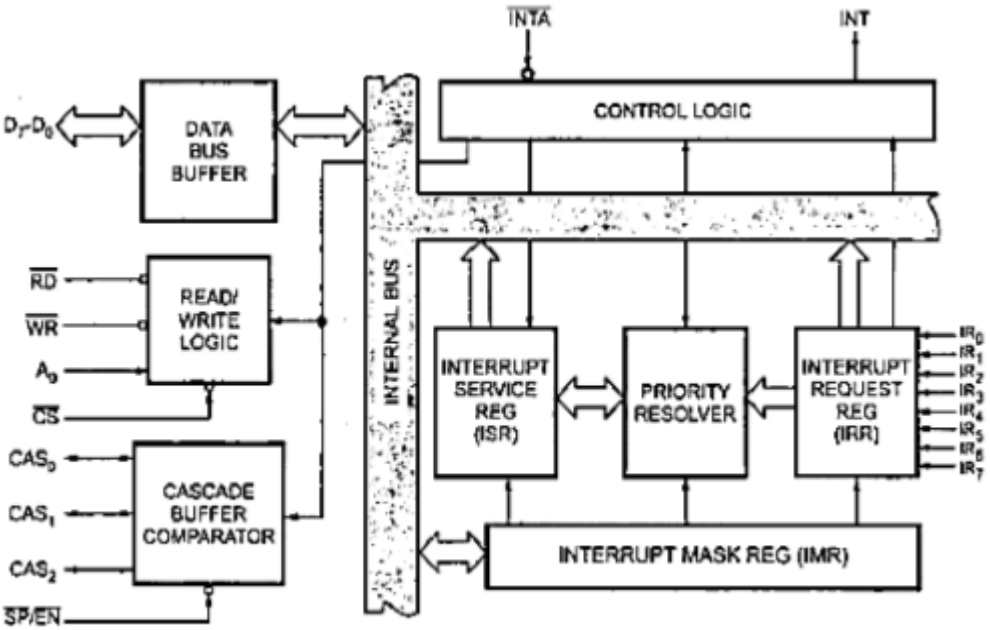


- **Mode 0 –**In this mode all the three ports (port A, B, C) can work as simple input function or simple output function. In this mode there is no interrupt handling capacity.
- **Mode 1 –** Handshake I/O mode or strobed I/O mode. In this mode either port A or port B can work as simple input port or simple output port, and port C bits are used for handshake signals before actual data transmission. It has interrupt handling capacity and input and output are latched.
  Example: A CPU wants to transfer data to a printer. In this case since speed of processor is very fast as compared to relatively slow printer, so before actual data transfer it will send handshake signals to the printer for synchronization of the speed of the CPU and the peripherals.

- **Mode 2 –** Bi-directional data bus mode. In this mode only port A works, and port B can work either in mode 0 or mode 1. 6 bits port C are used as handshake signals. It also has interrupt handling capacity.

(b) Draw and explain the block diagram of 8259 PIC .

1. Ans: Fig below shows the internal block diagram of the 8259A.
2. It includes eight blocks: data bus buffer, read/write logic, control logic, three registers (IRR, ISR and IMR), priority resolver, and cascade buffer.



Block Diagram of 8259A

1. **Data Bus Buffer:** The data bus buffer allows the 8085 to send control words to the 8259A and read a status word from the 8259A. The 8•bit data bus buffer also allows the 8259A to send interrupt opcode and address of the interrupt service subroutine to the 8085.
2. **Read/Write Logic:** The RD and WR inputs control the data flow on the data bus when the device is selected by asserting its chip select (CS) input low.
3. **Control Logic:** This block has an input and an output line. If the 8259A is properly enabled, the interrupt request will cause the 8259A to assert its INT output pin high. If this pin is connected to the INTR pin of an 8085 and if the 8085 Interrupt Enable (IE) flag is set, then this high signal will cause the 8085 to respond INTR as explained earlier.
4. **Interrupt Request Register (IRR):** The IRR is used to store all the interrupt levels which are requesting the service. The eight interrupt inputs set corresponding bits of the Interrupt Request

Register upon service request.

5. **Interrupt Service Register (ISR):** The Interrupt Service Register (ISR) stores all the levels that are currently being serviced.
6. **Interrupt Mask Register (IMR):** Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked. This register can be programmed by an Operation Command Word (OCW). An interrupt which is masked by software will not be recognized and serviced even if it sets the corresponding bits in the IRR.
7. **Priority Resolver:** The priority resolver determines the priorities of the bits set in the IRR. The bit corresponding to the highest priority interrupt input is set in the ISR during the MITA input.
8. **Cascade Buffer Comparator:** This section generates control signals necessary for cascade operations. It also generates Buffer-Enable signals. As stated earlier, the 8259 can be cascaded with other 825% in order to expand the interrupt handling capacity to sixty-four levels. In such a case, the former is called a master, and the latter are called slaves. The 8259 can be set up as a master or a slave by the SP/ER pin.
9. **CAS_0 - CAS_2:** For a master 8259, the CAS_0 - CAS_2pins are output pins, and for slave 8259s, these are input pins. When the 8259 is a master (that is, when it accepts interrupt requests from other 8259s), the CALL opcode is generated by the Master in response to the first INTA. The vector address must be released by the slave 8259. The master sends an identification code of three-bits to select one out of the eight possible slave 8259s on the CAS_0 - CAS_2lines. The slave 8259s accept these three signals as inputs (on their CAS_0 - CAS_2 pins) and compare the code sent by the master with the codes assigned to them during initialization. The slave thus selected (which had originally placed an interrupt request to the master 8259) then puts the address of the interrupt service routine during the second and third INTA pulses from the CPU.
10. **SP ER (Slave Program /Enable Buffer):** The SP/EN signal is tied high for the master. However it is grounded for the slave. In large systems where buffers are used to drive the data bus, the data sent by the 8259 in response to INTA cannot be accessed by the CPU (due to the data bus buffer being disabled). If an 8259 is used in the buffered mode (buffered or non-buffered modes of operation can be specified at the time of initializing the 8259), the SP/ER pin is used as an output which can be used to enable the system data bus buffer whenever the data bus outputs of 8259 are enabled (i.e. when it is ready to send data). Thus, in non-buffered mode, the SP/EN pin of an 8259 is used to specify whether the 8259 is to operate as a master or as a slave, and in the buffered mode, the SP / EN pin is used as an output to enable the data bus buffer of the system.

(c) Draw and Explain format of ICWs and OCW s of 8259.

Ans: **Initialization command words(ICW) :**

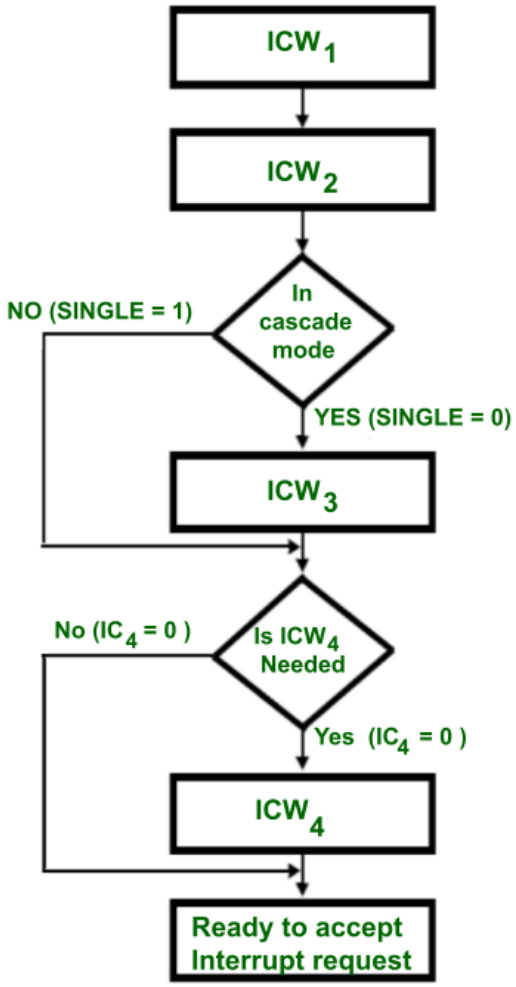
- ICW is given during the initialization of 8259 i.e. before its start functioning.
- ICW_1 and ICW_2 commands are compulsory for initialization.
- ICW_3 command is given during a cascaded configuration.
- If ICW_4 is needed, then it is specified in ICW_1.
- The sequence order of giving ICW commands is fixed i.e. ICW_1 is given first and then ICW_2 and then ICW_3.
- Any of the ICW commands can not be repeated, but the entire initialization process can be repeated if required.

Operating command words(OCW) :

- OCW is given during the operation of 8259 i.e. microprocessor starts using 8259.
- OCW commands are not compulsory for 8259.

- The sequence order of giving OCW commands is not fixed.
- The OCW commands can be repeated.

Initialization sequence of 8259 :



ICW_1 command :

- The control word is recognized as ICW_1 when $A_0 = 0$ and $D_4 = 1$.
- It has the control bits for Edge and level triggering mode, single/cascaded mode, call address interval and whether ICW4 is required or not.
- Address lines A_7 to A_5 are used for interrupt vector addresses.

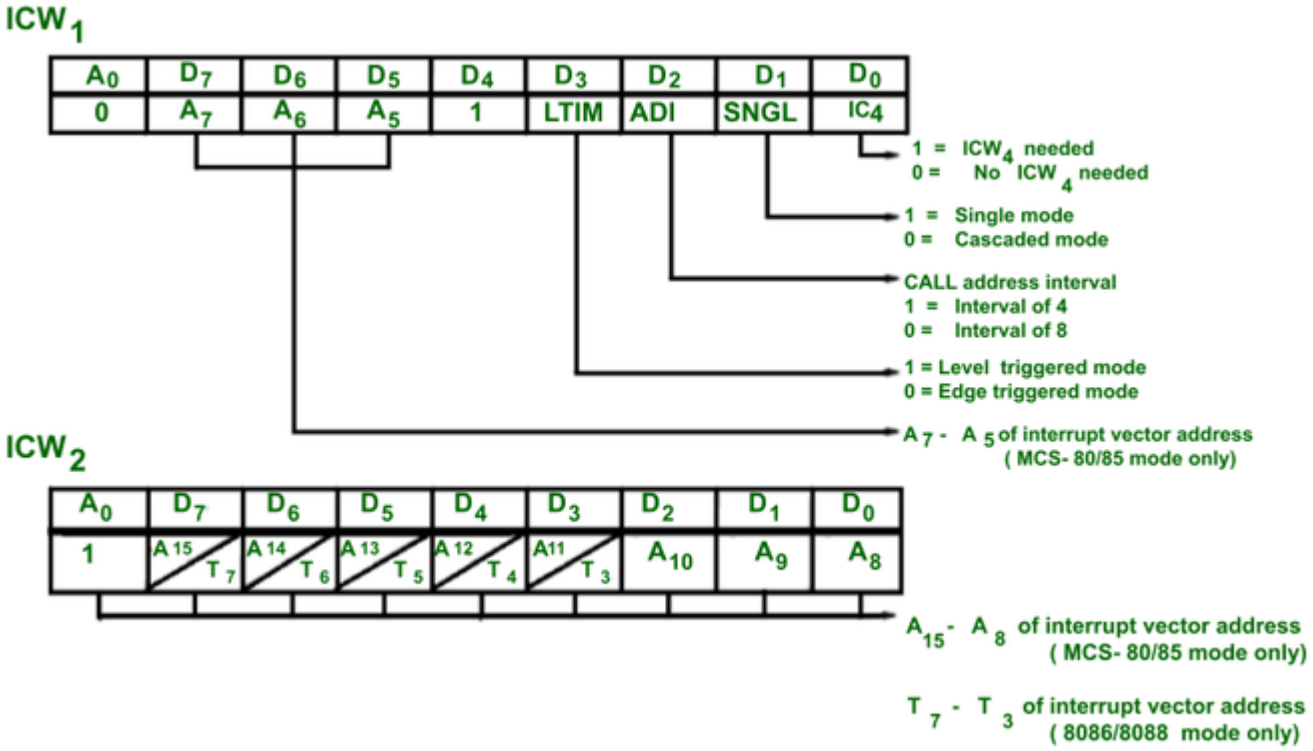
When the ICW_1 is loaded, then the initializations performed are:

- The edge sense circuit is reset because, by default, 8259 interrupt is edge triggered.
- The interrupt mask register is cleared.
- IR7 is assigned to priority 7.
- Slave mode address is assigned as 7.
- When $D_0 = 0$, this means IC_4 command is not required. Therefore, functions used in IC4 are reset.
- Special mask mode is reset and status read is assigned to IRR.

ICW_2 command :

- The control word is recognized as ICW_2 when $A_0 = 1$.

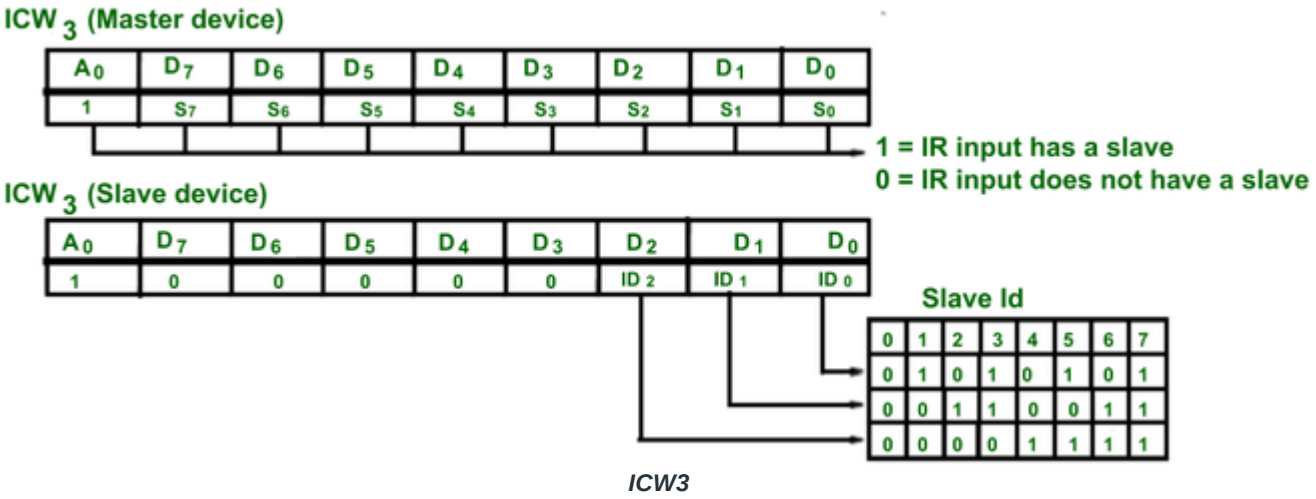
- It stores the information regarding the interrupt vector address.
- In the 8085 based system, the A15 to A_8 bits of control word is used for interrupt vector addresses.
- In the 8086 based system, T_6 to T_3 bits are inserted instead of A_{15} to A_8 and A_{10} to A_8 are used for selecting interrupt level, i.e. 000 for IR_0 and 111 for IR_7.



Initialization of 8259 by ICW1 and ICW2 command words

ICW_3 :

ICW_3 command word is used when there is more than one 8259 present in the system i.e. when SNGL bit in ICW_1 is 0, then it will load 8-bit slave register.



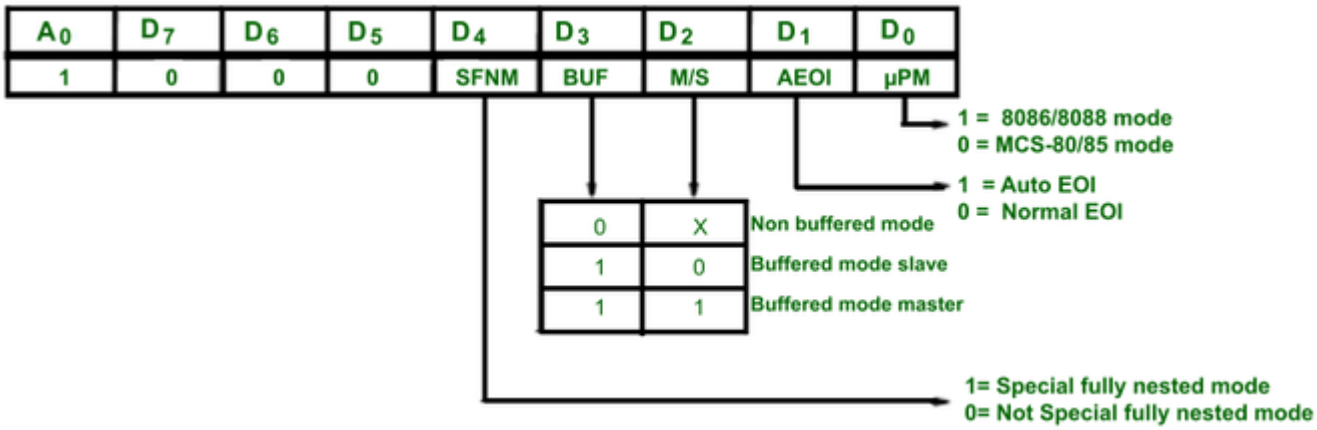
ICW3

ICW_4 :

- When AEOI = 1, then Automatic end of interrupt mode is selected.
- When SFMN = 1, then a special fully nested mode is selected.
- when BUF = 0 , then Non buffered mode is used (i.e. M/S is don't care) and when

M/S = 1, then 8259 is master, otherwise it is a slave.

- when µPM = 1, then 8086 operations are performed, otherwise 8085 operations are performed.



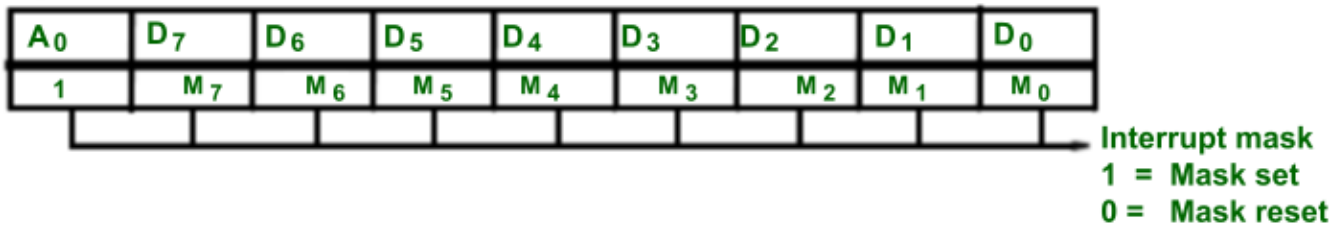
ICW4

Operational command word(OCW) :

OCW_1 –

It is used to set and reset the the mask bits in IMR(interrupt mask register). M_7 – M_0 describes 8 mask bits

OCW_1



OCW_2 –

It is used for selecting the mode of operation of 8259. Here L_2 to L_0 are used to describe interrupt level on which action need to be performed.

Detailed operations are described in the diagram below.

OCW_2

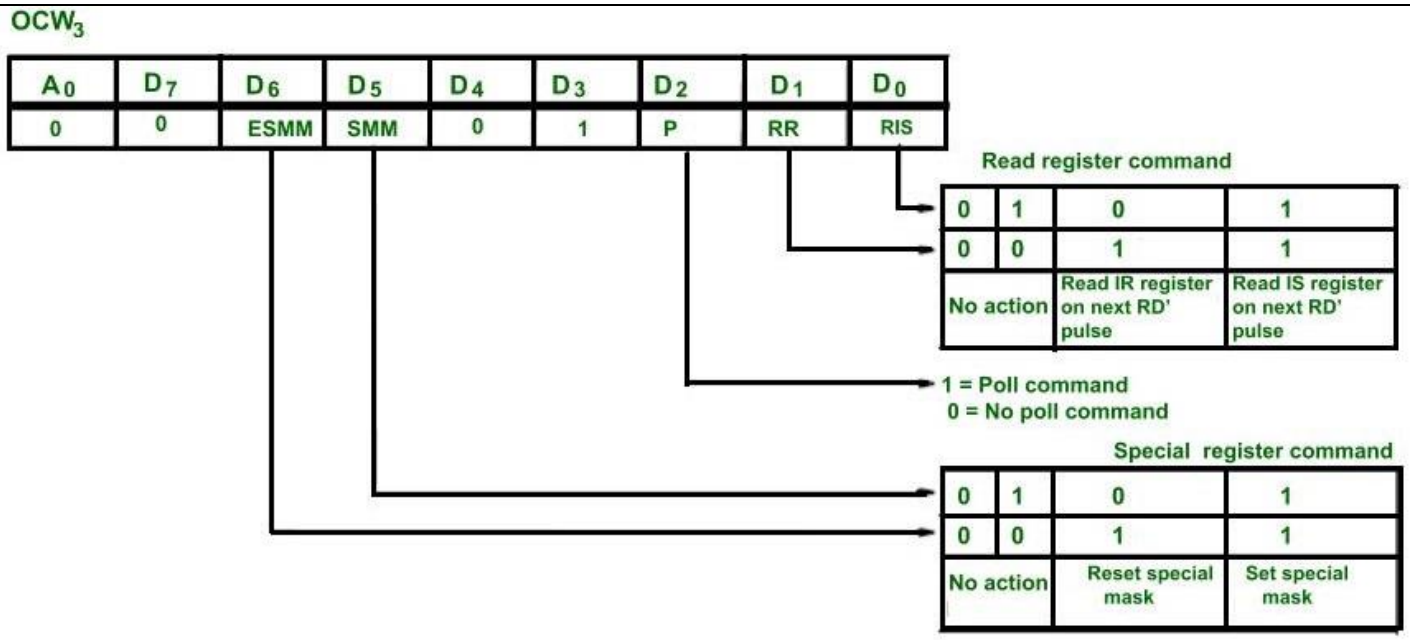
A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	R	SL	EOI	0	0	L_2	L_1	L_0

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

0	0	1	Non-specific EOi command	End of interrupt
0	1	1	Specific EOI command	
1	0	1	Rotate on non-specific EOI command	Automatic rotation
1	0	0	Rotate in automatic EOI mode(set)	
0	0	0	Rotate in automatic EOI mode(clear)	
1	1	1	Rotate on specific command	
1	1	0	Set priority command	Specific rotation
0	1	0	No operation	

OCW_3 –

- When the ESMM (Enable special mask mode) bit is set, then the SMM bit is don't care. If SMM = 1 and ESMM = 1, then 8259 will enter in Special mask mode.
- If ESMM = 1 and SMM = 0, then 8259 will return into normal mask mode.
- RR and RIS are used to give the read register command.
- P = 1 is used for poll command.



Q7. Think and Answer

(a) Why NMI interrupt has highest priority in 8086?

Ans: It is a single non-maskable interrupt pin (NMI) having higher priority than the maskable interrupt request pin (INTR)and it is of type 2 interrupt.

When this interrupt is activated, these actions take place −

- Completes the current instruction that is in progress.
- Pushes the Flag register values on to the stack.
- Pushes the CS (code segment) value and IP (instruction pointer) value of the return address on to the stack.
- IP is loaded from the contents of the word location 00008H.
- CS is loaded from the contents of the next word location 0000AH.
- Interrupt flag and trap flag are reset to 0.