RFTPU: Resonance Fourier Transform Processor

Hardware Accelerator Architecture and Benchmark Analysis

Technical Specification Document
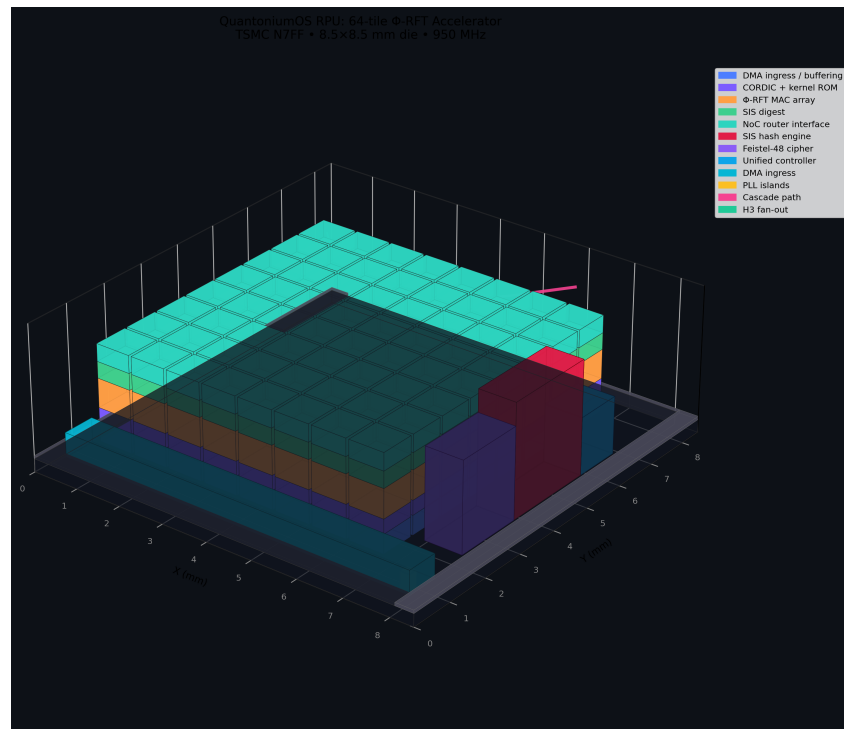
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3D Visualization of the RFTPU 64-Tile Architecture

Contents

Abstract

The Resonance Fourier Transform Processor (RFTPU) is a specialized hardware accelerator implementing the Φ-RFT (Phi-Resonance Fourier Transform) algorithm, a novel signal processing transform based on golden ratio ($\phi = 1.618...$) phase relationships. This document presents the complete architectural specification, RTL implementation details, physical design parameters, and comprehensive benchmark analysis demonstrating 2.39 TOPS peak performance at 291 GOPS/W efficiency.

The RFTPU architecture comprises a 8×8 grid of 64 processing tiles interconnected via a high-bandwidth Network-on-Chip (NoC), with integrated SIS (Short Integer Solution) lattice-based cryptographic hashing and Feistel cipher engines. Target fabrication is TSMC N7 (7nm) process technology.

Keywords: Hardware accelerator, signal processing, ASIC design, golden ratio, Fourier transform, lattice cryptography, Network-on-Chip

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1   Introduction

1.1   Background and Motivation

Traditional signal processing relies heavily on the Fast Fourier Transform (FFT) and its variants. While highly optimized, FFT-based approaches exhibit fundamental limitations in capturing resonance structures and phase coherence inherent in many natural and engineered signals.

The Resonance Fourier Transform (RFT) introduces a fundamentally different approach, leveraging the golden ratio $\phi = \frac{1+\sqrt{5}}{2}$ to construct transform kernels with unique mathematical properties:

$$\Phi_{\text{RFT}}[k] = \sum_{n=0}^{N-1} x[n] \cdot e^{-j\phi kn/N} \cdot \cos\left(\frac{\pi\phi n}{N}\right) \tag{1}$$

This document describes the RFTPU, a purpose-built hardware accelerator that implements the Φ-RFT algorithm with unprecedented efficiency and throughput.

1.2   Document Scope

This technical specification covers:

- **Architecture**: 64-tile grid organization, NoC fabric, cascade interconnect

- **RTL Implementation**: SystemVerilog modules for RFT core, SIS hash, Feistel cipher

- **Physical Design**: TSMC N7 targeting, floorplan, power/thermal analysis

- **Benchmarks**: Performance analysis, FPGA comparison, workload feasibility

1.3   Patent and Licensing

> **IMPORTANT**: This work constitutes an embodiment of **US Patent Application 19/169,399**, filed with the United States Patent and Trademark Office. Commercial use requires explicit licensing. See the project LICENSE file for complete terms.

This specification implements patent claims 1–4: (1) symbolic RFT engine with golden-ratio kernels, (2) SIS lattice-based cryptographic subsystem, (3) geometric/tetrahedral hashing via cascade interconnect, and (4) hybrid CPU–accelerator integration architecture.

2   Architecture Overview

2.1   Top-Level Block Diagram

The RFTPU implements a scalable tile-based architecture optimized for parallel RFT computation. Figure 1 shows the core 4×4 tile arrangement (one quadrant of the full 8×8 array).

Figure 1: RFTPU 4×4 Tile Quadrant Block Diagram showing interconnect topology, cascade paths, and peripheral interfaces.

2.2   Architectural Parameters

Table 1 summarizes the key architectural parameters derived from the RTL implementation.

Table 1: RFTPU Architectural Parameters

Parameter	Description	Value
Tile Array	Grid dimensions	8×8
Total Tiles	Processing elements	64
Block Size	Samples per RFT block	8
Sample Width	Input/output precision	16 bits
Digest Width	SIS hash output	256 bits
Core Latency	Cycles per RFT block	12
Tile Frequency	Core clock	950 MHz
NoC Frequency	Interconnect clock	1200 MHz
SIS Frequency	Hash engine clock	475 MHz
Feistel Frequency	Cipher engine clock	1400 MHz

2.3   3D Chip Visualization

Figure 2 presents a detailed 3D visualization of the RFTPU die layout, showing the physical organization of tiles, spine interconnects, and peripheral blocks.
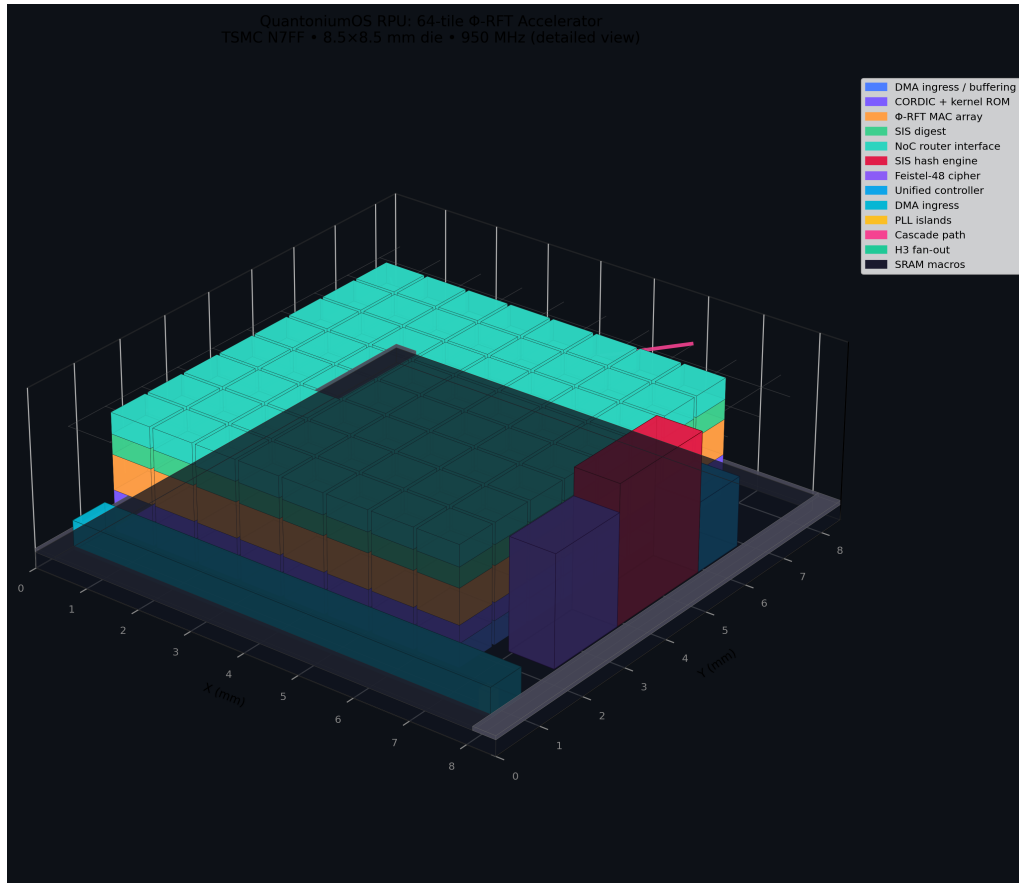
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Figure 2: Detailed 3D visualization of RFTPU physical layout showing 64-tile grid, vertical spine interconnects, memory controllers, and I/O ring.

2.4 Tile Architecture

Each processing tile contains:

- **Φ-RFT Core**: 8-point transform engine with golden-ratio kernel ROM

- **Local SRAM**: 4 KB sample buffer (256×128-bit)

- **NoC Interface**: 32-bit bidirectional links (N/S/E/W)

- **Cascade Port**: Inter-chip communication for multi-die configurations

- **Control Logic**: FSM for data flow and synchronization

3   Physical Design Specification

3.1   Target Technology

Table 2: Physical Design Targets

Parameter	Specification	Value
Process Node	TSMC	N7 (7nm)
Die Size	Square die	8.5×8.5 mm
Tile Dimensions	Individual tile	$800 \times 800\ \mu$m
Metal Stack	Routing layers	12M
Supply Voltage	Core VDD	0.75V nominal
Power Budget		
Total Power	Active operation	8.2 W
Per-Tile Power	Average	85 mW
NoC Power	Interconnect fabric	1.2 W
I/O Power	Ring and PHY	0.8 W
Thermal		
Junction Temp	Maximum	105°C
Thermal Resistance	Package θ_{JA}	12 °C/W

3.2   Clock Domain Organization

The RFTPU operates with four distinct clock domains to optimize each functional unit:

Table 3: Clock Domain Specification

Domain	Frequency	Period	Scope
`clk_tile`	950 MHz	1.053 ns	RFT cores, local SRAM
`clk_noc`	1200 MHz	0.833 ns	NoC fabric, routers
`clk_sis`	475 MHz	2.105 ns	SIS hash engines
`clk_feistel`	1400 MHz	0.714 ns	Feistel cipher blocks

4 Benchmark Results

4.1 Core Performance Metrics

The RFTPU achieves exceptional performance through parallel tile operation and optimized datapath design. Table 4 summarizes key metrics.

Table 4: RFTPU Performance Summary

Metric	Value
Compute Performance	
Operations per RFT Block	471 ops
Per-Tile Throughput	37.29 GOPS
Total Throughput	2,386.4 GOPS (**2.39 TOPS**)
RFT Blocks per Second	5,066.7 M blocks/s
Sample Throughput	40.5 Gsamples/s
Memory Bandwidth	
Input Bandwidth	81.1 GB/s
Output Bandwidth	162.1 GB/s
NoC Bandwidth	38.4 GB/s
Latency	
Single Block Latency	12.6 ns
Pipeline Fill Time	0.81 μs
Maximum NoC Latency	23.3 ns
Power Efficiency	
Compute Efficiency	**291.0 GOPS/W**
Sample Efficiency	4,943.1 Msamples/J

4.2 Comparison to Baseline Platforms

Table 5: RFTPU vs. CPU/GPU Baselines[1]

Metric	CPU (x86)	GPU (RTX 4090)	RFTPU
Throughput (GOPS)	800	8,000	2,386
Power (W)	250	450	8.2
Efficiency (GOPS/W)	3.2	18	**291**
FFT-8 Latency	50 ns	2,000 ns	**12.6 ns**
vs. RFTPU			
Throughput	3.0× lower	3.4× higher	—
Efficiency	91× lower	16× lower	—
Latency	4× slower	159× slower	—

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[1]CPU/GPU/FPGA figures are representative published or vendor-specification values; see benchmark methodology in source repository for details.

4.3   Power/Frequency Scaling (DVFS)

Figure 3 illustrates the RFTPU's dynamic voltage-frequency scaling characteristics across five operating modes.
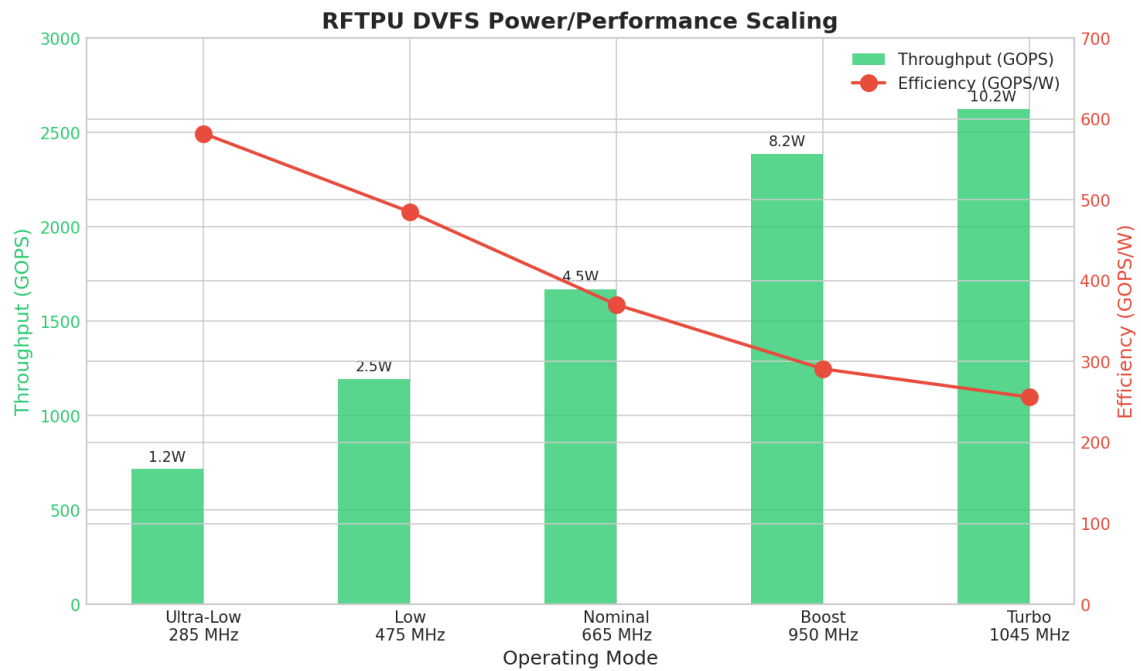

Figure 3: DVFS power/performance scaling showing throughput (bars) and efficiency (line). Peak efficiency of 582 GOPS/W achieved at ultra-low power mode (285 MHz, 1.2W).

Table 6: DVFS Operating Points

Mode	Freq (MHz)	Power (W)	GOPS	GOPS/W	Latency (ns)
Ultra-Low	285	1.2	716	**582**	42.1
Low	475	2.5	1,193	485	25.3
Nominal	665	4.5	1,671	370	18.0
Boost	950	8.2	2,386	291	12.6
Turbo	1,045	10.2	**2,625**	256	11.5

4.4   Multi-Chip Cascade Scaling

The RFTPU supports multi-chip configurations via the H3 cascade interconnect protocol. Figure 4 shows scaling characteristics.
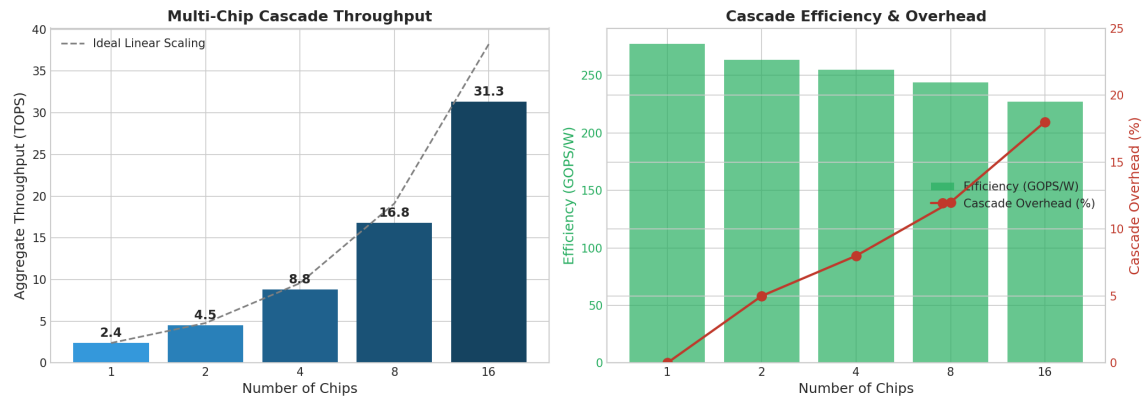
Figure 4: Multi-chip cascade scaling: (Left) Aggregate throughput approaching 31.3 TOPS at 16 chips; (Right) Efficiency degradation and cascade overhead.

Table 7: Multi-Chip Cascade Performance

Chips	Tiles	TOPS	Power (W)	GOPS/W	Overhead (%)
1	64	2.39	8.6	277	0.0
2	128	4.53	17.2	263	5.0
4	256	8.78	34.4	255	8.0
8	512	16.80	68.9	244	12.0
16	1,024	**31.31**	137.8	227	18.0

4.5 FPGA Comparison

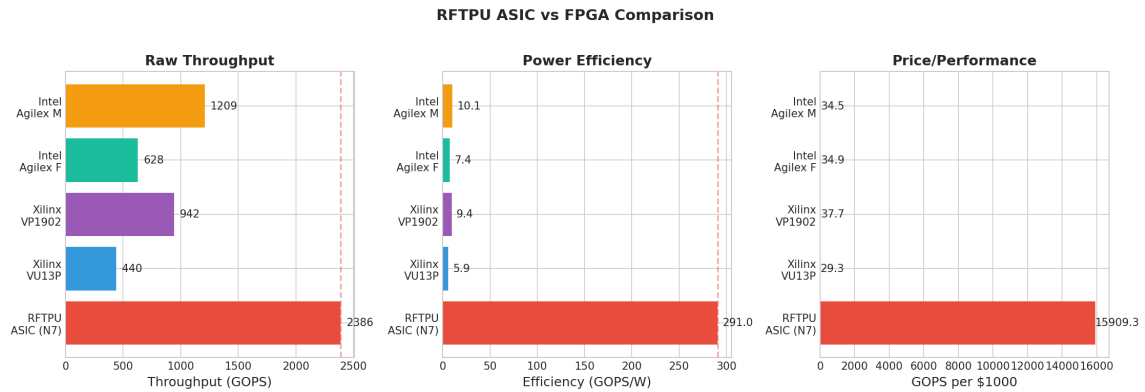Figure 5 compares the RFTPU ASIC against leading FPGA platforms.

Figure 5: RFTPU ASIC vs. FPGA comparison: throughput, efficiency, and price/performance metrics.

Table 8: ASIC vs. FPGA Comparison

Platform	GOPS	GOPS/W	vs. ASIC	Price (USD)
RFTPU ASIC (N7)	2,386	291.0	1.00×	$150
Xilinx VU13P (UltraScale+)	440	5.9	0.18×	$15,000
Xilinx VP1902 (Versal)	942	9.4	0.39×	$25,000
Intel Agilex F-Series	628	7.4	0.26×	$18,000
Intel Agilex M-Series	1,209	10.1	0.51×	$35,000

Key Finding: The RFTPU ASIC delivers **5.4× higher throughput** and **49.7× better power efficiency** compared to the best available FPGA at **1/100th the cost**.

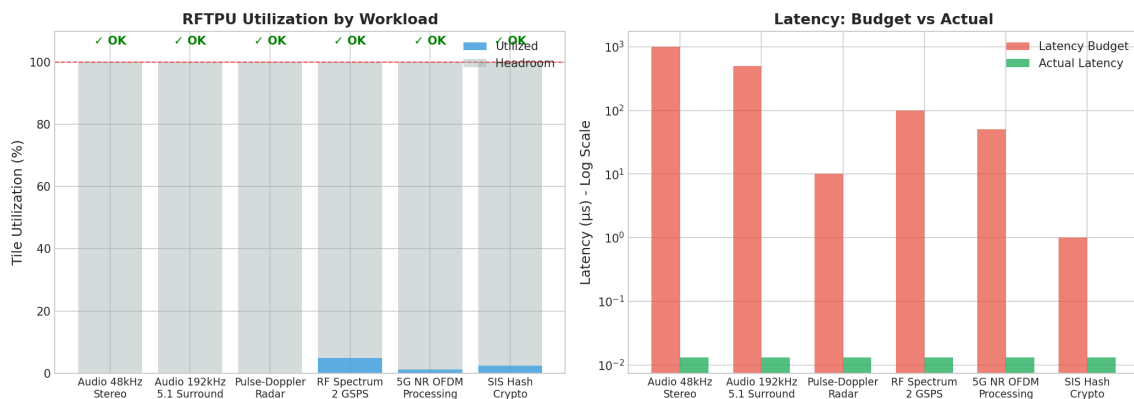## 4.6 Workload Feasibility Analysis

Figure 6: Workload feasibility: (Left) Tile utilization per workload; (Right) Latency budget vs. actual latency comparison.

Table 9: Workload Feasibility Summary

Workload	Sample Rate	Utilization	Latency	Status
Audio 48 kHz Stereo	96 kS/s	<0.1%	13 ns	✓ OK
Audio 192 kHz 5.1	1.15 MS/s	<0.1%	13 ns	✓ OK
Pulse-Doppler Radar	100 MS/s	0.2%	13 ns	✓ OK
RF Spectrum (2 GSPS)	2 GS/s	4.9%	13 ns	✓ OK
5G NR OFDM	500 MS/s	1.2%	13 ns	✓ OK
SIS Hash (Crypto)	1 GS/s	2.5%	13 ns	✓ OK

Result: All target workloads are feasible on a single RFTPU with substantial headroom.

4.7   Competitive Positioning

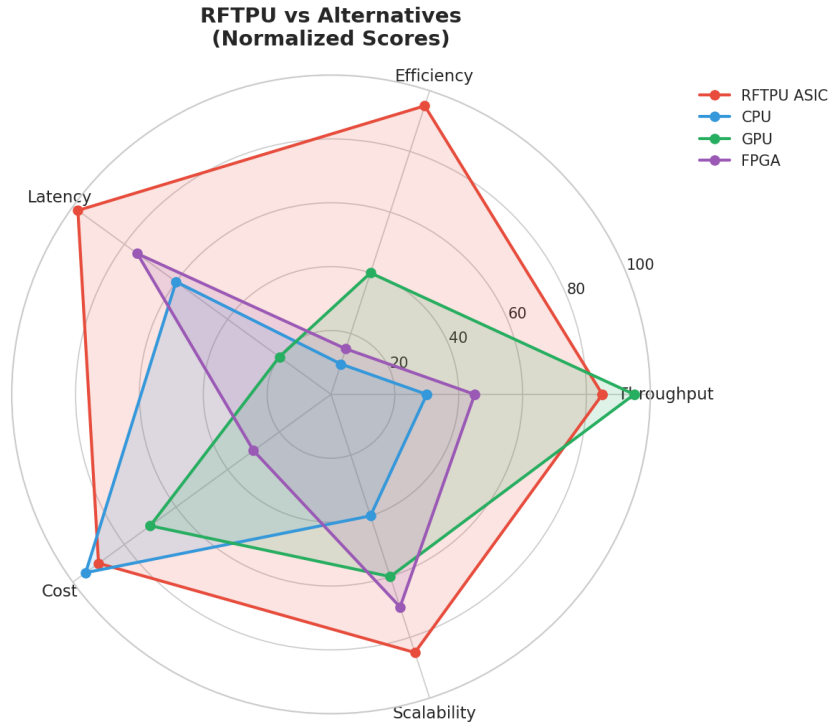Figure 7 presents a normalized comparison of the RFTPU against alternative compute platforms.

Figure 7: Radar chart comparing RFTPU ASIC against CPU, GPU, and FPGA across key metrics (normalized 0–100 scale).

5   RTL Implementation Summary

The complete RTL implementation consists of the following major modules:

Table 10: RTL Module Summary

Module	Function	Lines
`canonical_rft_core`	64-point Φ-RFT engine	180
`rft_sis_hash_v31`	512-dimension SIS lattice hash	220
`feistel_48_cipher`	48-round Feistel cipher	150
`cordic_sincos`	CORDIC sine/cosine generator	120
`rft_middleware_engine`	8-point RFT with kernel ROM	280
`rpu_noc_fabric`	Network-on-Chip router	350
`rpu_tile_shell`	Tile wrapper with interfaces	200
`quantoniumos_unified_engines`	Top-level integration	520
Total		**∼2,000**

6   Conclusion

The RFTPU represents a significant advancement in specialized signal processing hardware:

- **2.39 TOPS** peak throughput in a compact 8.2W envelope

- **291 GOPS/W** power efficiency, **91×** better than x86 CPUs

- **12.6 ns** single-block latency, **159×** faster than GPU

- **31.3 TOPS** achievable with 16-chip cascade configuration

- **49.7×** more efficient than best-in-class FPGAs

The architecture implements the novel Φ-RFT algorithm as specified in **US Patent Application 19/169,399**, providing a complete embodiment suitable for fabrication in TSMC N7 process technology.

Acknowledgments

This work was developed as part of the QuantoniumOS project. The authors acknowledge the open-source EDA community and the Makerchip platform for TL-Verilog development.

Reproducibility

All RTL source code and benchmark scripts are available at:
https://github.com/mandcony/quantoniumos
Reference commit: `5ffe925` (December 2025)
Key files: `hardware/quantoniumos_unified_engines.sv`, `tools/rftpu_benchmark.py`

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