Computer Organization and Software Systems

Contact Session 5

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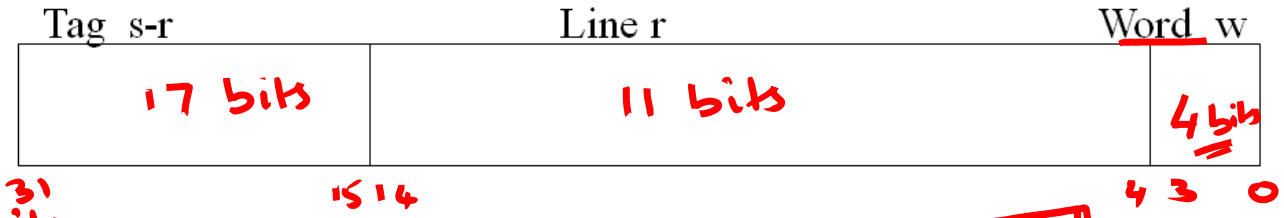
Problem 4



- The system uses a L1 cache with direct mapping and 32-bit address format is as follows:
- bits 0 - 3 = offset (word)
- bits 4 - 14 = index bits (Line)
- bits15 - 31 = tag

a) What is the size of cache line?

b) How many Cache lines are there?

c) How much space is required to store the tags in the L1 cache?

d) What is the total Capacity of cache including tag storage?

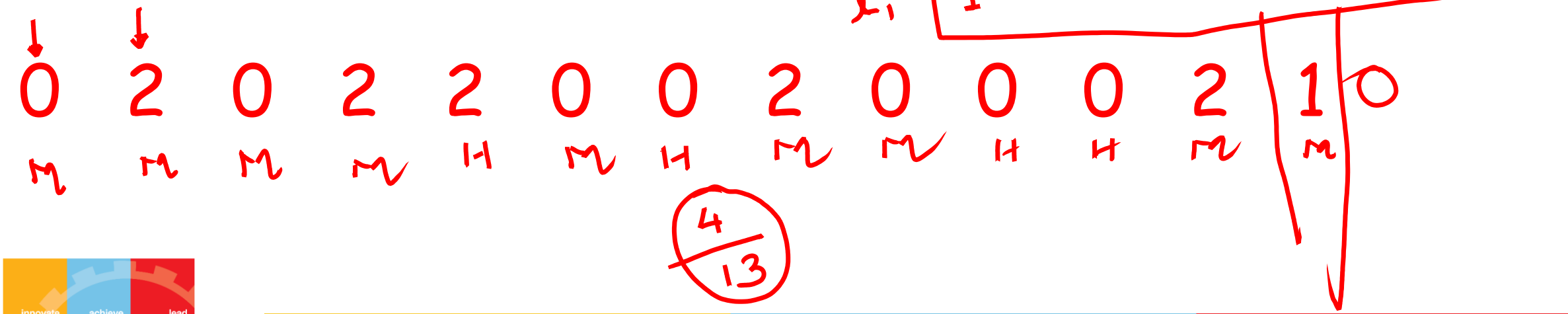
Problem 5 - Direct Mapped Cache

- 16 Bytes main memory, Memory block size is 4 bytes, Cache of 8 Byte (cache is 2 lines of 4 bytes each)

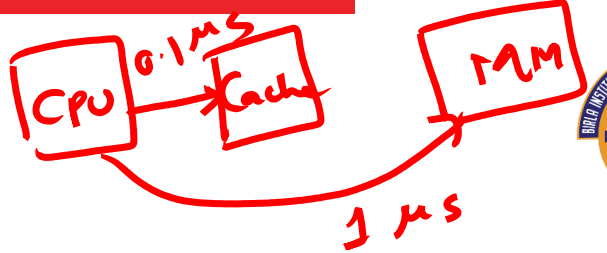
Block access sequence :

0 2 0 2 2 0 0 2 0 0 0 2 1

Find out hit ratio.



Problem 6



- Suppose a 1024-byte cache has an access time of 0.1 microseconds and the main memory stores 1 Mbytes with an access time of 1 microsecond. A referenced memory block that is not in cache must be loaded into cache .
- Answer the following questions:

a) What is the number of bits needed to address the main memory?

Capacity of main memory = 1 MBytes

# of bits in main memory address = 2^{20} → 20 bits

a) If the cache hit ratio is 95%, what is the average access time for a memory reference?

Avg access time = hit ratio * cache access + (1- hit ratio) * (cache access + memory access)

= 0.95 * 0.1 μsec + 1-0.95

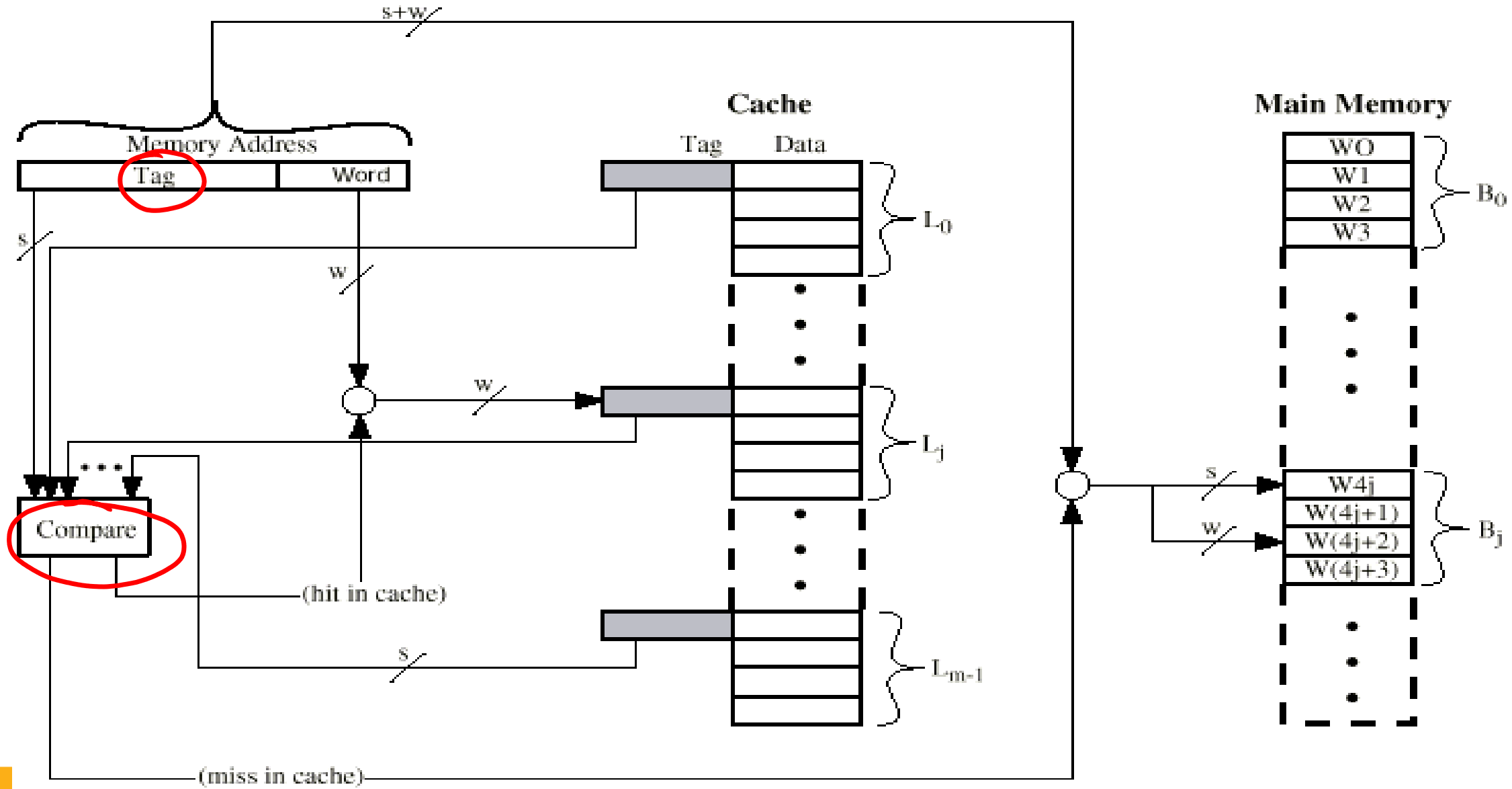
0.05 * (0.1μs + 1 μs)

=

Associative Mapping = fully associative mapped cache

- A main memory block can load into any line of cache
- Memory address is interpreted as tag and word
- Tag uniquely identifies block of memory
- Every line's tag is examined for a match
- Cache searching gets expensive

Associative Cache Organization



Associative Mapping Summary

- Address length = (s + w) bits
- Number of addressable units = 2^{s+w} words or bytes
- Block size = line size = 2^{w} words or bytes
- Number of blocks in main memory = $2^{s+ w}/2^{w} = 2^{s}$
- Number of lines in cache = undetermined
- Size of tag = s bits

Problem 7 => Associative mapping

- Given : $2^7 \cdot 2^{10}$ 2^3 => Main memory block size
  - Cache of 128KByte, Cache block of 8 bytes
  - 32 MBytes main memory
- Find out

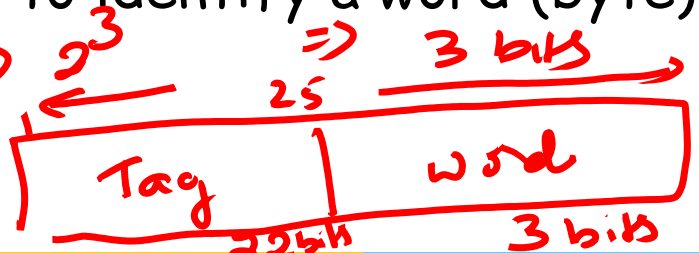
a) Number of bits required to address the memory
Main Memory Capacity = 32 MB => $2^5 \cdot 2^{20}$ => 2^{25} => 25 bits for addressing

b) Number of blocks in main memory
MM capacity / Block size : $\frac{2^{25}}{2^3} = 2^{25-3} = 2^{22}$ = 4M Blocks

c) Number of cache lines
= Capacity of cache / Block size : $\frac{128 \times 2^{10}\,B}{2^3\,B} = \frac{2^7 \cdot 2^{10}}{2^3} = 2^{14}$ = 16K lines
$2^{14} = 2^4 \cdot 2^{10}$

d) Number of bits required to identify a word (byte) in a block?
Block sz => 2^3 => 3 bits

e) Tag, Word



Problem 8

2^6 2^{10} Bytes 2^2

- Cache of 64KByte, Cache block of 4 bytes , 16 M Bytes main memory and associative mapping.

Fill in the blanks:

Number of bits in main memory address = 24 bit 2^4 2^{20}

Number of lines in the cache memory = 16 K lines $2^{16} / 2^2 = 2^{14} \Rightarrow$ 16 K Lines

Word bits = 2 bits

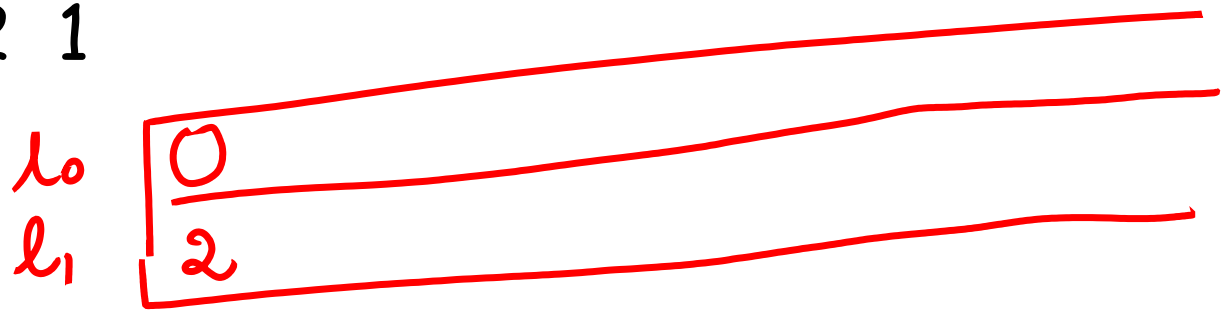
Tag bits = 22 bits

Problem 9

- 16 Bytes main memory, Memory block size is 4 bytes, Cache of 8 Byte (cache is 2 lines of 4 bytes each) and associative mapping. Block access sequence :

  0 2 0 2 2 0 0 2 0 0 0 2 1

  Find out hit ratio.



0 2 0 2 2 0 0 2 0 0 0 2 1

M M H H H H H H H H H H M

ATQ ⇒ Hit Ratio = 10/13

DM ⇒ 4/13

Set Associative Mapping

m: # lines in the cache
v: sets ⇒ k lines

- Cache is divided into a number of sets (v sets each with k lines)
- m = v * k
- i = j modulo v

  where i = cache set number

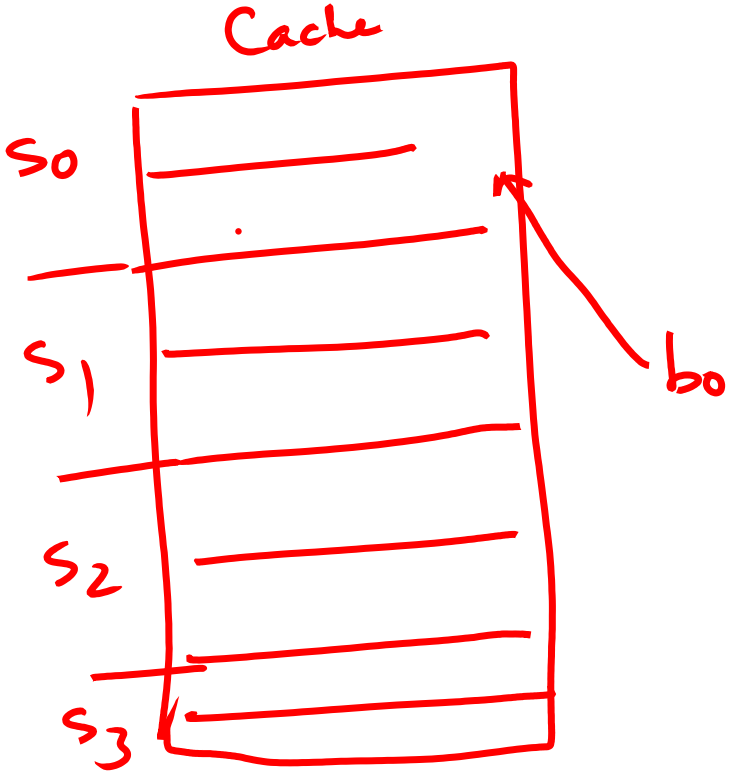
  j = main memory block number

  v = number of sets in the cache
- Each set contains 'k' number of lines
- A given block maps to any line in a given set
  - e.g. Block B can be in any line of set i
- m-way set associative cache
  - 2 way set associative mapping ➔ 2 lines per set
  - A given block can be in one of 2 lines in only one set

2-way
4-way

4 lines/set

m ⇒



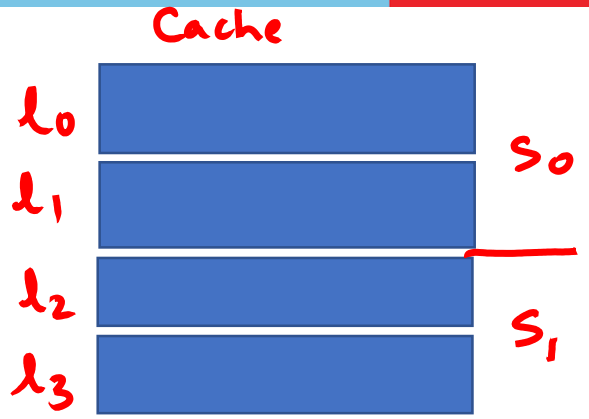
Example

- 16 Bytes main memory, Block Size is 2 Bytes,
- Cache of 8 Bytes, 2 way set associative cache
  - # address bits ⇒ 4 bits
  - Cache line size ⇒ 2 bytes
  - # main memory blocks ⇒ 8
  - # Number of cache lines = 4
  - # lines per set = 2
  - # of sets = 2

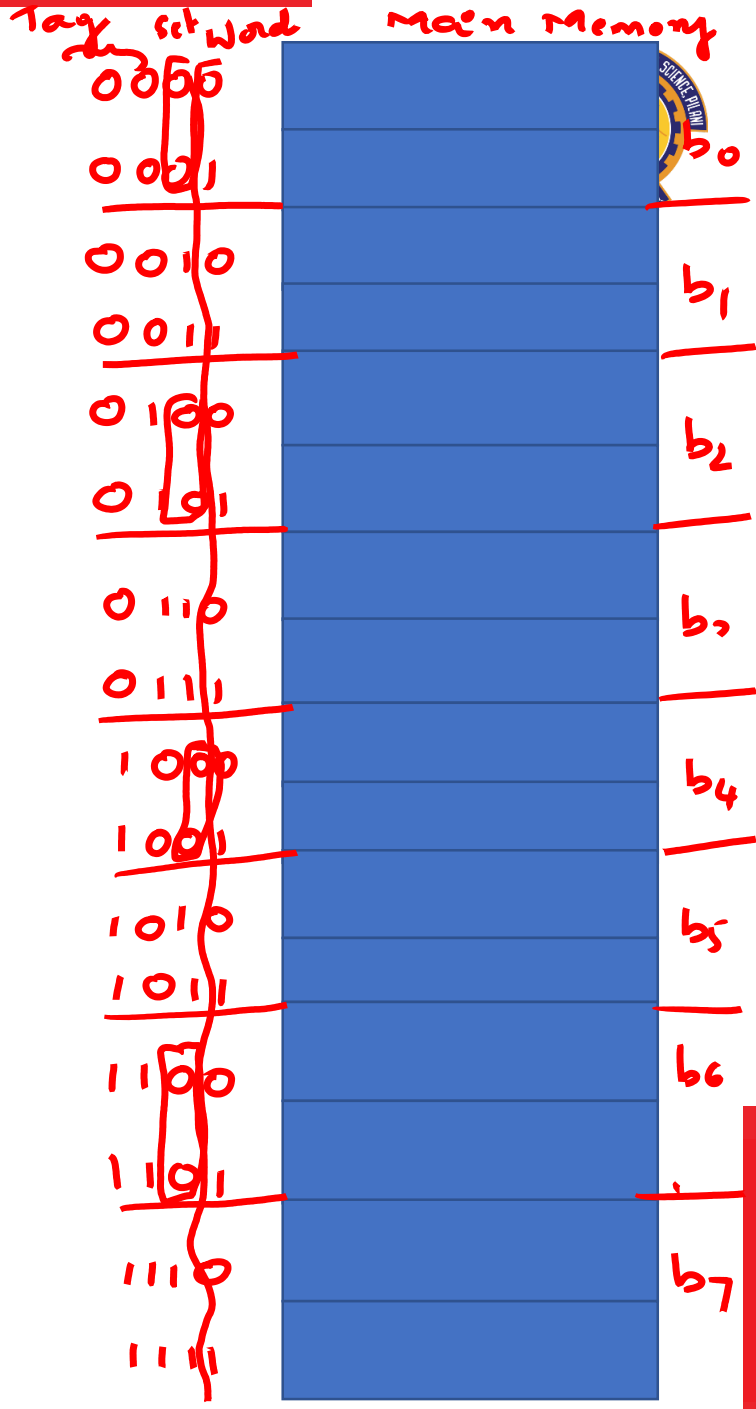
$b_0, b_2, b_4, b_6 \Rightarrow S_0$

$b_1, b_3, b_5, b_7 \Rightarrow S_1$

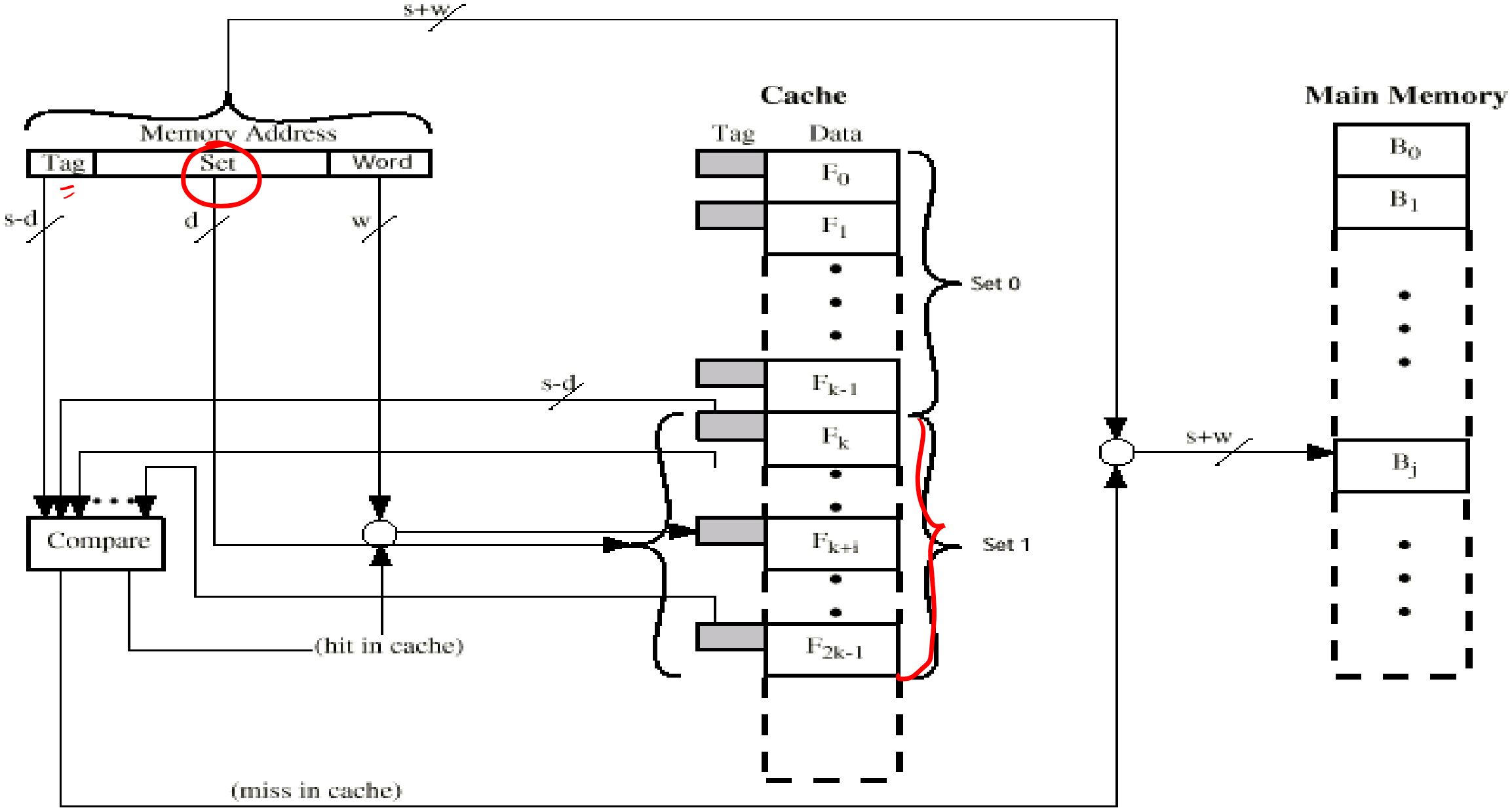
Tag | Set | word



i = j modulo v	Set #
0%2	0 ⇒ S_0
1%2	1 ⇒ S_1
2%2	0 ⇒ S_0
3%2	1 ⇒ S_1
4%2	0 ⇒ S_0
5%2	1 ⇒ S_1
6%2	0 ⇒ S_0
7%2	1 ⇒ S_1



Two-Way Set Associative Cache Organization



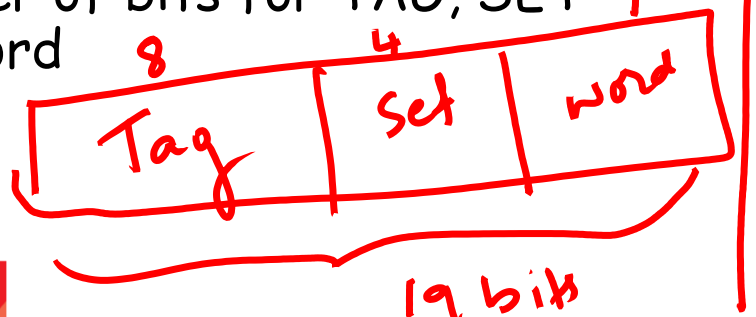
Set Associative Mapping Summary

- Address length = (s + w) bits
- Number of addressable units = 2^{s+w} words or bytes
- Block size = line size = 2^{w} words or bytes
- Number of blocks in main memory = 2^{d}
- Number of lines in set = k
- Number of sets = v = 2^{d}
- Number of lines in cache = kv = k * 2^{d}
- Size of tag = (s – d) bits

Problem 1

11.5]

- A set-associative cache consists of 64 lines, or slots, divided into four-line sets. = 4 way set associative
  Main memory contains 4K blocks of 128 bytes each.
  Find out
  a) • Total main memory capacity
  b) • Total cache memory capacity
  c) • Total number of sets in the cache
  d) • Number of bits for TAG, SET and word



a) Total main memory capacity
= # of blocks × block size
= 4K × 128 bytes
= $2^2 \cdot 2^{10} \times 2^7$ bytes
= 2^{19} bytes $= 2^9 \times 2^{10} = 512$ KB

(b) Total cache memory capacity
= # of lines × block size
= 64 × 128 Bytes $= 2^6 \cdot 2^7 = 2^{13}$ bytes
$= 8$ KB

(c) Total number of sets
= # of lines / lines per set $= \frac{64}{4} = 16$

(d) word: $[2^x = 128] = 7$ bits
set $= [2^x = 16] = 4$ bits
Tag $= 19 - 7 - 4 = 8$ bits

Problem 2: Home work

- A computer has an 8 GByte memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses **word level addressing**. What is the address format? If we change the cache to a 4- way set associative cache, what is the new address format?

Replacement Algorithms (1/3)

Direct mapped cache

- No choice
- Each block maps to one line and replace that line

Replacement Algorithms (2/3)

- Needed in Associative & Set Associative mapped cache
- Hardware implemented algorithm (speed)
- Methods:
  - Least Recently Used (LRU)
  - Least Frequently Used (LFU)
  - First In First Out (FIFO)
  - Random

Replacement Algorithms (3/3)

- Least Recently used (LRU): Replace the block that has been in the cache longest with no reference to it
  - e.g. 2 way set associative
  - Uses "USE" bits
  - Most effective method
- Least frequently used: Replace block which has had fewest hits
  - Uses counter with each line
- First in first out (FIFO): Replace block that has been in cache longest
  - Round robin or circular buffer technique
- Random

Problem 3

- Consider a reference pattern that accesses the sequence of blocks 0, 4, 0, 2, 1, 8, 0, 1, 2, 3, 0, 4. Assuming that the cache uses associative mapping, find the hit ratio for a cache with four lines

a) LRU

b) LFU

c) FIFO

Problem 2 - LRU

Ref	0	4	0	2	1	8	0	1	2	3	0	4
time	0	1	2	3	4	5	6	7	8	9	10	11
L0	0_0	0_0	0_2	0_2	0_2	0_2	0_6	0_6	0_6	0_6	0_{10}	0_{10}
L1		4_1	4_1	4_1	4_1	8_5	8_5	8_5	8_5	3_9	3_9	3_9
L2				2_3	2_3	2_3	2_3	2_3	2_8	2_8	2_8	2_8
L3					1_4	1_4	1_4	1_7	1_7	1_7	1_7	4_{11}
H/M	M	M	H	M	M	M	H	H	H	M	H	M

Hit Ratio : $\frac{5}{12}$

$L_0 - B_0$
$L_1 - B_3$
$L_2 - B_2$
$L_3 - B_4$

Problem 2 - LFU

Ref	0	4	0	2	1	8	0	1	2	3	0	4
L0	O_1	O_1	O_2	O_2	O_2	O_2	O_3	O_3	O_3	O_3	O_4	O_4
L1		4_1	4_1	4_1	4_1	8_1	8_1	8_1	8_1	3_1	3_1	4_1
L2				2_1	2_1	2_1	2_1	2_1	2_2	2_2	2_2	2_2
L3					1_1	1_1	1_1	1_2	1_2	1_2	1_2	1_2
H/M	M	M	H	M	M	M	H	H	H	M	H	M

Hit ratio : $\frac{5}{12}$

Final content

L0 - B0
L1 - B4
L2 - B2
L3 - B1

Problem 2 - FIFO

LRU → timing information is changed as and when block is referenced

FIFO → timing information is recorded only once

time 0 1 2 3 4 5 6 7 8 9 10 11

Ref	0	4	0	2	1	8	0	1	2	3	0	4
L0	0_0	0_0	0_0	0_0	0_0	8_5	8_5	8_5	8_5	8_5	8_5	8_5
L1		4_1	4_1	4_1	4_1	4_1	0_6	0_6	0_6	0_6	0_6	0_6
L2				2_3	2_3	2_3	2_3	2_3	2_3	3_9	3_9	3_9
L3					1_4	1_4	1_4	1_4	1_4	1_4	1_4	4_{11}
H/M	M	M	H	M	M	M	M	H	H	M	H	M

Hit Ratio = $\frac{4}{12}$

L0 B8
L1 B0
L2 B3
L3 B4