

Name - Chandrawanshi Mangesh Shivaji

Roll No - 180CB16

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(a) Prepare a summary sheet on microprocessors in the market.

Company	Micro Processor	Year	Architecture No. of Transistors	Clock Rate	Memory Capacity	Data Bus width	Address Bus width	No. of Cores	Process (Lithography)
Intel	4004	1971	moultic pro cessor 2250 x86	240kHz	4KB / 640 byte	6 bit	12 bit	1	10 μ m
	8086 (16-bit)	1978	CasCade lake ~10 billion 29000	4.7GHz 5 to 10 MHz	256 GB/ ~8 KB	16 bit	20 bit	1	-
	Xeon Platinum 8180	2017	Skylake-SP ~8 billion	2.5 GHz	786 GB/ 385MB	64 bit	64 bit	28	14 nm
	i9-10900X	2020	CasCade lake ~10 billion	4.7GHz	256 GB/ 19.25 MB	64 bit	64 bit	10	14 nm
	ARM	1985	VLSI Techology 24800	8 MHz	64 MB/ 110KiB/core	32 bit	26 bit	1	3 μ m
SPARC	ARM Cortex A-78	2020	ARM v8.2 3 billion	8.3GHz	NA/ 8 MB L3	128 bits	40 bit	1 to 4	5 nm
	SPARC M886900	1986	SPARC/ 0.11 million	~33MHz	NA/ 128 KB	-	-	1	-
	LEON5	2019	SPARC V8 ~Billions	~4.52GHz	NA/ 8 MB	128 bit	128 bit	NA	-
DEC	Alpha 21064	1992	Alpha AXP 1.68 million	200MHz	16GB/ 8 KB	64 bit	NA	1	-

	Alpha 21464	2004	Alpha AXP 250 million	2000 MHz	16 GB/ 3 MB	64 bit	64 bit	1	~
Motorola	MC6800	1974	MOS / 2000	1 MHz	128 bytes/ NA	8 bit	16 bit	1	~
	MCF5407	2005	V4 ColdFire NA	220 MHz	4 KB SRAM/ 16 KB L	32 bit	32 bit	1	~
Apple	A4	2010	ARM Cortex A8 3 million	1 GHz	256 MB/ 512 KB	64 bit	64 bit	1	~
	A13	2019	ARM V8.4 ISA 8.5 billion	2.66 GHz	8 GB/ 8 MB	64 bit	64 bit	6	~
Huawei	K8V2	2012	ARM V7 0.6 billion	1.4 GHz	2 GB/1 MB	64 bit	64 bit	4	~
	Kirin 9905G	2019	Cortex-A76 10.3 billion	2.86 GHz	16 GB/4 MB	64 bit	64 bit	4	~
AMD	29000 AMD	1982	RISC / 29000	4 10 MHz	1 MB / 8 KB	16 bit	20 bit	1	~
	Ryzen 93950X	2019	Zen 2 / 3.8 billion	3.5- 4.7 GHz	128 GB/ 13 64 MB	64 bit	64 bit	16	~
Samsung	Exynos 990	2020	ARM V8.2/ 8.5 billion	2.5 GHz	12 GB/ 2 MB	64 bit	64 bit	8	7 nm
MIPS	R2000	1985	RISC/110k	4.5 MHz	NA/64 KB	32 bit	32 bit	-	-
	MC250	2015	RISC/billion	0.75 GHz	NA/64 KB	64 bit	64 bit	-	-

(b) List of microcontrollers available in the market

Company Name	Microcontroller
Altera	Nios II 32-bit config. soft microprocessor. Nios 16-bit config. soft microprocessor
Analog Devices	Blackfin, SHARC, ARM7 and 8052 cores.
Atmel	MARC4, AVR32, AT91SAM.
Cypress Semiconductor	CY8C5XXX, ARM Cortex M3.
ELAN Microelectronics Corp.	EM78 PXXXN.
EPSON Semiconductor	S1C33 (32-bit), S1C17 (16-bit)
Espressif Systems	ESP32, ESP8266 (32-bit)
Freescal Semiconductor	MPC 577 (32-bit)
Fujitsu/Spansion	FCR4, FM4
Holtek	HT32XX 32-bit ARM core series
Hyperstone	32-bit Hyperstone RISC microprocessor
Infineon	Embedded Power 3Phase Bridge driver IC (TLE987x)
Intel	i5-10600K, i310100, i7-10700K, i910900K, etc. (These are few latest processors for PCs)

Lattice Semiconductor
Maxim Integrated
Microchip Tech.
National Semiconductor
NEC

NXP - Semiconductors

Nuvoton Tech.

Parallax

Rabbit Semiconductor

Renesas Electronics

Redpine Signals

Rockwell

Silicon Laboratories

Silicon Motion

Sony

Xeon Processors are
other high end Intel
processors available in
the market

Mi82 32-bit soft microprocessor

MIPS4kSD, ARM922T

PIC32MZ, PIC32MX

CR16, COP8

V60-V80, V850 (32-bit)

ARM Cortex M7

(RT1050, RT1050 series)

AM series, AM32 series

Propeller (8-core 32bit)

Rabbit 6000

H8SX, M32R

RS13100

R8070

ARM Cortex-M4 (EFM32)

SM370, SM350

SR110, SPC970,

SPC900, SPC700

STMicroelectronics
Texas Instruments

Toshiba

Ubicom

Xemics

Xilinx

XMOS

Zilog

8TM32 F7, H7.

TMS570, RM4 ARM

Cortex R4

TX19A (32-bit RISC)

TLCC-900 (16 & 32bit CISC)

IP3022, IP2022

XE8006 (8-bit)

Picoblaze, Microblaze

XCore XS1 - 32bit

Z16, eZ80, eZ8

(C) List of processor simulators available

① General Simulators

① PSIM (Processor Simulator): (2010)

② It graphically displays the architecture while showing the detailed operation on a per clock cycle basis. The instruction set consists of 25-instructions which can be combined to execute other complex capabilities along with conditional branching.

③ The ability to display and write to a file the contents of the program memory at any point in the.

Simulation. The "Bus Viewer" is a very powerful tool for understanding the internal operation of the processor architecture. It is a multicycle architecture, meaning that every instruction takes multiple clock cycles to execute.

b) The web elemental processor simulator :-

It enables us to see how values are modified for each clock cycle (at microprogramming level), and for each assembly instruction (at assembly level). Also we can compare different hardware, firmware, instruction sets, etc and assess the advantages/disadvantages. Multiplatform: web browser, standalone app, Android, IOS, Bash. Verbalised output for easy readability.

II) For ARM, MIPS32r5, MIPS32r6, Nios 2 :-

CPULator Computer System Simulator:

CPULator is a Nios II, ARMv7, and MIPS simulator of a computer system (processor and I/O devices). Runs in a modern web browser (no install required). Designed as a tool for learning assembly-language programming and computer organization. Support for some I/O devices. Input: Accepts both assembly source code and ELF executables. Debugger: Single step, Breakpoints, watchpoints, trace, call-stack, examine

memory and registers. Debug assertions: Optional runtime assertions catch many potential errors. Modify registers and memory in debugger. Max usable memory = 2042 MB, Max simulation speed 13 Minst/sec.

III) For ~~ARM TDM~~ MIPS:

1. MARS (MIPS Assembler and Runtime Simulator)

- Integrated editor, featuring multiple file editing tabs, context sensitive IP and color-coded assembly syntax. All assembly files in a single (folder) may be assembled into a single executable.
- Floating point registers, coprocessor(0) and (1).
- Variable speed execution.
- Any imaginable pseudo-~~code~~ ~~file~~ can be interfaced to MIPS assembly code, or extended to physical devices.
- Easily editable register and memory values, (like a spreadsheet).
- Developed by Missouri State Univ.

2. SPIM: A MIPS32 Simulator

- spim does not execute binary program.
- Provides a minimal set of OS services.
- spim implements almost the entire MIPS32 assembler extended instruction set.
- spim comes with complete source code and documentation.
- spim implements both a terminal & windows interface.

④ For x86 Simulators

MARS x86 simulator features :

- ① Multicore simulation environment for the x86-64 ISA with detailed pipeline model, including the breakdown of instructions into ops.
- ② Based on PLSim with extensive enhancements for improved simulation accuracy and performance. Avg. simulation commit rate of 200K+ INST/sec.
- ③ Ability to include pre-compiled libraries with the simulator.
- ④ Full debugging support using standard debuggers like GDB.
- ⑤ Full system simulation, including the simulation of unmodified OS.