Computer Architecture CS322 Lab 7 Report

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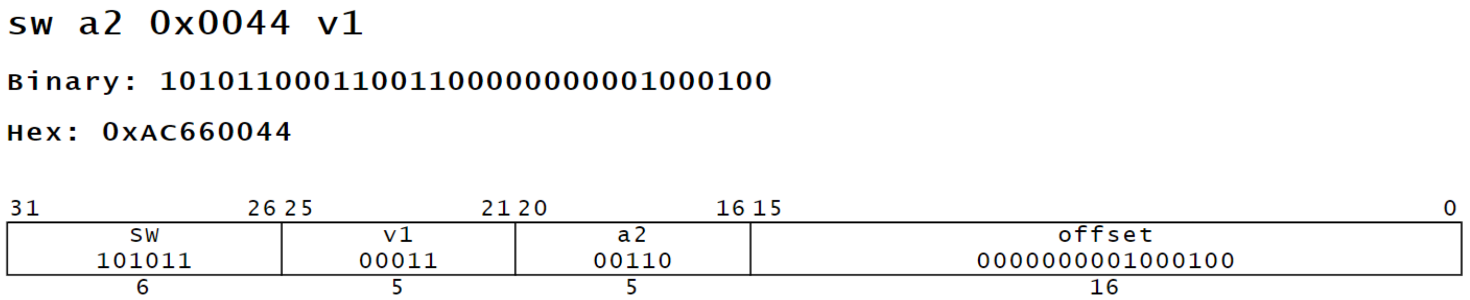
Task 1: Using blocks given blocks and other glue logic, implement single cycle RISC processor Instructions (given 32-bit reg file and 32-bit, memory blocks, ALU).

(a) sw $6, 68($3)

Encoding of the Instruction: -

$6 => $a2
68 => 0x0044
$3 => $v1

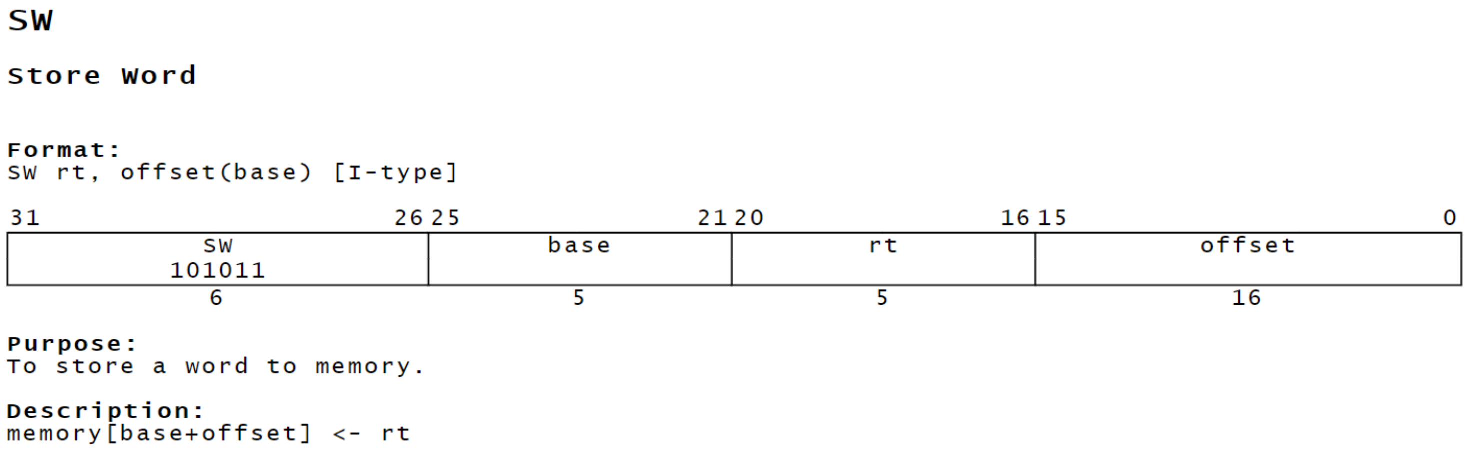


sw a2 0x0044 v1

Binary: 10101100011001100000000001000100

Hex: 0xAC660044

31 26	25 21	20 16	15 0
SW 101011	v1 00011	a2 00110	offset 0000000001000100
6	5	5	16



SW

Store Word

Format:
SW rt, offset(base) [I-type]

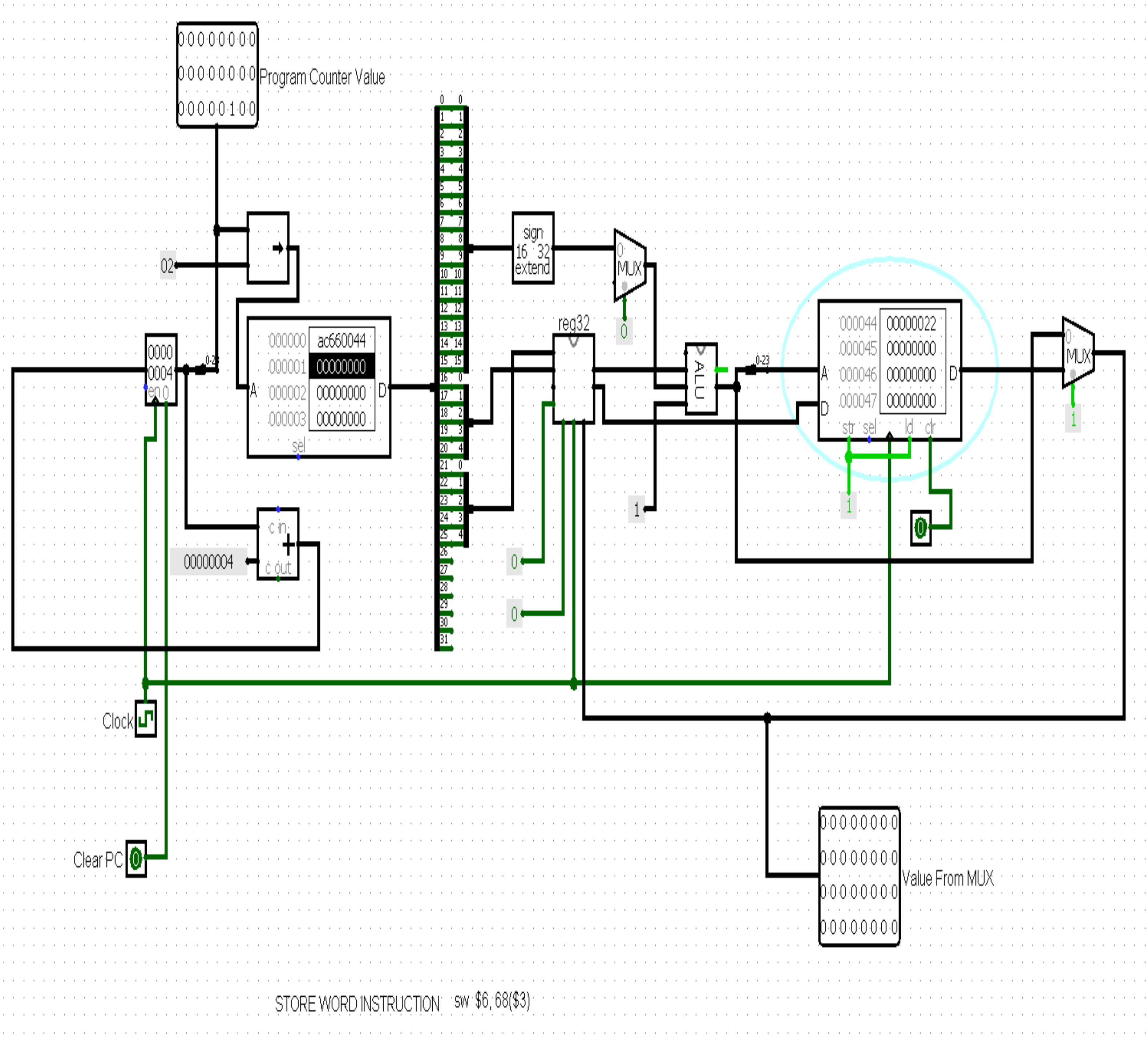
31 26	25 21	20 16	15 0
SW 101011	base	rt	offset
6	5	5	16

Purpose:
To store a word to memory.

Description:
memory[base+offset] <- rt

Used Hex Encoding: **0xAC660044**

Logisim Implementation:

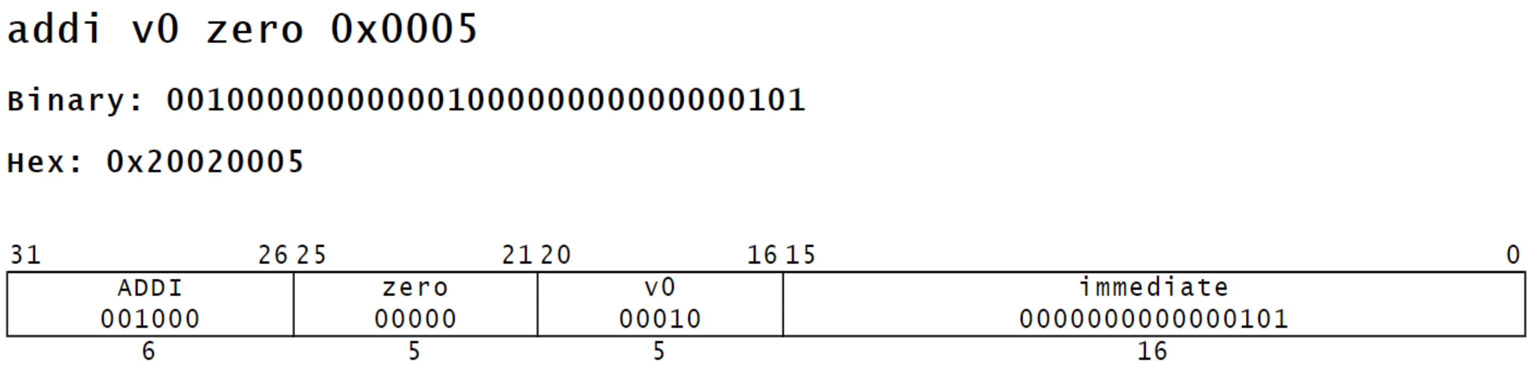


Stores value at given memory location (here, M[$3+68]) from source register (here, $6).

(b) addi $2, $0, 5

Encoding of the Instruction: -

$2 => $v0
5 => 0x0005
$0 => $zero



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addi v0 zero 0x0005

Binary: 00100000000000100000000000000101

Hex: 0x20020005
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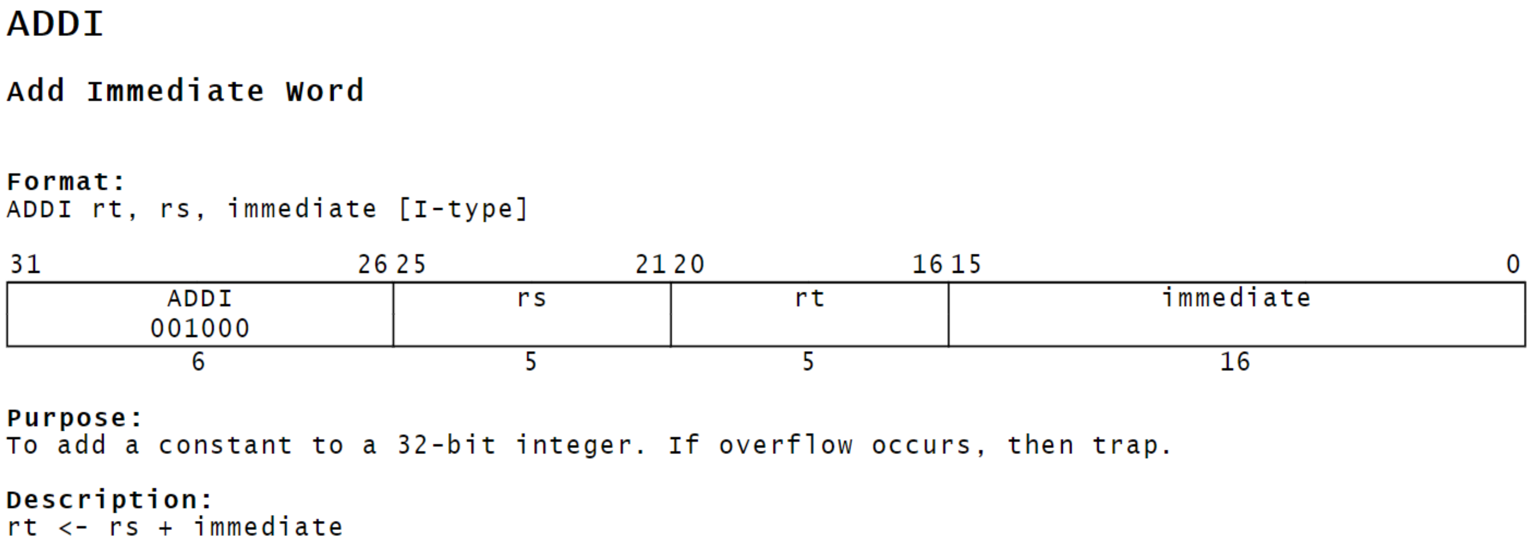
31 26	25 21	20 16	15 0
ADDI 001000	zero 00000	v0 00010	immediate 0000000000000101
6	5	5	16



ADDI

Add Immediate Word

Format:
ADDI rt, rs, immediate [I-type]

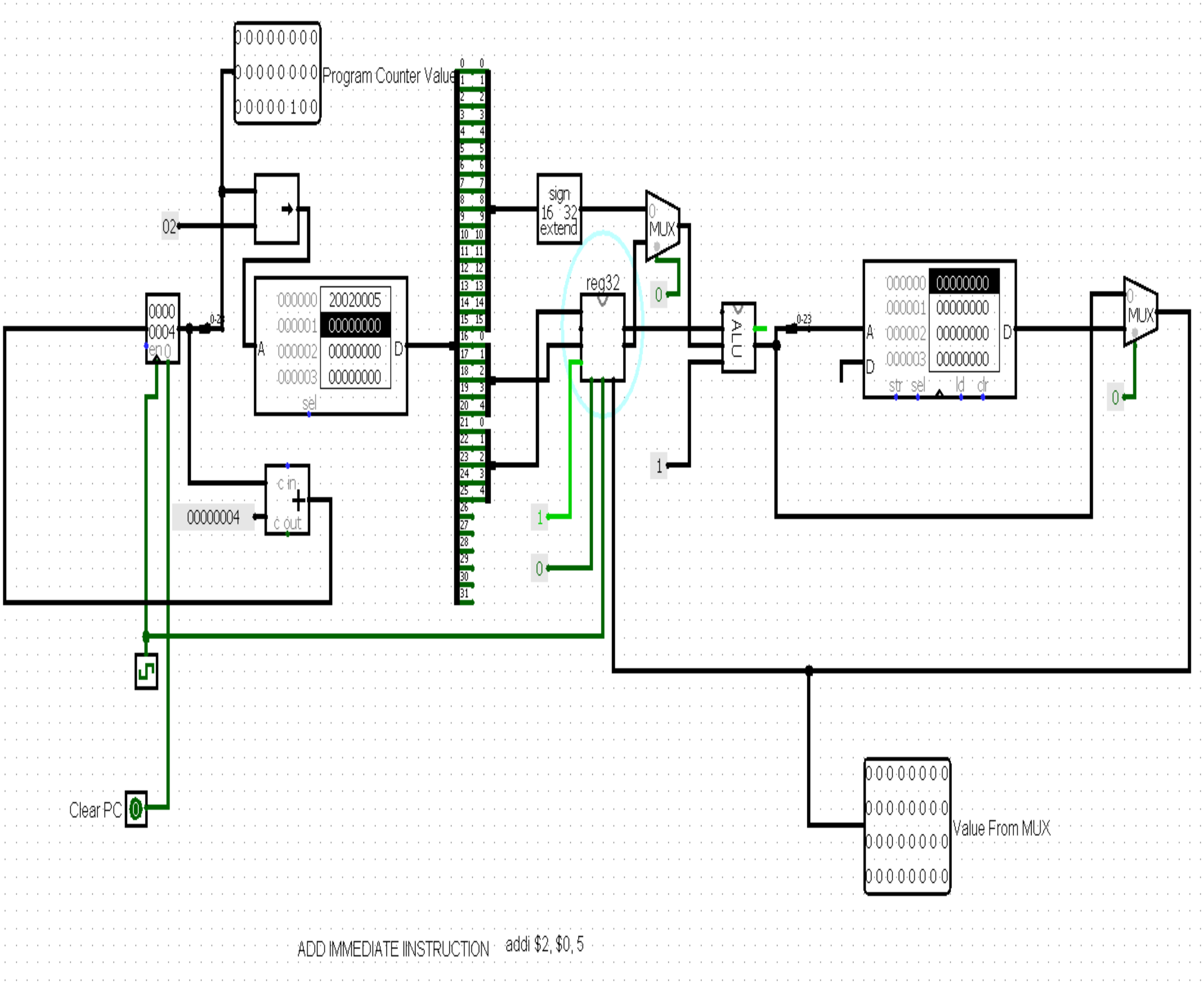
31 26	25 21	20 16	15 0
ADDI 001000	rs	rt	immediate
6	5	5	16

Purpose:
To add a constant to a 32-bit integer. If overflow occurs, then trap.

Description:
rt <- rs + immediate

Used Hex Encoding: 0x20020005

<u>Logisim Implementation</u>:

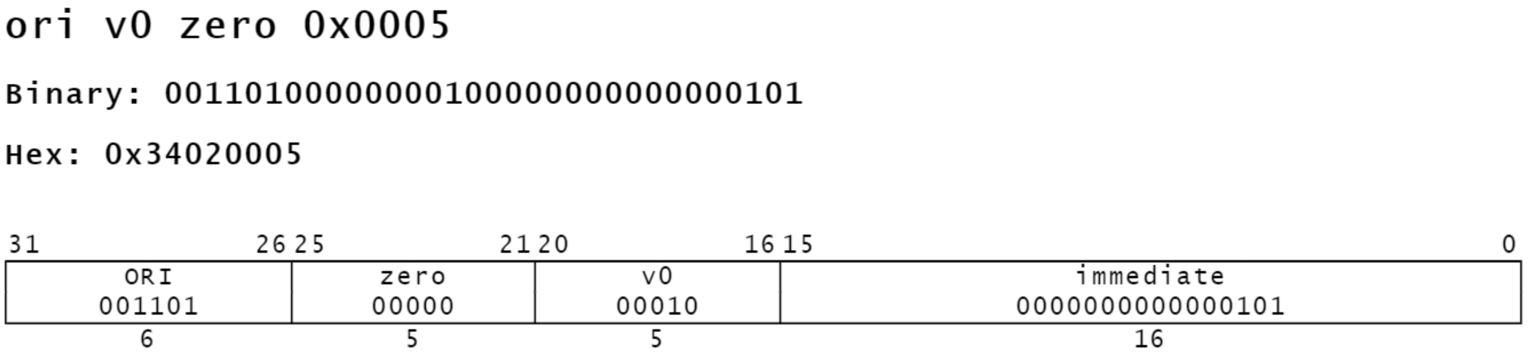


Adds immediate value (here,5) to source register (here, $0) and then stores the sum back to target register (here, $2)

(c) ori $2, $0, 5

<u>Encoding of the Instruction</u>: -

$2 => $v0
5 => 0x0005
$0 => $zero

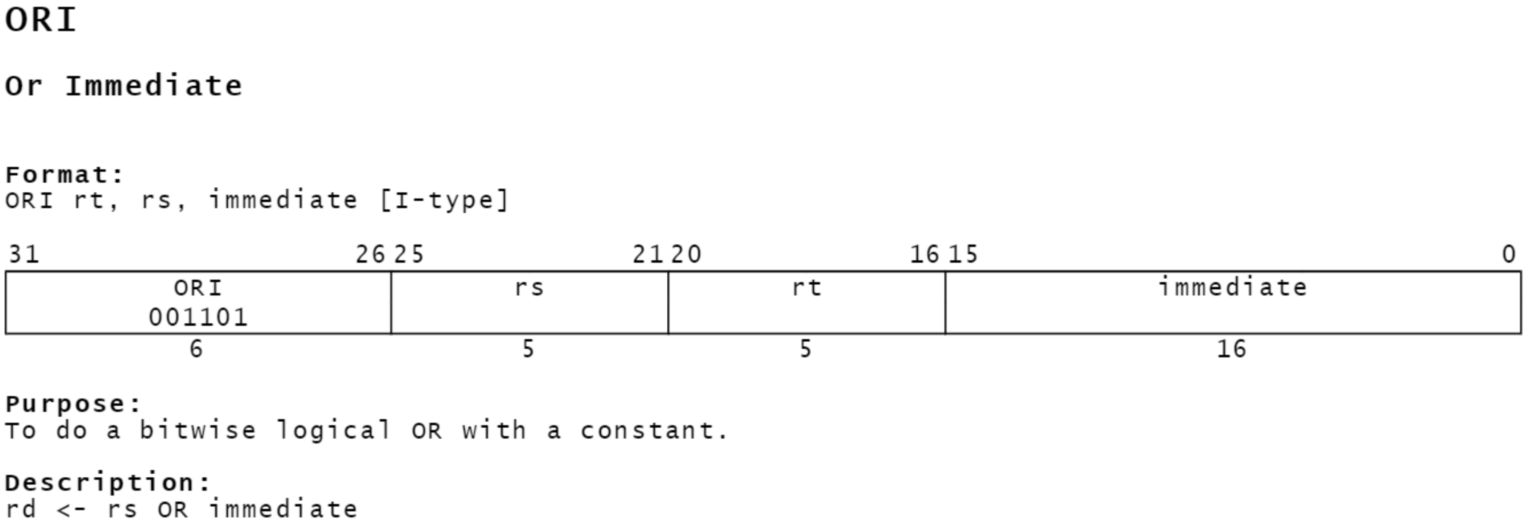


ori v0 zero 0x0005

Binary: 00110100000000010000000000000101

Hex: 0x34020005

31 26	25 21	20 16	15 0
ORI 001101	zero 00000	v0 00010	immediate 0000000000000101
6	5	5	16



ORI

Or Immediate

Format:
ORI rt, rs, immediate [I-type]

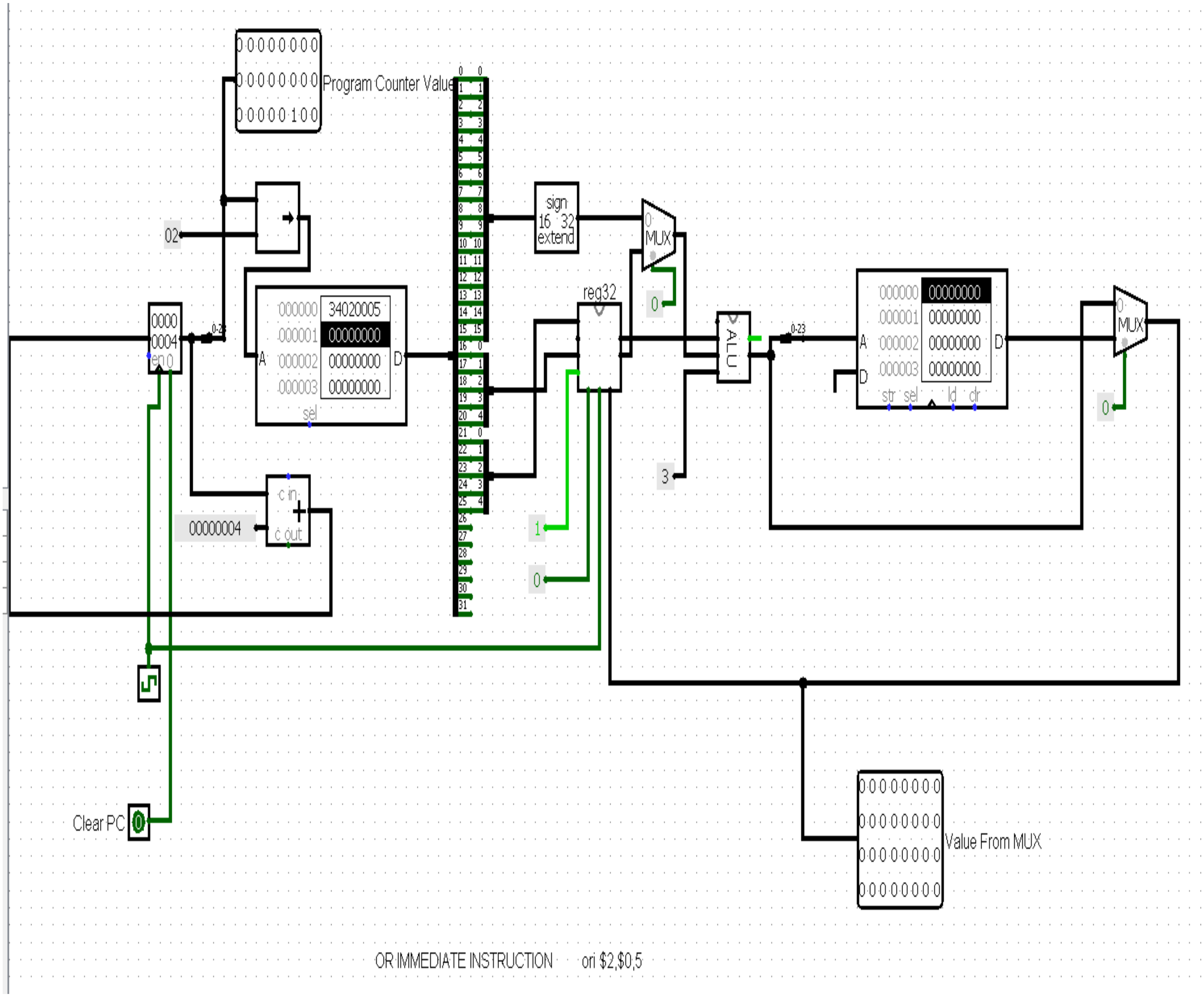
31 26	25 21	20 16	15 0
ORI 001101	rs	rt	immediate
6	5	5	16

Purpose:
To do a bitwise logical OR with a constant.

Description:
rd <- rs OR immediate

Used Hex Encoding: <u>0x34020005</u>

Logisim Implementation:



Performs or with immediate value (here,5) for source register (here, $0) and then stores the result back to target register (here, $2)