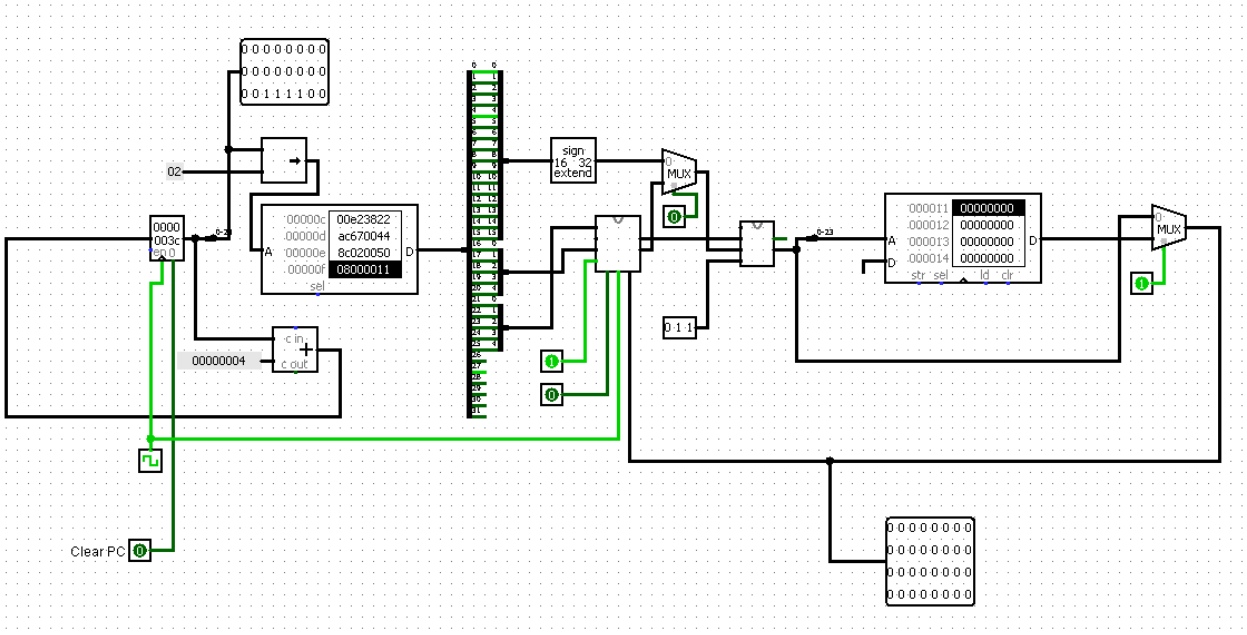
# Lab 7:Implement a RISC single Cycle Processor

Task 1: Using blocks given blocks and other glue logic, implement single cycle RISC processor instructions (a) sw $6, 68($3), (b) addi, $2, $0, 5, and (c) ori $2, $0, 5 (given 32 bit reg file and 32 bit, memory blocks, ALU). Implementation of lw $2, 80($0) is given below.

**(100 points** (30+30+40))




**Submission :**

Submit single doc/pdf file with above answers and *.circ files . Document should contain encoding of the instruction and screen shot of the implementation ( 3 different diagram) and respective *.circ files. Use file name Rollno_Lab7_1.circ, Rollno_Lab7_2.circ, Rollno_Lab7_3.circ

Submission through
https://u.pcloud.com/#page=puplink&code=a2E7ZfjUqWsGprVSLK1HtgW6n0XnqJhNX

**Due on 30th** October 2020, 11 PM**.**