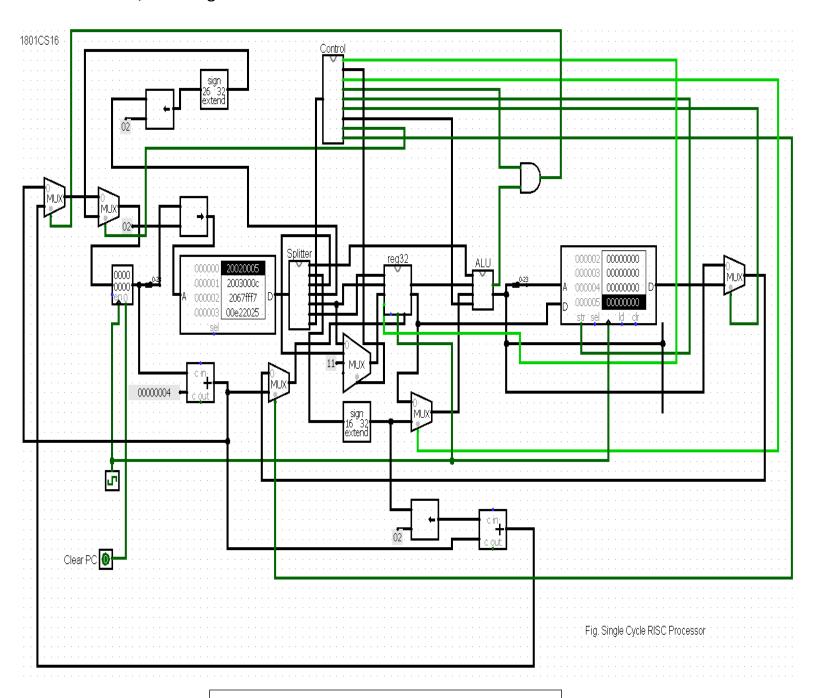
# **Computer Architecture CS322 Lab 8 Report**

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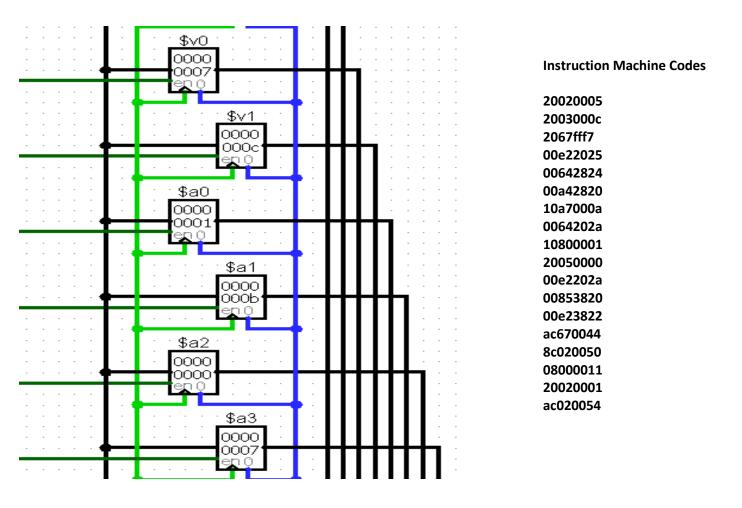
Date: 06/11/2020

**Task 1**: Using blocks from lab 7 and other glue logic, implement single cycle processor RISC which could run instructions/test file given.

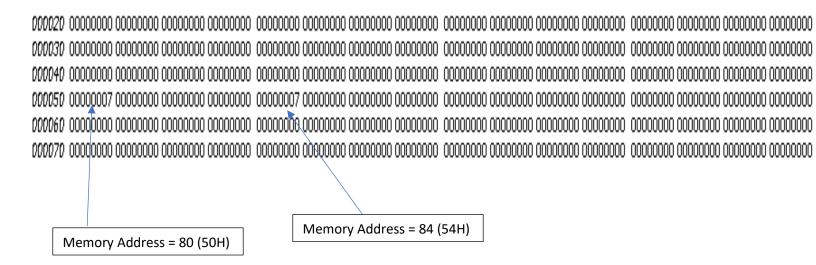


**Logisim Circuit: single cycle processor RISC** 

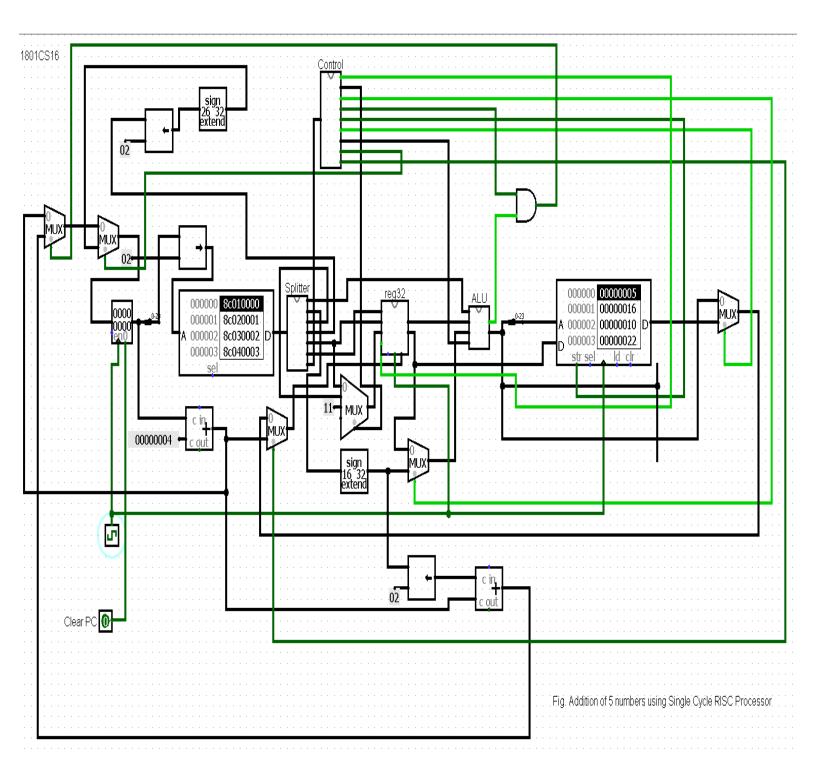
#### Final State of used registers after executing all instructions in instructions file



### Final State of Data Memory after execution of all instructions in instructions file



**Task 2**: Write a program to add 5 numbers and store the result in data memory location X. ( show the encoding process and machine language instruction with comments in the report). Also add screen shots of numbers in memory and result location in the report.

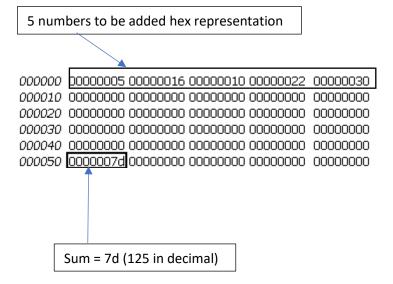


**Logisim Circuit: Addition using single cycle processor RISC** 

#### Assembly Code with corresponding encoding

```
# Test the MIPS Processor Task 2
# Write a program to add 5 numbers and store the result in data memory location X
# First data (5(05H),22(16H),16(10H),34(22H),48(30H)) [all in decimal rep.] is stored in memory location 0 to 5
sequentially
# sum will be stored in register $6 and then at memory location 80 i.e. 50H
#
        Assembly
                        Description
                                                 Address
                                                             Machine
        lw $1,0($0)
                        # $1 = 5
                                                0
                                                             8c010000
        lw $2,1($0)
                        # $2 = 22
                                                4
                                                             8c020001
        lw $3,2($0)
                        # $3 = 16
                                                8
                                                             8c030002
                        # $4 = 34
        lw $4,3($0)
                                                12
                                                             8c040003
                        # $5 = 48
        lw $5,4($0)
                                                16
                                                             8c050004
        addi $6,$0,$0 # $6 = 0
                                                 20
                                                             20060000
        add $6,$1,$2
                       # $6 <= 5 + 22 = 27
                                                 24
                                                             00223020
        add $6,$6,$3
                      # $6 <= 27 + 16 = 43
                                                 28
                                                             00c33020
                      # $6 <= 43 + 34 = 77
        add $6,$6,$4
                                                32
                                                             00c43020
        add $6,$6,$5
                      # $6 <= 77 + 48 = 125
                                                 36
                                                             00c53020
        sw $6,80($0)
                      # write addr 80 = 125
                                                40
                                                             ac060050
# mem addr 50H(80) \Rightarrow 7DH(125)
```

#### **Final Data Memory after Execution of Addition**



## Final state of used registers

