# Computer Architecture CS322 Lab 10 Report

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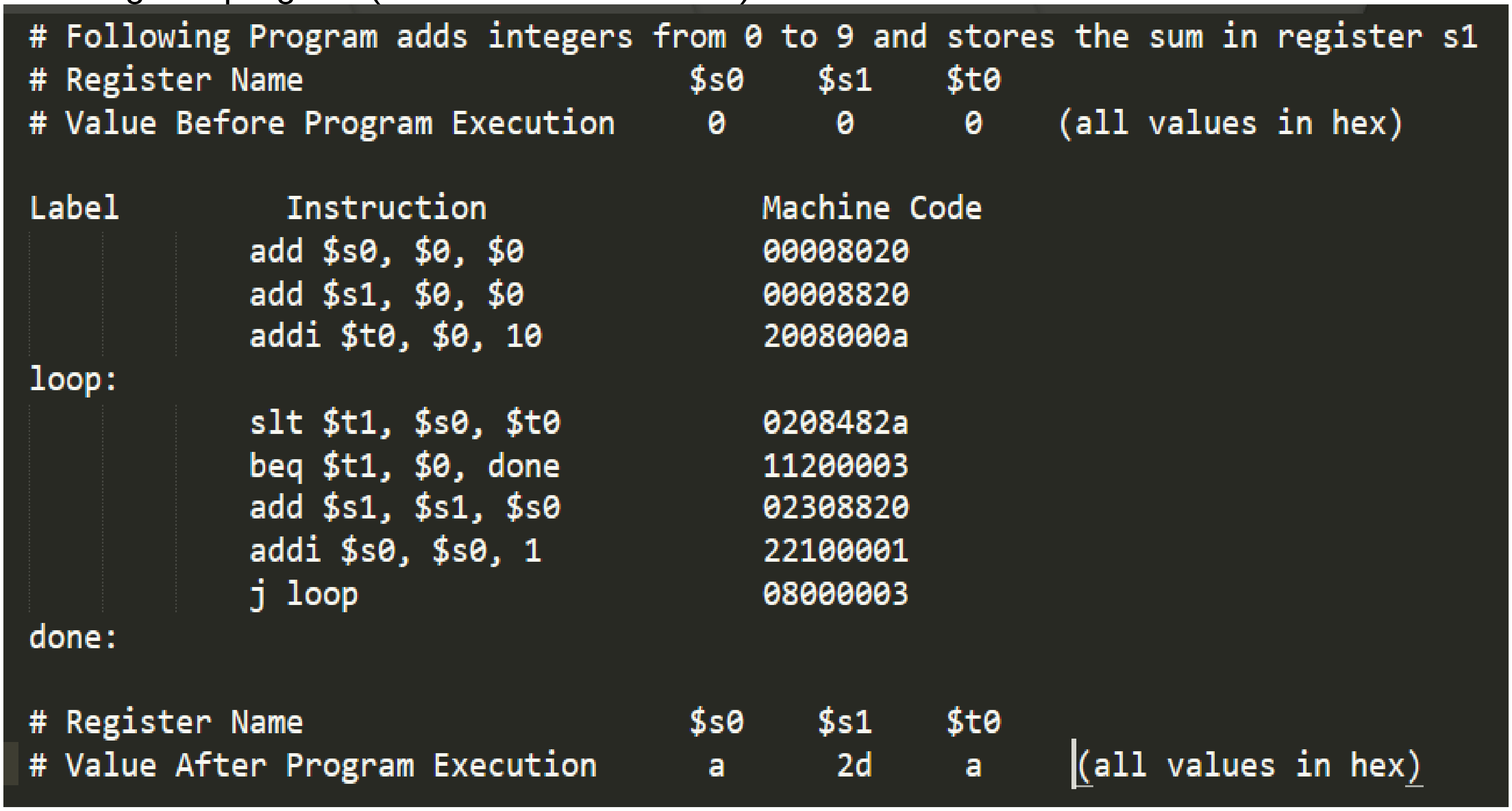
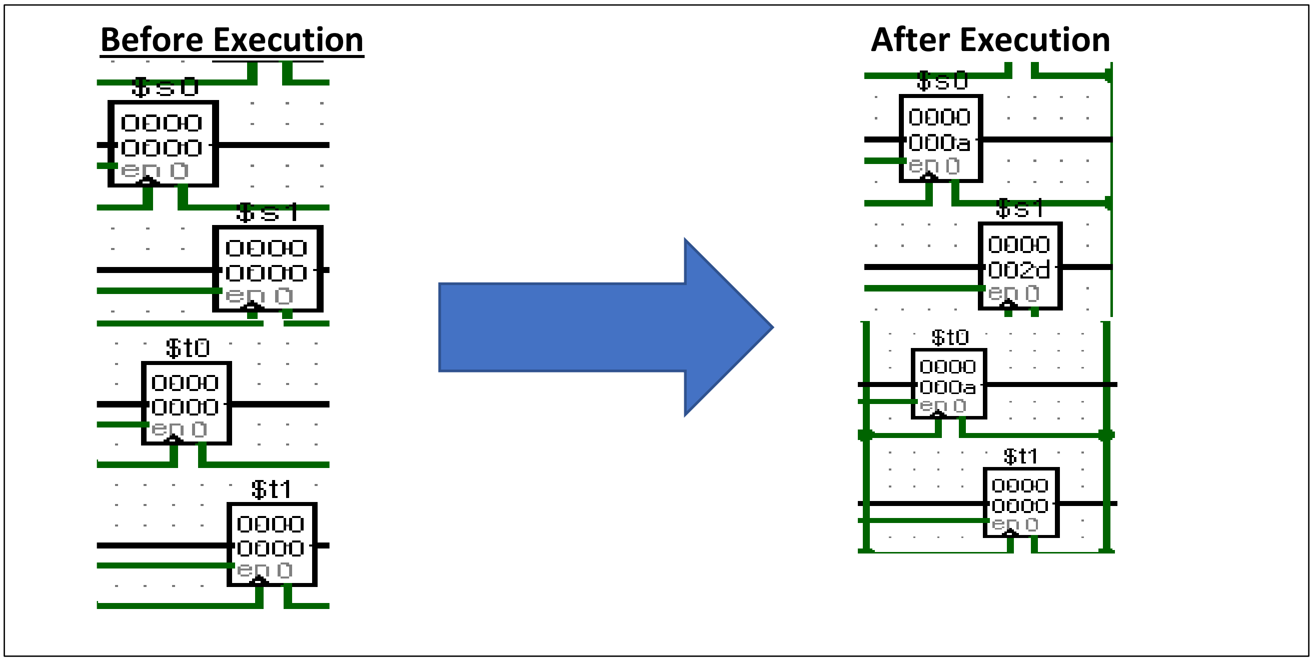
**Task 1**: Study the given ***piplelined-mips*** implementation of the processor and test using the following test program (create a new mem.dat)



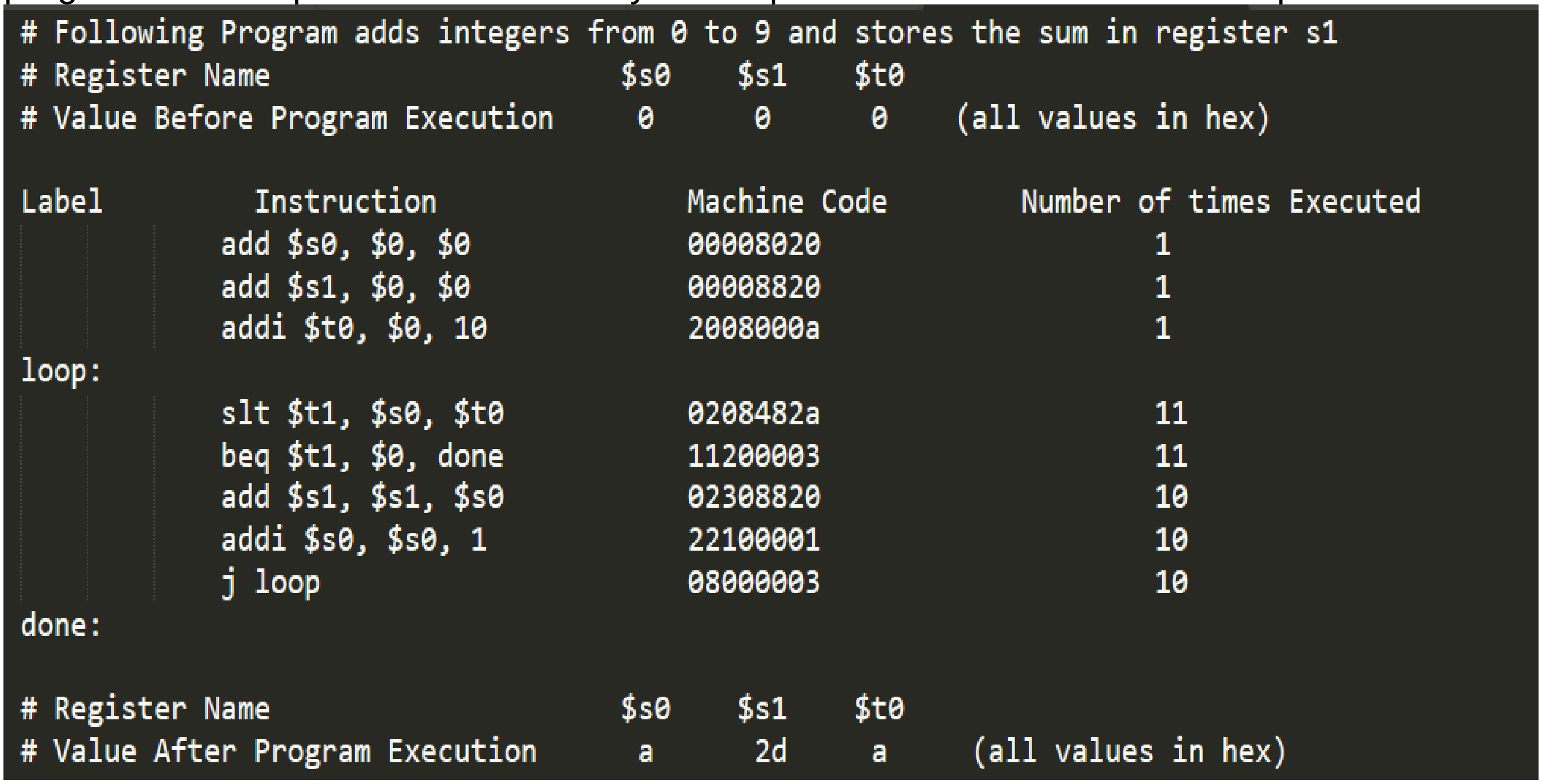
```
# Following Program adds integers from 0 to 9 and stores the sum in register s1
# Register Name                        $s0     $s1     $t0
# Value Before Program Execution        0       0       0     (all values in hex)

Label          Instruction                Machine Code
             add $s0, $0, $0              00008020
             add $s1, $0, $0              00008820
             addi $t0, $0, 10             2008000a
loop:
             slt $t1, $s0, $t0            0208482a
             beq $t1, $0, done            11200003
             add $s1, $s1, $s0            02308820
             addi $s0, $s0, 1             22100001
             j loop                       08000003
done:

# Register Name                        $s0     $s1     $t0
# Value After Program Execution         a       2d      a      (all values in hex)
```



**Task 2**: Compare given single-cycle, multi-cycle and pipe-line implementation. Run the above program and compute the number of cycles required in each of the case. Compute the CPI



```
# Following Program adds integers from 0 to 9 and stores the sum in register s1
# Register Name                     $s0    $s1    $t0
# Value Before Program Execution     0      0      0    (all values in hex)

Label         Instruction              Machine Code        Number of times Executed
            add $s0, $0, $0            00008020                   1
            add $s1, $0, $0            00008820                   1
            addi $t0, $0, 10           2008000a                   1
loop:
            slt $t1, $s0, $t0          0208482a                   11
            beq $t1, $0, done          11200003                   11
            add $s1, $s1, $s0          02308820                   10
            addi $s0, $s0, 1           22100001                   10
            j loop                     08000003                   10
done:

# Register Name                     $s0    $s1    $t0
# Value After Program Execution      a      2d     a     (all values in hex)
```

# **Total number of instructions executed** = 1 + 1 + 1 + 11 + 11 + 10 + 10 + 10 = **55**

# **Cycles Per Instruction (CPI)** = $\frac{\textbf{Total Number of Execution Cycles}}{\textbf{Total Number of Instructions Executed}}$

# **Single-Cycle Architecture**

Number of Cycles in Single Cycle Architecture = Total number of instructions executed = 55

For Single-Cycle Architecture, **CPI =** $\frac{55}{55}$ **= 1**

# **Multi-Cycle Architecture**

Number of Cycles in Multi Cycle Architecture = 1*4 + 1*4 +1*4 + 11*4 + 11*3 + 10*4 + 10*4 + 10*3 = 199

For Multi-Cycle Architecture, **CPI =** $\frac{199}{55}$ **= 3.6181**

# **Pipelined Architecture**

Number of Cycles in Pipelined Architecture = 128 (Calculated using Logisim)

For Pipelined Architecture, **CPI =** $\frac{128}{55}$ **= 2.3272**

**Submission Files:**

**Task 1:**

**Logisim: 1801CS16_Lab10_task1.circ**

**Code: code_task1.txt**

**Load Image File: loadfile_task1_and_task2**

**Task 2:**

**Logisim: 1801CS16_Lab10_task2_MIPS_MultiCycle.circ**

**Logisim: 1801CS16_Lab10_task2_MIPS_Pipelined.circ**

**Logisim: 1801CS16_Lab10_task2_MIPS_SingleCycle.circ**

**Code: code_task2.txt**

**Load Image File: loadfile_task1_and_task2**