INDIAN INSTITUTE OF TECHNOLOGY PATNA

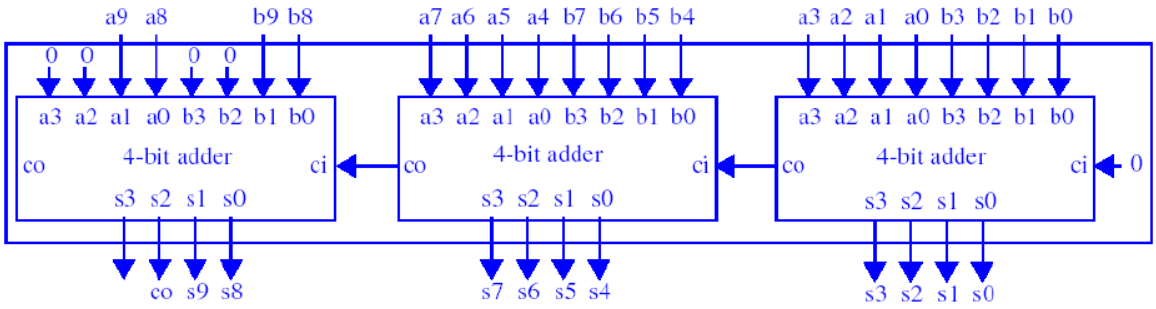
CS226-Lab

ALU- Design (Lab 6)

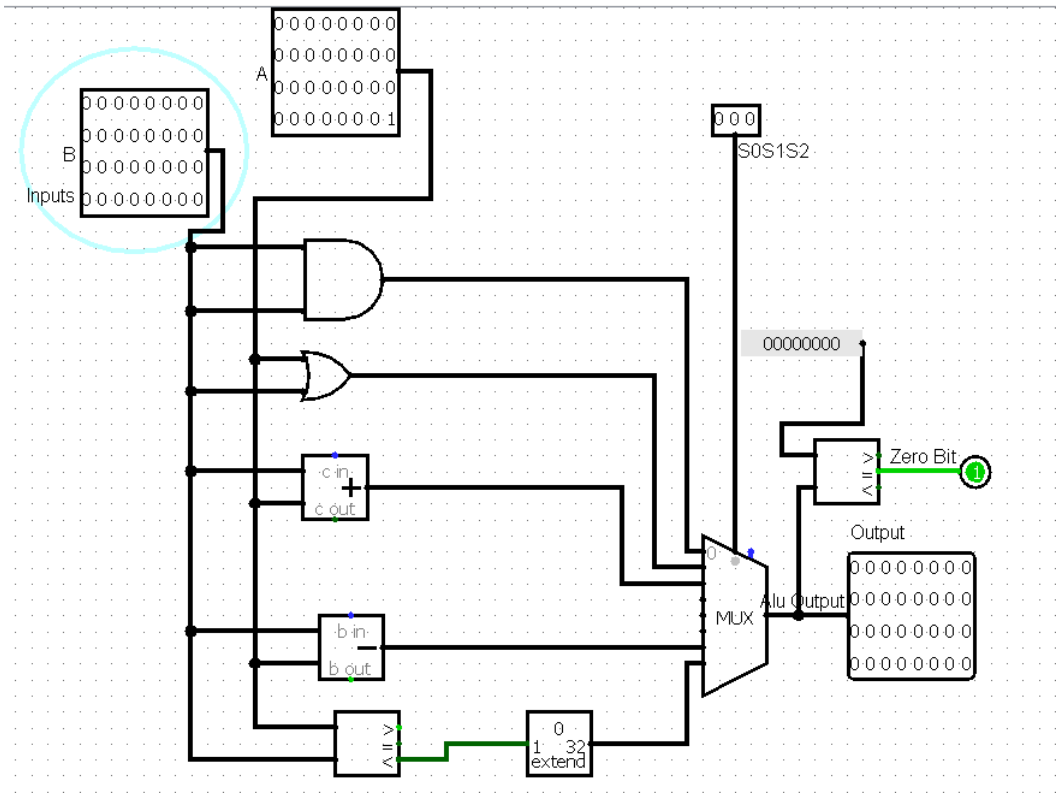
1. Design a 4 bit ALU which implements the flowing functionality (Addition, subtraction, AND & OR operating) (build 4 bit adder/subtractor from basic gates) A: a3 a2 a1 a0 ; B=b3b2b1b0 .

(25 points)

2. Design 10 bit adder using 4 bit adder from Problem 1**.**



3. Build 16 bit/32 bit ALU using logic-sim blocks (submit separate files ALU16.circ, ALU32.circ, test16.circ, test32.circ) . Functionality: Addition, subtraction, multiplication, division, AND , OR, XOR, NAND, NOR, XNOR and SLT (set less than). Also add a **zero-flag** detector. Whenever ALU output is zero, zero-flag is '1'



Submission:

Submit your .circ file containing your various transistor-level/logic level implementations. Hardcopy of the submission is required for this assignment. Show the simulations to TAs.

- The simulation files
- Zip the above files. Zip; file name is your role number.

Course work submission through Email: cs225.iitp@gmail.com
(use email subject Lab6_Logicsim_your roll number).
This work is due on: : 18th Feb 2020

Appendix