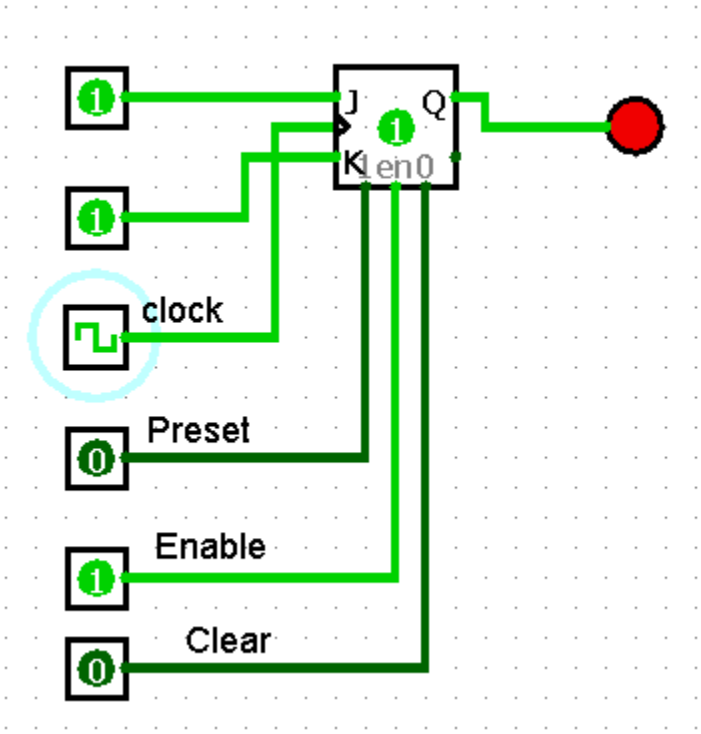
INDIAN INSTITUTE OF TECHNOLOGY PATNA

CS226- Lab 8

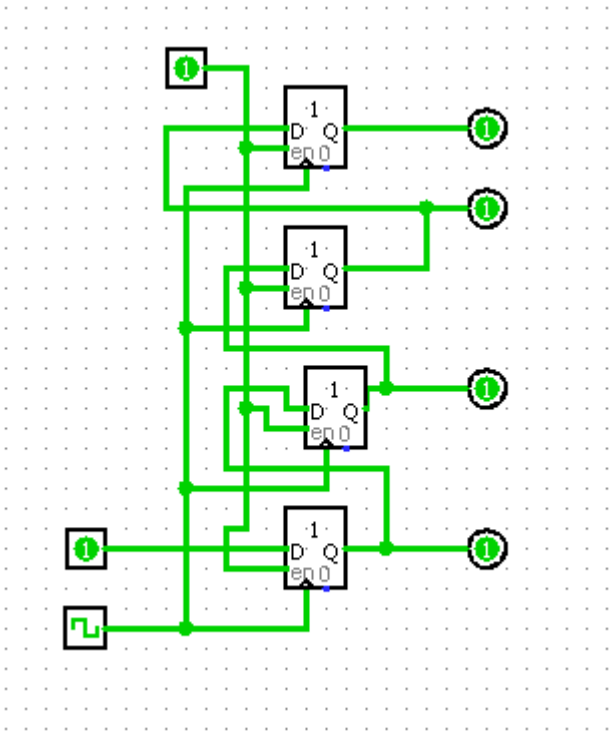
(Sequential Logic Design)

Q0: Study basic sequential elements SR, J-K ,T and D flip flops.

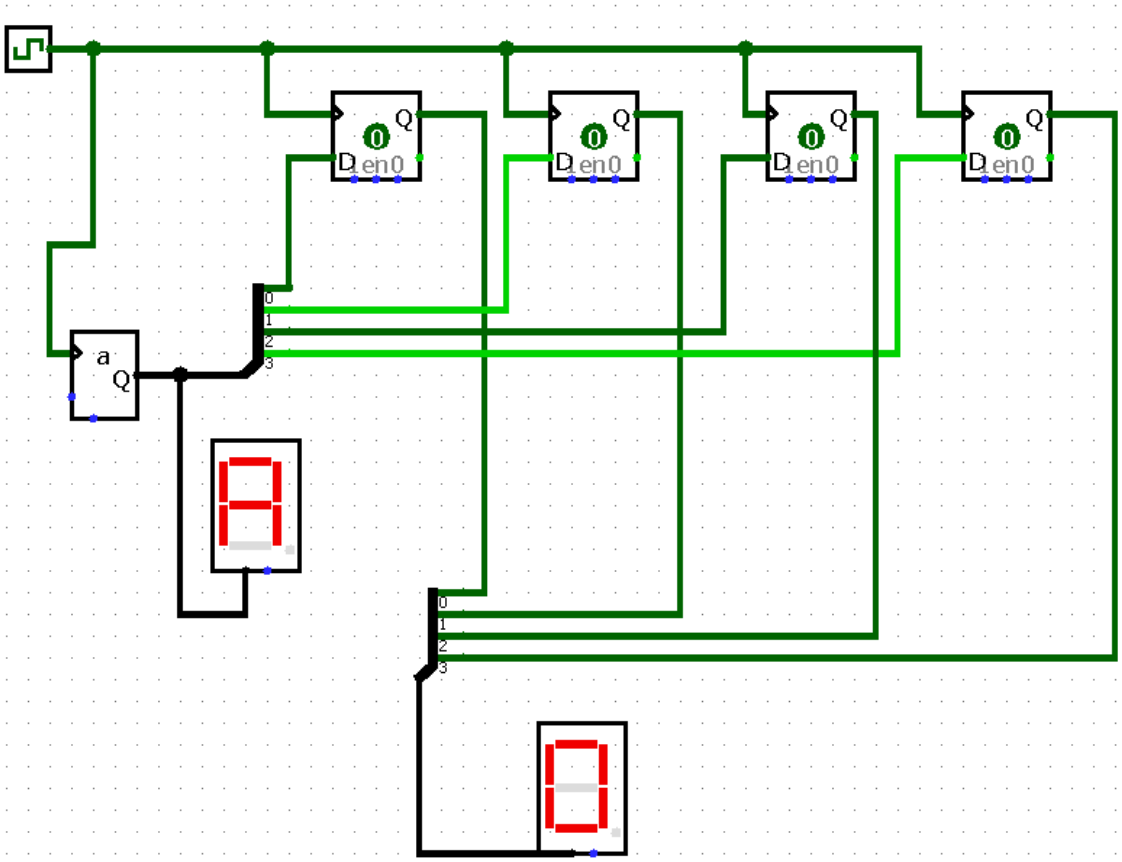
Eg. J-K example is shown here. Test all possible input combinations for each of the memory elements.



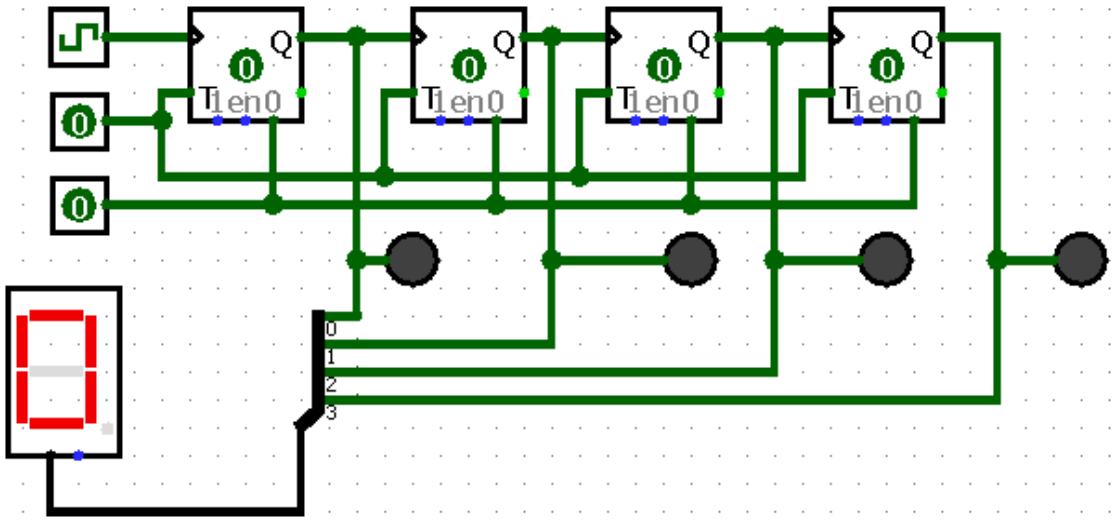
Q1: Simulate a 8 bit shift register using logic-sim. A 4 bit shift register design is shown.



Q2: Simulate a 4 bit parallel in Parallel out(PIPO) register. Design a 4 bit parallel in Parallel out(PIPO) register.



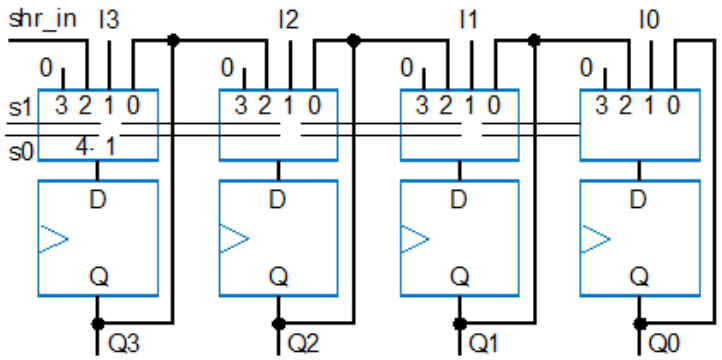
Q3: Simulate a 4 bit counter using T flip flops. Design a 6 bit counter using T flip flops



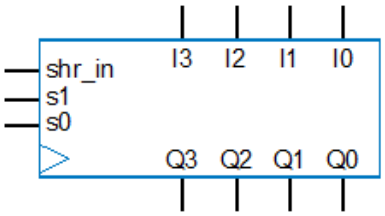
Q4:Simulate the multi-function Shift register using logic-sim. Design an 8 bit version.

Functions:

s1	s0	Operation
0	0	Maintain present value
0	1	Parallel load
1	0	Shift right
1	1	(unused - let's load 0s)

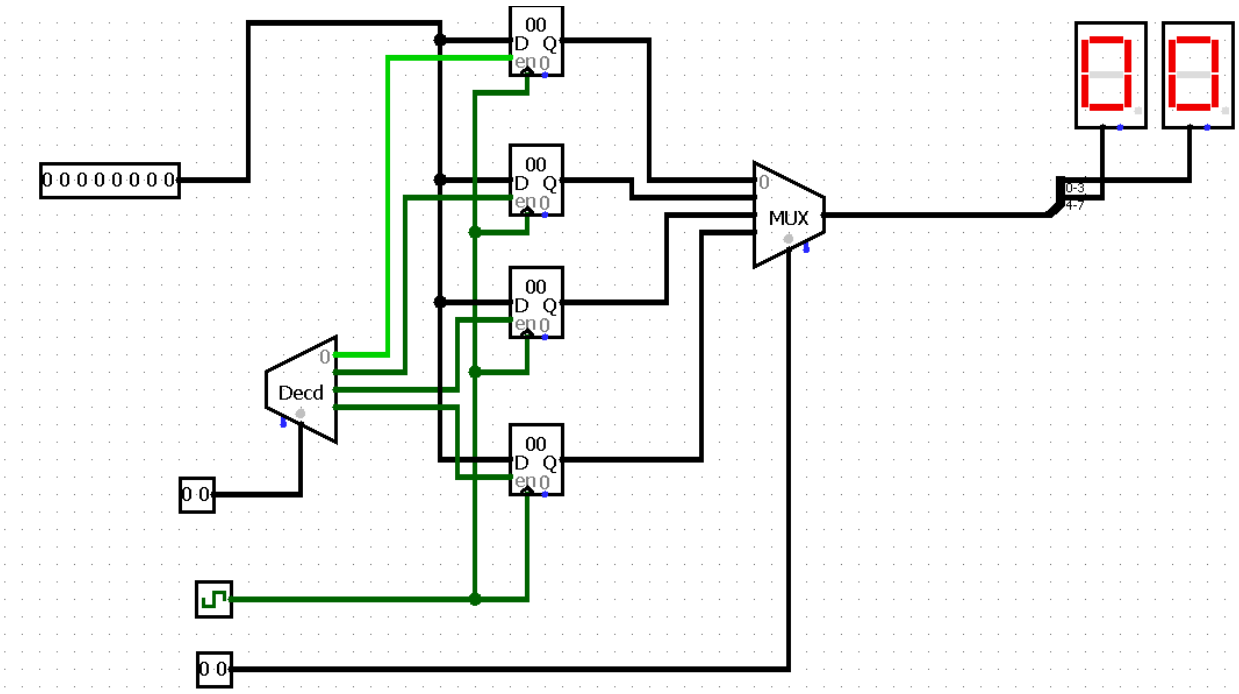


(a)



(b)

Q5: Here a 4x8 register file is shown. Design a 16x16 register file (include register file enable)



Logic-sim simulation submission should be individual. Course work submission through Email: cs225.iitp@gmail.com
(use email subject Lab8_Logicsim_your roll number).

Include a detailed word document or pdf with answers to each of the questions along with .circ file.

(submit a single zip file-doc+ *.circ s). Submission deadline 7th April 5 PM.

Meeting Information

Meeting Topic:	jimson jimson's Personal Room
Location:	https://iitpatna.webex.com/iitpa...
Meeting number:	577 377 383
India Toll (Delhi):	+91-11-6480-0114
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> Global call-in numbers	
Access code:	577 377 383