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Date :- 23/04/2020

CS226 - Switching Theory Lab-10

Q.1) Design a two bit counter with following specs.

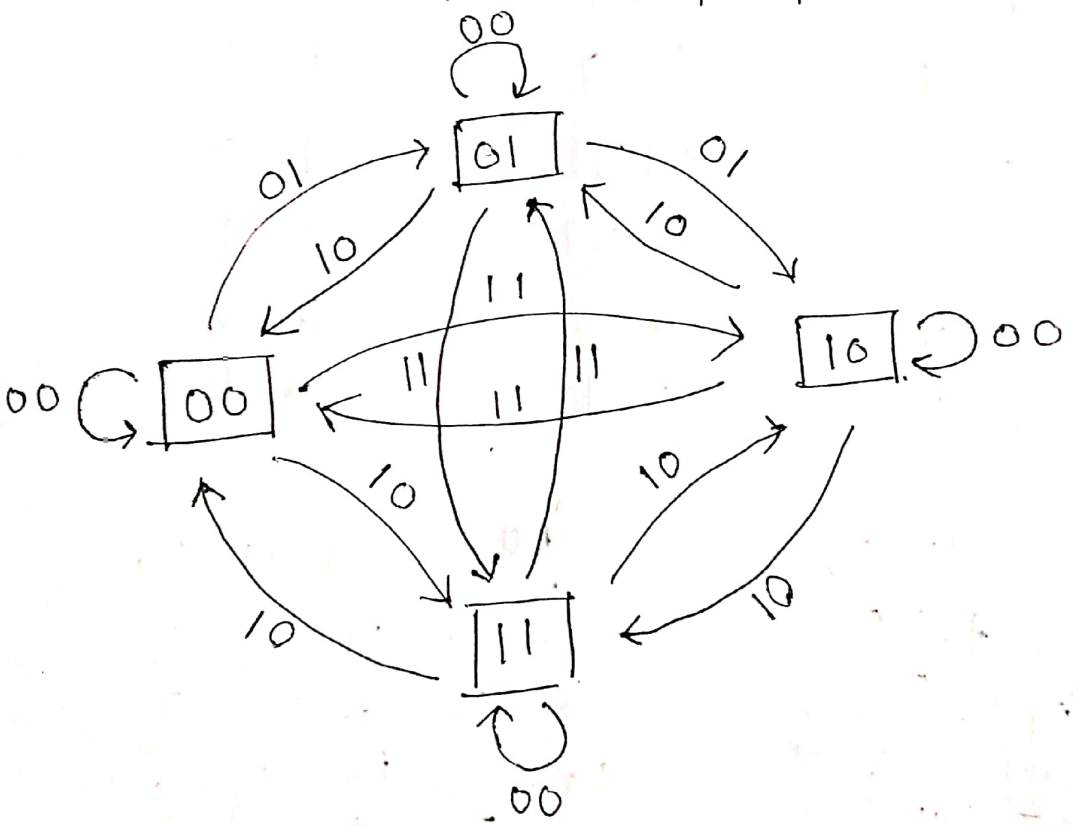
C_0	C_1	Operation
0	0	Stop Counting
0	1	Count up by one
1	0	Count down by one
1	1	Count by two.

State diagram

Total no. of states = 4.

00, 01, 10, 11.

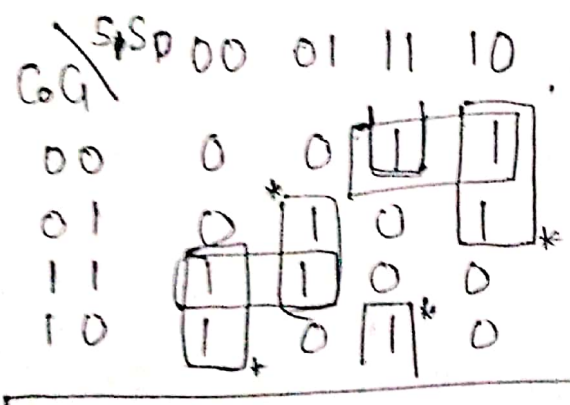
No. of flipflops required = 2.



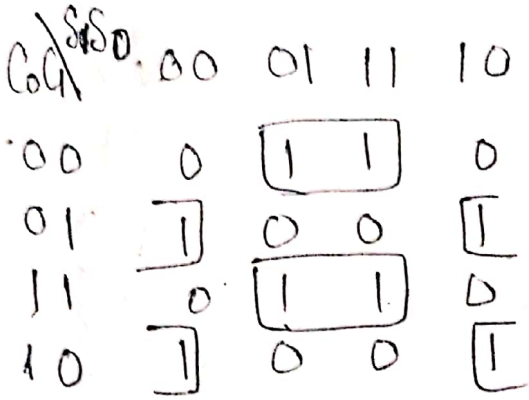
On each arrow, in the direction of arrow Inputs C_0, C_1 are mentioned respectively.

② Implementation using D-flipflop

Inputs		Current State		Next State		Flipflop Inputs	
C_0	C_1	S_1	S_0	N_1	N_0	D_1	D_0
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0
0	0	1	1	1	1	1	1
0	1	0	0	0	1	0	1
0	1	0	1	1	0	1	0
0	1	1	0	1	1	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1
1	0	0	1	0	0	0	0
1	0	1	0	0	1	0	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	1	0	1



$$D_1 = C_0\bar{S}_0\bar{S}_1 + C_1\bar{S}_0\bar{S}_1 + \bar{C}_1S_0S_1 + \bar{C}_0\bar{S}_0\bar{S}_1$$



$$D_0 = S_0(\bar{C}_1\bar{C}_0 + C_1C_0) + \bar{S}_0(C_1 \oplus C_0)$$

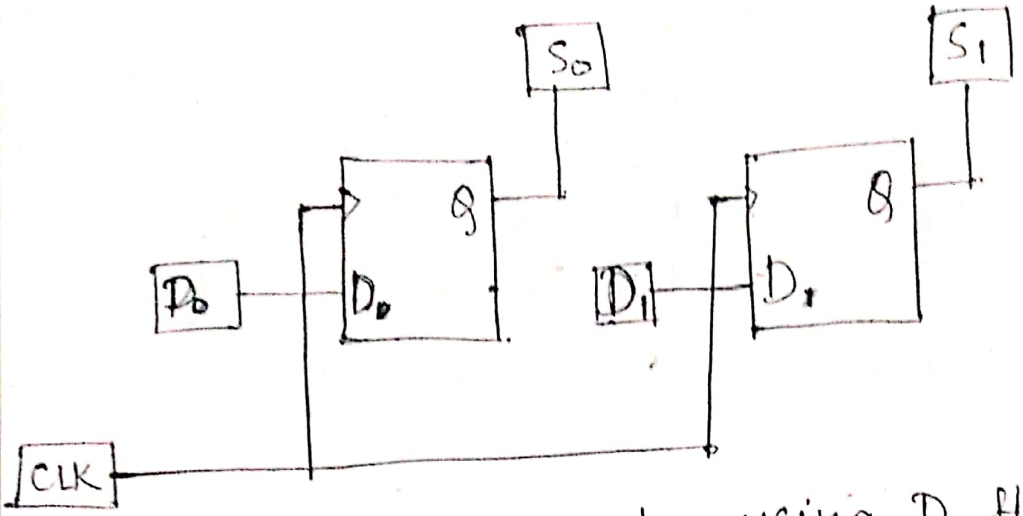


Fig. 2-bit counter using D flip-flops.

(b) Implementation using T-flipflop.

Operation		Current State		Next State		Flipflop Inputs	
C_0	C_1	S_1	S_0	N_1	N_0	T_1	T_0
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	0	0	1
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	1
1	1	0	0	1	0	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	0
1	1	1	1	0	1	1	0

C_0C_1 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	1	1
10	1	0	0	1

$$T_1 = S_0C_1 + \bar{S_0}C_0$$

C_0C_1 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$$T_0 = C_0 \oplus C_1$$

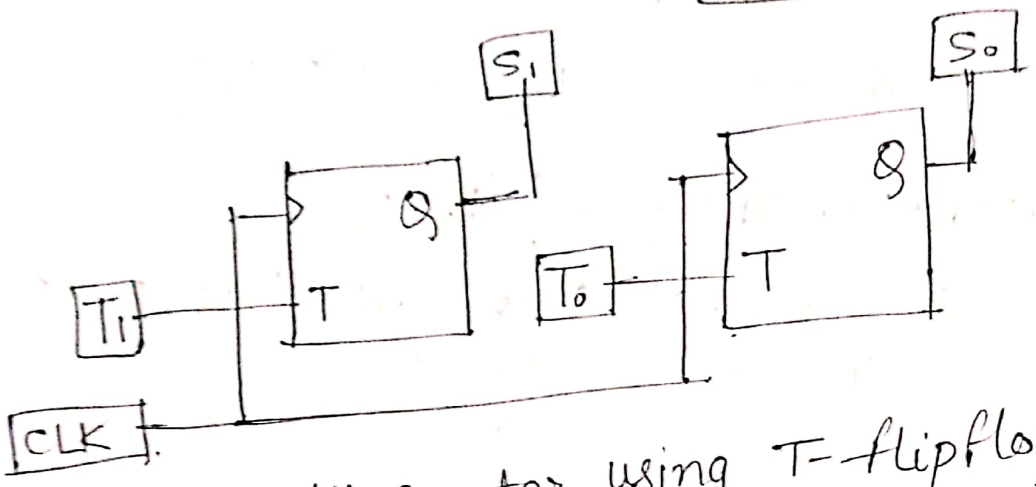


Fig. 2-bit counter using T-flipflop.

(c) Implementation using SR flipflop:

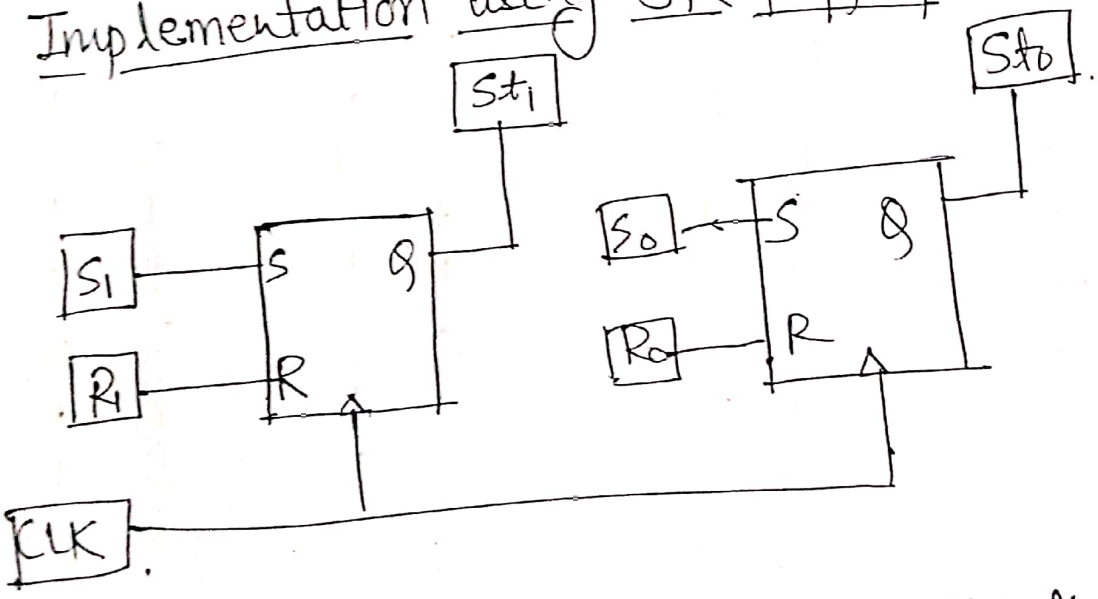


Fig. 2-bit counter using SR flipflop.

Inputs		Current State		Next State		Flipflop Inputs			
C_0	C_1	S_{t_1}	S_{t_0}	N_1	N_0	S_1	R_1	S_0	R_0
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	1	0	X	X	0
0	0	1	0	1	0	X	0	0	X
0	0	1	1	1	1	X	0	X	0
0	1	0	0	0	1	0	X	1	0
0	1	0	1	1	0	1	0	0	1
0	1	1	0	1	1	X	0	1	0
0	1	1	1	0	0	0	1	0	1
1	0	0	0	1	1	1	0	1	0
1	0	0	1	0	0	0	X	0	1
1	0	1	0	0	1	0	1	1	0
1	0	1	1	1	0	X	0	0	1
1	1	0	0	1	0	1	0	0	X
1	1	0	1	1	1	1	0	X	0
1	1	1	0	0	0	0	1	0	X
1	1	1	1	0	1	0	1	X	0

C_0C_1 \ $S_{t_1}S_{t_0}$	00	01	11	10
00	0	0	X	X
01	0	1	0	X
11	1	1	0	0
10	1	0	X	X

$$S_1 = C_0\overline{S_{t_1}}\,\overline{S_{t_0}} + C_1\overline{S_{t_1}}S_{t_0}$$

C_0C_1 \ $S_{t_1}S_{t_0}$	00	01	11	10
00	0	X	X	0
01	1	0	0	1
11	0	X	X	0
10	1	0	0	1

$$S_0 = \overline{C_0}C_1\overline{S_{t_0}} + C_0\overline{C_1}\,\overline{S_{t_0}}$$

C_0C_1 \ $S_{t_1}S_{t_0}$	00	01	11	10
00	X	X	0	0
01	X	0	1	0
11	0	0	1	1
10	0	X	0	1

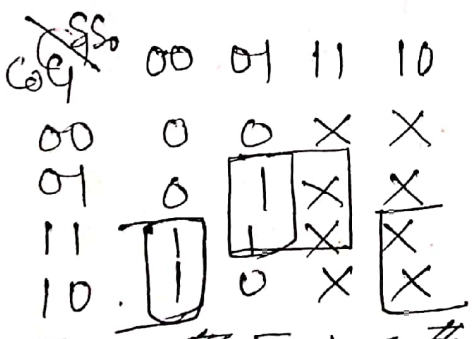
$$R_1 = C_1S_{t_1}S_{t_0} + C_0S_{t_1}\overline{S_{t_0}}$$

C_0C_1 \ $S_{t_1}S_{t_0}$	00	01	11	10
00	X	0	0	X
01	0	1	1	0
11	X	0	0	X
10	0	1	1	0

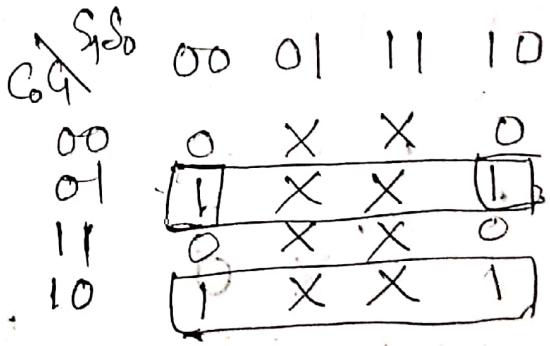
$$R_0 = \overline{C_0}C_1S_{t_0} + C_0\overline{C_1}S_{t_0}$$

(d) Implementation using JK flipflop

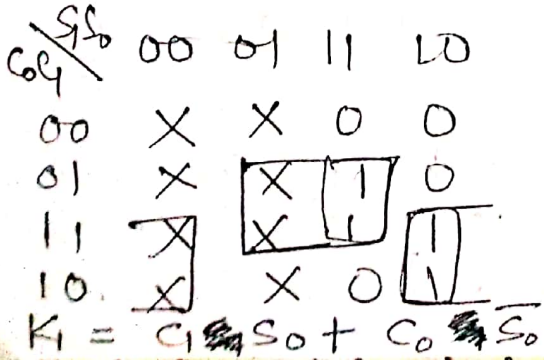
Inputs		Current State		Next State		Flipflop Inputs			
C_0	C_1	S_1	S_0	N_1	N_0	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	1	0	X	X	0
0	0	1	0	1	0	X	0	0	X
0	0	1	1	1	1	X	0	X	0
0	1	0	0	0	1	0	X	1	X
0	1	0	1	1	0	1	X	X	1
0	1	1	0	1	1	X	0	1	X
0	1	1	1	0	0	X	1	X	1
1	0	0	0	1	1	1	X	1	X
1	0	0	1	0	0	0	X	X	1
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	0	X	0	X	1
1	1	0	0	1	0	1	X	0	X
1	1	0	1	1	1	1	X	X	0
1	1	1	0	0	0	X	1	0	X
1	1	1	1	0	1	X	1	X	0



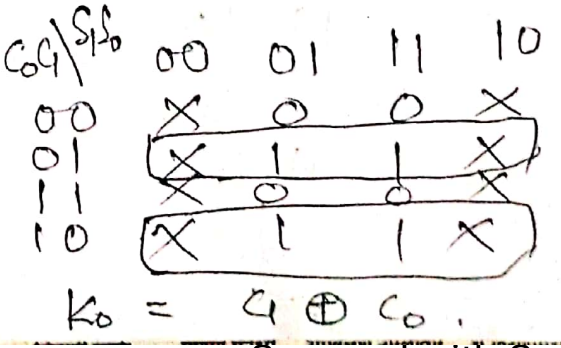
$J_1 = C_0 \bar{S}_0 + C_1 S_0$



$J_0 = \bar{C}_0 C_1 + C_0 \bar{C}_1 = C_1 \oplus C_0$



$K_1 = C_1 S_0 + C_0 \bar{S}_0$



$K_0 = C_1 \oplus C_0$

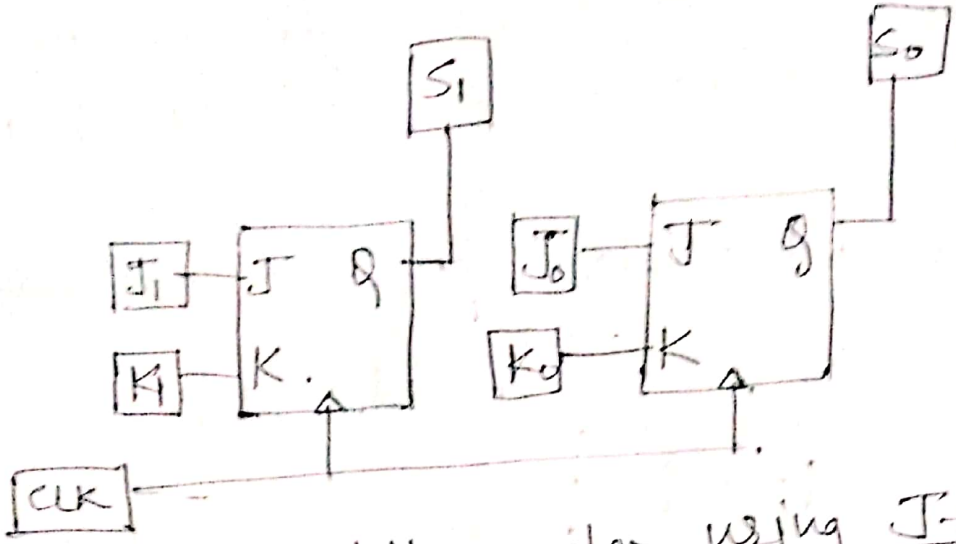


Fig. 2-bit counter using J-K flipflop

Q.2) Design 8-bit adder using a single bit full-Adder and shift register. A,B (Inputs) Y (output).

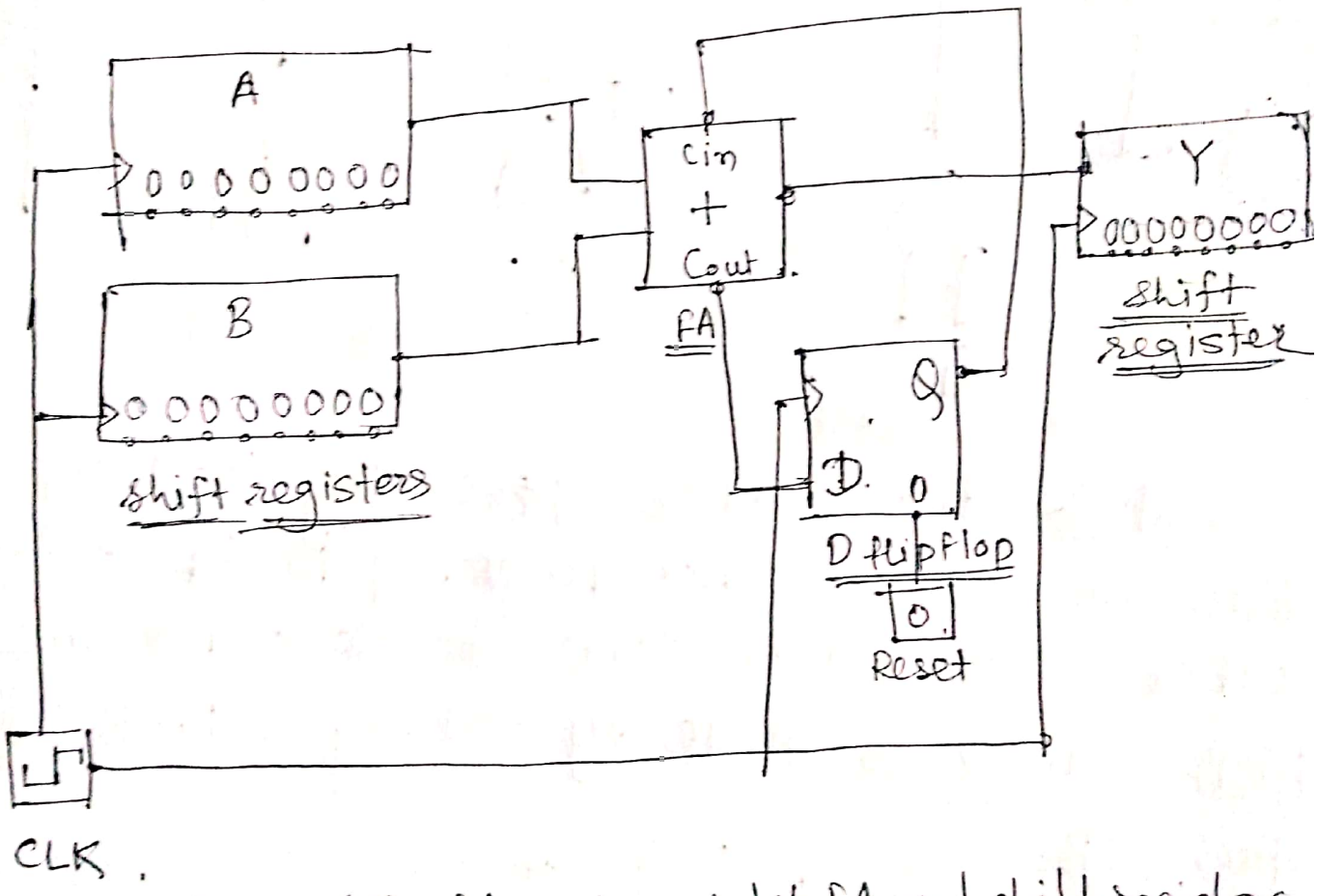
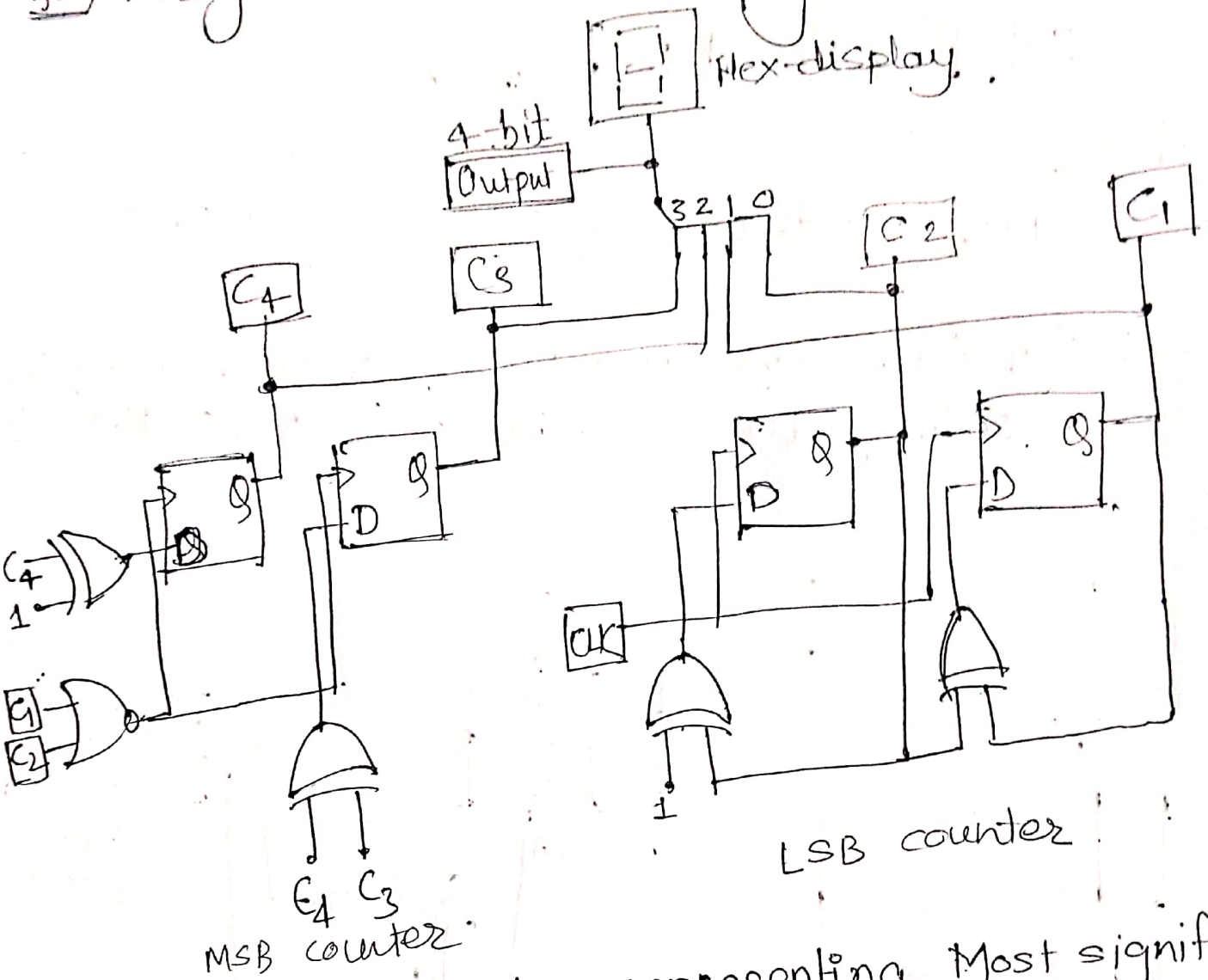


Fig. 8-bit FA using 1-bit FA and shift registers.

It will require 8 clock pulses for complete addition i.e Y=A+B. If we use a FA which is capa

-ble of adding more no. of bits, then consequently no of clock pulses (time) req. will reduce proportionately.

Q.3) Design a 4-bit counter using two 2-bit counters.



Just for the counter representing Most significant bits we have to reduce frequency to 1/4 of the other. This can be done if clock for the MSB counter is made by taking a NOR of two LSBs.