**Switching Theory Lab (CS226) - 12**

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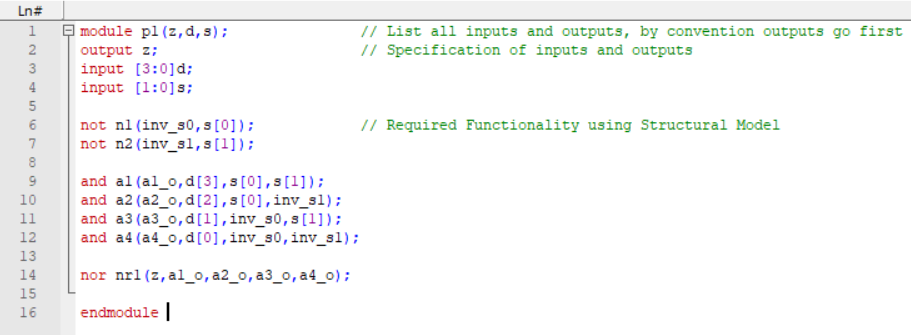
Roll No. : 1801cs16

Date : 09/05/2020

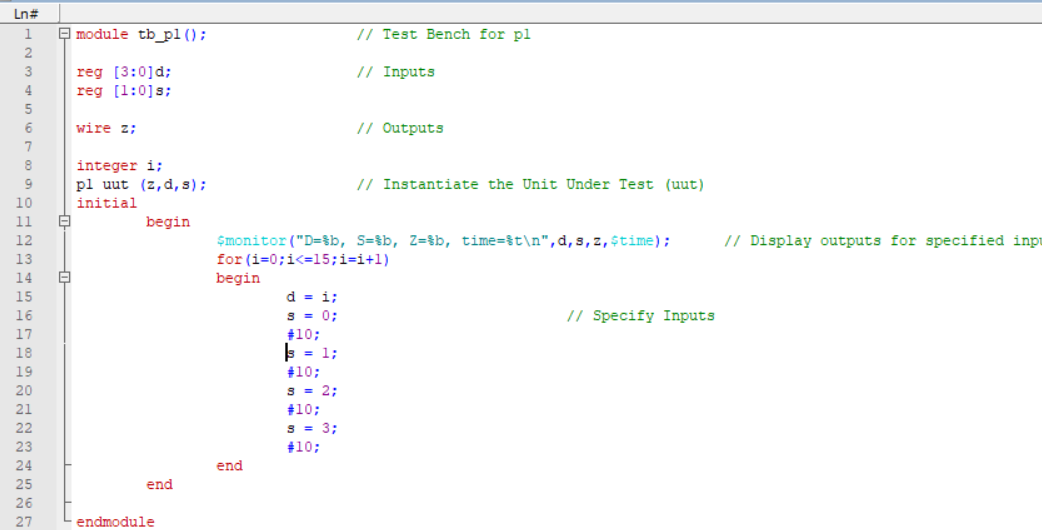
(Q1) Model the following logic function using Verilog gate level description and design appropriate test bench.

Sol : -

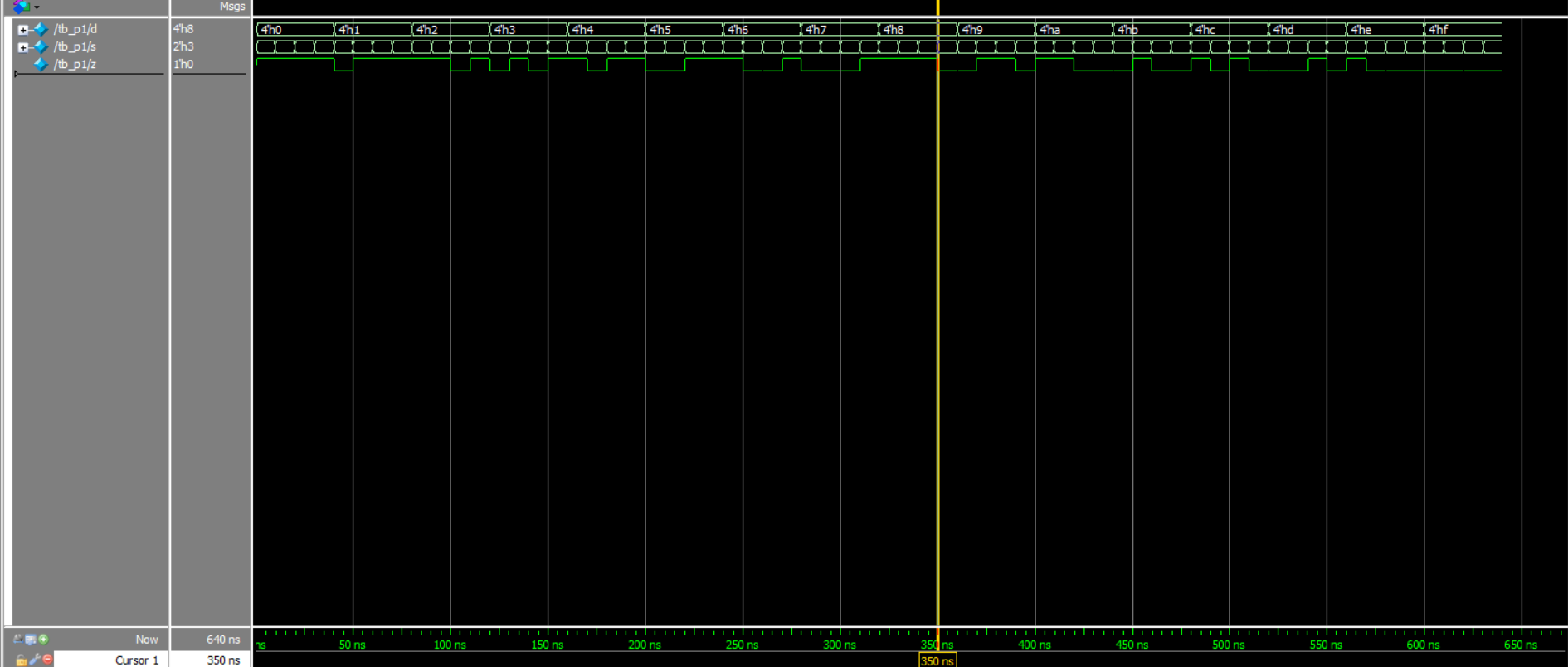
// Verilog Code



// Test Bench



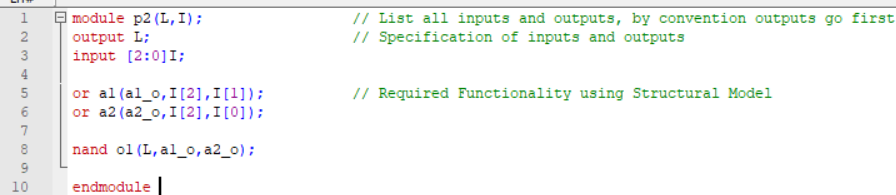
// wave\_p1



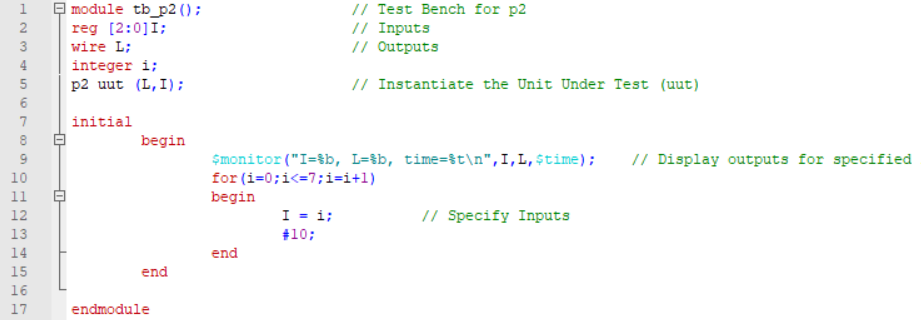
(Q2) A car has a fuel level detector that outputs the current fuel level as a 3-bit binary number, with 000 meaning empty and 111 meaning full. Create a simplified logic circuit (use Boolean algebra for simplification) that illuminates a “low fuel” indicator light (by setting an output L to 1) when the fuel level drops below level 3. Develop a Verilog model for the logic and test bench to verify the model.

Sol :-

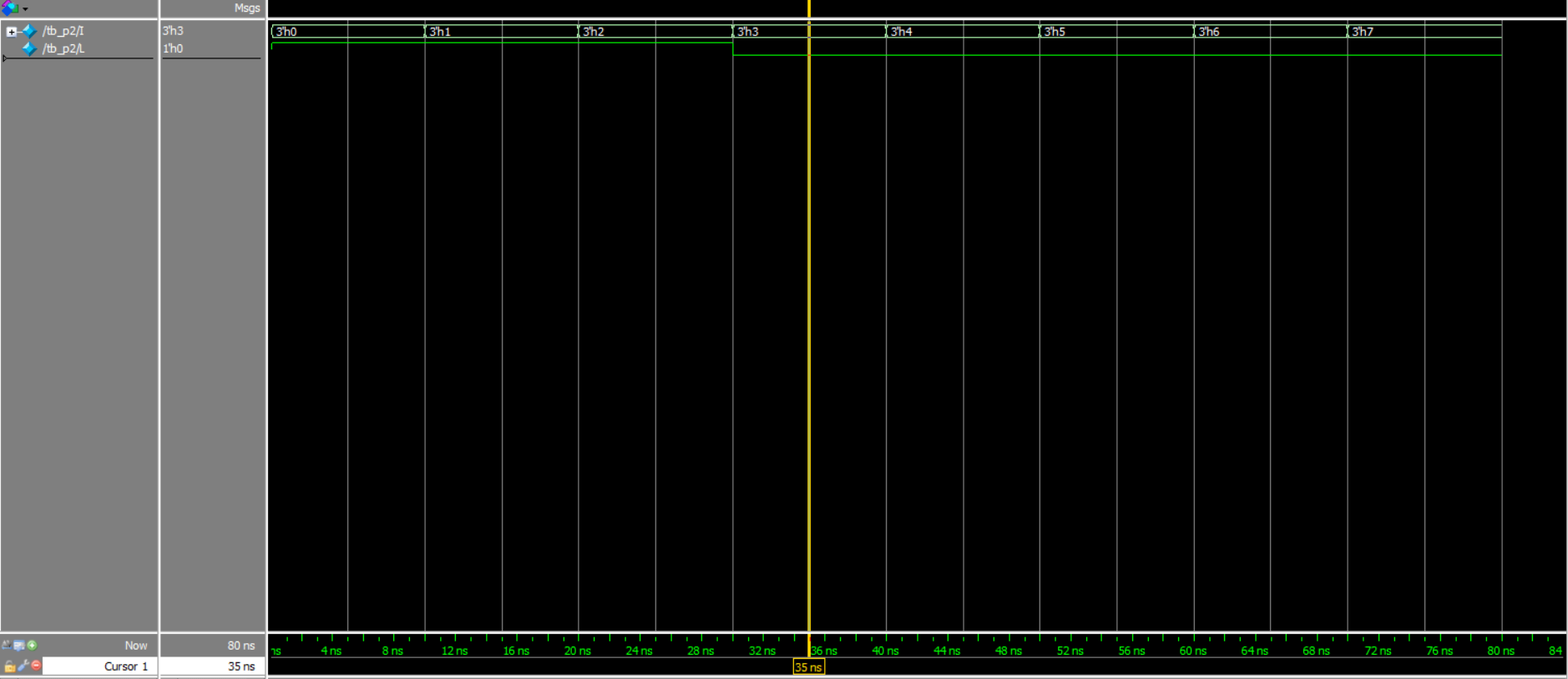
// Verilog Code



// Test Bench



// wave\_p2



(Q3) Use a simulation to demonstrate whether or not the following functions are equal. (Be sure to state which, if any, are equal.) and verify using truth table

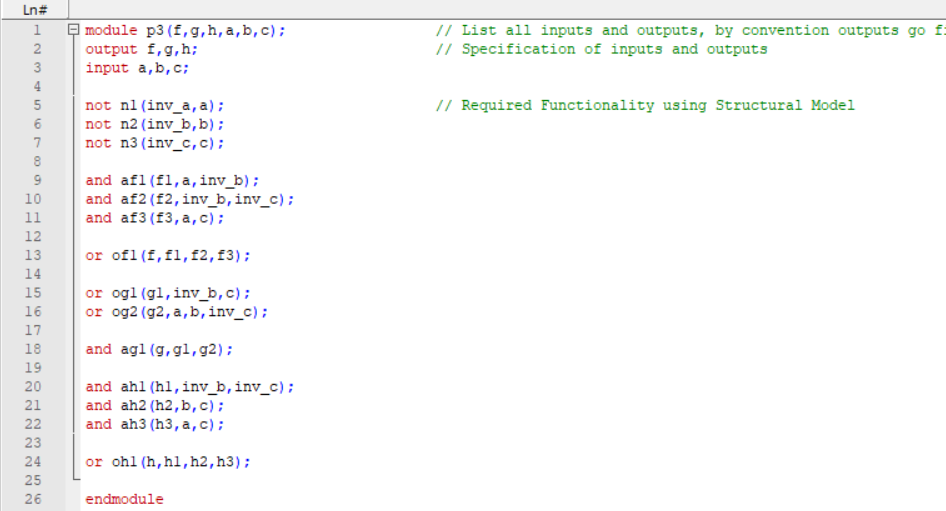
f = a b' + b' c' + a c

g = (b' + c) (a + b + c')

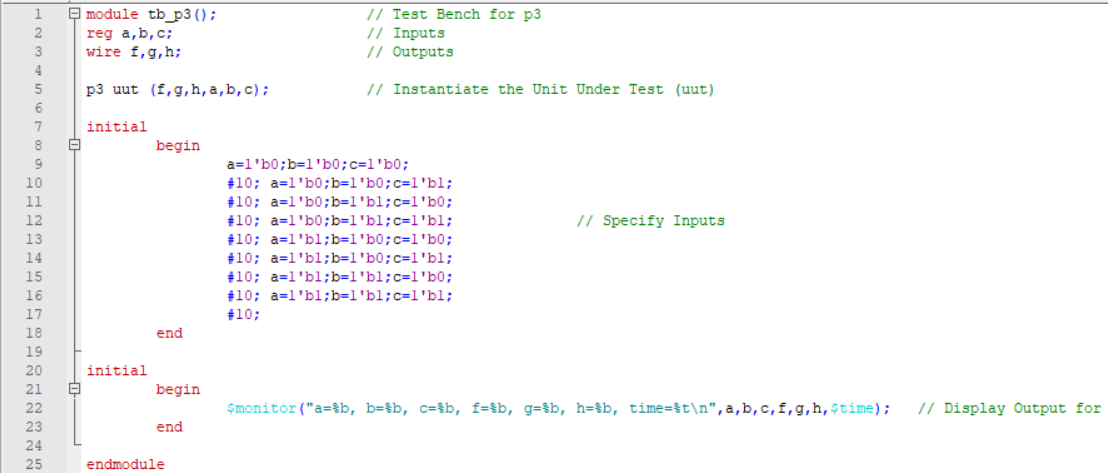
h = b' c' + b c + a c

Sol:-

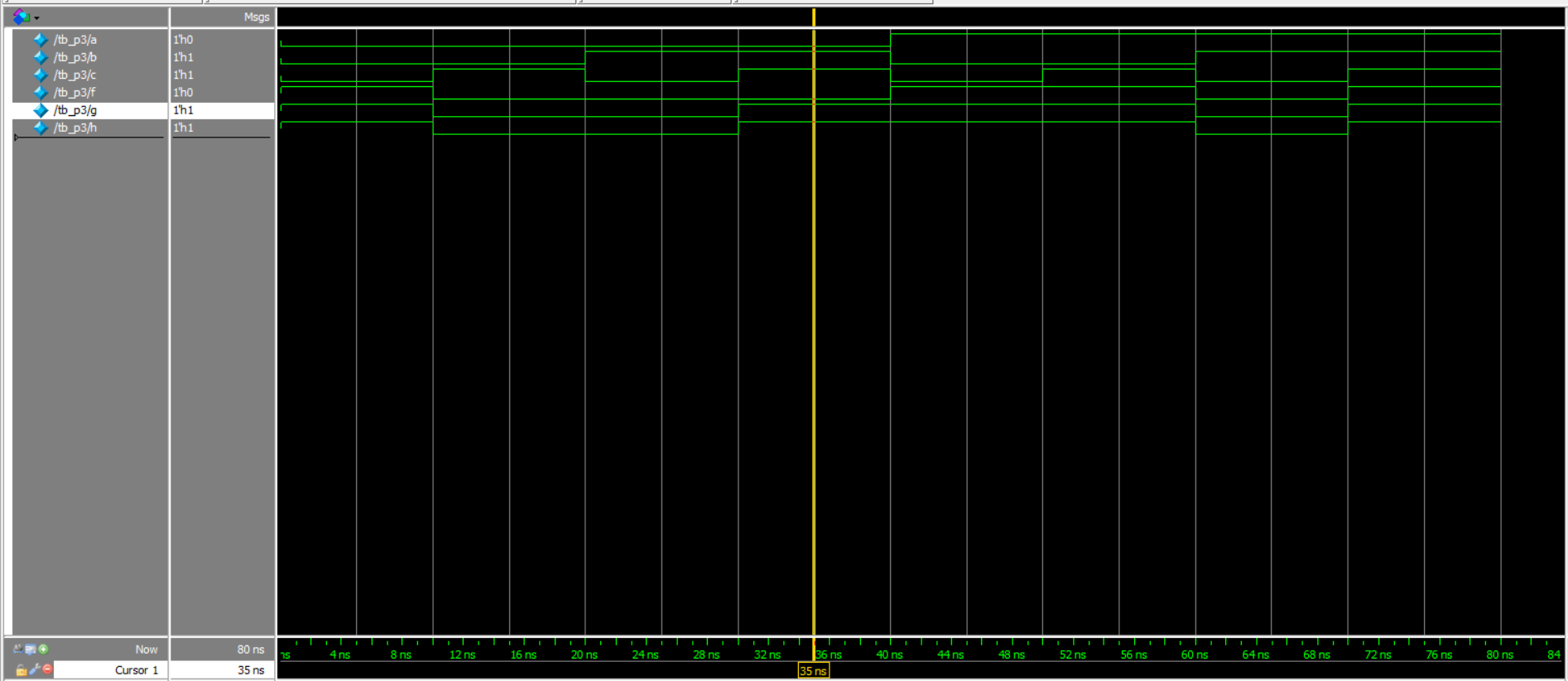
// Verilog code



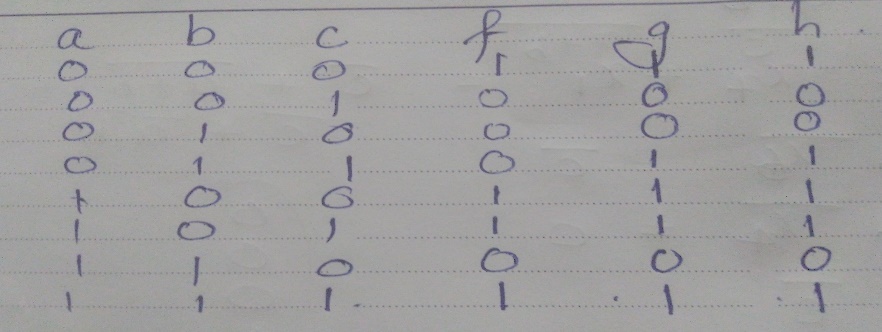
// Test Bench



// wave\_p3



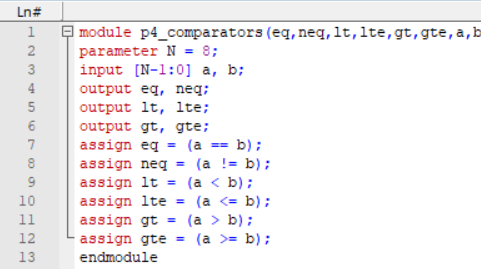
Functions g and h are equal. While f is different to both of them.



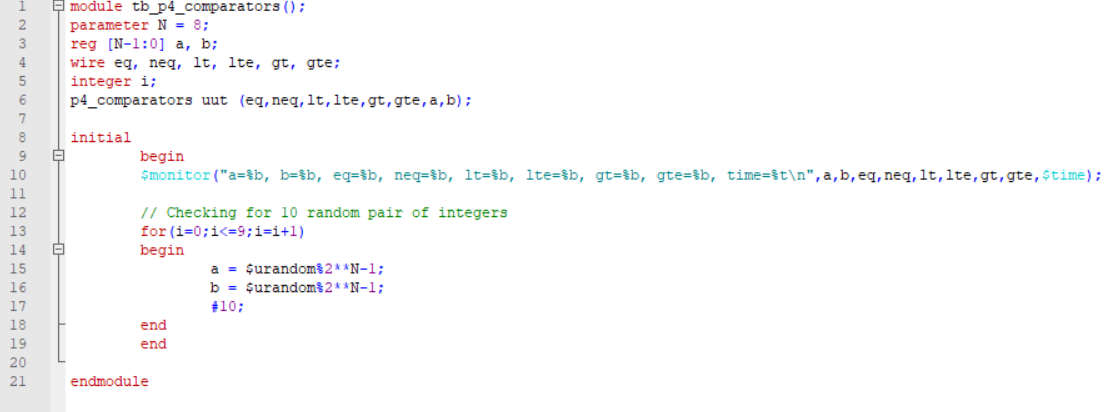
(Q4) Simulate the following function using appropriate test bench

Sol:-

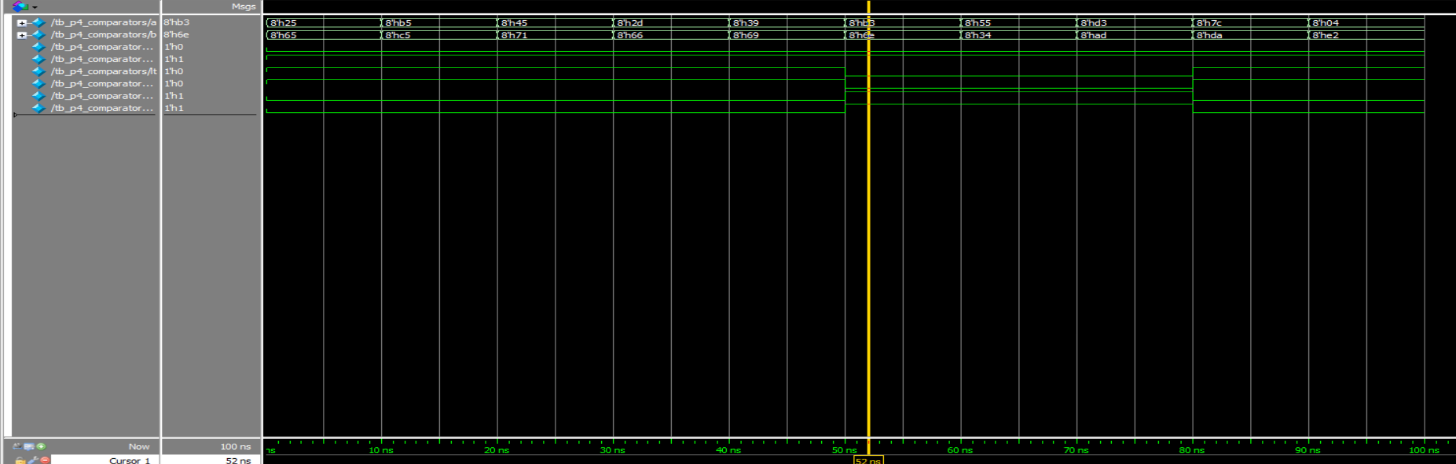
// Verilog code



// Test Bench



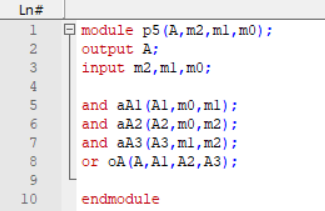
// wave\_p4



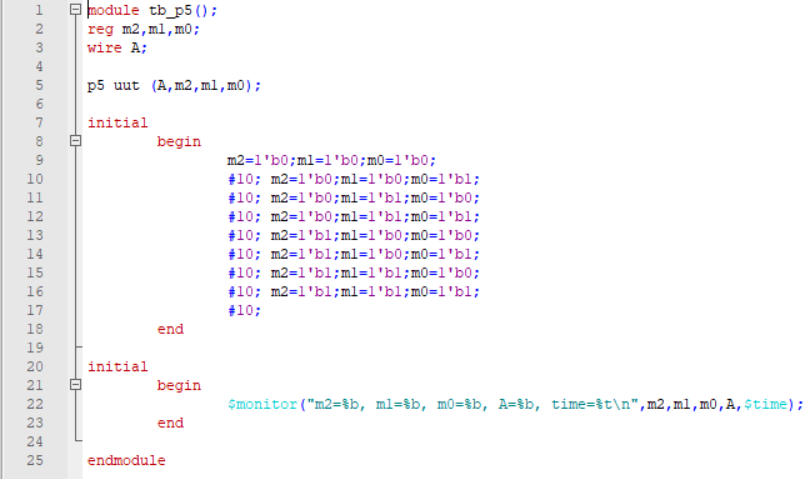
(5) A museum has three rooms, each with a motion sensor (m0, m1, m2) that outputs 1 when motion is detected. At night, the only person in the museum is one security guard who walks from room to room. Create a circuit that sounds an alarm (by setting an output A to 1) if motion is ever detected in more than one room at a time (i.e., in two or three rooms), meaning there must be an intruder or intruders in the museum. Develop a Verilog model for the above and write a test bench to verify the model.

Sol:-

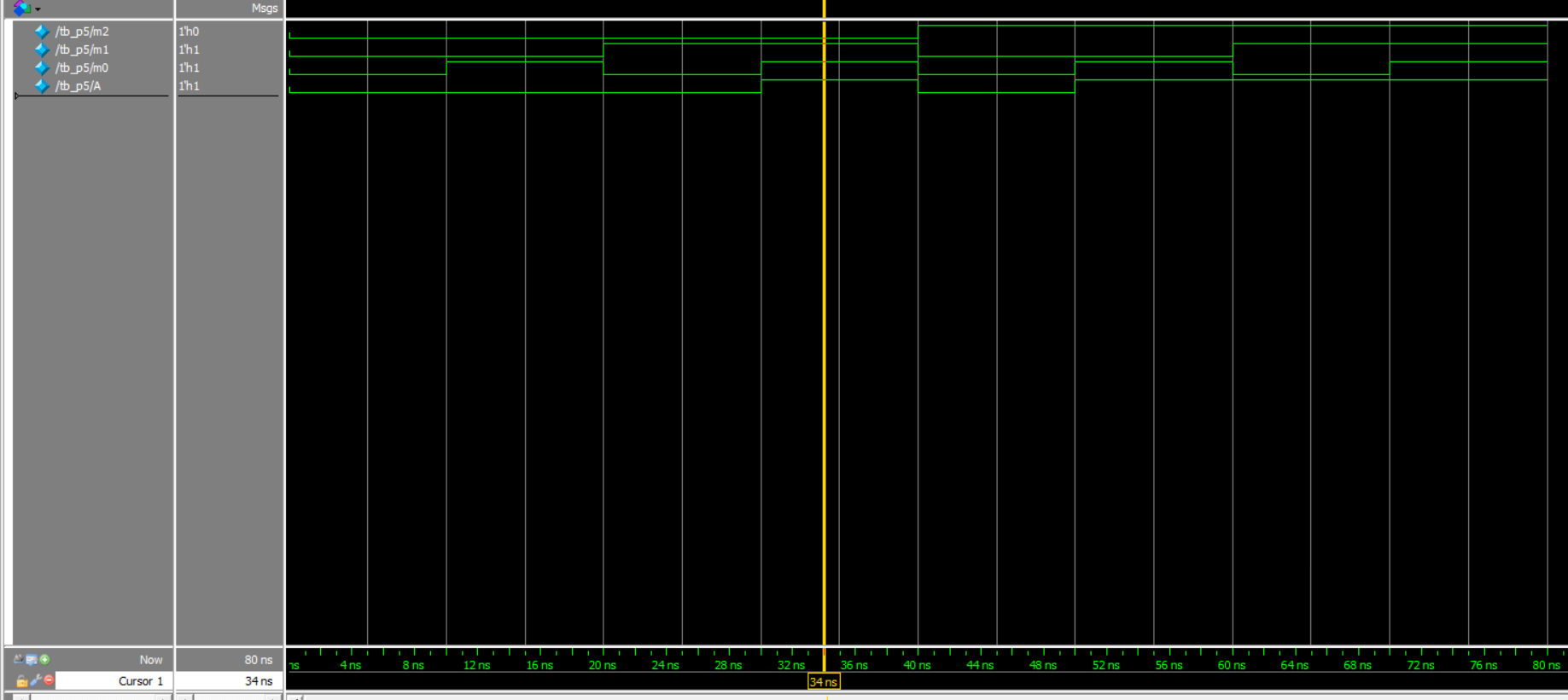
// Verilog Code



// Test Bench



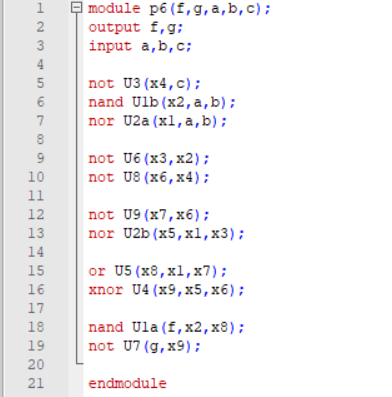
// wave\_p5



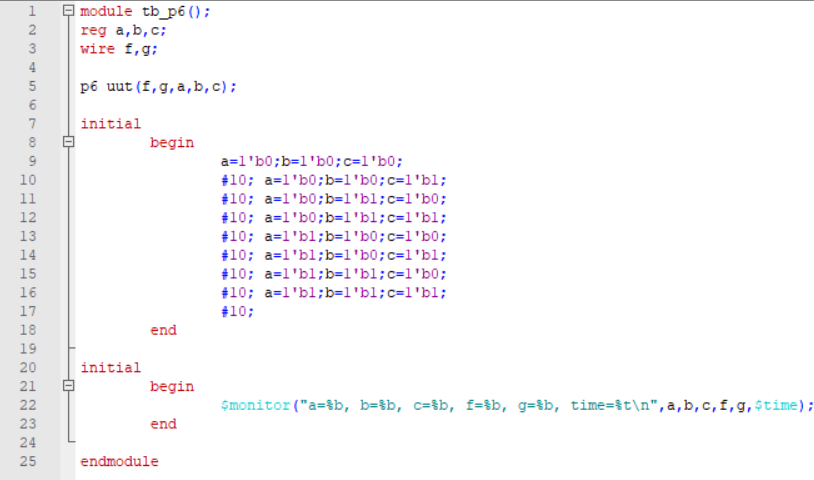
**(6**) Write a structural description of the following schematic. Check the functionality of the circuit by writing appropriate test bench.

Sol:-

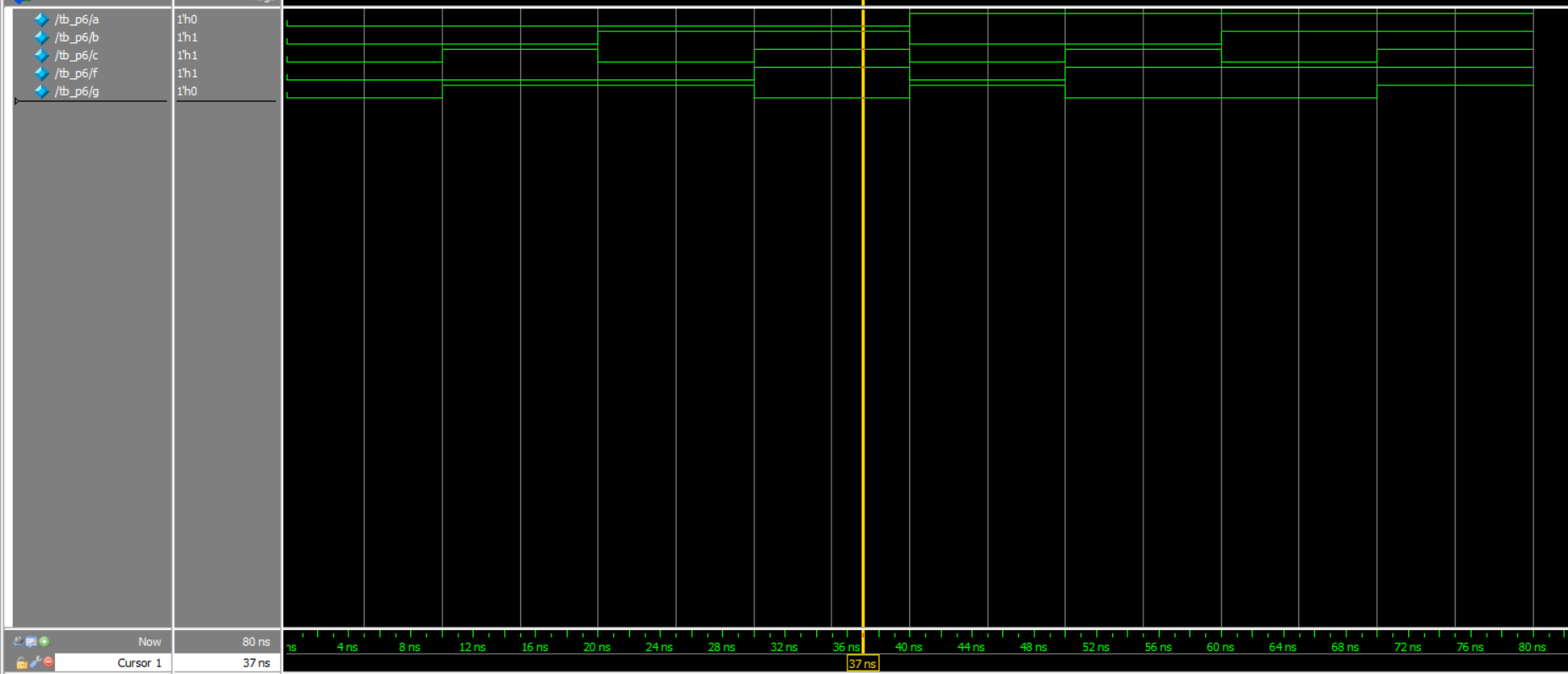
// Verilog Code



// Test Bench



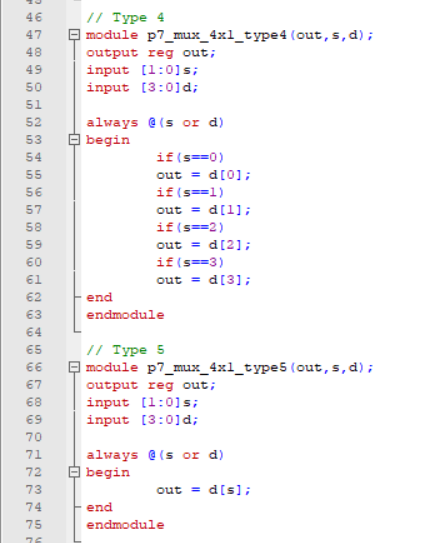
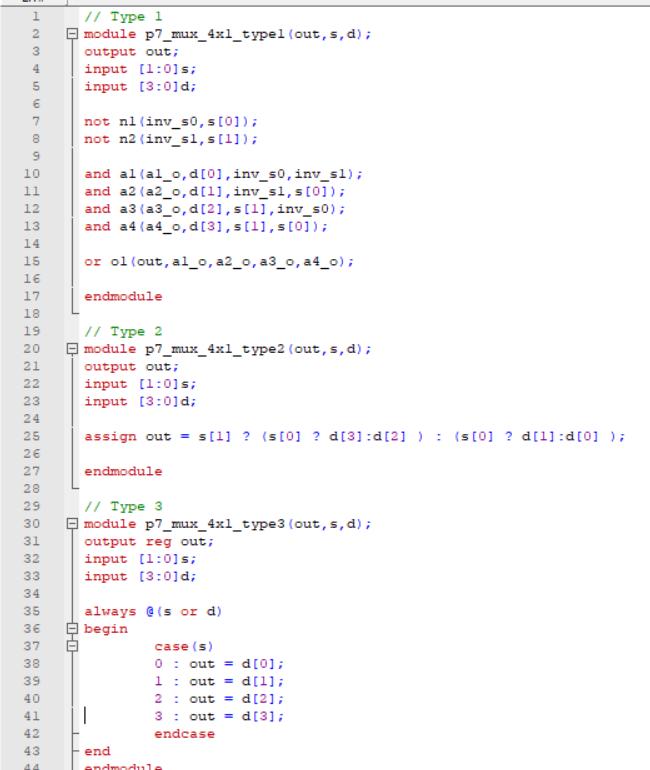
// wave\_p6

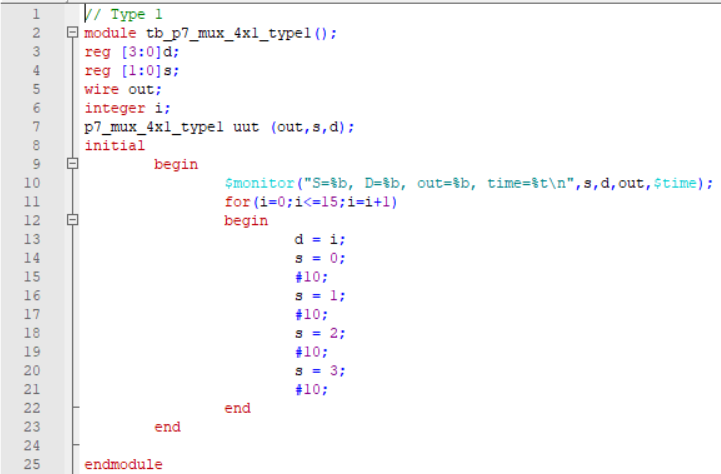


(Q7) Design 4 to 1 multiplexer with different coding styles ( at least 5) and test using appropriate test bench. Include all the designs in a single file (p7.v and tb\_p7.v) and submit.

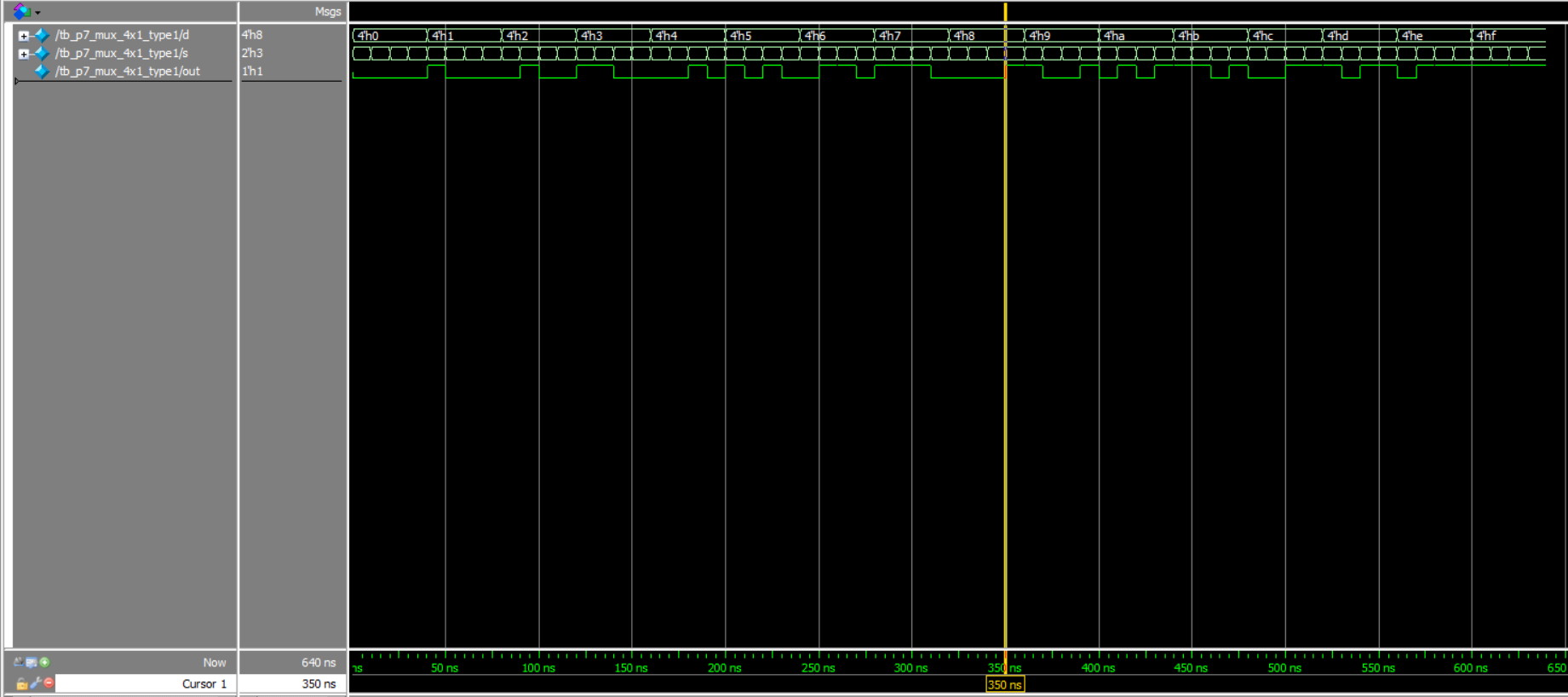
Sol:-

// Verilog Code



// For all other similar test bench is required just we have to change type in the implementation (Test Bench)

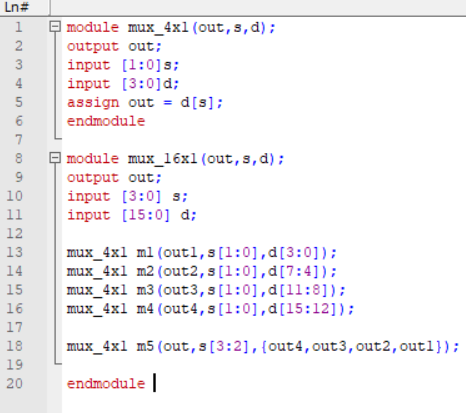
// wave\_p7



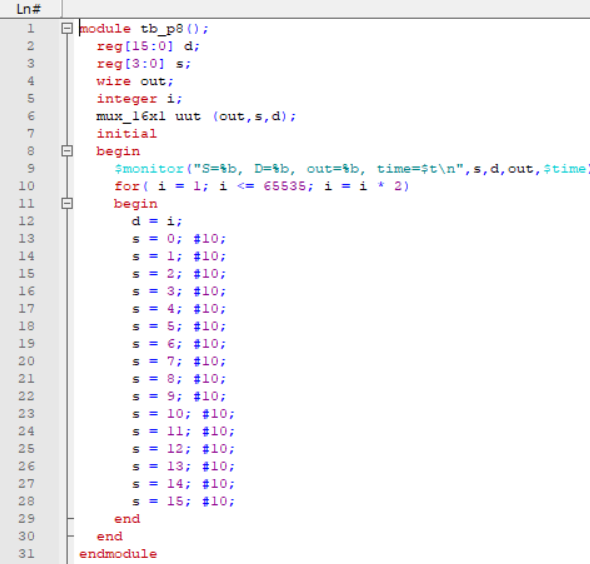
(Q8) Design 16 to 1 multiplexer using 4 to 1 MUXs and test using appropriate test bench. Include all the designs in a single file (p8.v and tb\_p8.v) and submit

Sol:-

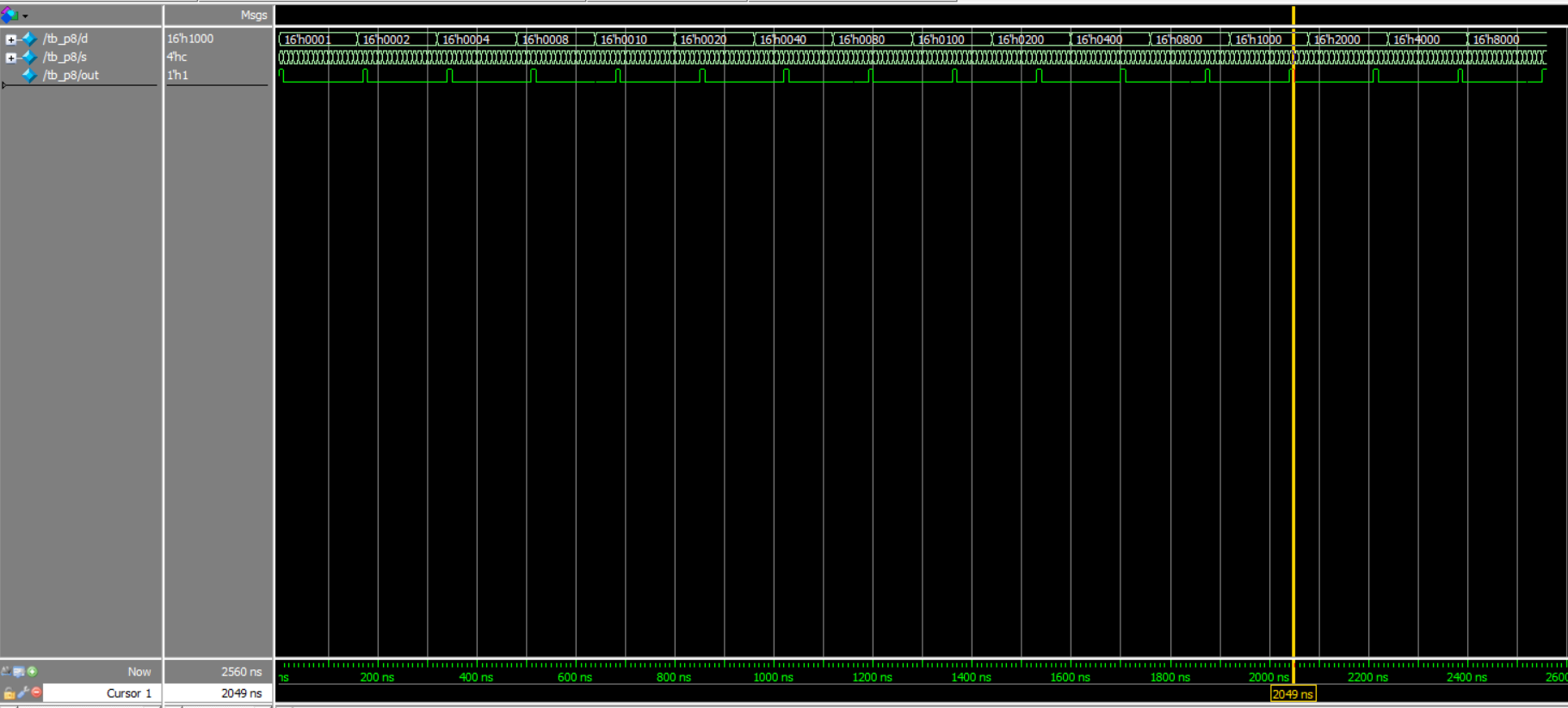
// Verilog Code



// Test Bench



// wave\_p8



// End of Document