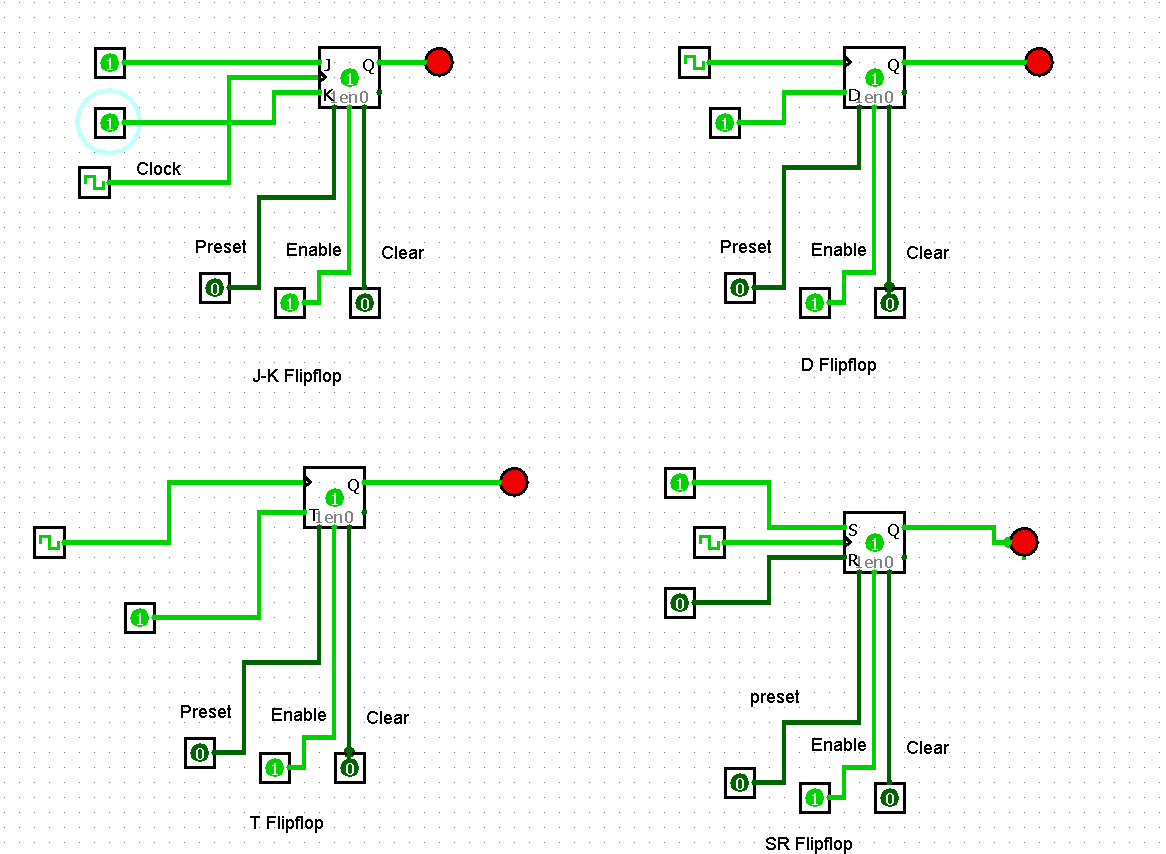
**Switching Theory Lab (CS226) - 8**

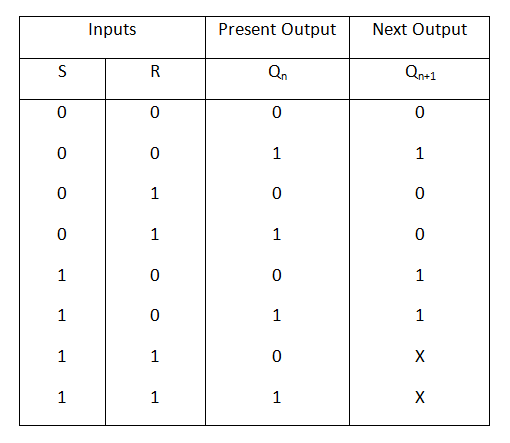
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Roll No. : 1801cs16

Date : 08/04/2020

**Q0)** **Study basic sequential elements SR, J-K, T and D flip flops**

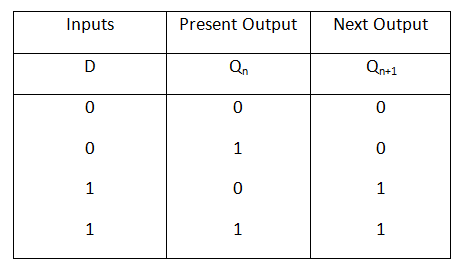


**SR flip-flop:**

The expression for next output will be:

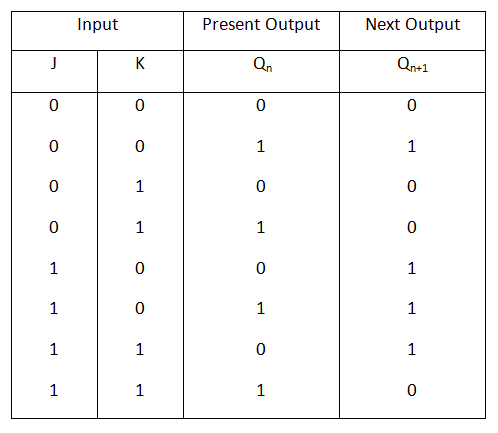
**Qn+1= (S + R’) Qn**

**D flip-flop:**

We can construct the equation for D flip-flop

from the characteristic’s equation of SR flip-flop.

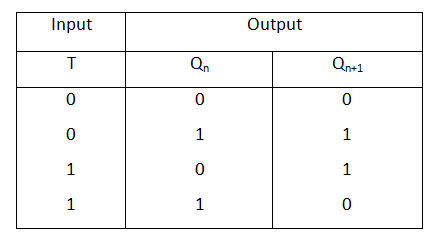
So, we can obtain: **Qn+1= D and Qn+1= D + Q’**

**JK flip flop:**

The characteristic equation for JK flip-flop

Is given by:

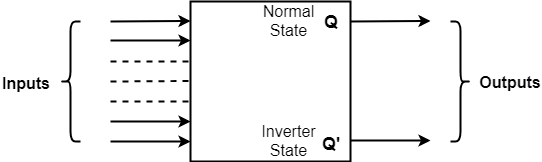
**Q(n+1) = K'Q(n) + JQ'(n)**

**T flip flop:**

The characteristic equation of T flip-flop

can be made as: **Qn+1= TQ’n + T’Qn**

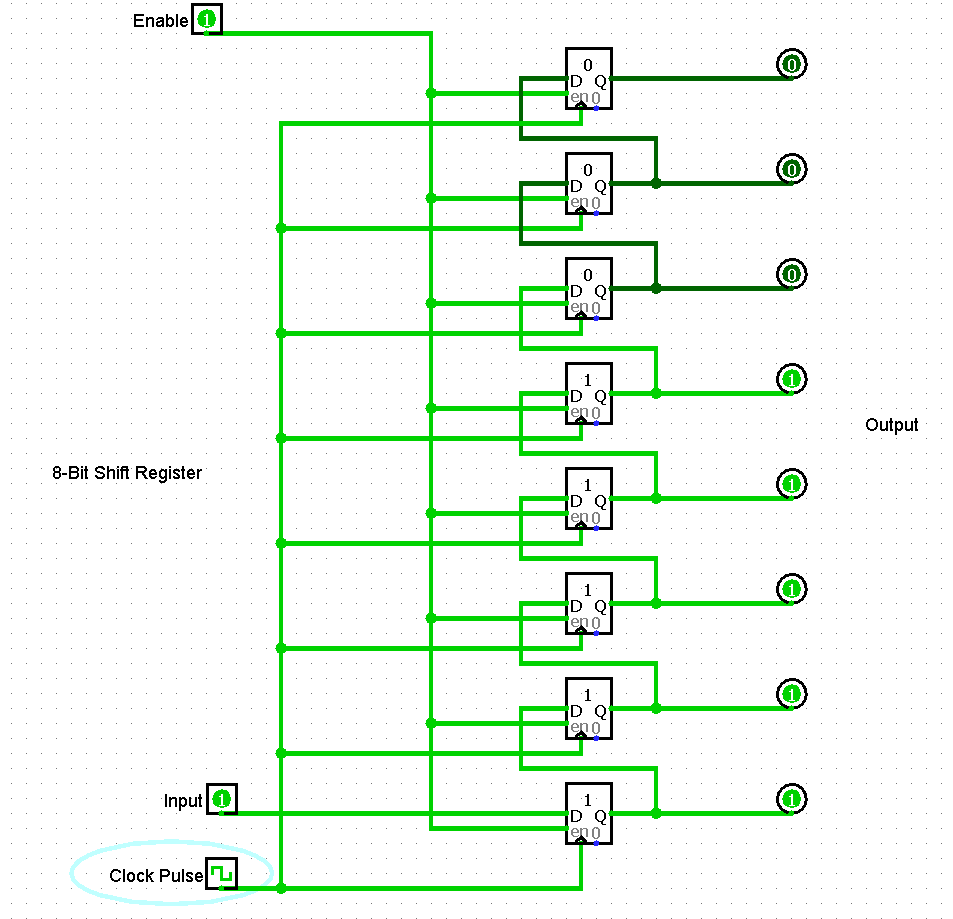
The basic 1-bit digital memory circuit is known as flip-flops. It can have only two states, either the state 1 or 0. A flip-flop is also known as bit stable multi-vibrator. Flip-flops can be constructed by using NAND and NOR gates. The general block diagram represents a flip-flop that has one or more inputs and two outputs.



The two outputs are complementary to each other.

* If Q is 1 that is set Q’ to 0.
* If Q is 0, reset Q’ to 1. (Q and Q’ can’t be at the same state simultaneously. If it happens, it will violate the definition of the flip-flop and hence is called undefined condition).
* Q is called the state of the flip-flop whereas Q’ is called complementary state of the flip-flop.
* When the output Q is either 0 or 1, it remains in that state unless one or more inputs are excited to effect the change on the output.

**Q1)** **Simulate 8-bit shift register using logic-sim.**

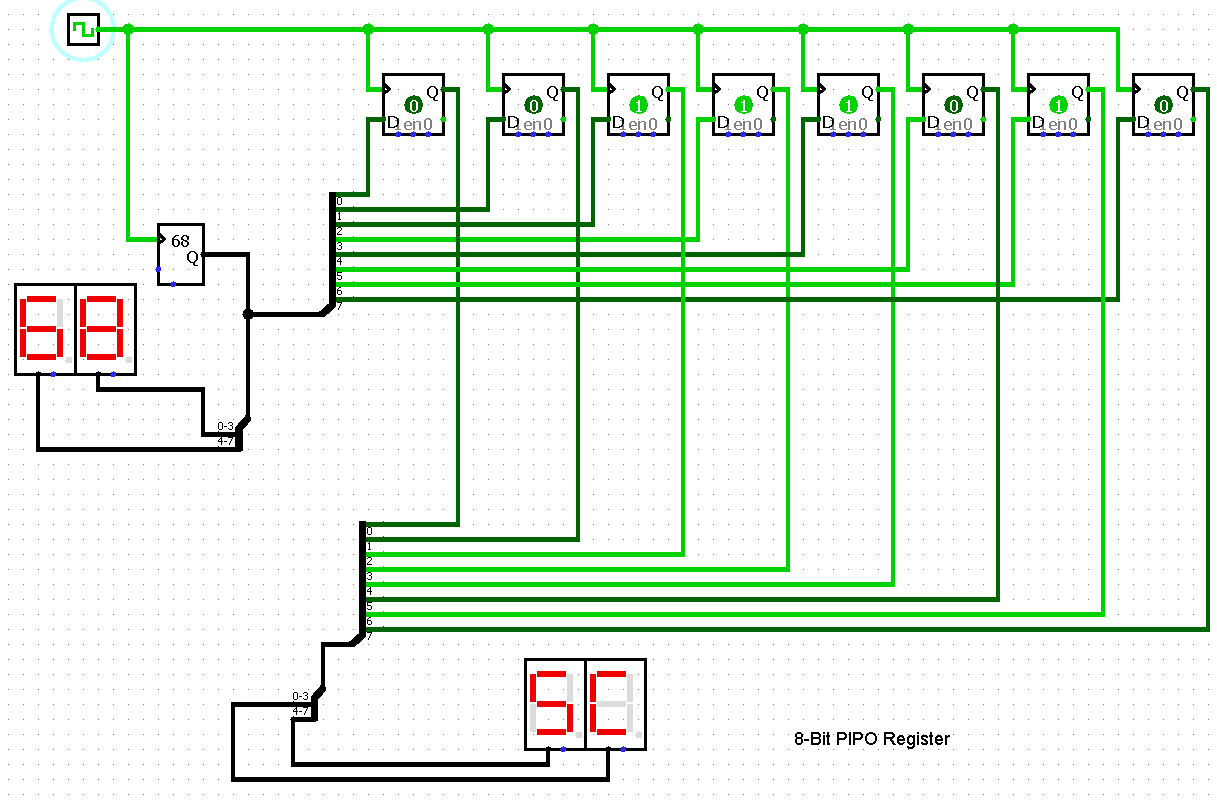
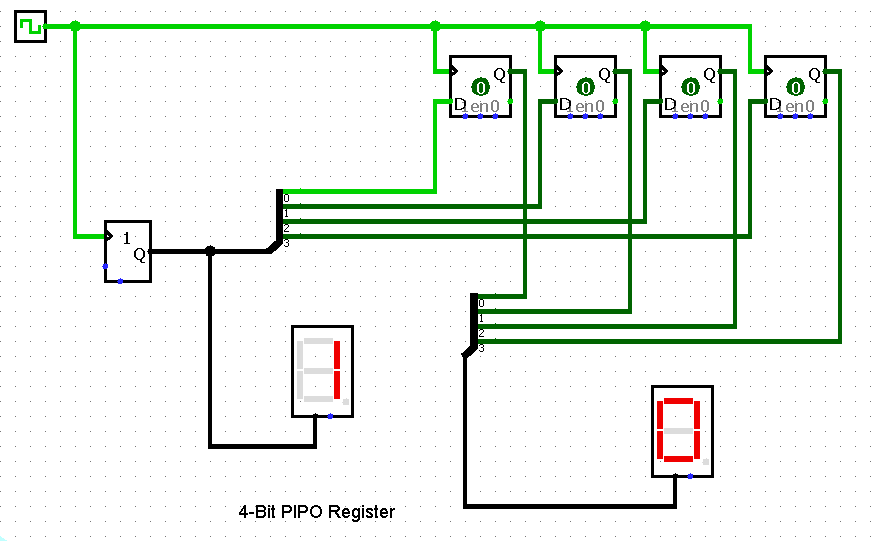


The shift register, which allows serial input and produces serial output is known as Serial In – Serial Out (SISO) shift register. The above diagram is of 8-bit SISO shift register.

This block diagram consists of 8 D registers, which are cascaded. That means, output of one D register is connected as the input of next. All these are synchronous with each other since, the same clock signal is applied to each one.

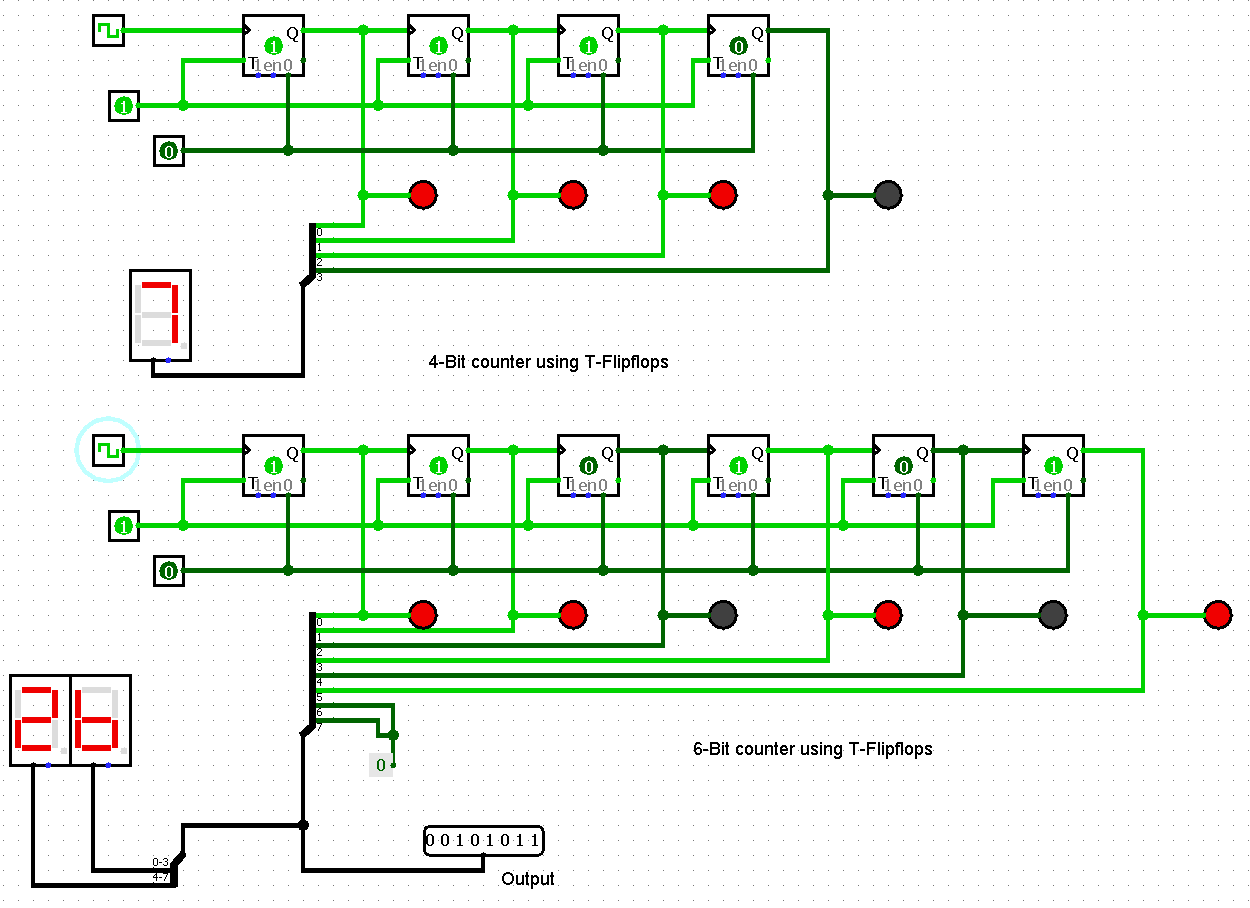
In this shift register, we can send the bits serially from the input of bottom-most D resgister. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of top-most D register. Hence, this output is also called as serial output.

**Q2) Simulate a 4-bit parallel in Parallel out (PIPO) register. Design a 8-bit parallel in Parallel out (PIPO) register.**



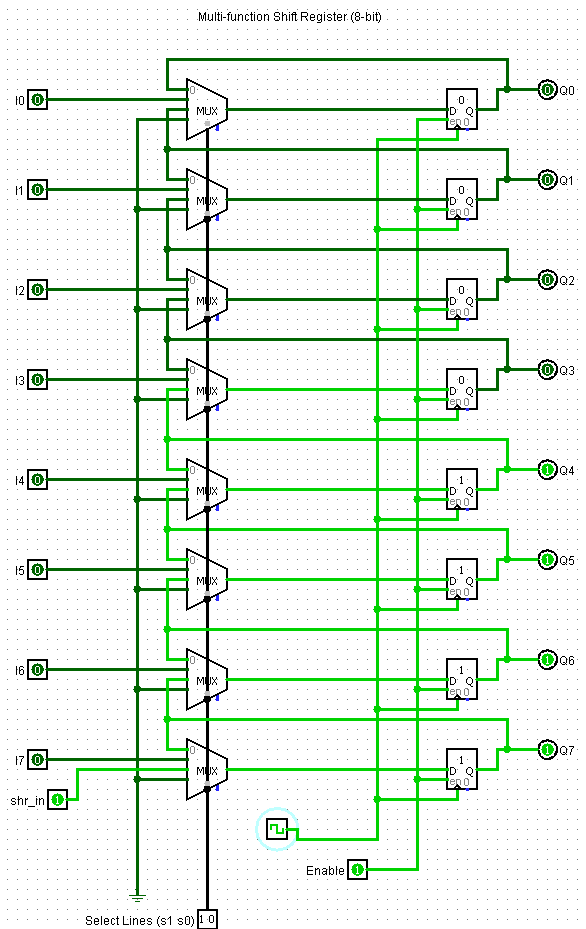
The shift register, which allows parallel input and produces parallel output is known as Parallel In − Parallel Out (PIPO) shift register. The above diagram shows 4-bit and 8-bit PIPO shift registers. For a N-bit PIPO shift register, circuit consists of n D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.In this shift register, we can apply the parallel inputs to each D flip-flop by making Preset Enable to 1. We can apply the parallel inputs through preset or clear. These two are asynchronous inputs. That means, the flip-flops produce the corresponding outputs, based on the values of asynchronous inputs. In this case, the effect of outputs is independent of clock transition. So, we will get the parallel outputs from each D flip-flop.

**Q3) Simulate a 4-bit counter using T flip flops. Design a 6-bit counter using T flip flops**



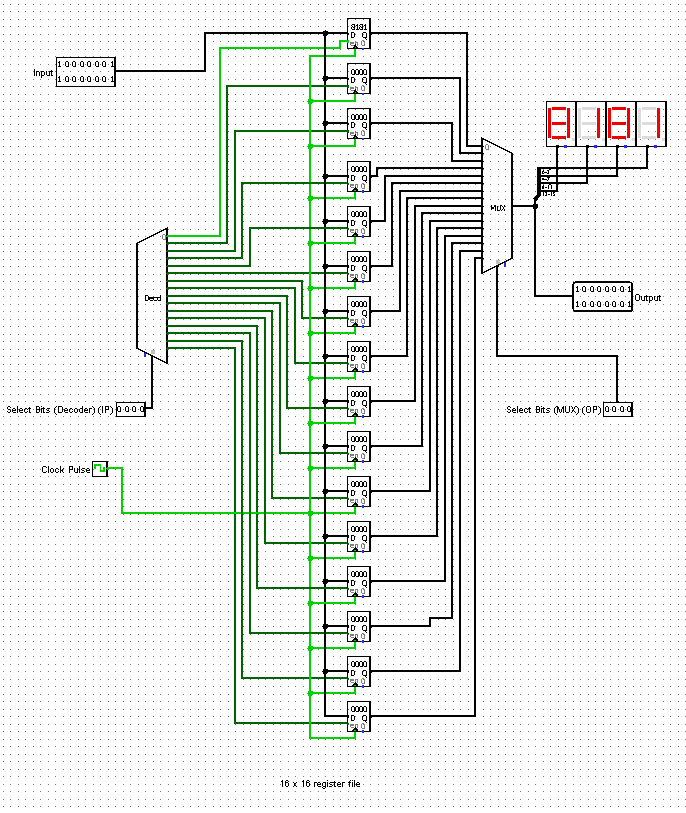
The output of first T flip-flop is applied as clock signal for next T flip-flop and so on. So, the output of a specific T flip-flop toggles for every negative edge of output of previous T flip-flop. When input bit is set to 1, for every clock cycle, the output bits are reduced by 1, initially set as 111111 to 011111 and so on. Till it reaches 000000, the (6-Bit counter) circuit counts 64 clock cycles.

**Q4) Simulate the multi-function Shift register using logic-sim. Design an 8-bit version.**



When “shr\_in” is set to 1, all flipflops are enabled and the selector inputs for the MUX is set to “10”, for every clock cycle the output bits are set to 1 consecutively from bottom to the top. If “shr\_in” is set to 0, the output bits are set to 0 and if the selector inputs are set to “01” and clock signal is applied, for every input signal (i0, i1, i2…) which is set to 1, the corresponding output bit is also set to 1.

**Q5) Design a 16x16 register file (include register file enable)**



If the select bits for the decoder are same as those of the MUX, when a clock frequency is applied, the output bits store the input bits which is retained until a new clock pulse is generated which changes the output to the current input provided the selector bits are same for the MUX and the decoder. If not, the previous output is retained. The output is displayed as a Hexadecimal number.