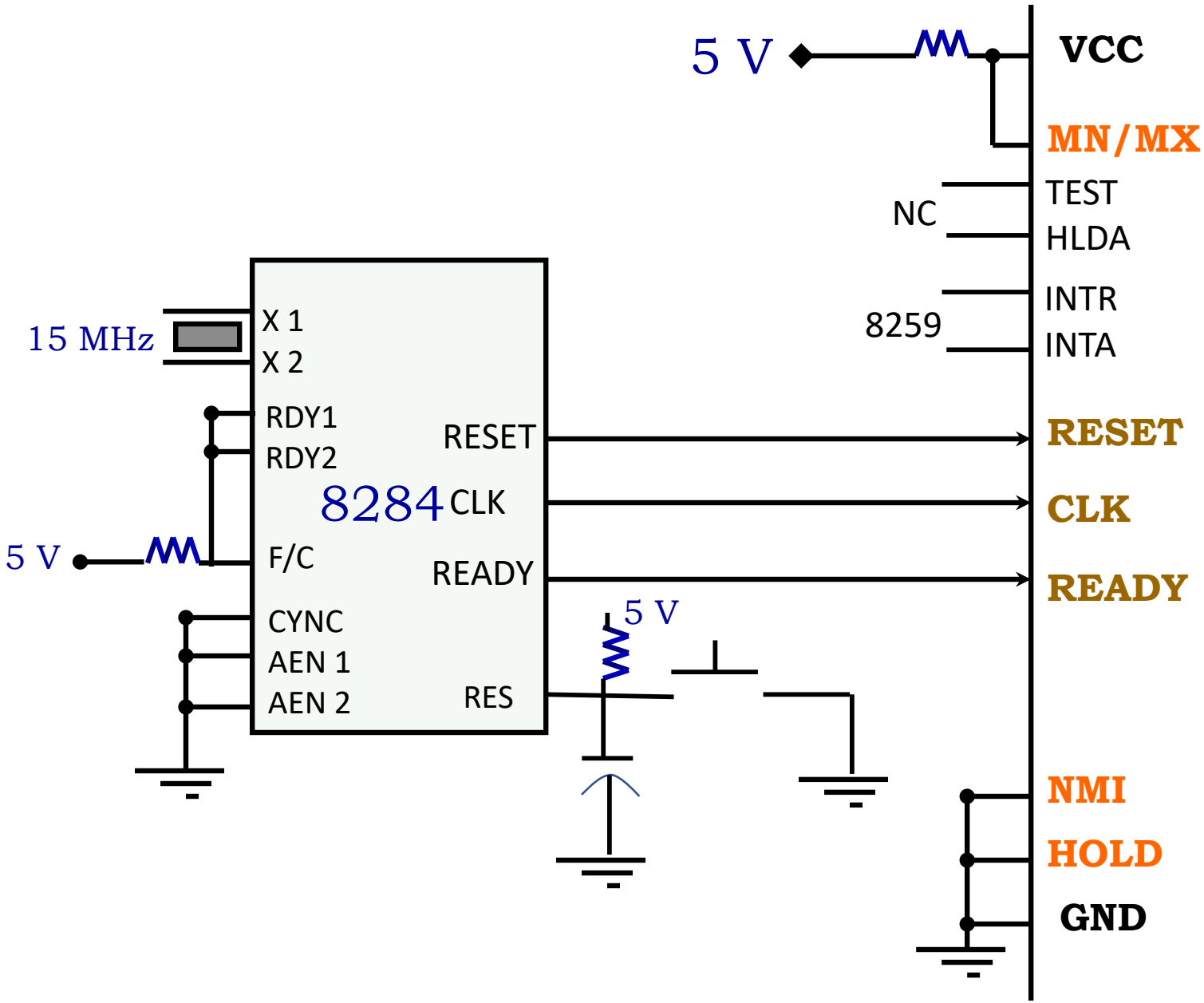
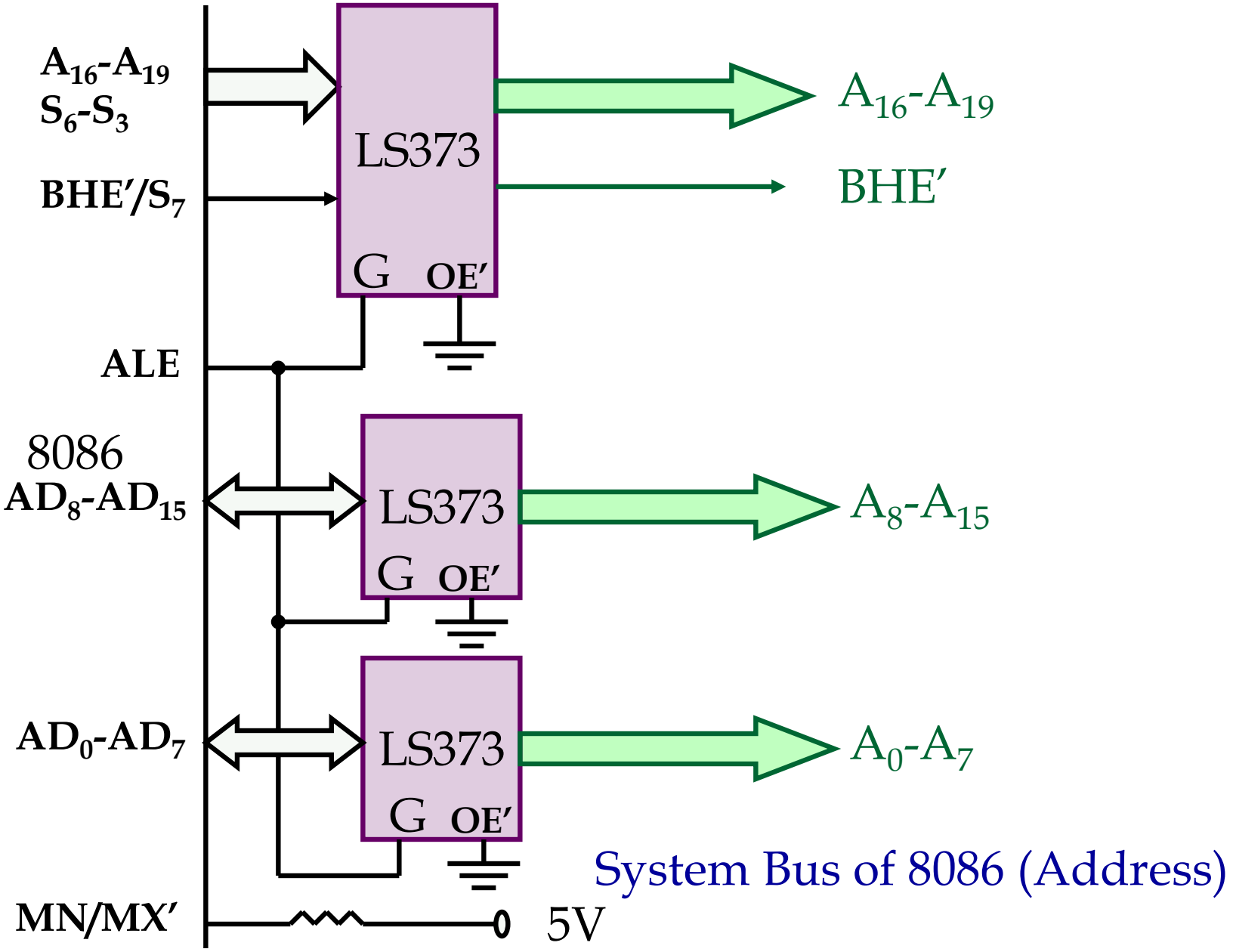
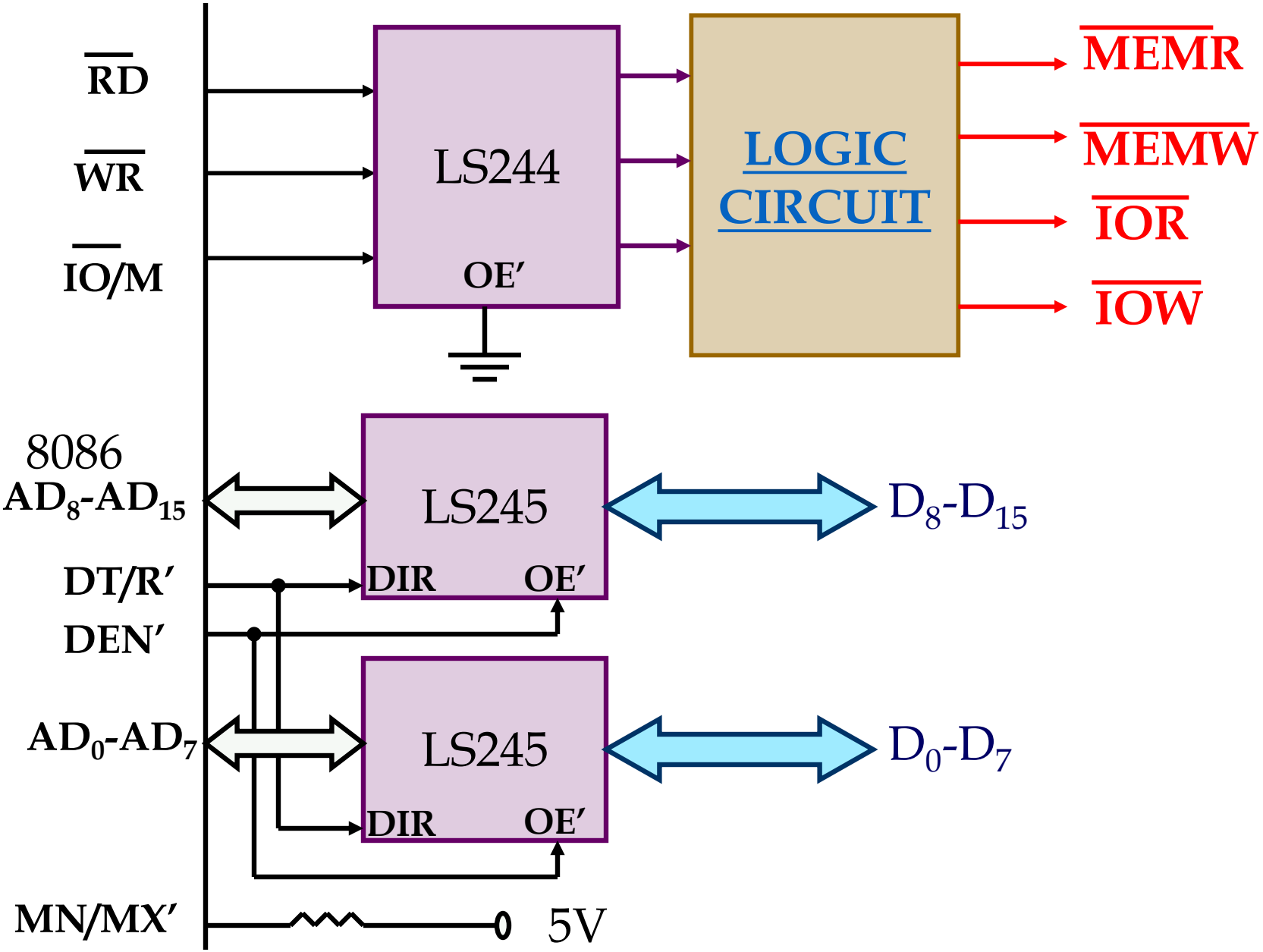

5 V
VCC
MN/MX
TEST
NC
HLDA
INTR
8259
INTA
15 MHz
X 1
X 2
RDY1
RDY2
RESET
8284
CLK
5 V
F/C
READY
5 V
CYNC
AEN 1
AEN 2
RES
RESET
CLK
READY
NMI
HOLD
GND

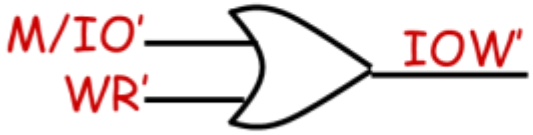
8086 Inputs



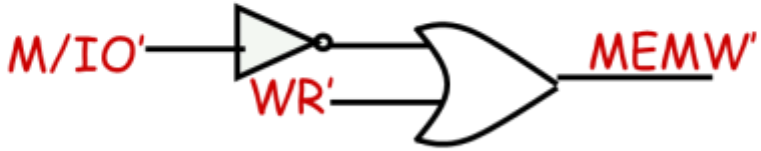
System Bus of 8086 (Address)



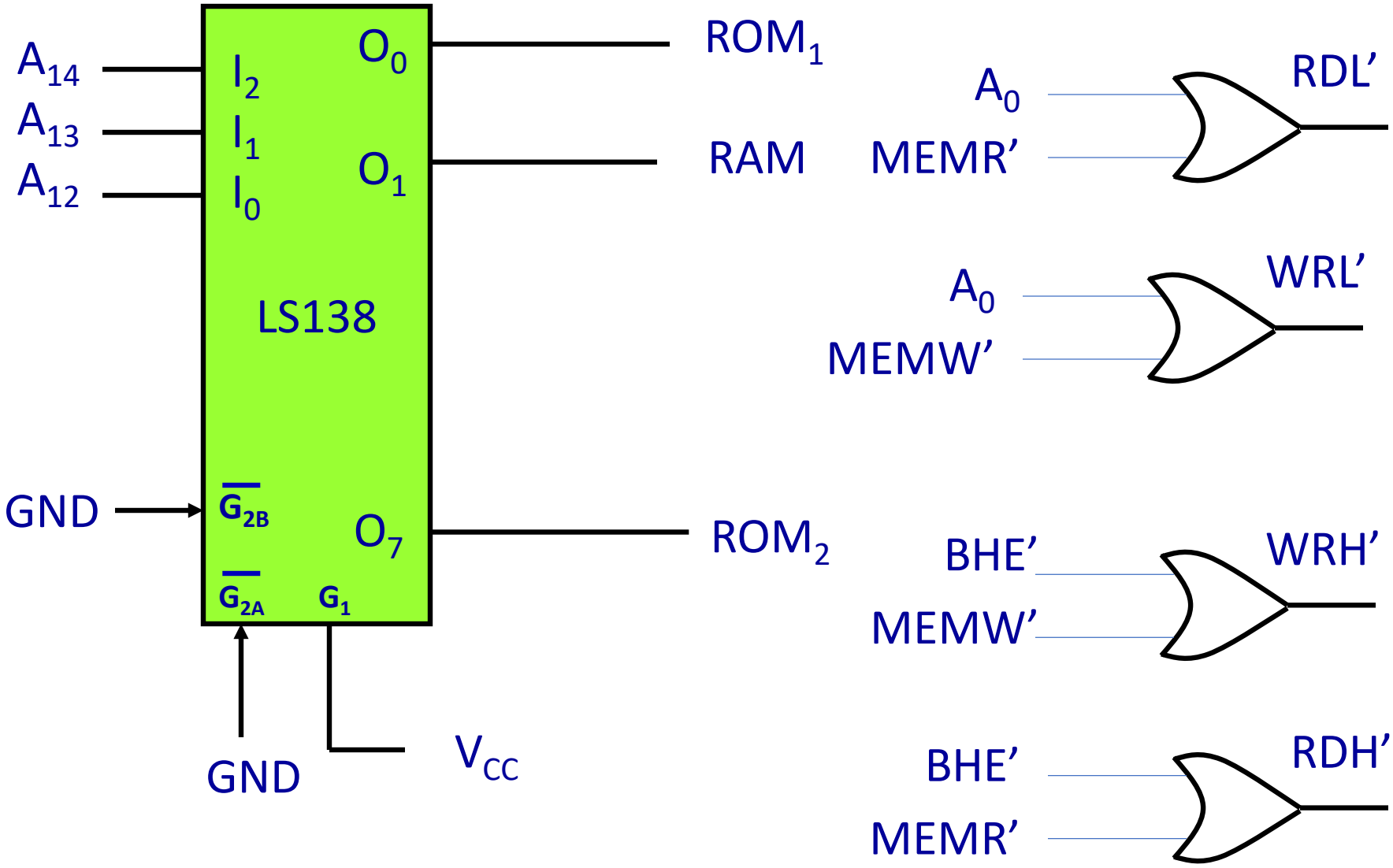
System Bus of 8086(Data + Control)



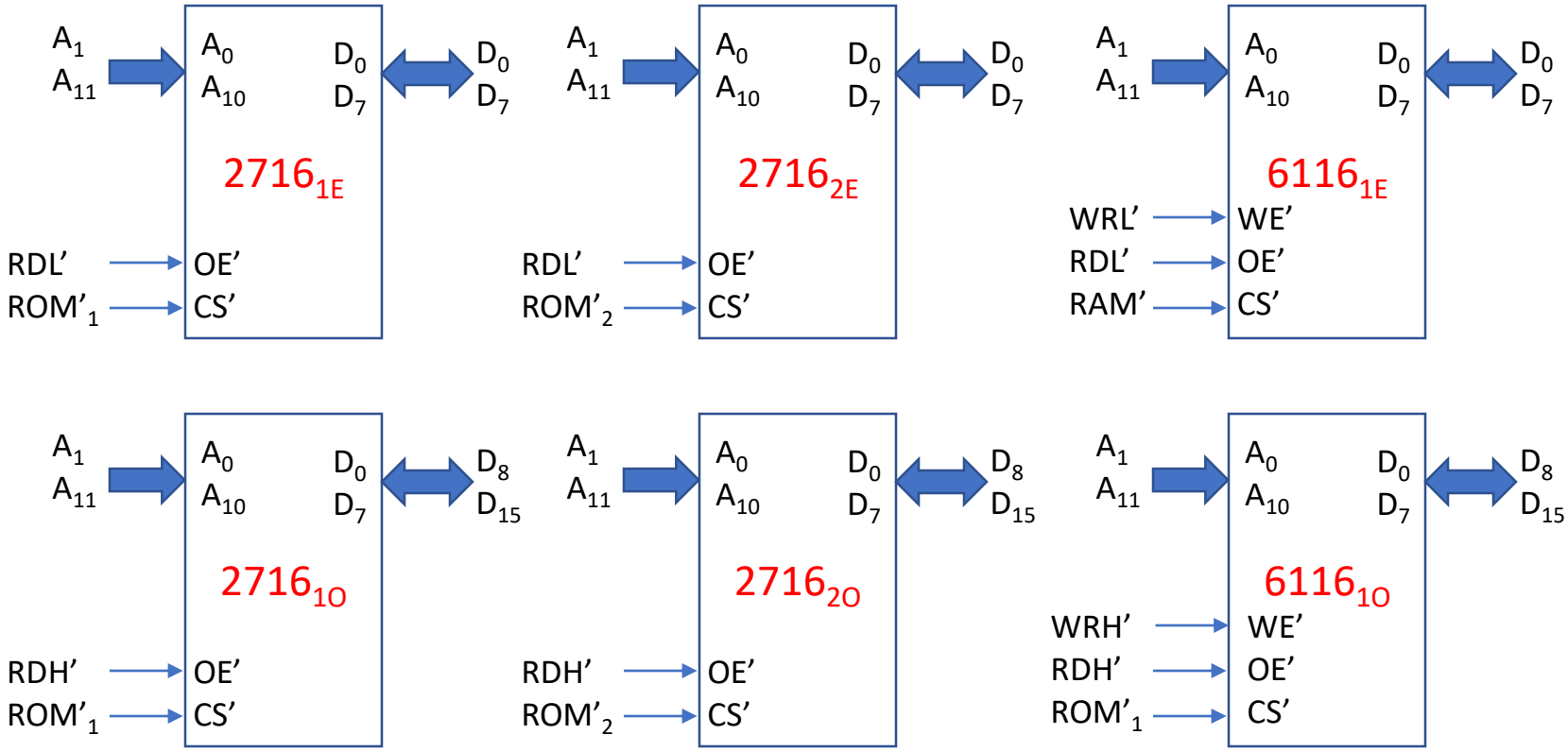
M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'



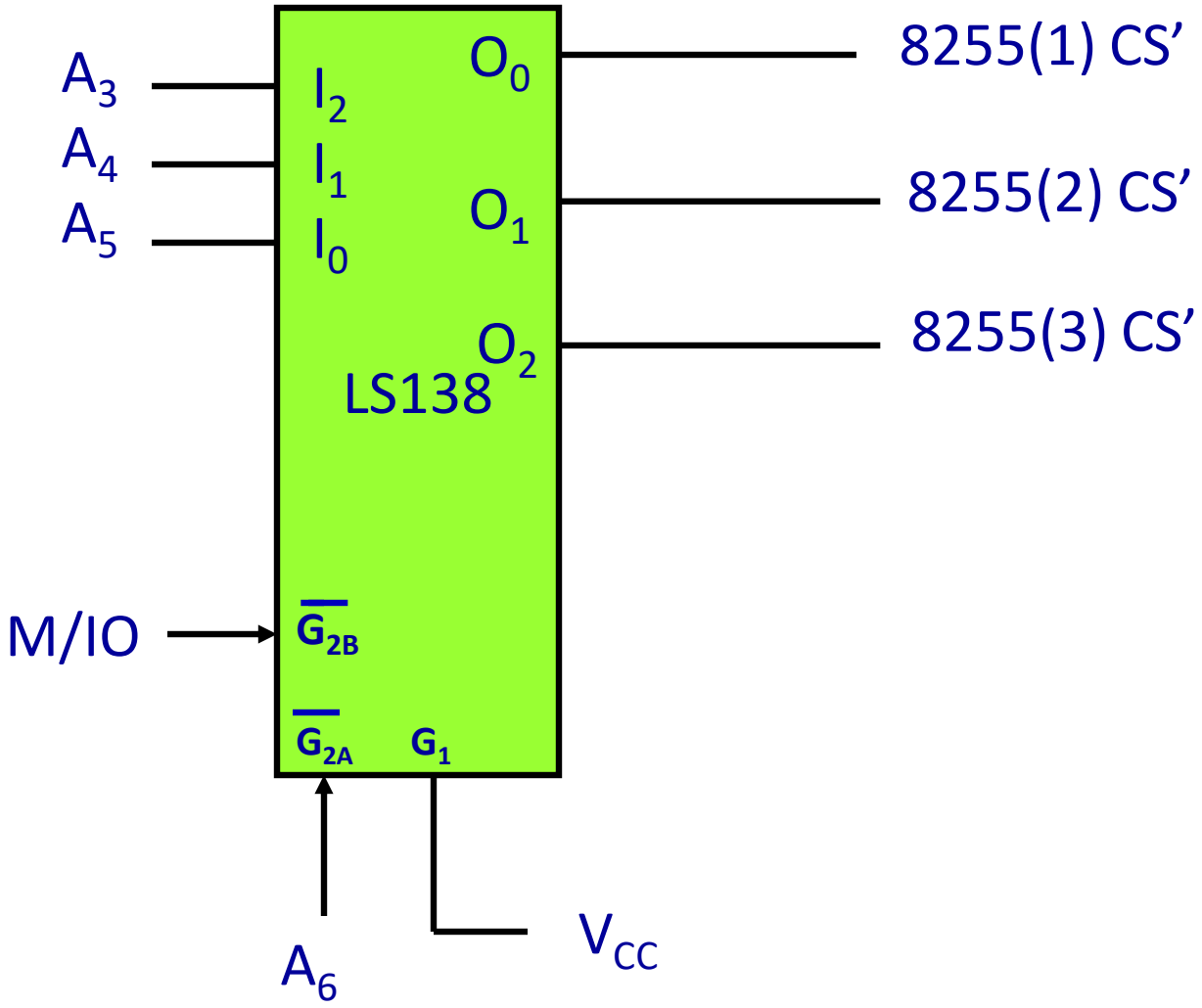
back



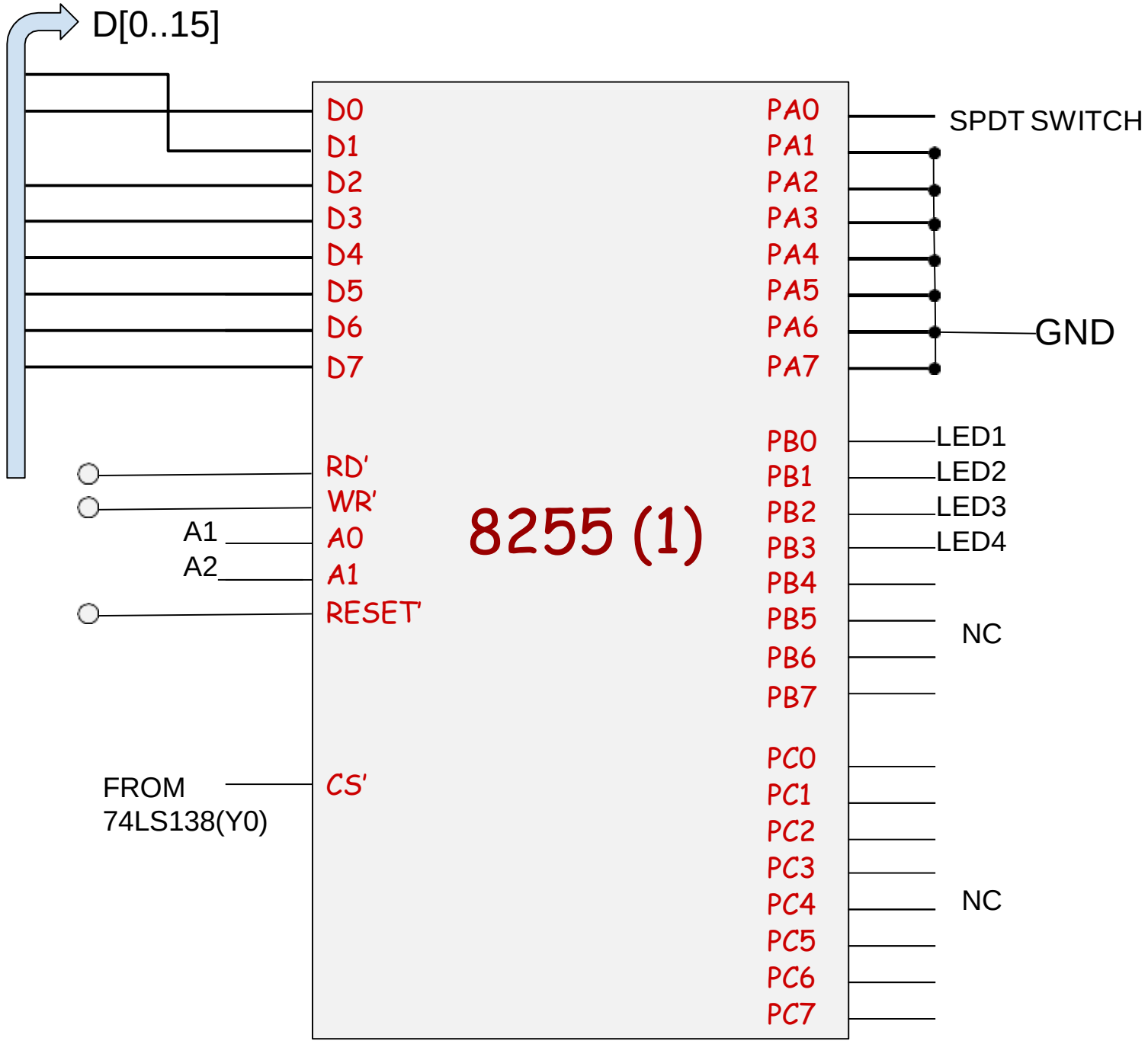
Memory Decoder

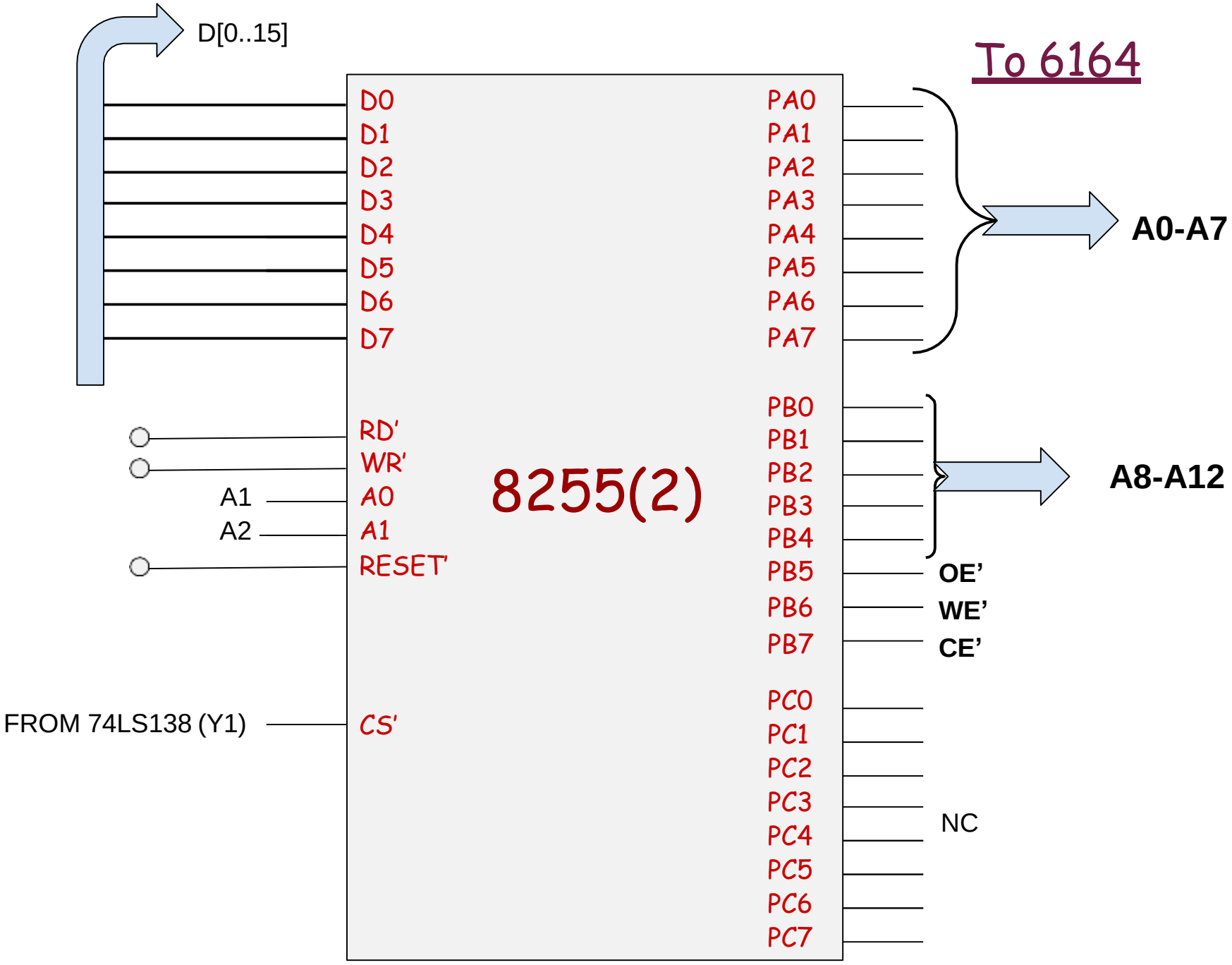


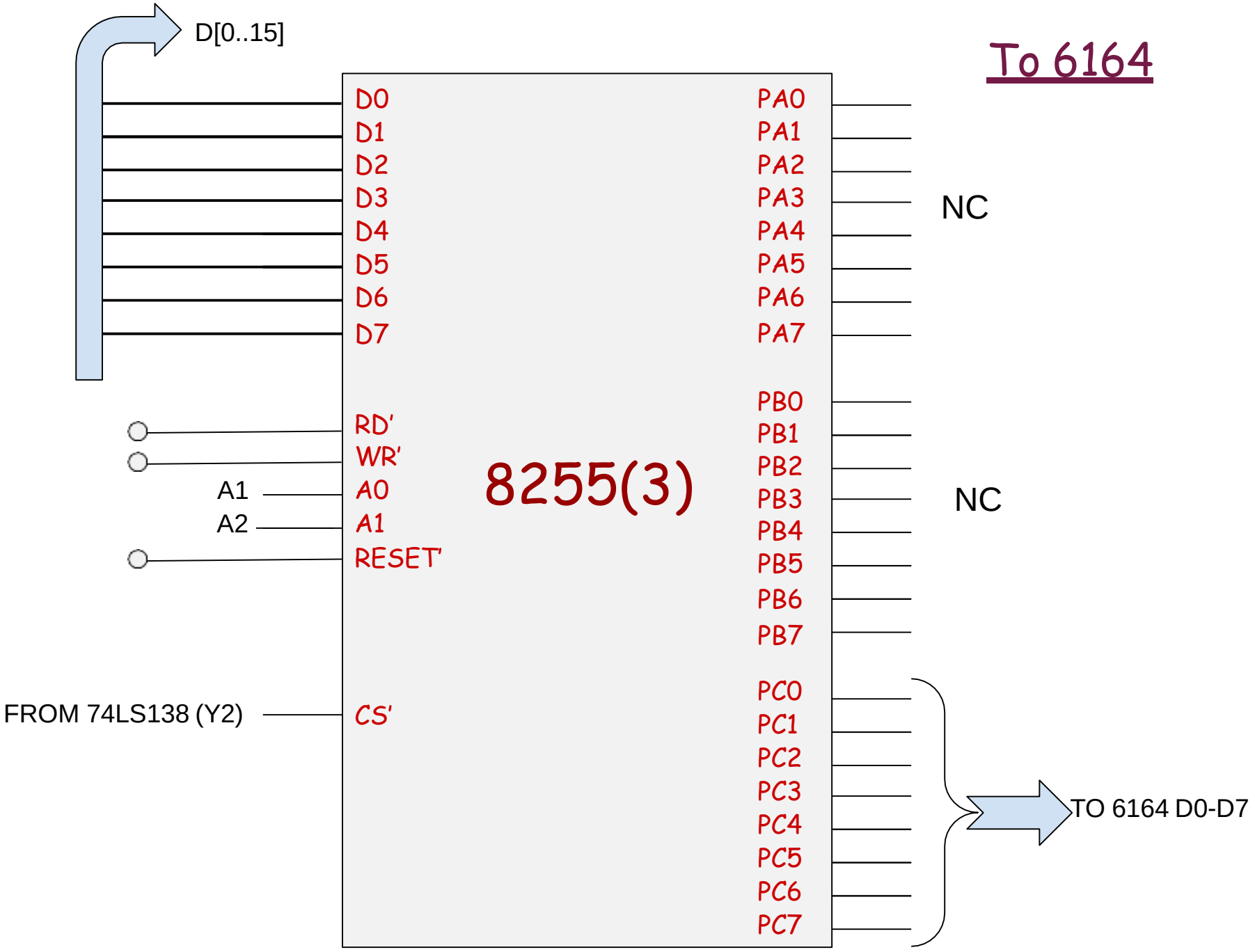
Memory Interfacing

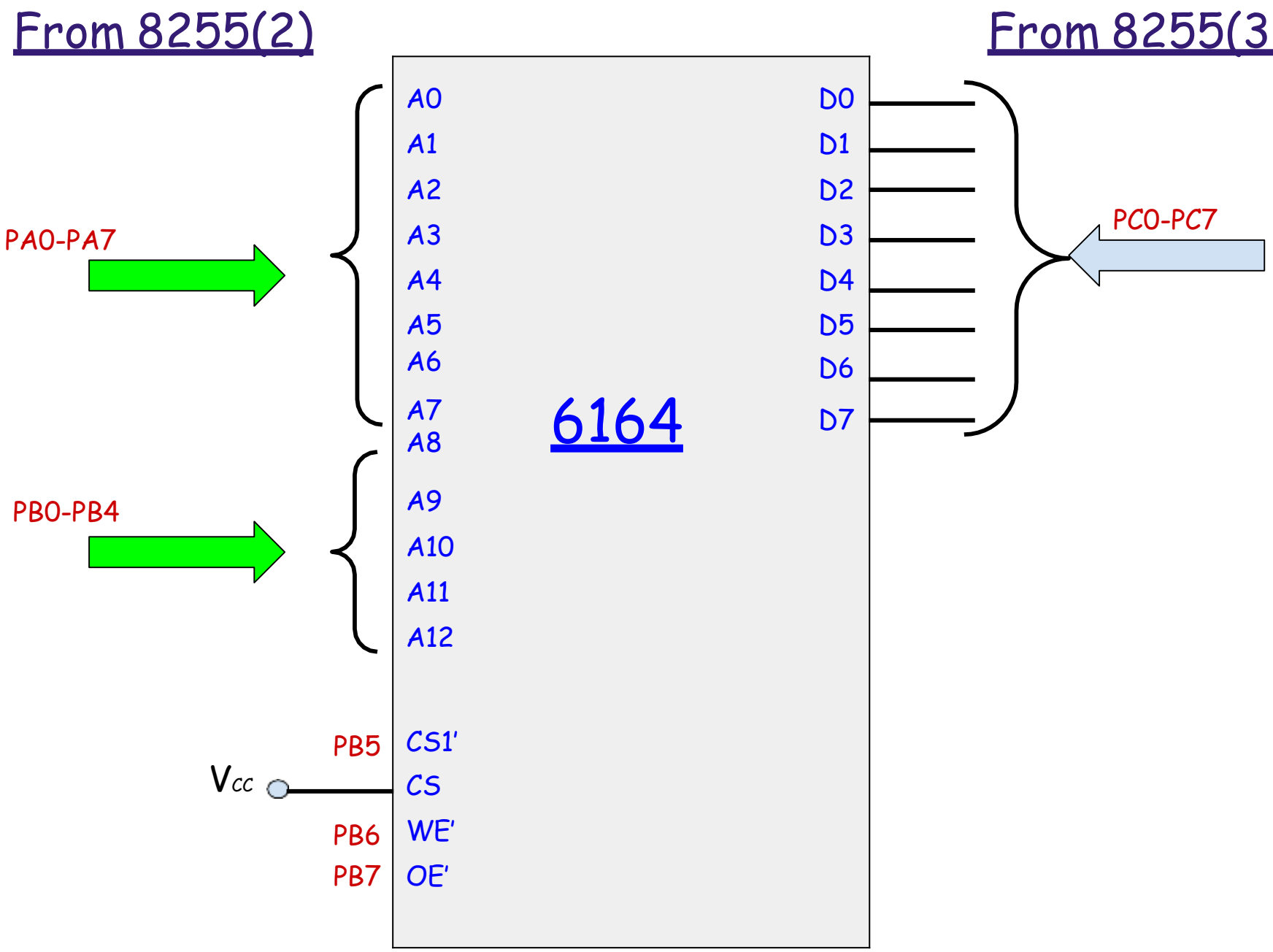

A3
A4
A5
I2
I1
I0
O0
O1
O2
LS138
8255(1) CS'
8255(2) CS'
8255(3) CS'
M/IO
G2B
G2A
G1
A6
VCC

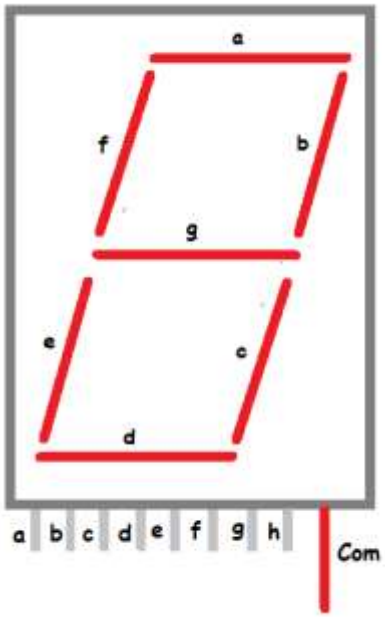
I/O Decoder


D[0..15]
D0
D1
D2
D3
D4
D5
D6
D7
RD'
WR'
A0
A1
RESET'
CS'
8255 (1)
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
SPDT SWITCH
GND
LED1
LED2
LED3
LED4
NC
NC
A1
A2
FROM
74LS138(Y0)


D[0..15]
To 6164
D0
D1
D2
D3
D4
D5
D6
D7
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
A0-A7
RD'
WR'
A1
A2
A0
A1
RESET'
8255(2)
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
A8-A12
OE'
WE'
CE'
FROM 74LS138 (Y1)
CS'
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
NC


D[0..15]
To 6164
D0
D1
D2
D3
D4
D5
D6
D7
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
NC
RD'
WR'
A1
A2
RESET'
8255(3)
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
NC
FROM 74LS138 (Y2)
CS'
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
TO 6164 D0-D7

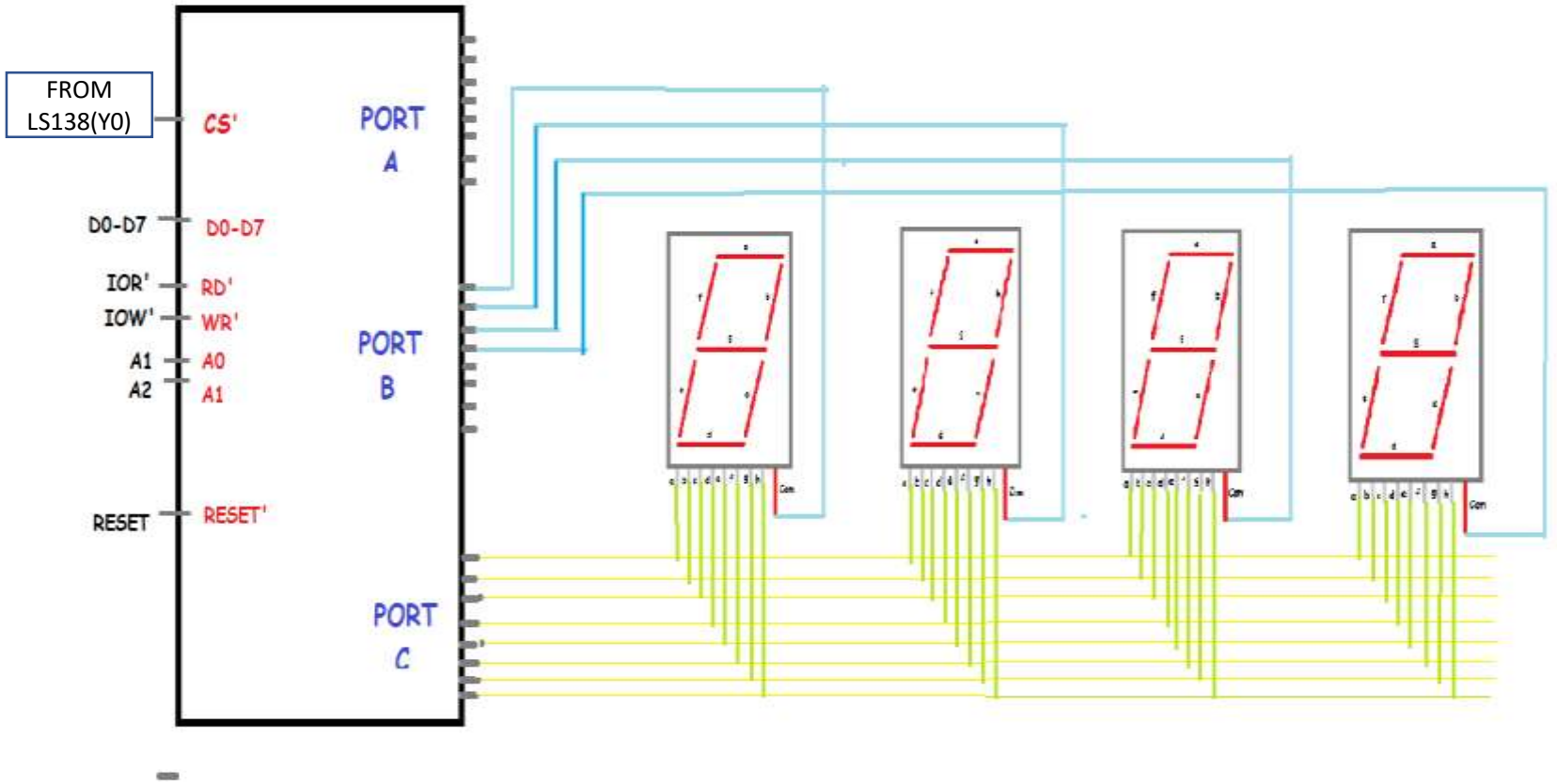

From 8255(2)
From 8255(3)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
6164
D0
D1
D2
D3
D4
D5
D6
D7
PA0-PA7
PB0-PB4
PC0-PC7
PB5
CS1'
Vcc
CS
PB6
WE'
PB7
OE'



a -> PC0
b -> PC1
c -> PC2
d -> PC3
e -> PC4
f -> PC5
g -> PC6
h -> PC7

Com
to be
connected to

P or F	A(2nd)	S or I	S or L
PB0	PB1	PB2	PB3


FROM
LS138(Y0)
CS'
PORT
A
D0-D7
D0-D7
IOR'
RD'
IOW'
WR'
PORT
B
A1
A0
A2
A1
RESET
RESET'
PORT
C