


Lecturer: _____ (Date) _____ (Signature & Fullname)	Approved by: _____ (Date) _____ (Signature, Position & Fullname)
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(The above part must be hidden when copying for exam)

<div></div> <div>Ho Chi Minh City University of Technology</div> <div>Faculty of Computer Science and Engineering</div>	MIDTERM	Semester / AY	1	2020-2021
		Date	October 2020	
	Course name	Computer Architecture		
	Course ID	CO2007		
	Duration	60 minutes	Code	201m1

Notes:

- Write you answers right after every question;
- Students are allowed to use materials printed/written on **ONE** A4 paper (2 pages);
- All pages of this question sheet **MUST** be returned. Any missing page will let you get 0 mark!

Student's name: SOLUTIONS

Student's ID:

Learning outcomes - Questions mapping:

- L.O.1 - Estimate performance of a computer under given parameters: 1 - 10;
- L.O.2 - Explain basic instructions in the instruction sets: 11 - 30

Questions for the midterm test are started from here:

1. Contemporary computers can be categorized into classes:

Answer: Embedded computers, personal computers, server computers, and super computers

2. Is “throughput” or “response time” affected when the current processor is replaced by a faster one?

Answer: Both

3. To improve system performance, which below approaches can we do?
 A - Using an another programming language to reduce machine instructions
 B - Changing the algorithm to reduce the cycles required by the application
 C - Reducing cycle time of processors

Answer: A, B, and C

Following data is used for questions from 4 to 7:

A program consists of 1000 assembly instructions of which 30% are load/store instructions, 10% are jump instructions, 20% are branch instructions while the rest are arithmetic instructions. CPI for load/store, jump, branch, and arithmetic instructions is 2.5, 1, 1.5, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

4. What is the execution time of the above program?

Answer: 975 ns/0.975 × 10⁻⁶s

5. By how much must we improve the CPI of L/S instructions if we want the program to run $1.5\times$ faster?

Answer: $\text{newCPI(L/S)} = 0.33/\text{reduce by } 2.17/\text{reduce by } 86,6\%$

6. What is the weight average CPI of the above program?

Answer: 1.95

7. What is speed-up of the above program if CPI of load/store instructions is reduced by a factor of 2?

Answer: ≈ 1.24

8. According to the Moore's Law, how long does it take for the number of transistors integrated into a chip to get double?

Answer: 18 - 24 months

9. A clock signal becomes logic 0 in total 2×10^9 times per second, what is the rate of the clock?

Answer: 2 GHz

10. Is the MIPS instruction **sb** `$t1, 0x2020($t0)` legal?

Answer: Yes

11. Given the following MIPS instruction

lhu `$s0, $s0($s0)`

What will this instruction do?

Answer: This instruction is not a standard MIPS instruction

12. Given the following MIPS sequence:

lw `$t0, 30($s3) # load word`
add `$s1, $s2, $t0`

Assume that the `$s3` register stores a base address of an integer array. What will we get in `$s1` after the sequence gets executed?

Answer: The sequence causes a runtime error

13. To assign value 12345678 to the `$t0` register, which standard MIPS instructions should be executed?

Answer:

lui `$t0, 0x00BC`
ori `$t0, $t0, 0x614E`

Following data is used for questions from 14 to 16:

Given the following memory locations/cells used in a standard MIPS-based system:

address:	8	9	10	11
	0x12	0x34	0x56	0x78
	0x9A	0xBC	0xDE	0xF0
address:	12	13	14	15

Assume that the `$s0` register stores value of 8.

14. What is the value of the `$t0` register after the instruction `lh $t0, 6($s0)` is executed?

Answer: 0xFFFFDEF0

15. What is the value of the `$t0` register after the instruction `lw $t0, 6($s0)` is executed?

Answer: The instruction causes a runtime error

16. What will be changed after the instruction `sw $t1, 4($s0)` is executed? Assume that the `$t1` register stores value of `0x00000000`.

Answer: Memory cells: 12, 13, 14, and 15

17. What is (are) NOT (an) operand(s) for standard MIPS instructions among: Integer numbers, Real numbers, Memory cells, and Registers

Answer: Real numbers

Following data is used for questions from 18 to 19:

Assume that the `$s0` and `$s1` registers store values of `12345678` and `0xFACECAFE`, respectively.

18. What is the value of the `$s2` register after the following instruction is executed?

`andi $s2, $s0, 2020`

Answer: 0x00000144

19. What is the value of the `$s2` register after the following MIPS instructions are executed?

`srl $s2, $s0, 4`
`or $s2, $s1, $s0`

Answer: 0xFAFEEBFE

20. Which is the machine instruction of the `add $t0, $s1, 2020` MIPS instruction?

Answer: Instruction is not correct

21. Which is the MIPS instruction according to the following machine instruction?

`0000_0000_0001_0000_0101_0000_1100_00002`

Answer: `sll $t2, $s0, 3`

22. Which is the machine instruction of the `lw $t0, -32($s1)` MIPS instruction (written in hexadecimal)?

Answer: 0x8E28FFE0

23. What is stored in the Program counter (PC) register in the context of the MIPS architecture?

Answer: Address of the next instruction

Following MIPS instructions are used for questions from 24 to 26:

Assume that the following sequence of instructions is executed by a standard MIPS processor. The pseudo instruction `la` will assign the base address of an array to a register.

```

.data
    array: .word 2020, 20, -20
.text
main:    la      $t0, array
        lhu     $s0, 2($t0)
        lh      $s1, 6($t0)
        addu    $s3, $s1, $s0
        sb      $s3, 8($t0)
        lh      $s4, 10($t0)

```

24. What is value of the \$s0 register?

Answer: 0x000007E4

25. What is value of the \$s1 register?

Answer: 0x00000014

26. What is value of the \$s4 register?

Answer: 0xFFFFFEC

The following sequence of MIPS instructions is used for questions from 27 to 28:

```

                addi    $t1, $zero, 10
                add     $t2, $zero, $zero
FindMean:      addi     $t1, $t1, -1
                addi     $t2, $t2, 1
                bne      $t1, $t2, FindMean

```

27. What is value of the \$t1 register after the above sequence is executed?

Answer: \$t1 = 5

28. Assume that the above sequence is executed by a 10 MHz MIPS processor. The processor can process 1 instruction per cycle. What is the execution time of the above sequence?

Answer: 1.7 μ sec

The following sequence of MIPS instructions is used for questions from 29 to 30:

```

label:  addi $t0, $t0, -1
        addi $t1, $t1, 1
        bne $t0, $t1, exit
        j label
exit:

```

29. What is the offset (16 bit) of the **bne** \$t0, \$t1, exit instruction:

Answer: 0x0001

30. Given that the **bne** \$t0, \$t1, exit instruction is stored at memory location 0xCAFE00C. Which is the offset field (26 bit) of MIPS instruction **j** label?

Answer: 0x2BFB001

— The test consists of **30** questions printed on **4** pages —