Digital design with the Verilog-HDL – CO1025
Lab 3: RTL model

Note:

- Please submit your work no later than 21-July, 2021 (**in only one week**)
- Your submission should include Verilog file(s), waveform(s), and a short report describing your modules.

Question:

please design and implement the Rock-Paper-Scissor game as follows

- **module** rps(win, player, p0guess, p1guess);
- Assumptions:
  - Input: p0guess, p1guess = {3 for rock, 2 for paper, 1 for scissors}; values can be changed
  - Output: player is 0 if p0 wins, 1 if p1 wins, and don't care if there is a tie
  - Output: win is 0 if there is a tie and 1 if a player wins
- Reminders
  - Paper beats rock, scissors beats paper, rock beats scissors
  - Same values tie
- Two possible approaches
  - Figure out the Boolean equations for win and player and implement these using continuous assignments
    - Use bitwise operators
  - Examine what the various items equal and do logical operations on these
    - Use equality and logical operators

1. Implement the rps module with the first approach (name rps1), write a testbench to check
2. Implement the rps module with the second approach (name rps2), write a testbench to check
3. Design a "checker" as following model to compare the two approaches, write a testbench to check