Digital Design with the Verilog-HDL – CO1025
Lab 5: Finite State Machine

Note:

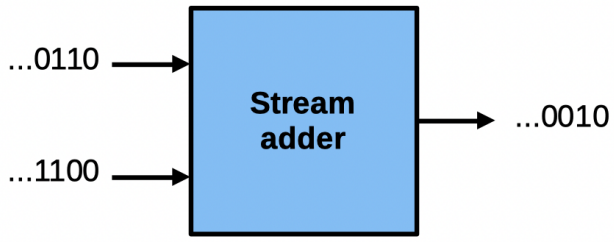
- Please submit your work no later than 4-August, 2021 (**in two weeks**)
- Your submission should include Verilog file(s), waveform(s), and a short report describing your modules.

Question 1 (6 points):

1. Draw an FSM (Moore style) that receives a string of bits (one by cycle). Bits are received from MSB to LSB. The output will be 1 if the values (in decimal) of the string is multiple of 3; otherwise, it will be 0.
2. Implement the FSM by Verilog. Write a test bench to check.

Question 2 (4 points):

1. Design an FSM (Moore style) for a module that adds two infinite input bitstreams. Streams sent every cycle with the least significant bit (LSB) first.



2. Implement the FSM by Verilog. Write a test bench to check

Hint: *For each FSM, please identify how many states we should have. Each state represents the status (a case) of the system.*