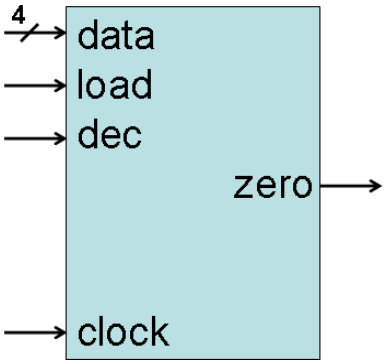
Digital Design with the Verilog-HDL – CO1025
Lab 4: Behavioral model

**Note**:

- Please submit your work no later than 26-July, 2021 (**in only one week**)
- Your submission should include Verilog file(s), waveform(s), and a short report describing your modules.

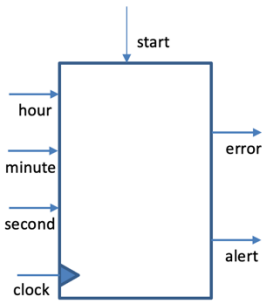
**Question 1**:
please design and implement a J-K flip flop (please consult the Digital Design course for JK flip flop)

**Question 2:**




- Design and implement a module as the block diagram above with the following requirements:
  - A count number will be loaded to the module via the "data" input at a rising clock edge when the "load" signal is 1
  - The count number will be reduced by 1 at a rising clock edge if the "dec" signal is 1
  - When the count number is 0, the module is halt and waits for a new number loaded
  - The "zero" is 1 if the count number is 0
- Write a testbench to verify the module

**Question 3**: Given a timer as depicted in the following figure.




- "hour", "minute", and "second" are inputs to set-up the timer (maximum amount is 12 hours)
- The period of the "clock" input is half of a second
- When "start" is active (synchronous, active low), the timer takes values of "hour," "minute," and "second" into account and starts counting down until zero.
- When there is no error and the timer has counted to zero, the "alert" output is active (active high)

- When there exists any error (for example, the value of minute is greater than 59), the “error” signal is active (active high)

Please design and implement the timer with Verilog, verify the module with a test bench.