



# On-Chip Voltage Scaler Circuits with Energy-Efficient Charging and Recycling

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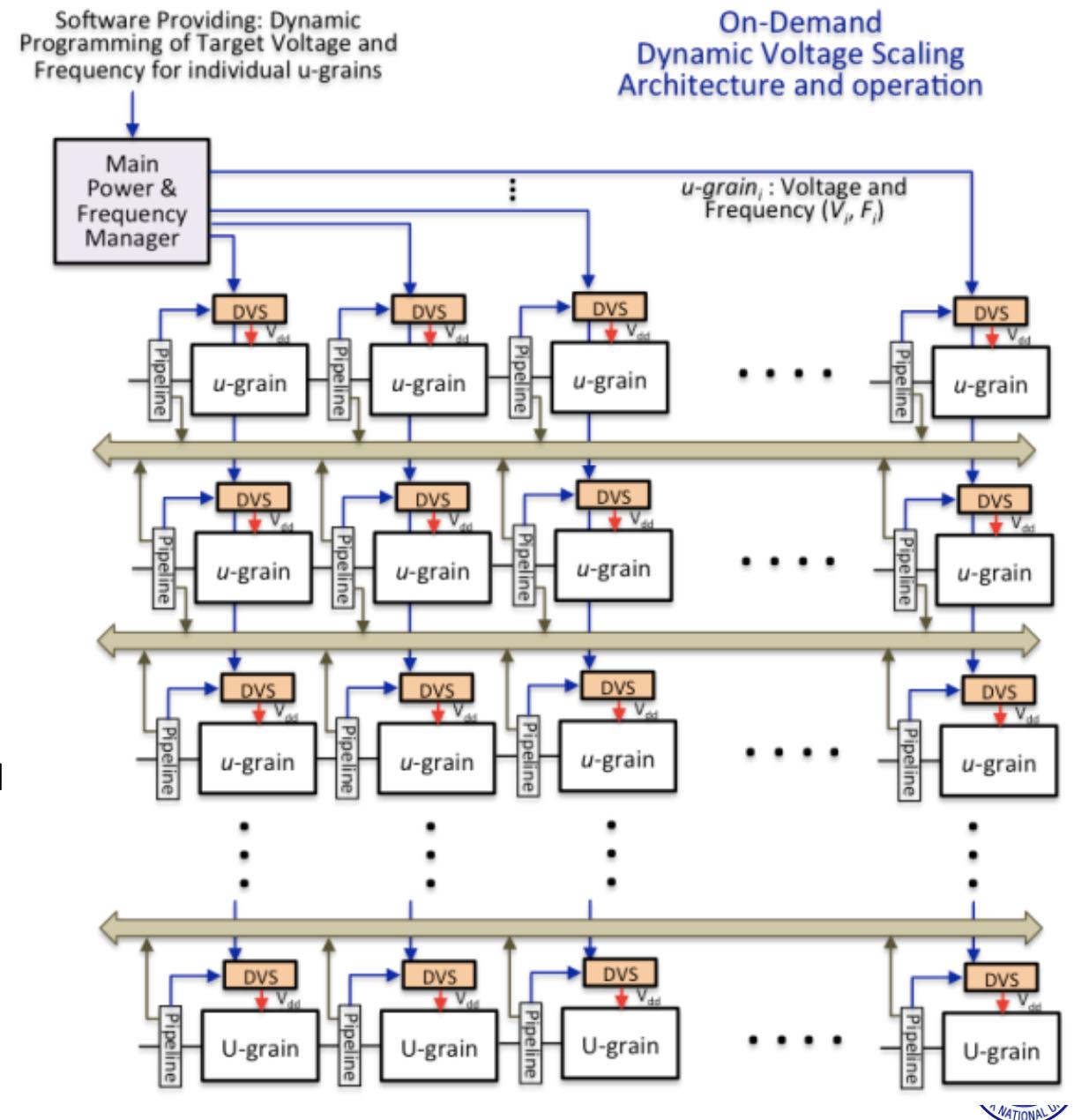
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# Research Goal of Low Power Voltage Scaler

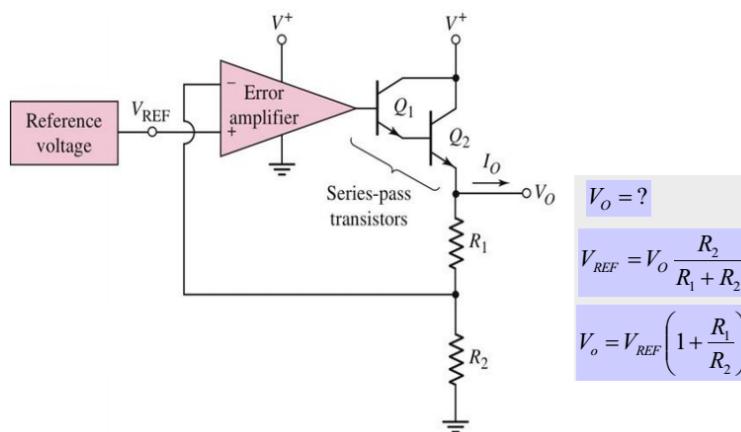
## ❖ On-Chip Dynamic Voltage Scaler for Multiple Power Domain

- Dynamic Power Management For Multiple micro-grain power domains
- Wide input and output voltage range
- On-Demand Dynamic output voltage scaling
- Small form factor On-chip Switched Capacitor Voltage converter and Scaler



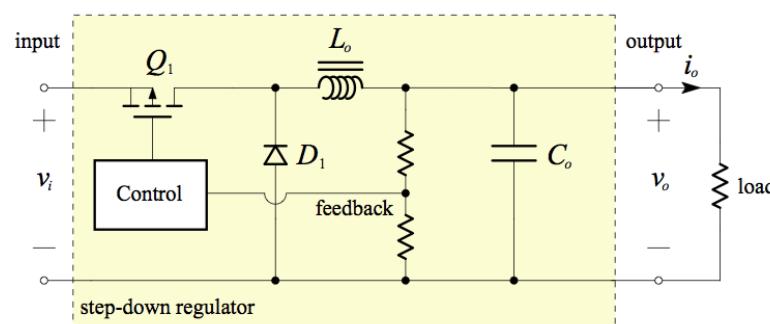
# Conventional Voltage Converters

- ❖ Linear Voltage Regulator: LDO (Low Drop Out)

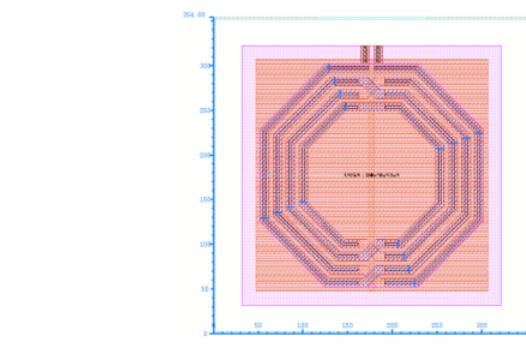


$$\eta \equiv \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{LOAD}}{V_{IN} I_{LOAD}} = \frac{V_{OUT}}{V_{IN}} = \frac{V_{IN} - V_{DO}}{V_{IN}}$$

- ❖ Inductor Based DC-DC Converters (Buck Converter)



Specification	Linear	Switched-Mode
Line Regulation	0.02%–0.05%	0.05%–0.1%
Load Regulation	0.02%–0.1%	0.1%–1.0%
Output Ripple	0.5 mV–2 mV RMS	10 mV–100 mVp-p
Input Voltage Range	±10%	±20%
Efficiency	40%–55%	60%–95%
Power Density	30 mW/cm <sup>3</sup>	10 mW–600 mW/cm <sup>3</sup>
Transient Recovery	50 µs	300 µs
Hold-Up Time	2 ms	34 ms



Layout of 5.5 nH inductor with area of  $(354.08 \mu\text{m})^2$

# Switched Capacitor (SC) DC-DC Converters

## ❖ Requirements for On-Chip DC-DC Converters and Regulators

- Multicore processors dissipate power in the range of 1 W/mm<sup>2</sup>
- Integrated dc–dc conversion requirements:
  - Steps down from a conveniently chosen voltage above typical CMOS core operating voltages;
  - Provides high efficiency over a wide load and voltage range;
  - Highly scalable for granular implementation

## ❖ Problems of Inductor DC-DC Converters

- High-power requires intensive integrated inductor or a bulky off-chip inductor
- Transistors rated for the full input voltage and the full output current of the application

## ❖ Advantage of SC Converters

- Requires only capacitors as passives
- Capacitors have significantly higher energy and power densities
- More easily integrated than inductors

## ❖ Drawback of SC Converters

- Limited to low-power (<100 mW) applications
- High ripple voltages & relatively large output voltage granularity
- On-chip capacitors still requires large chip area

## ❖ Additional Benefits of SC Converters

- NMOS Switches need about 1 V rating (whereas buck converters need 10 V rating)
- No inductive switching losses, and less overshoots, body diode conduction, and less timing issues
- Low-power operation without control complexity, reducing clock rate.
- Higher Energy density of capacitors, orders of magnitude greater than inductors.

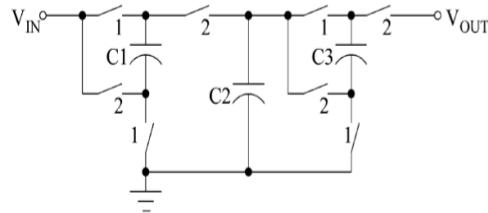


# Switched Capacitor (SC) DC-DC Converters

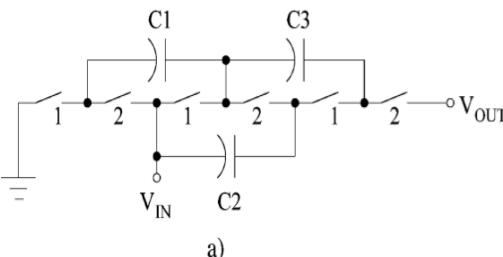
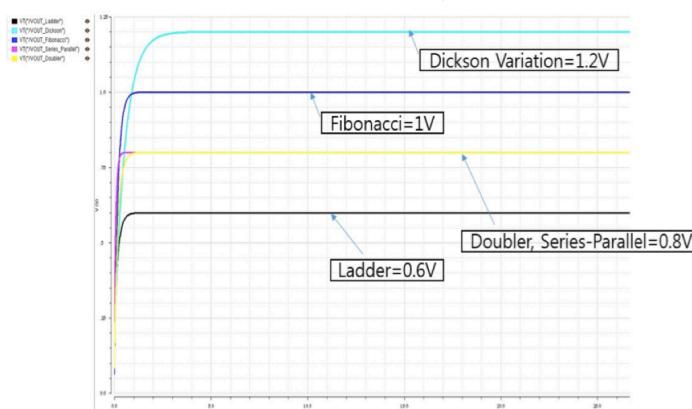
## ❖ Switched Capacitor Voltage Converter Types

### ● Five Step-Up Converters Compared

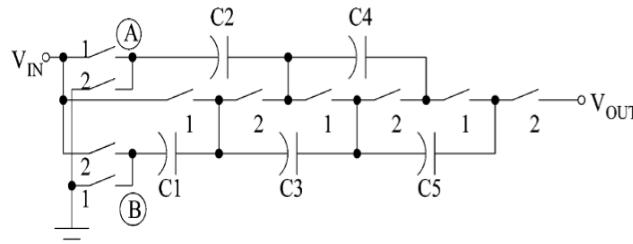
- (a) Ladder
- (b) Cockcroft-Walton Multiplier (Dickson Variation)
- (c) Fibonacci
- (d) Series-Parallel (or Parallel Series)
- (e) Doubler



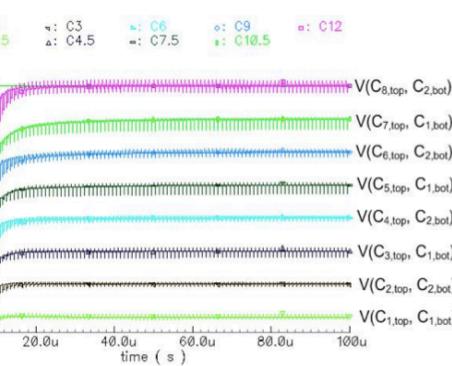
e)



a)

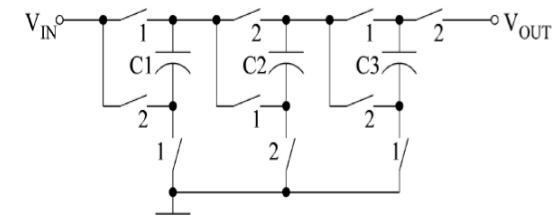


b)

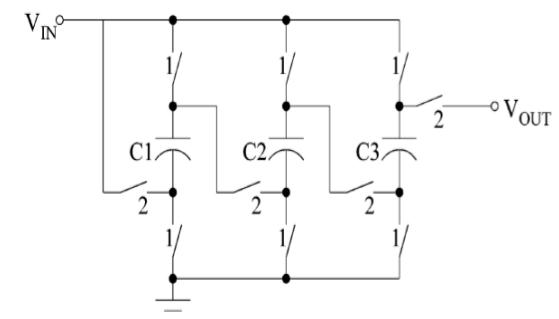


(a) When the capacitors are in a ladder configuration

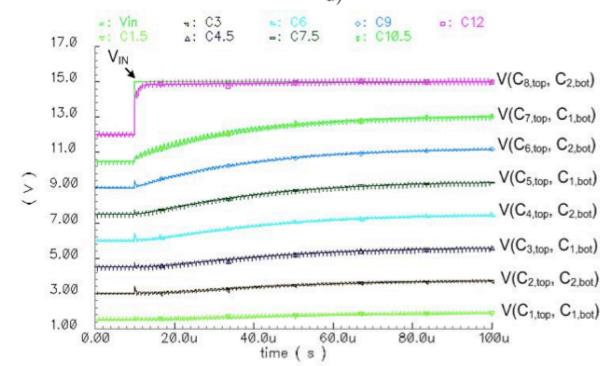
Ladder (Variation) Converter



c)



d)



(b) When the capacitors are in a star configuration

Dickson Star Converter



# Target Architecture of Dynamic Voltage Scaler

## ❖ Target Dynamic Voltage Scaler Structure

### ● Main Blocks and Path of DVS

- ✓ Voltage Converter and Storage Analog Block

### ● 1<sup>st</sup> Stage

- ✓ Reconfigurable Voltage Buck-Boosting Energy Storage
- ✓ Reconfigurable Coarse level Voltage Output

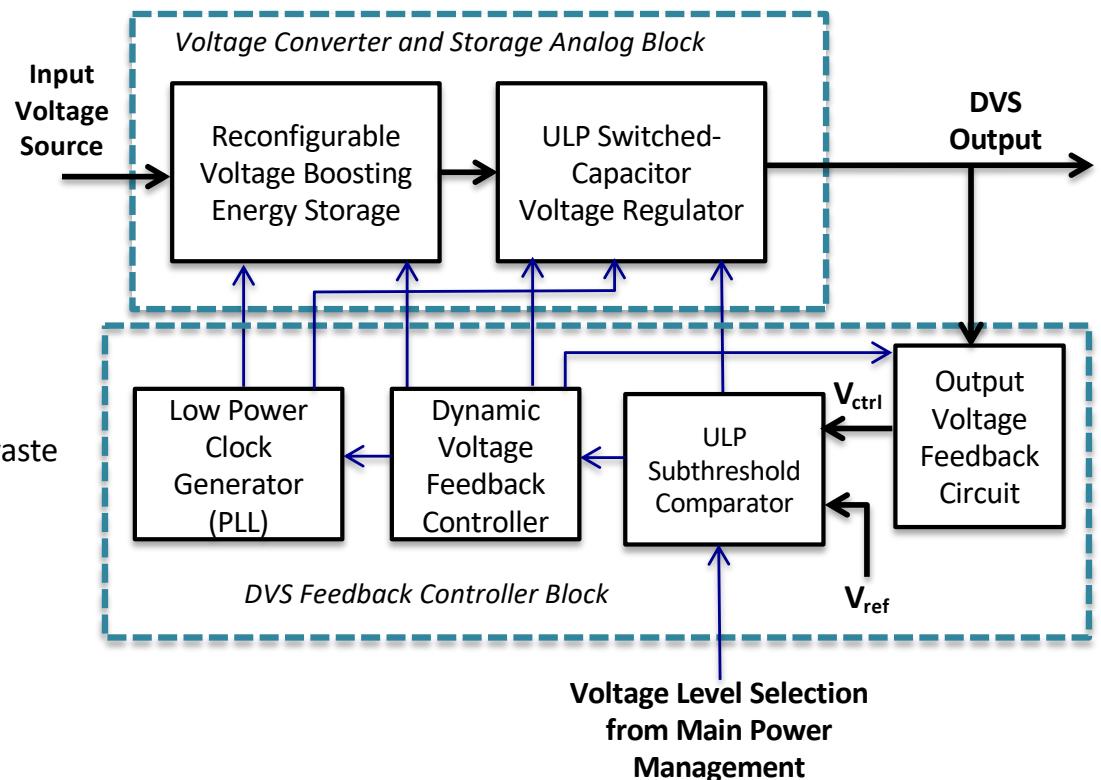
### ● 2<sup>nd</sup> stage

- ✓ ULP Switched-Capacitor Voltage Regulator block
- ✓ Minimize Voltage ripple to further reduce energy waste

### ● DVS feedback controller block

- ✓ Output voltage feedback circuit
  - DVS output voltage  $\ominus$  measurement
- ✓ Ultra Low Powr comparator Circuit
  - Compare with the target Reference voltage
- ✓ Dynamic feedback controller
  - With Comparator's result, control the Energy storage and Voltage regulator
- ✓ Low power PLL (Phase Locked Loop) clock generator
  - Provide control clocks to Energy storage and Voltage regulator

## Low Energy Loss Dynamic Voltage Scale Controller Architecture





# An Energy Efficient Charging Technique for Switched Capacitor Voltage Converters with Low Duty-Ratio

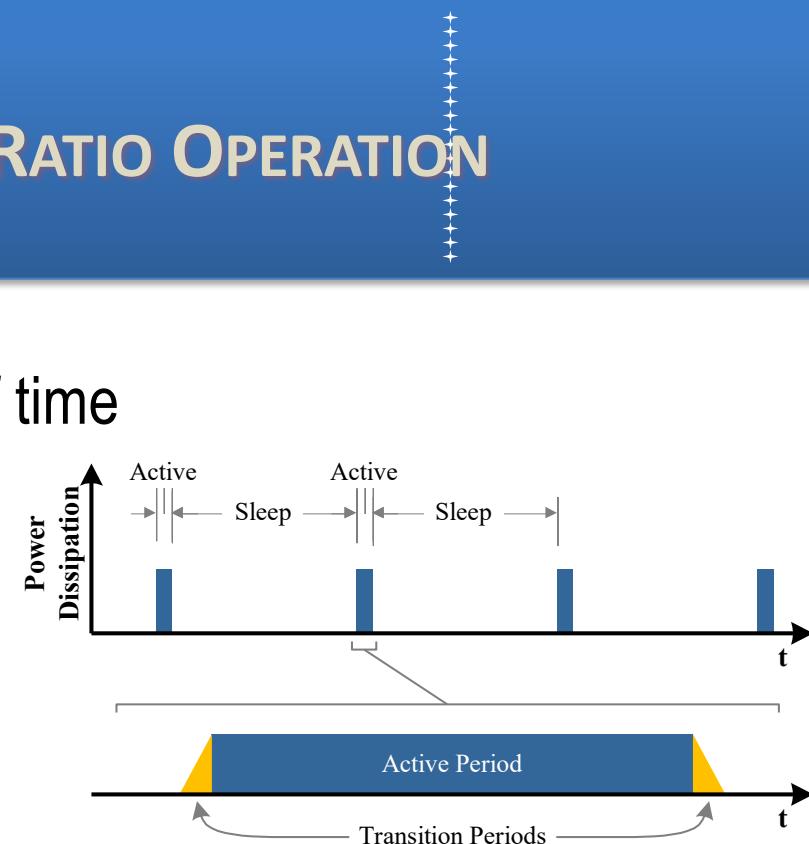
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# TARGET APPLICATIONS: Low DUTY RATIO OPERATION

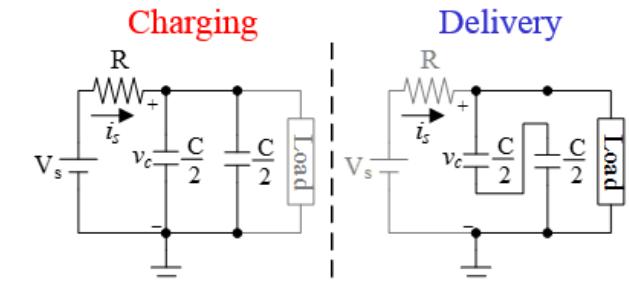
- A circuit is active for a small period of time
  - Followed by a long sleep period
- Problems of dynamic power
  - Suffer with poor energy efficiency
  - Due to losses in transition periods
- During sleep-to-active transition
  - DC-DC converter's capacitor bank is charged
  - From zero to a certain voltage
- In Switched-Capacitor (SC) DC-DC converter
  - The initial charging is done at 50% energy efficiency
  - Half the energy from the source is wasted and only half is stored in capacitors



# INITIAL CHARGING OF AN SC DC-DC CONVERTER (1/2)

## -CONVENTIONAL CONVERTER (ONE-STEP CHARGING)

- Consider a conventional SC boost converter
  - With voltage conversion ratio of duty
- Consider initial voltage on the capacitor  $V_0$ 
  - Charging voltage:  $v_c(t) = V_S + (V_0 - V_S)e^{-t/\tau}$
  - Charging current:  $i_s(t) = \frac{v_S - V_0}{R} e^{-t/\tau}$
  - Instant. power loss:  $P_R(t) = \frac{v_R(t)^2}{R} = \frac{(V_0 - V_S)^2}{R} e^{-2t/\tau}$
  - Energy lost:  $E_R = \int_0^{\infty} P_R(t)dt = \frac{1}{2} C(V_0 - V_S)^2$
  - Energy stored:  $E_C = E_{C,final} - E_{C,initial} = \frac{1}{2} C(V_S^2 - V_0^2)$
  - Efficiency  $\eta = \frac{E_C}{E_C + E_R} = \frac{\frac{1}{2} C(V_S^2 - V_0^2)}{\frac{1}{2} C(V_S^2 - V_0^2) + \frac{1}{2} C(V_0 - V_S)^2} = \frac{1}{2} \left(1 + \frac{V_0}{V_S}\right)$



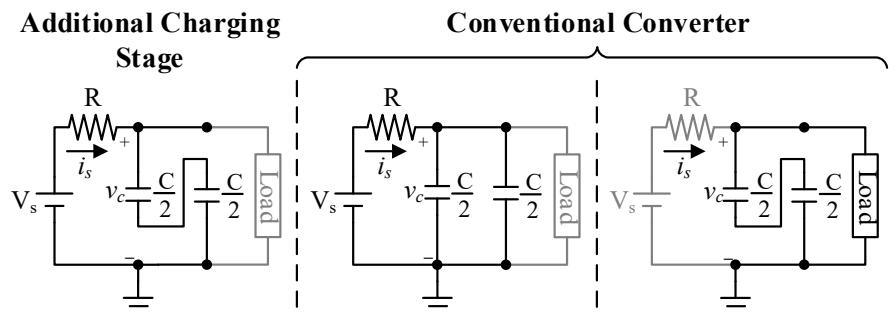
$V_0/V_S$	Efficiency $\eta$
0.00	50.0 %
0.25	62.5 %
0.33	66.5 %
0.50	75.0 %
0.67	83.3 %
0.75	87.5 %
0.80	90.0 %
0.90	95.0 %

- The charging efficiency is independent of the resistor size
- Higher initial voltages results in better charging energy efficiency
  - Use multiple step charging with smaller  $\Delta V = V_S - V_0$

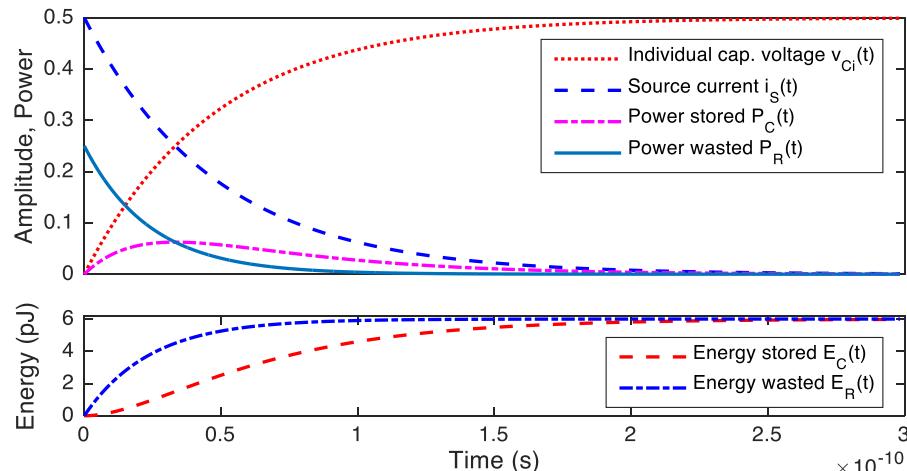
## INITIAL CHARGING OF AN SC DC-DC CONVERTER (2/2)

### -TWO STEP CHARGING

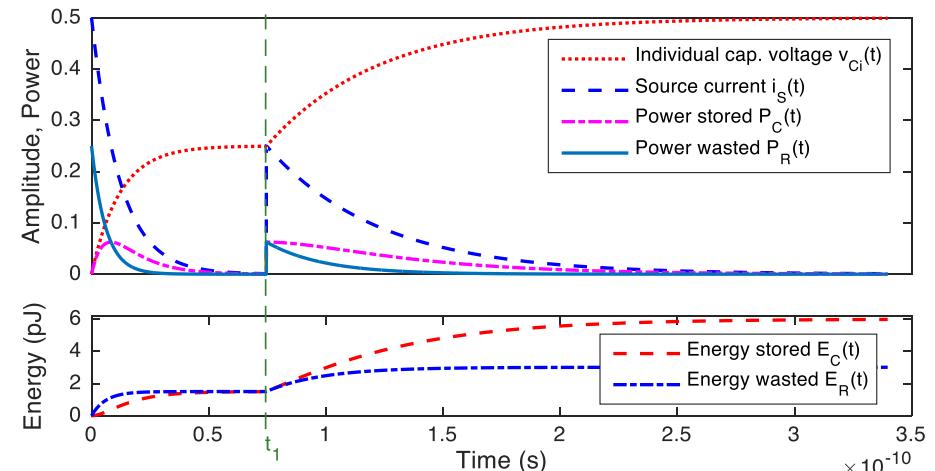
- Using additional charging stage
- Efficiency of step 1 & 2 is
  - $\eta_1 = 50\%$  and  $\eta_2 = 75\%$
- Total charging efficiency  $\eta = 66.67\%$
- By adding more charging steps, efficiency can be further improved



Simulation results by using mathematical model in MATLAB



Conventional (one-step charging)

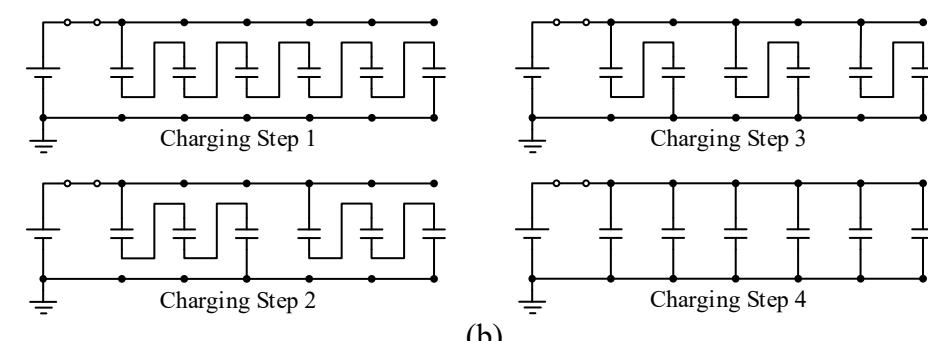
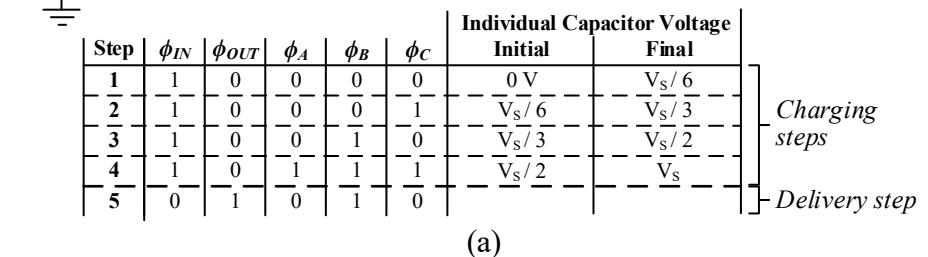
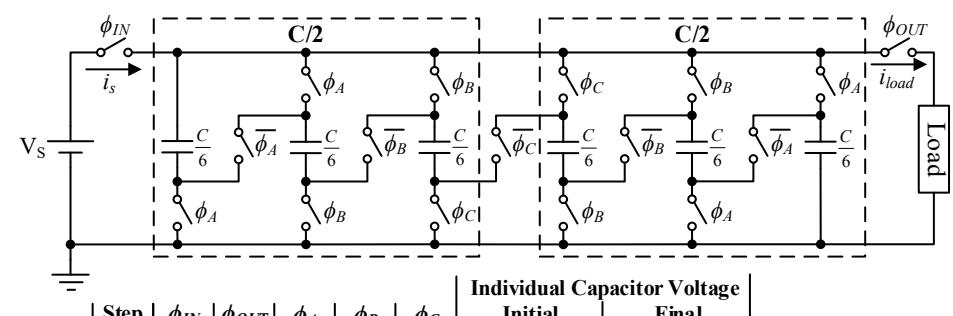
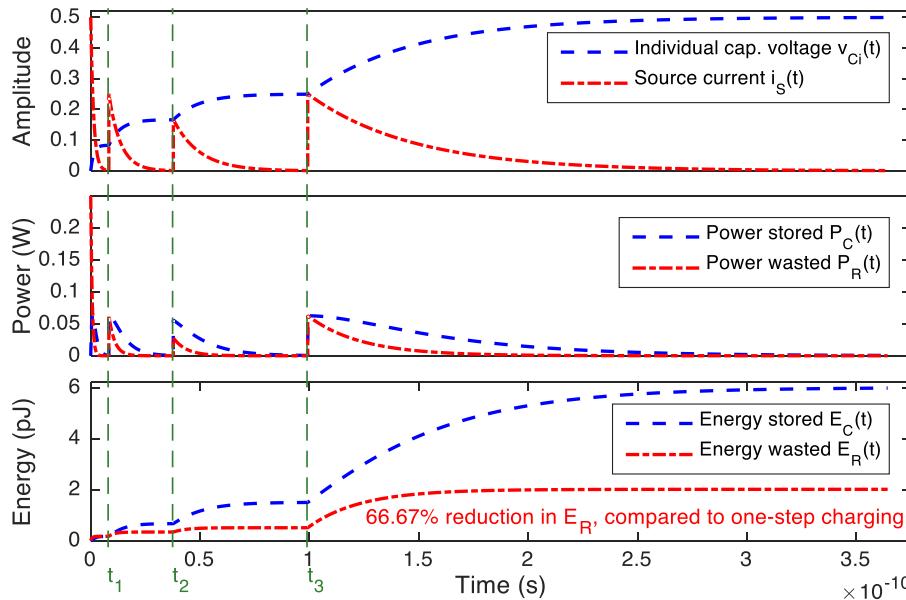


Two-step charging

# INITIAL CHARGING OF AN SC DC-DC CONVERTER

## -SPLIT-CAPACITOR CHARGING (FOUR-STEP CHARGING)

- Splitting each capacitor into smaller units, allow more charging steps
- By splitting each into three
  - Four-step charging is obtained
  - With charging efficiency of 75%
  - 66.67% reduction in energy wastage



Proposed six capacitor bank

(a) Architecture

(b) Configurations during each charging step

# INITIAL CHARGING OF AN SC DC-DC CONVERTER

## -COMPARISON OF N-STEP CHARGING

- The table shows summary of MATLAB simulation results
  - For various number of charging steps (including split-capacitor charging),
  - Showing total efficiency, efficiency of each step and capacitor configuration

	Total	Charging Steps							
		1	2	3	4	5	6	7	8
Capacitors	1	1,1							
Efficiency	49.9%	49.9%							
Capacitors	2	1,2	2,1						
Efficiency	66.6%	49.9%	75.0%						
Capacitors	4	1,4	2,2	4,1					
Efficiency	72.7%	49.7%	75.0%	75.0%					
Capacitors	6	1,6	2,3	3,2	6,1				
Efficiency	75.0%	49.6%	75.0%	83.3%	75.0%				
Capacitors	8	1,8	2,4	4,2	8,1				
Efficiency	74.4%	49.5%	74.9%	75.0%	75.0%				
Capacitors	12	1,2	2,6	3,4	4,3	6,2	12,1		
Efficiency	76.6%	49.2%	74.9%	83.3%	87.5%	83.3%	75.0%		
Capacitors	24	1,24	2,12	3,8	4,6	6,4	8,3	12,2	24,1
Efficiency	77.0%	48.5%	74.8%	83.3%	87.5%	83.3%	87.5%	83.3%	75.0%

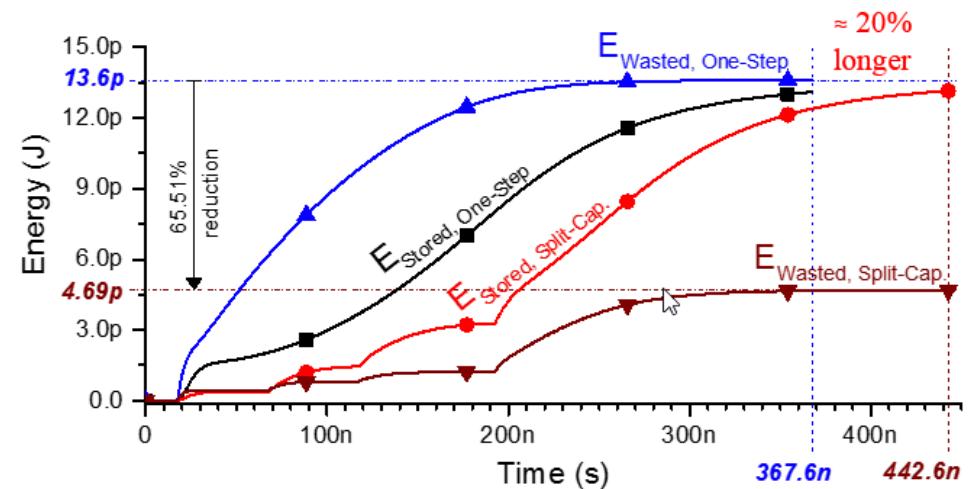
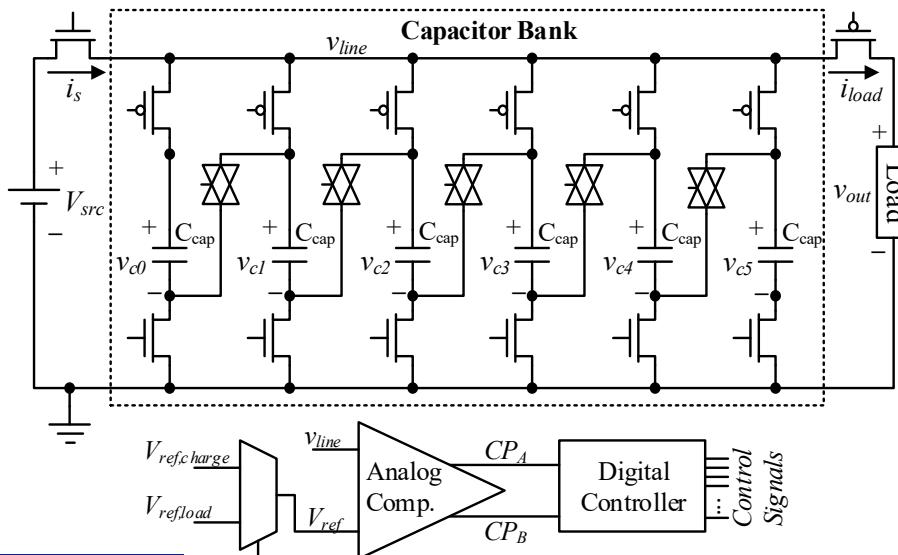
\*Capacitors arrangement represented as  
(Number of Branches, Number of series capacitors in each branch)

# SCHEMATIC SIMULATION ONE-STEP VS. SPLIT-CAP. CHARGING

- Compares Charging behavior of Split-Capacitor Charging (four-step)
  - With one-step charging
- Split-Cap. Charging outperforms, by providing 73.73% efficiency
  - Reducing energy wastage by 65.51%
  - With only 20% overhead of charging period

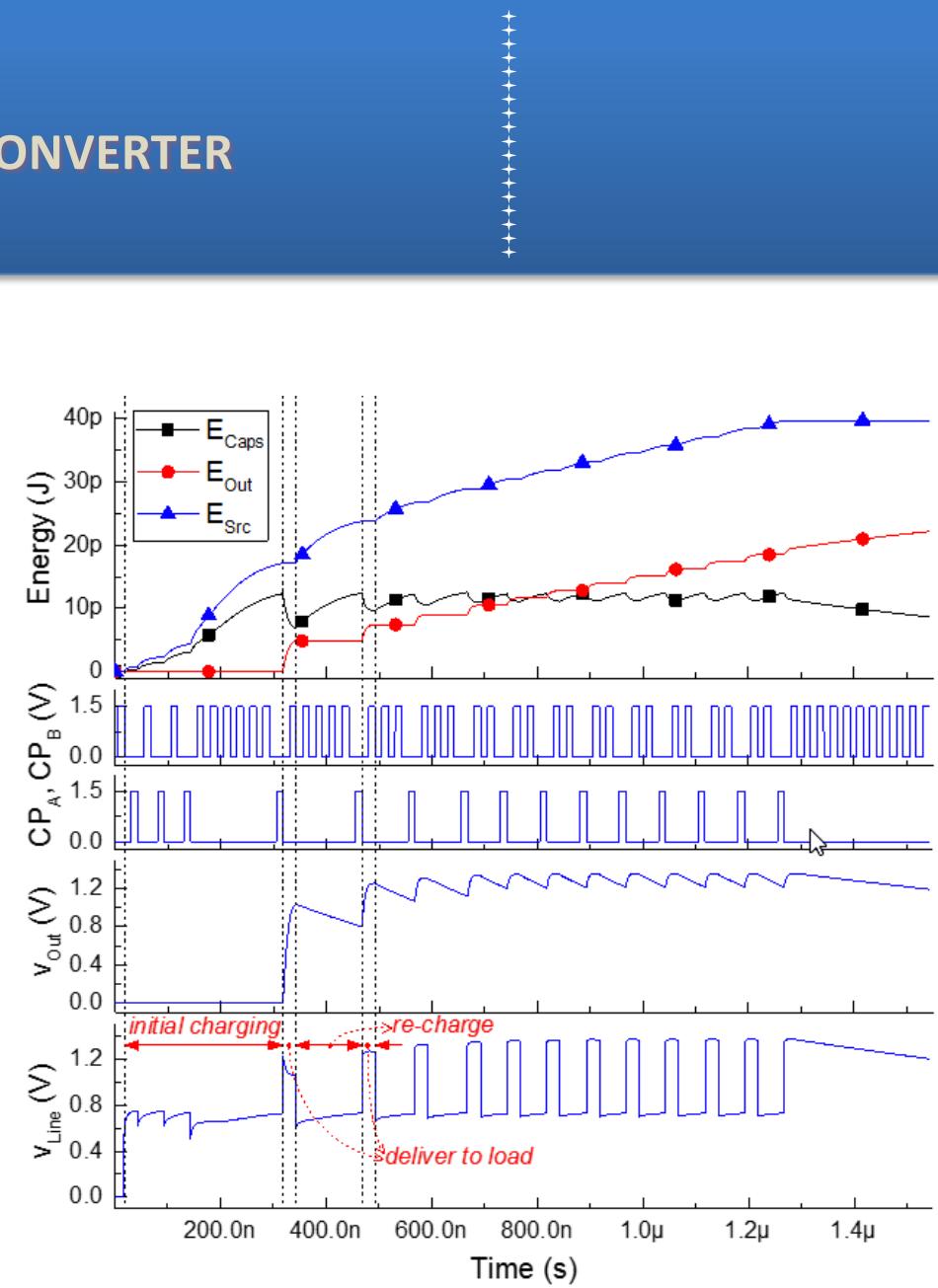
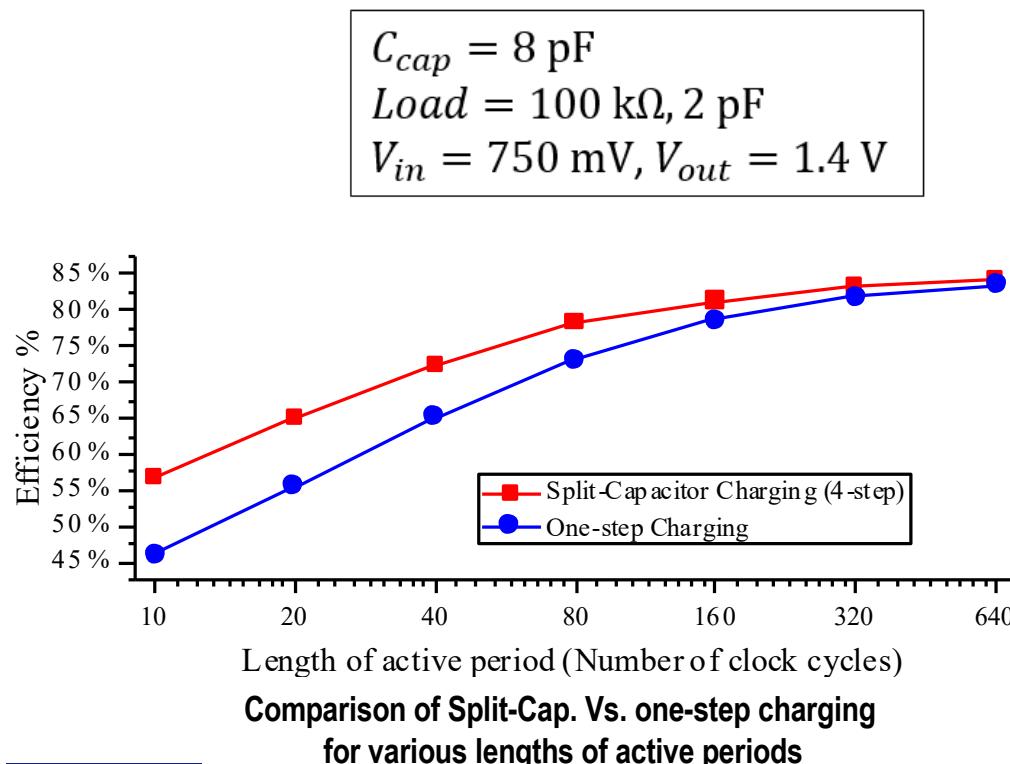
$$C_{cap} = 8 \text{ pF}$$

$$V_{C,final} = 750 \text{ mV}$$



# SPLIT-CAP. CHARGING BASED BOOST CONVERTER

- Simulation results show
  - Improvement for short active periods
  - By incorporating Split-Cap. Charging



# VIABILITY OF MEMS SWITCHES IN SC DC-DC CONVERTER

- To evaluate the viability, following five scenarios are used
  - All MOSFET switches
  - Input switch is ideal (MEMS), rest are MOSFETs
  - Output switch is ideal (MEMS), rest are MOSFETs
  - Both Input and output switches are ideal (MEMS), rest are MOSFETs
  - All switches are ideal (MEMS)
- Non-overlapping signals are used to minimize switching losses

$$\begin{aligned}R_{on,ideal} &= 2 \text{ m}\Omega \\C_{cap} &= 8 \text{ pF} \\Load &= 120 \text{ k}\Omega, 4 \text{ pF} \\V_{in} &= 750 \text{ mV}, V_{out} \approx 1.5 \text{ V}\end{aligned}$$

Act. Period (# cycles)	All are MOSFET SW	Only Input is Ideal SW	Only Output is Ideal SW	Both In/Output are Ideal SW	All are Ideal SW
20	69%	71.96	69.55%	72.97%	72.12%
40	73.73%	76.85%	74.37%	77.98%	79.38%
250	80.35%	83.46%	81.12%	84.77%	89.34%
500	81.2%	84.29%	81.98%	85.62%	90.6%
1000	81.65%	84.72%	82.43%	86.06%	91.25%



\*Using Split-Cap. Chrg. & Energy Recycling converter



# Energy Recycling Voltage Scaler Based on Reconfigurable Capacitive Array

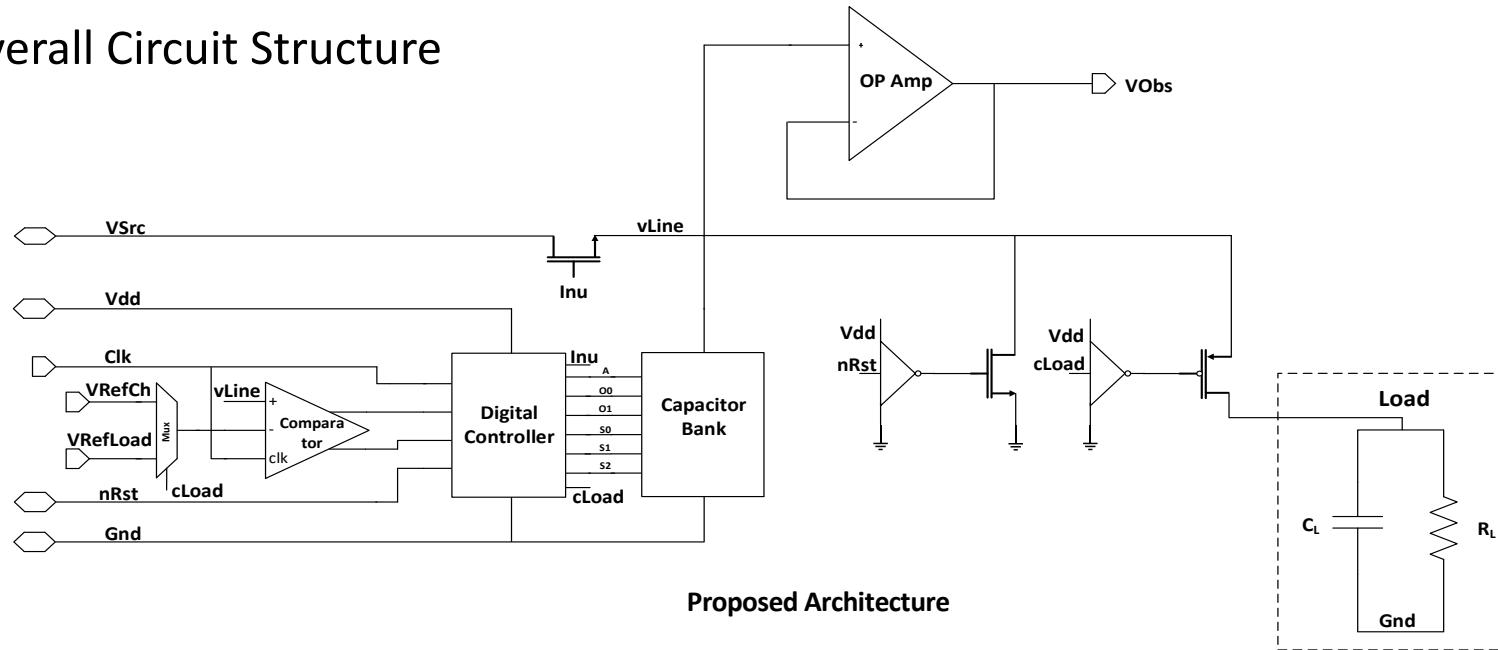
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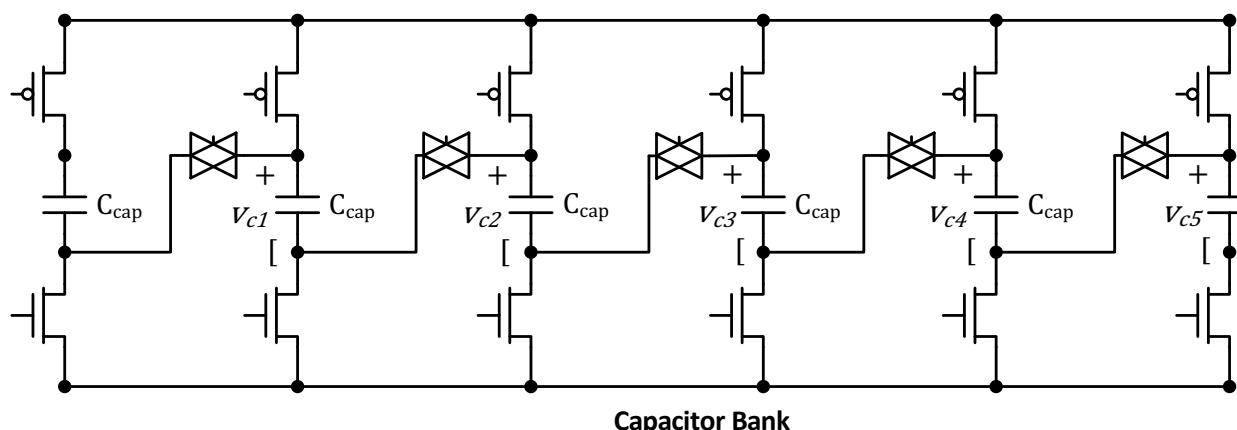


# COMBINING SPLIT CHARGING AND ENERGY RECYCLING

## ❖ Overall Circuit Structure

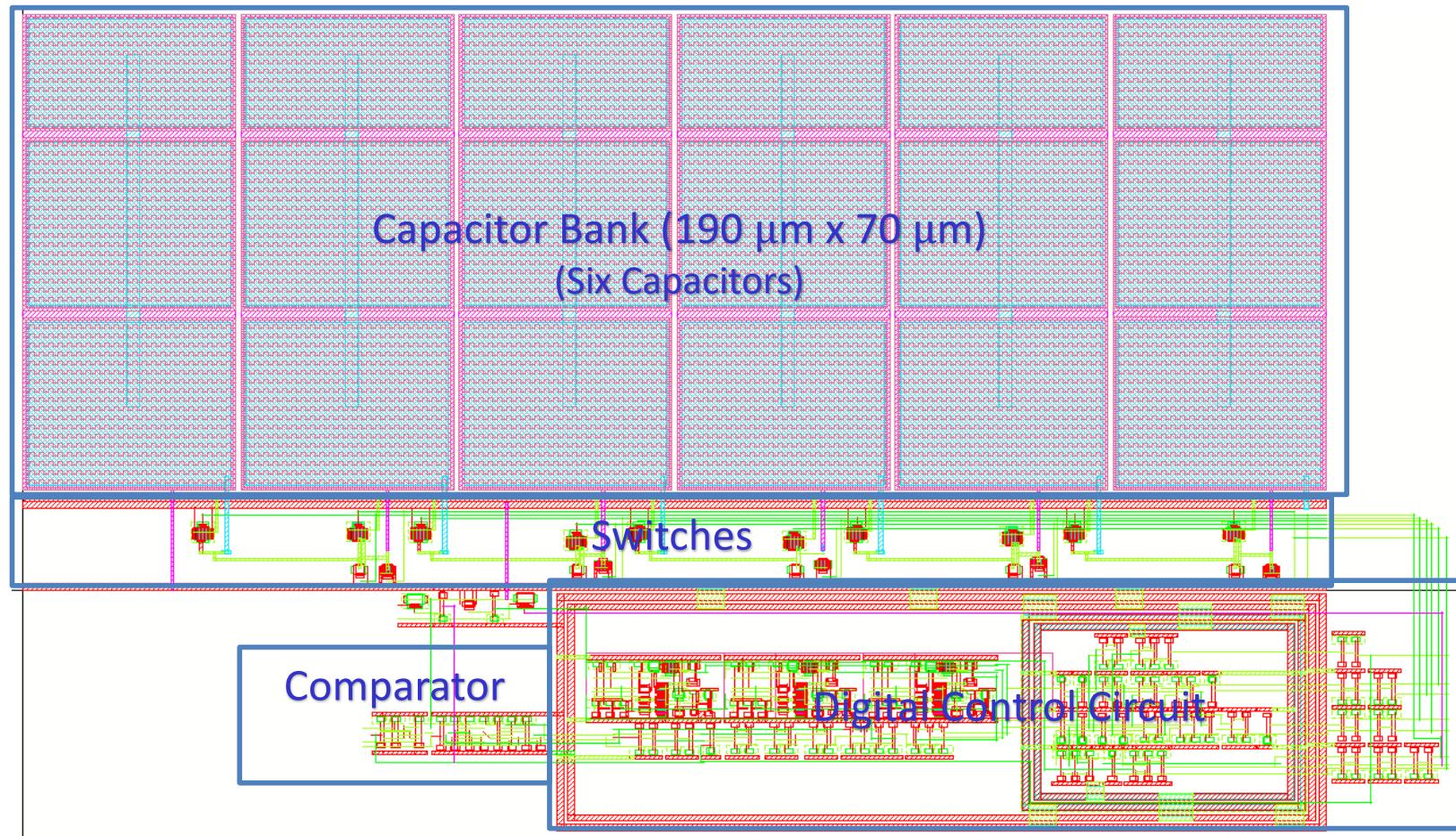


## ❖ Capacitor Bank with Reconfigurable switches



# COMBINING SPLIT CHARGING AND ENERGY RECYCLING

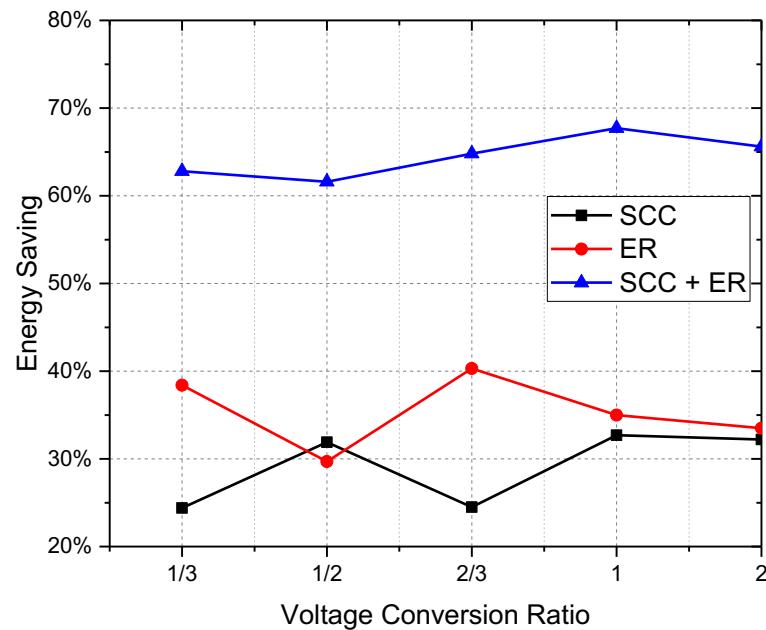
- Cadence Virtuoso Layout



Layout of the Proposed Architecture.

## EFFICIENCY IMPROVEMENT BY SCC AND ER

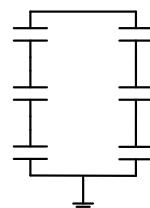
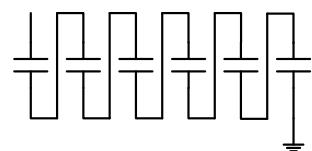
- For maximum power saving both the transitions should be optimized.  
i.e. SCC and ER



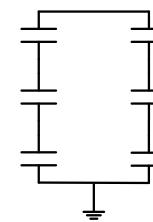
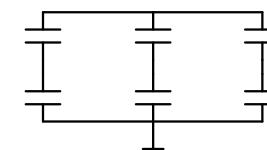
Relative gain of SCC and ER compared to conventional SC DC-DC converters

## PROPOSED ARCHITECTURE As A BUCK CONVERTER

- For generating a target voltage ratio of  $2/3 V_{in}$ , the capacitors are charged in two steps.
  - All of the capacitors are in series.
  - Two branches having three series capacitors.
- Energy Recycling will be carried out in three steps.
  - First configuration three branches each having two series capacitors.
  - Second configuration two branches having three series capacitors.
  - Third configuration one branch having six series capacitors



Split Cap. Charging Configurations

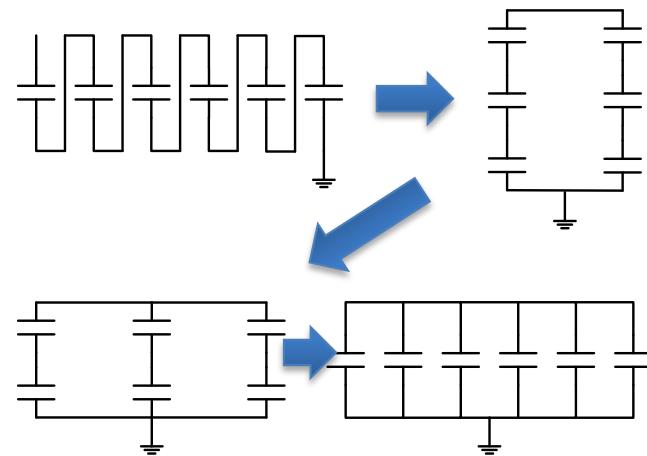


Energy Recycling Configurations

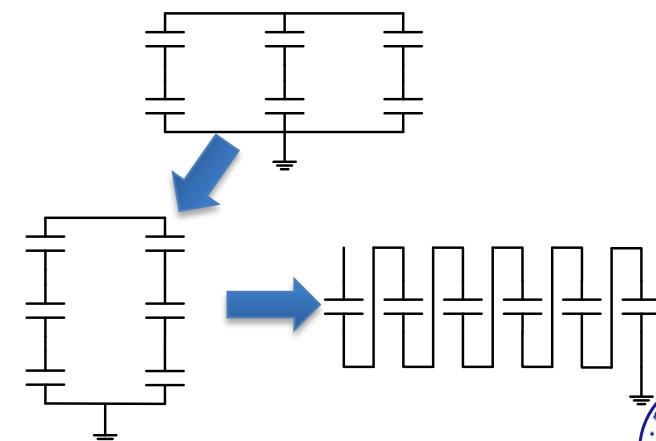
# PROPOSED ARCHITECTURE As A BOOST CONVERTER

- For generating a target voltage ratio of  $2V_{in}$  , the capacitors are charged in four steps.
  - All of the capacitors are in series.
  - Two branches having three series capacitors.
  - Three branches having two series capacitors.
  - Six branches having one capacitor in each branch.
- Energy Recycling will be carried out in three steps. (Same as Buck)

❖ Split Cap. Charging Configurations



❖ Energy Recycling Configurations



# ENERGY MODEL FOR ENERGY RECYCLING STEPS

- Remaining Energy in Each Recycling Steps

❖ Initial Energy After Charging:  $E_{\text{Total}} = \frac{1}{2}(6 C_r)V_{in}^2$

❖ Energy Recycling Step1:

$$E_1 = \frac{1}{2}(3(C_r \cdot 2 \cdot V_{in})^2)$$

$$E_2 = \frac{1}{2} \cdot 3C_r \cdot 2 \left(V_{in} - \frac{\Delta V_1}{2}\right)^2 \quad E_{\text{consumed}} = E_1 - E_2$$

$$E_3 = \frac{1}{2} \cdot 2C_r \cdot 3 \left(V_{in} - \frac{\Delta V_1}{2}\right)^2$$

$$E_4 = \frac{1}{2} \cdot 2C_r \cdot 3 \left(V_{in} - \frac{\Delta V_1}{2} - \frac{\Delta V_2}{3}\right)^2 \quad E_{\text{consumed}} = E_3 - E_4$$

$$E_5 = \frac{1}{2} \cdot C_r \cdot 6 \left(V_{in} - \frac{\Delta V_1}{2} - \frac{\Delta V_2}{3}\right)^2$$

$$E_6 = \frac{1}{2} \cdot C_r \cdot 6 \left(V_{in} - \frac{\Delta V_1}{2} - \frac{\Delta V_2}{3} - \frac{\Delta V_3}{6}\right)^2 \quad E_{\text{consumed}} = E_5 - E_6$$

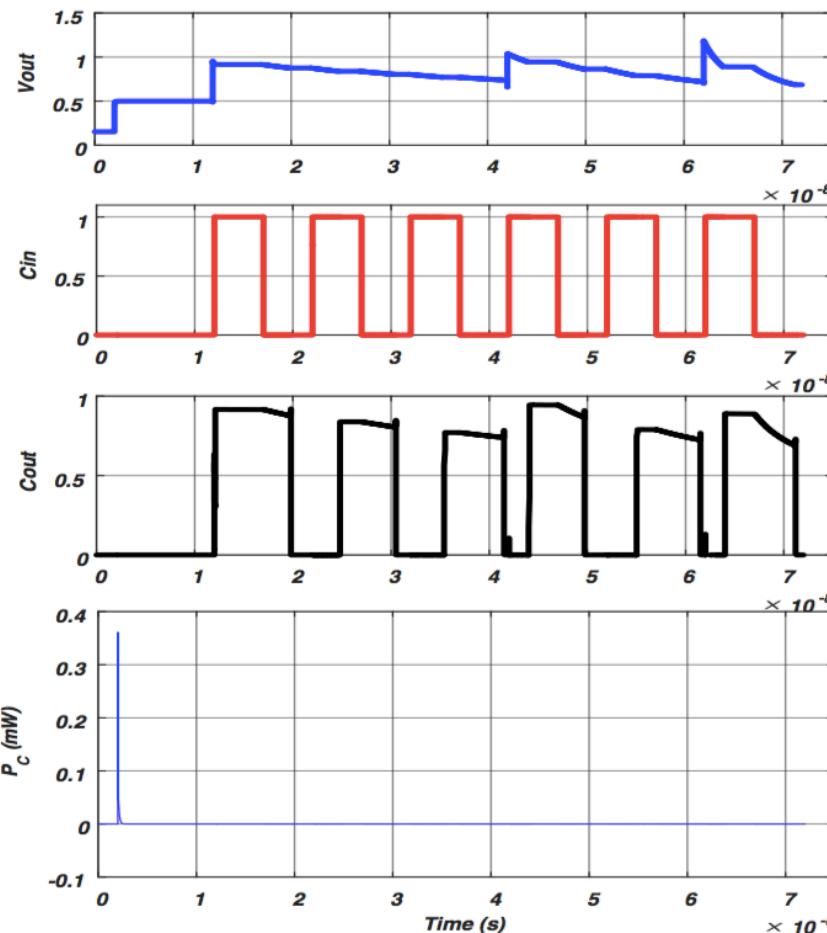
❖ Energy Recycling Step3:

❖ General Form of Remaining Energy :  $E_n = \frac{1}{2} \cdot C_r \cdot N \left(V_{in} - \sum_{i=1}^n \frac{\Delta V_i}{S_i}\right)^2$

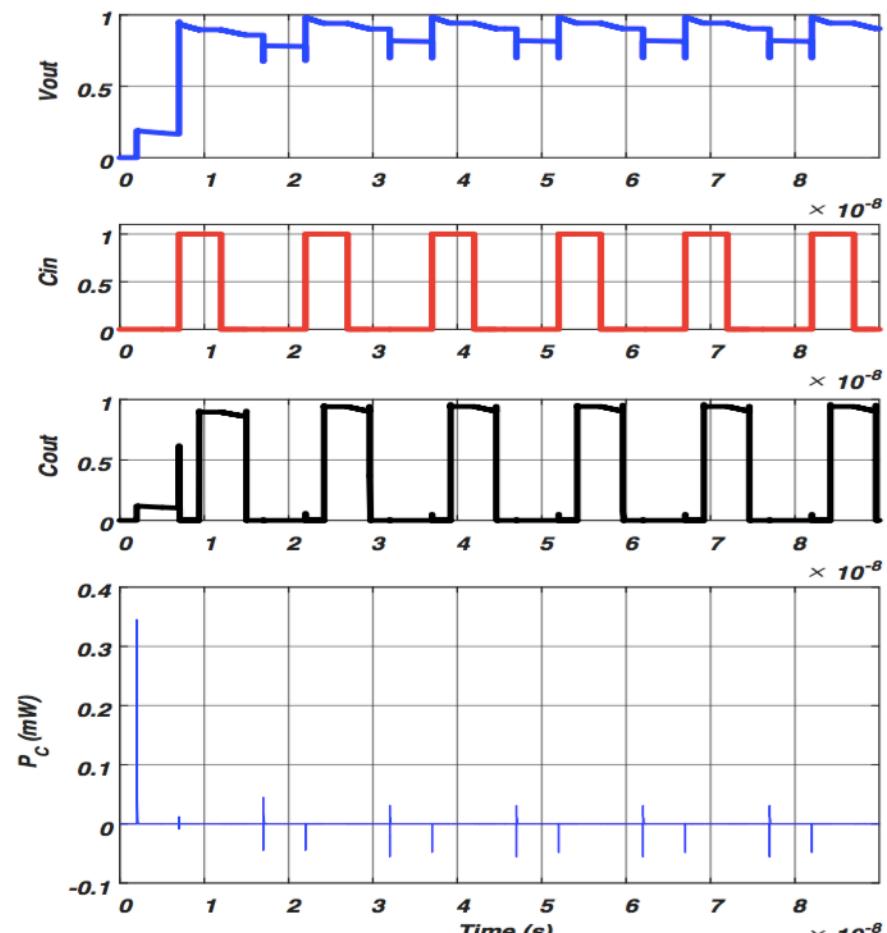
# SIMULATION RESULTS OF ENERGY RECYCLING STEPS

- Simulation results with an active period of 6 addition operations followed by a long sleep period

❖ Energy Recycling Voltage Converter



❖ Conventional Voltage Converter



# VIABILITY OF MEMS SWITCHES IN SC DC-DC CONVERTER FOR SHORT ACTIVE PERIOD CHARGE & RECYCLE (LIGHT LOAD)

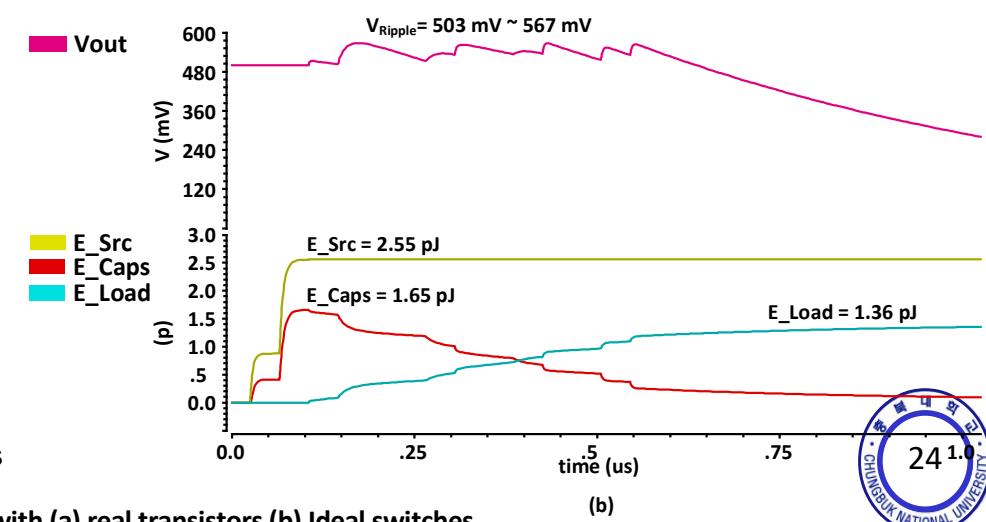
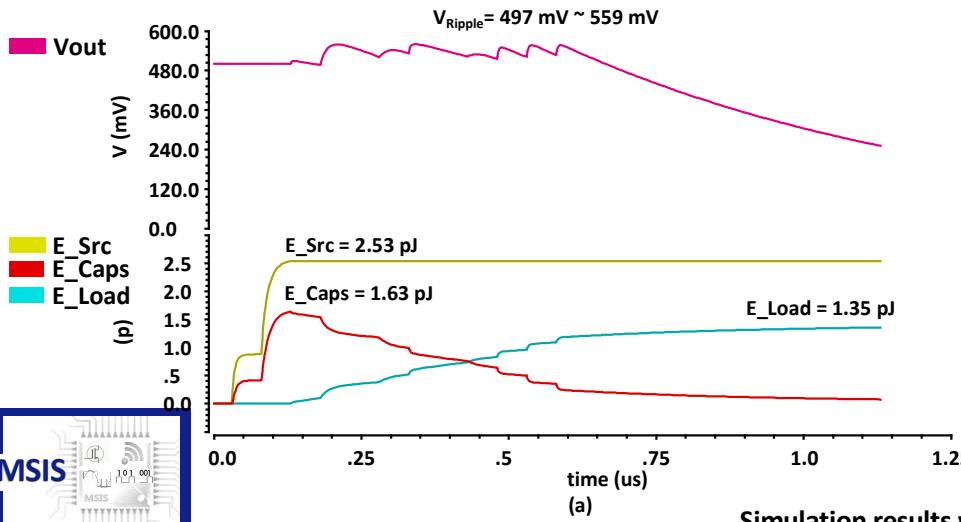
- Fig. compares the simulation results for MOSFET and MEMS switches at the input and output of the proposed architecture.
- MOSFET Switches
  - Charging Efficiency = 64.42 %.
  - Recycling Efficiency = 82.82 %.
- MEMS Switches
  - Charging Efficiency = 64.70 %.
  - Recycling Efficiency = 82.42 %.

$$C_{cap} = 8 \text{ pF}$$

$$Load = 125 \text{ k}\Omega, 4 \text{ pF}$$

$$V_{in} = 800 \text{ mV}, V_{out} = 500 \text{ mV}$$

$$R_{on,ideal} = 2 \text{ m}\Omega$$



Simulation results with (a) real transistors (b) Ideal switches.

# VIABILITY OF MEMS SWITCHES IN SC DC-DC CONVERTER FOR SHORT ACTIVE PERIOD CHARGE & RECYCLE (HEAVY LOAD)

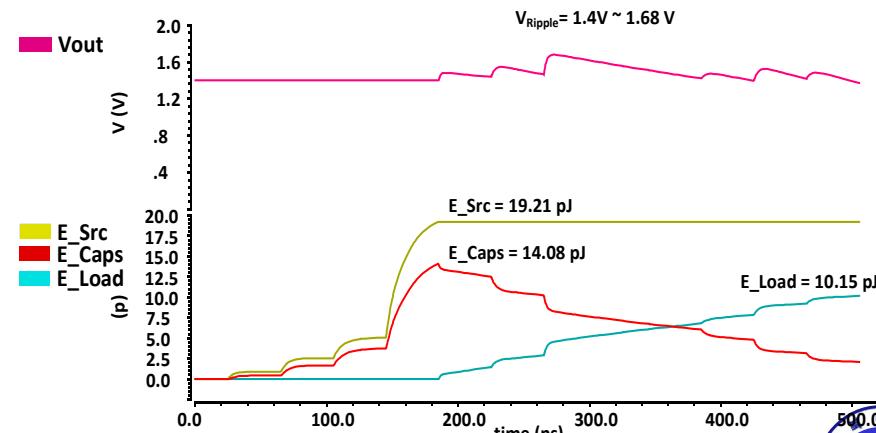
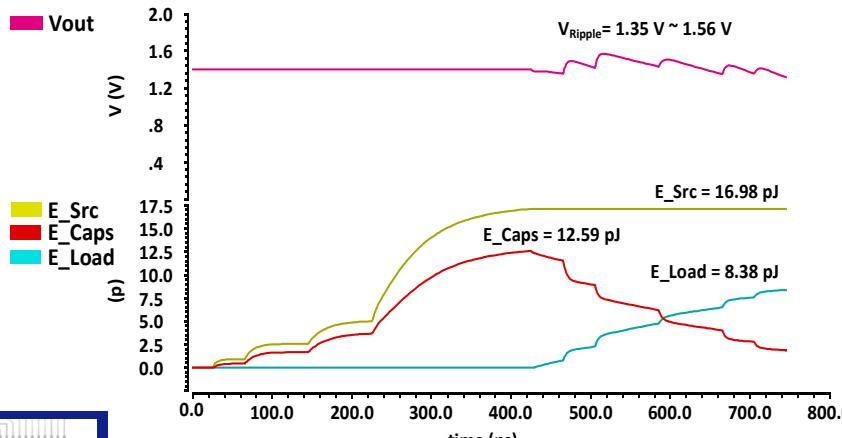
- Fig. compares the simulation results for MOSFET and MEMS switches at the input and output of the proposed architecture.
- MOSFET Switches
  - Charging Efficiency = 74.41 %.
  - Recycling Efficiency = 66.56 %.
- MEMS Switches
  - Charging Efficiency = 73.29 %.
  - Recycling Efficiency = 72.08 %.

$$C_{cap} = 8 \text{ pF}$$

$$Load = 70 \text{ k}\Omega, 4 \text{ pF}$$

$$V_{in} = 800 \text{ mV}, V_{out} = 1.4 \text{ V}$$

$$R_{on,ideal} = 2 \text{ m}\Omega$$



Simulation results with (a) real transistors (b) Ideal switches.

# VIABILITY OF MEMS SWITCHES IN SC DC-DC CONVERTER

## -CONCLUSION

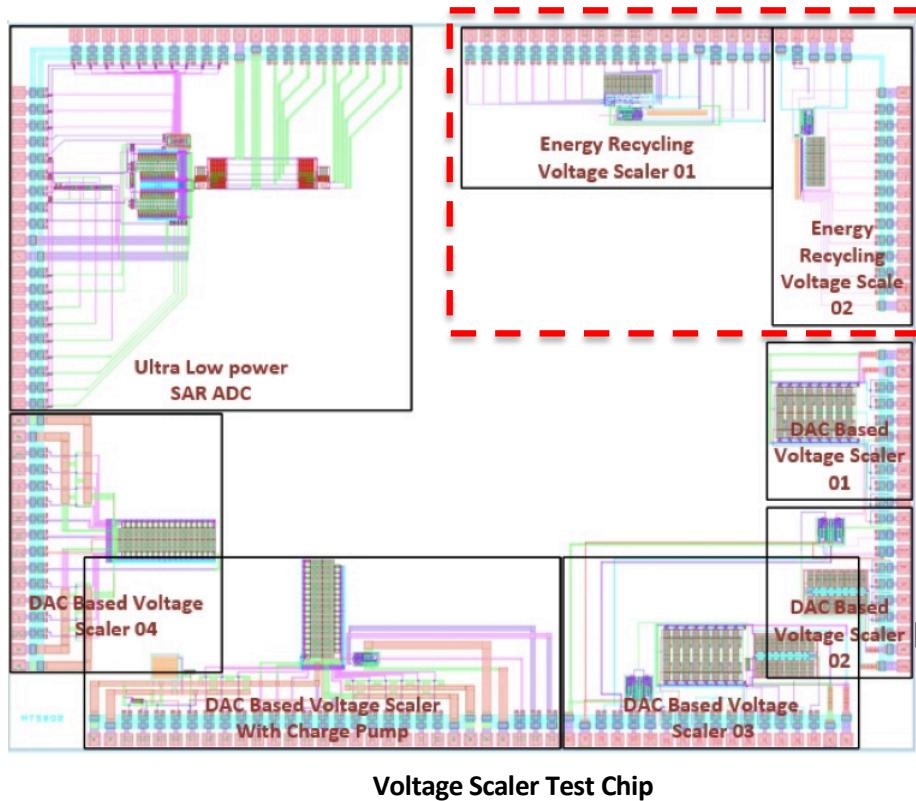
- Initial Charging
  - For charging capacitor bank using ideal switches will not give any additional benefits.
  - Because during charging a capacitor resistance ( $R$ ) doesn't impact energy.
- For Continuous phase
  - It shows improvement in energy efficiency
  - The charging is done quickly which reduces losses while delivery to load
- Energy Recycling
  - For Energy recycling for higher current (Heavy Load), we can have some improvements in efficiency.

However, a much higher operating frequency of the MEMS switches is needed

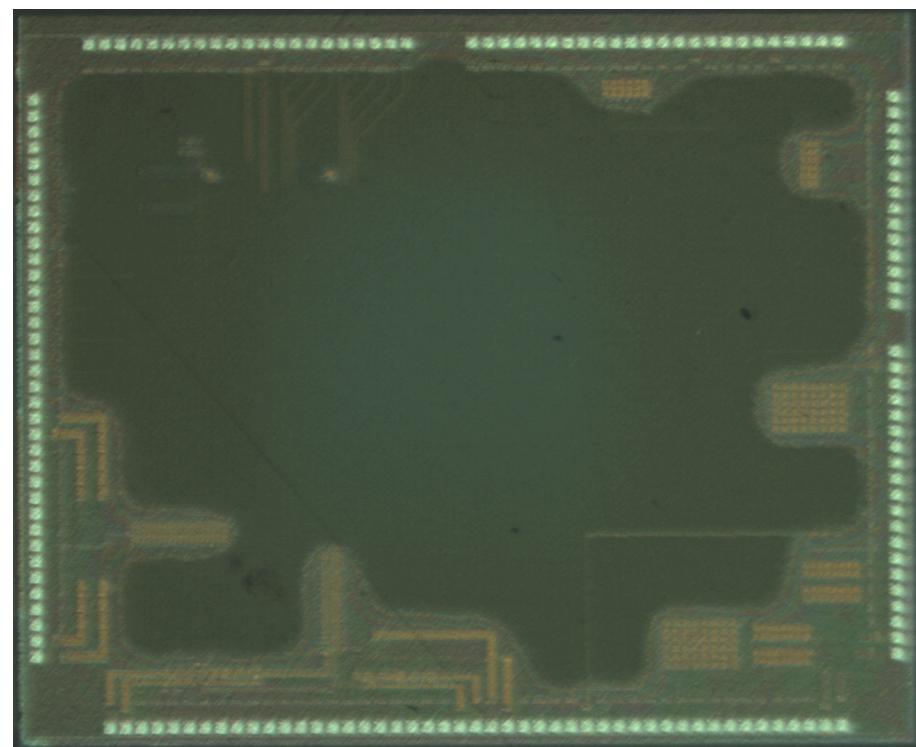
- To make them useable in low power circuits

# VOLTAGE SCALER TEST CHIP MPW

- MPW Process: Magnachip CMOS 0.13um 1.5V Vdd.
  - Chip Size 5x5mm



Voltage Scaler Test Chip



Voltage Scaler Test Chip