Design of a Frequency Division Concurrent Sine Wave Generator for an Efficient Touch Screen Controller SoC

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***Abstract*—This paper presents an interleaved sine wave generator using an efficient memory access technique for large touch screen controllers. It concurrently applies sine waves of different frequencies. The proposed circuit improves the speed of touch detection and reduces the chip area compared with conventional analog oscillators. The range of sine wave frequencies and the gap between each of frequencies can be configured by adjusting the address calculation algorithm to fetch samples values stored in memory. Therefore it provides higher flexibility with configurable sine wave frequencies than conventional schemes. It also minimizes the memory size required to regenerate all the sine waves needed. The proposed architecture has been implemented the proposed sine wave generator in a touch screen controller with FPGA and analog front end board.**

Keywords—interleaved sine wave generator; touch screen; touch screen controller; mutual-capacitance; SoC;

I. INTRODUCTION

As touch screens are becoming increasingly popular, they are recently being adopted by even large display applications such as medical equipment, PC monitor, and TV screen [1]. Among many types of excitation signals employed for various touch screen detection methods, square wave pulses are most widely used. A recent method called FDCS (Frequency Division Concurrent Sensing) [2] concurrently applies sine waves of different frequencies as excitation signals. It then detects the touch positions by analyzing the FFT (Fast Fourier Transform) of the sine waves. Since it generates all driving (TX) lines signals concurrently, it can provide a higher sensing rate and also higher detection accuracy especially for large touch screens. In this paper, we propose an efficient method of generating concurrent sine waves, which uses interleaved sine wave generation.

II. SINE WAVE GENERATION

A. Conventional generation

There are many types of sine wave oscillator circuits. Analog oscillators generate distortion free sine waves with high gain capabilities. However, they have serious drawback that one oscillator can generate only one sine wave. They also need large chip area due to the large number of resistors and capacitors. On the other hand, digital sine wave oscillator can generate multiples of sine waves with different frequencies. A digital sine generator generates address to the memory where the samples of sine wave are stored. Besides it consists of many generator blocks to generate a number of sine waves with different frequencies.

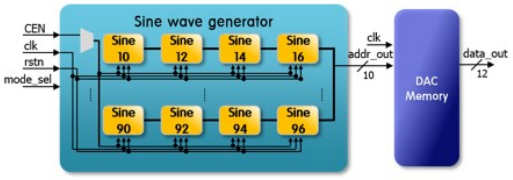

Fig. 1. Proposed scheme of interleaved sine wave generator

B. Proposed concurrent sine wave generator

Fig. 1 shows the proposed interleaved sine wave generator. It generates multiple sine waves for touch screen controller. One set of sine wave samples is pre-calculated and stored in the memory. Each sine wave of different frequency is generated by selecting a set of sine wave samples from the memory using following equation:

$$S_N(f_i) = S_{i\times N}(f_1) \qquad (1)$$

Here f_1 is the base frequency, and f_i is i-th generated frequency. $S_N(f_1)$ is the value of a sample (N) of the sine wave of a frequency. For example, suppose that we select the base frequency f_1 as 2 KHz, and the frequency increment as 2 KHz. Then the generated sine waves are f_2 = 4 KHz, f_3 = 6 KHz, f_4 = 8 KHz, and so on. All sine waves of f_i can be generated using one set of sine wave samples data in the memory. For example, the memory keeps sine wave samples only for one period of 2 KHz sine wave. A set of samples are selected for each frequency by an address generator circuit, which calculates the addresses of the memory based on (1). The number of samples for a certain frequency f_i is given by:

$$\frac{f_i}{f_1} = \frac{N_i}{N_1} \qquad (2)$$

The sampling frequency used to fetch data from the memory and drive DAC is given by:

$$f_s = f_1 \times N_S \times N_{TX} \qquad (3)$$

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Here Ns is the number of samples stored in the memory and N_{TX} is the number of TX lines.

Equation (2) shows the ratio between the base frequency f_1 and f_i. For instance, set the f_1 as 2 KHz and the number of its data samples, N_1, 256. Once f_i is 10 KHz, we only use about 51 samples for N_1 based on (2). Moreover with only 256 samples stored in the memory, we can generate 50 KHz with 10 samples.

Equation (3) shows sampling frequency required to fetch data from the memory and feed to TX lines. For example, a touch screen with 10 TX lines uses generated frequencies ranging from 2 KHz to 20 KHz. With 256 samples stored in the memory, 20 KHz sine wave uses 25 samples which are a reasonable resolution and the sampling frequency is 5.12 MHz which is also a reasonable sampling frequency for DAC.

III. Experiment Result

We implemented the proposed concurrent sine wave generator using Verilog HDL, and a Xilinx FPGA, xc7z020 as a part of touch screen controller [2]. We also implemented Analog Front-end (AFE) board and tested the performance of touch screen controller. Fig. 2 is a measurement result of oscilloscope that shows two sine waves of different frequency, 10 KHz, and 20 KHz. We calculated Signal-to-Noise Ratio (SNR) of sine waves with two frequencies that are generated by the proposed circuit implemented. The average SNR of the two sine waves was 41.34dB. TABLE I compares an analog oscillator, a conventional digital oscillator [3], and the proposed sine wave generator. It shows the estimated chip area, flexibility for changing frequency, memory efficiency, and memory size.

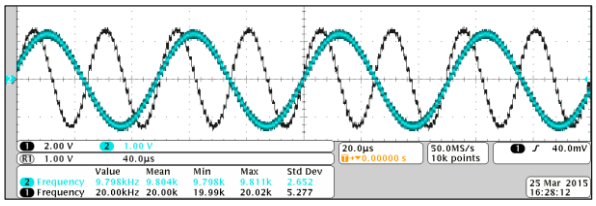

Fig. 2. Implemented block measurement result of oscilloscope

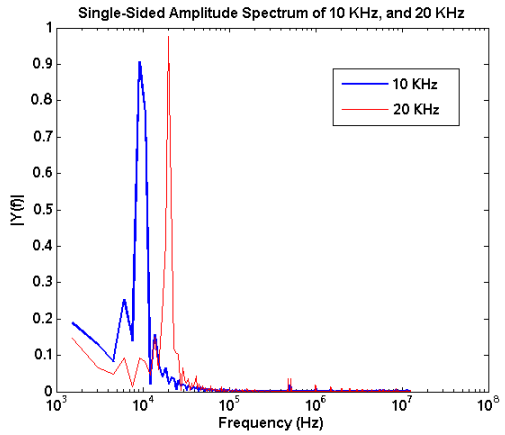

Fig. 3. Single-sided amplitude spectrum of 10 KHz, and 20 KHz sine

IV. Conclusion

In this paper, a concurrent sine wave generation circuit has been proposed. The proposed solution enables the generation of many sine wave with different frequencies using one sine wave generator. The proposed scheme provides much lower area costs, and higher flexibility with configurable sine wave frequencies than conventional schemes. It also ensures synchronization of all the sine waves for accurate touch detection. The proposed circuit needs only one set of samples for sine wave to generate all frequencies in the same time. Thus it can significantly reduce the memory size. The range of sine wave's frequencies and the gap between each of frequencies can be configured by readjusting the sampled data stored in memory and the sampling frequency. Measurement results show 41.34dB SNR for generated frequencies ranging from 2 KHz to 20 KHz.

Acknowledgment

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TABLE I. Comparison of conventional analog oscillators, sine generator [4], and the proposed circuit

Classification	Conventional analog oscillator [3]	Conventional sine generator [4]	The proposed sine generator
Flexibility for varying frequency	Fixed	Flexible	Flexible
Memory size	No memory used	Very large memory $N_{data\ width} \times N_{FFT\ points} \times N_{TX}$	Small memory $N_{data\ width} \times N_{FFT\ points}$
Estimation area	Very large $\simeq N_{tx} \times 21{,}900\ um^2$ * (varies depending on TX line count)	Large $\simeq N_{tx} \times 111{,}420\ um^2$ ** (including memory) (varies depending on TX line count)	Small $\simeq 111{,}420\ um^2$ (including memory) (Fixed area)

*This oscillator is for 1.59 KHz Wein-bridge oscillator fabricated in 0.18um CMOS technology [3].
**This circuit is used by our architecture which is implemented in 0.18um CMOS technology [4].