New FFT Design with Enhanced Scan Rate for Frequency Division Concurrent Sensing of Mutual-Capacitance Touch Screens

Gyeongseop Choi, M.G.A. Mohamed and HyungWon Kim
School of Electrical Engineering and Computer Science, Chungbuk National University, Cheongju, South Korea
Email: {gschoi, mgamohamed, hwkim}@cbnu.ac.kr

***Abstract*— As the touch screens become larger and demand higher resolution, various concurrent sensing methods have been developed for higher scanning speed and performance. One of such fast detection methods called the frequency division concurrent sensing (FDCS) employs an FFT to distinguish concurrent driving sine waves of different frequencies. In this paper, we propose a new FFT architecture and design, which can further improve the speed of the FDCS based controller for large mutual capacitance touch screens. The proposed FFT is used to increase the frame scan rate without duplicating sensing circuit. It uses only half the cycle of the driving signals to reconstruct the complete cycle of the signals, and so it can convert the signals to the complete frequency domain data. This paper shows that the proposed FFT architecture can double the frame scan rate with negligible loss in signal to noise ratio (SNR) and small area overhead.**

Keywords*— Touch screen; Fast fourier transform (FFT); Controller; Mutual-capacitance; Frequency division concurrent sensing.

I. INTRODUCTION

Recently capacitive touch screen panels (TSPs) with mutual capacitance type are widely used not only for mobile devices, but also for large size screens. Many scanning techniques have been developed for mutual-capacitance TSPs. Recently the frequency division concurrent sensing (FDCS) technique [1] has been proposed to improve frame scan rate and signal to noise ratio (SNR) to scan large TSPs. It concurrently drives sine waves for all driving (TX) lines, while sequentially senses all sensing (RX) lines using Fast Fourier Transform (FFT). [2]

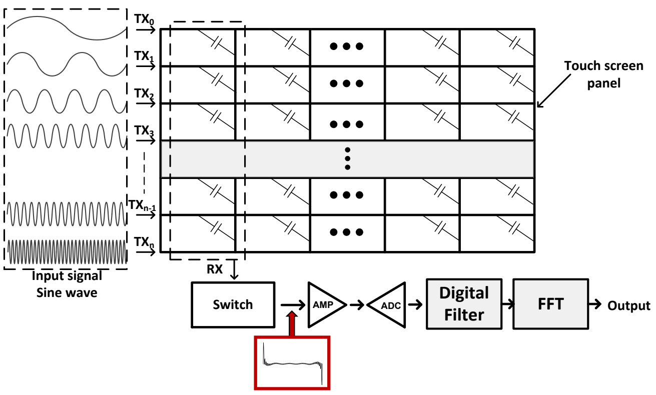


Fig. 1. FDCS touch screen scanning system

This research was supported by the MSIP Korea, under the Human Resource Development Project for SoC (NIPA-2014-H0601-14-1001).

Most conventional methods try to increase the frame scan rate by duplicating sensing circuits to enable concurrent sensing of multiple cells. Such methods, however, often incur high hardware overhead. In contract, this paper proposes a new FFT architecture for FDCS technique, which improves the frame scan rate by reducing the required time to scan one sensing line, and requires negligible hardware overhead.

II. FREQUENCY DIVISION CONCURRENT SENSING (FDCS)

The frequency Division Concurrent Sensing (FDCS) technique has been developed to speed up the detection process of projected mutual capacitance TSPs. An FDCS-based controller drives sine waves with different frequencies to all TX lines and senses RX lines sequentially. FDCS employs an FFT, which converts the RX output signals to frequency domain and detects the amplitude changes at the frequency of all driven sine waves. Therefore all the touch points on each RX line are determined concurrently. Fig.1. shows an FDCS touch screen detection system.

For example, to scan a commercial 23-inches touch screen panel with 44 TX lines and 78 RX lines, the FDCS system applies 44 sine waves of orthogonal frequencies. All these sine waves are summed up in each Rx line as passing through the

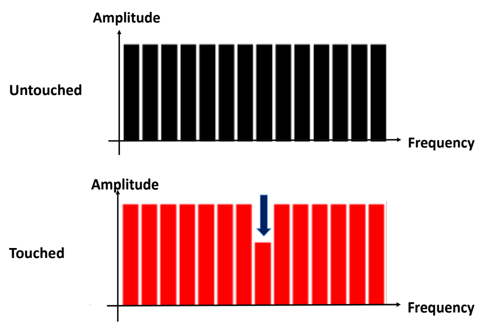


Fig. 2. Touched and no-touch cases after FFT result

TSP. One RX line is selected at a time, whose output signal is amplified and sampled by an ADC. This signal then is converted to the frequency domain by FFT. We can detect the changes in all mutual capacitance over the selected RX line by measuring the changes in amplitudes of corresponding frequencies of the sine waves. For instance, Fig. 2 shows that for a touched cell, the amplitude at the corresponding frequency decreases.

III. Proposed FFT Architecture

In the FDCS technique, the frequency range of input signal is limited by the frequency response (transfer function) of touch screen panel (TSP). Thus the frame scan rate is also limited. Sine waves of higher range of frequencies cannot be selected because TSP behaves as a band pass filter. Therefore a naive way for increasing the frame scan rate is using multiple sensing circuits, analog-to-digital (ADC) converters, and FFTs. This method, however, tends to incur a high area overhead.

a) Output signal characteristics

For accurate frequency analysis, an FFT needs to take as input the sine waves of a full period or multiple periods. If an FFT receives input signal with length less than one period, it results in wrong Fourier transform for the signal. To overcome this restriction, we propose an FFT architecture, which needs only half period of the input signal and still gives accurate frequency analysis.

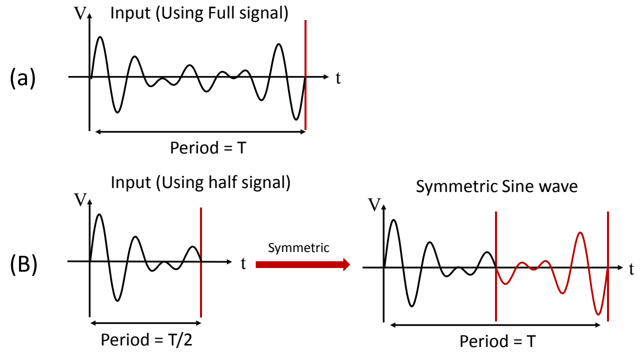


Fig. 3. (a) One period of RX output signal (b) Recover of RX output signal by reading half-period of the signal and using it for generating the second-half

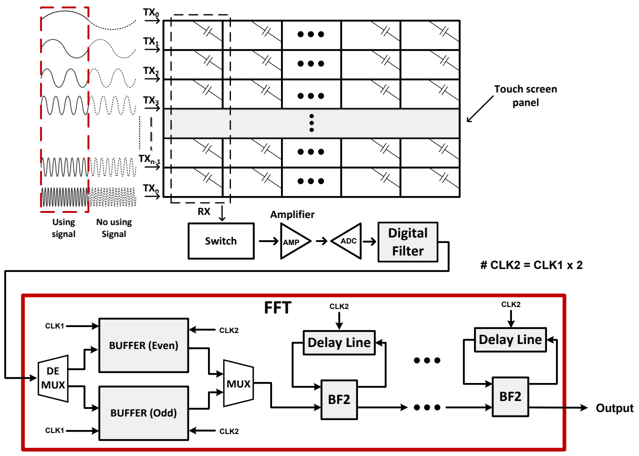


Fig. 4. New FFT architecture to restore symmetric RX output signal

The propose technique recovers the full period of signal from the half period of the input signal using the symmetry property of the sinusoids. Fig.3. shows the symmetry of RX output signal and how we can generate full signal from half-period signal by flipping the first half. Using only half-period of RX signals doubles the scan rate of FDCS.

b) FFT architecture

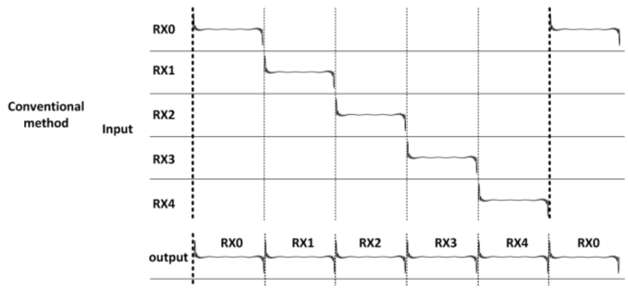
Our proposed FFT uses single delay path FFT architecture for its small area. We add two buffers for storing both half-periods of the signal. One is Even-Buffer for even Rx line (ex. Rx0, Rx2, …), the other is Odd-Buffer for odd Rx line (ex. Rx1, Rx3, …). Different pointers are used for reading and writing operations as shown in Fig. 4. Reading and writing in the buffer are done in two different speeds. The read pointers are two times faster than write pointers to enable reading the next input signal at the same time as writing the first half-period.

c) Frame Scan rate improvement

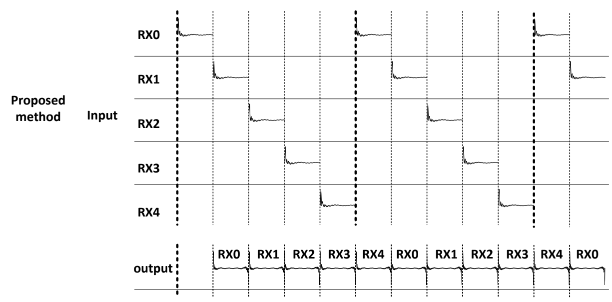
For conventional FDCS, the frame scan rate is given by:

$$Frame\ scan\ rate\ = \frac{1}{T_{Period} \times N_{RX}} \qquad (1)$$

Here T_{period} is the period of RX output signal, and N_{RX} is the number of Rx lines. To increase the scan rate, we may try to reduce the period of RX signal by increasing the frequency of the input signal. However, it may not be possible to increase input frequency because of the limited frequency range for TSP.



(a)



(b)

Fig. 5. Reading operation of RX output signals in (a) conventional FDCS (b) proposed architecture

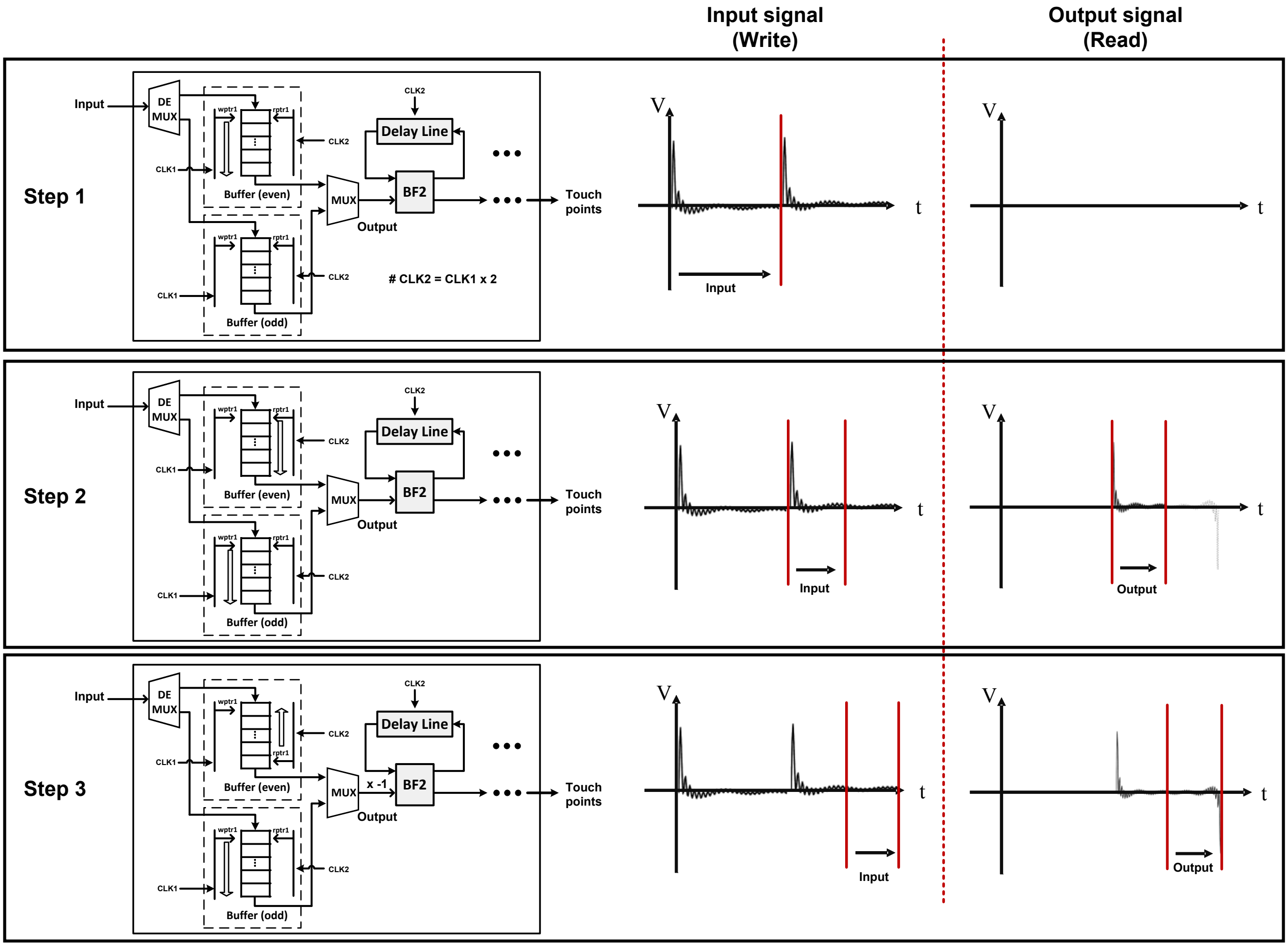


Fig. 6. The process of new FFT design using symmetric signal restoring FFT

Instead, our proposed technique uses the signal of only half-period to enhance the Frame scan rate.

$$Frame\ scan\ rate\ (proposed) = \frac{1}{(T_{period}\,/\,2)\times N_{RX}} = \frac{2}{T_{period}\times N_{RX}} \quad (2)$$

The frame rate of Eq. (2) is 2 times of EQ(1). Fig. 5 shows repeated signal cycles for the case of conventional FFT (a), and the case of the proposed FFT used for FDCS system.

b) Process of the New FFT design

Fig. 6 shows the operations of the proposed technique in three steps:

Step 1) All sine waves are applied to all TX lines, and one RX line is selected. The RX output signal is stored in Even-Buffer. And then, save input data following write pointer. Write data of half signals. .

Step 2) After receiving the data of the selected RX line, Odd-Buffer is activated to store the data of the next RX line. At the same time, the data of the first RX line is read from Even Buffer. Through this process the read pointer is two times faster than the write pointer to feed one period of the first RX output signal to the butter-fly block.

Step 3) To reconstruct the complete period of RX signal, the read point sweeps the buffer twice: once by incrementing it, and then by decrementing it.

By repeating the above steps, we can reconstruct the complete RX signals in the half cycle of one period, and so doubling the scan rate.

IV. Implementation Result

We implemented the FDCS system using a conventional FFT and also the proposed FFT architecture in a silicon chip using CMOS 65nm process. As shown in table I, the proposed FFT has a negligible (3.4%) area overhead compared with the conventional FFT, while it gives twice faster scan rate.

The simulation experiment shows that reconstructing the full RX output signal from its half-period signal results in only 3dB loss in SNR compared with conventional scheme. This loss was a result of using identical halves of the signal with the same noise distribution.

TABLE I. MEASUREMENT OF IMPLEMENTED RESULT

Method	**Area(um2)**	**The number of gates**	**Signal to Noise (SNR)**			***Frame scan rate***
			Max (dB)	***Min (dB)***	***Avg(dB)***	
Conventional	127046.1	66170	33.1820	4.6255	24.8874	128.20
Proposed	130159.1	68260	29.7202	6.1159	21.3868	248.40

We tested the proposed architecture using a 23-inch commercial TSP with 44 TX lines and 78 RX lines. Using sine waves with frequency range from 10 kHz to 96 kHz, the proposed FFT provided a scan rate of 248.2 Hz while the conventional FFT gives a scan rate of 128.2 Hz.

V. CONCLUSION

This paper presented a new architecture of FFT for FDCS touch screen controller system, which increase the frame scan rate by reconstructing the symmetrical signals. We have implemented the proposed FFT architecture for FDCS touch screen controller SoC using 65nm CMOS process. The simulation experiments have shown that the proposed FFT provides 2 times higher frame scan rate than the conventional FFT. We also have shown that it has very small SNR loss (3dB) and negligible area overhead. Therefore the proposed FFT architecture can be considered as an effective solution to increasing the touch detection speed for large touch screens whose transfer function often restricts the signal frequency range.

REFERENCES

[1] I. Seo, T.W. Cho, H.G. Jang, S. Lee, H.W. Kim, “Frequency Domain Concurrent Sensing Technique for Large Touch Screen Panels”, Institute of Electronics Engineers of Korea fall (IEEK Fall)., pp. 55-58, Nov. 2013.

[2] J.H.Kim, M.G.A.Mohamed, H.W.Kim“Design of a Frequency Division Concurrent sine wave generator for an dfficient touch screen controller SoC”, International Symposium of Consumer Electronics (ISCE), IEEE , Jun.2015

[3] KAIST, Daejeon, Korea, Zinitix, Daejeon, Korea; Seunghoon Ko, Hyungcheol Shin , Hongjae Jang , Ilhyun Yun , Kwyro Lee1 ; “A 70dB SNR capacitive touch screen panel readout IC using capacitorless trans-impedance amplifier and coded Orthogonal Frequency Division Multiple Sensing scheme”, 2013 Symposium on VLSI Circuits (VLSIC 2013), pp.C216-C217, IEEE, Kyoto, Japan, June 2013

[4] Dongmin Won, HyungWon Kim, "Touch Screen Sensing Circuit with Rotating Auto-Zeroing Offset Cancellation", Journal of information andcommunication convergence engineering (JICCE), 2015 Accepted for Publication

[5] G.Choi, M.G.A.Mohamed, H.W.Kim, “Distributed architecture of touch screen controller SoC for large touch screen panels,” Proceedings of the International SoC Design Conference (ISOCC ’ 14), pp.22–23, IEEE, Jeju, Korea, November 2014.