[A. pen IC] FFT-32 Hardware module.

Abstract:

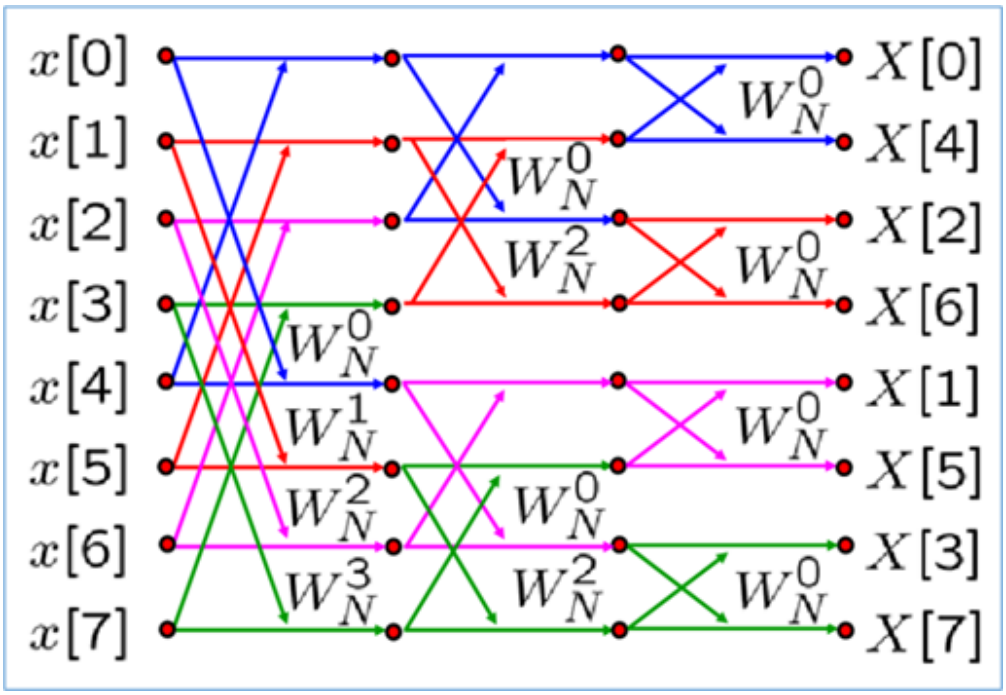
This article, I present the hardware module implementation of Fast Fourier transform (FFT).

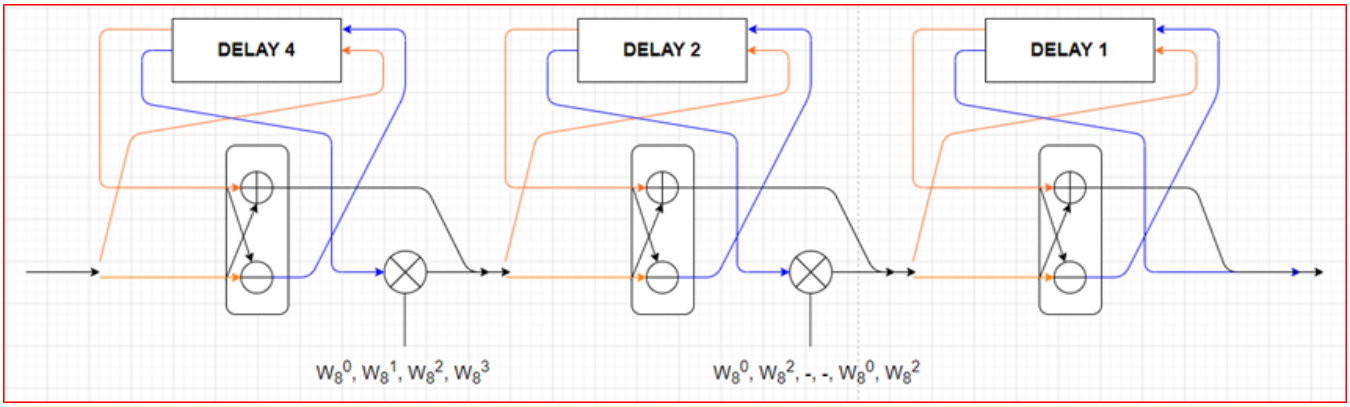
First, the FFT algorithm is explained in detail. Next, the design of constant values (Twiddle factors) are done by MATLAB.

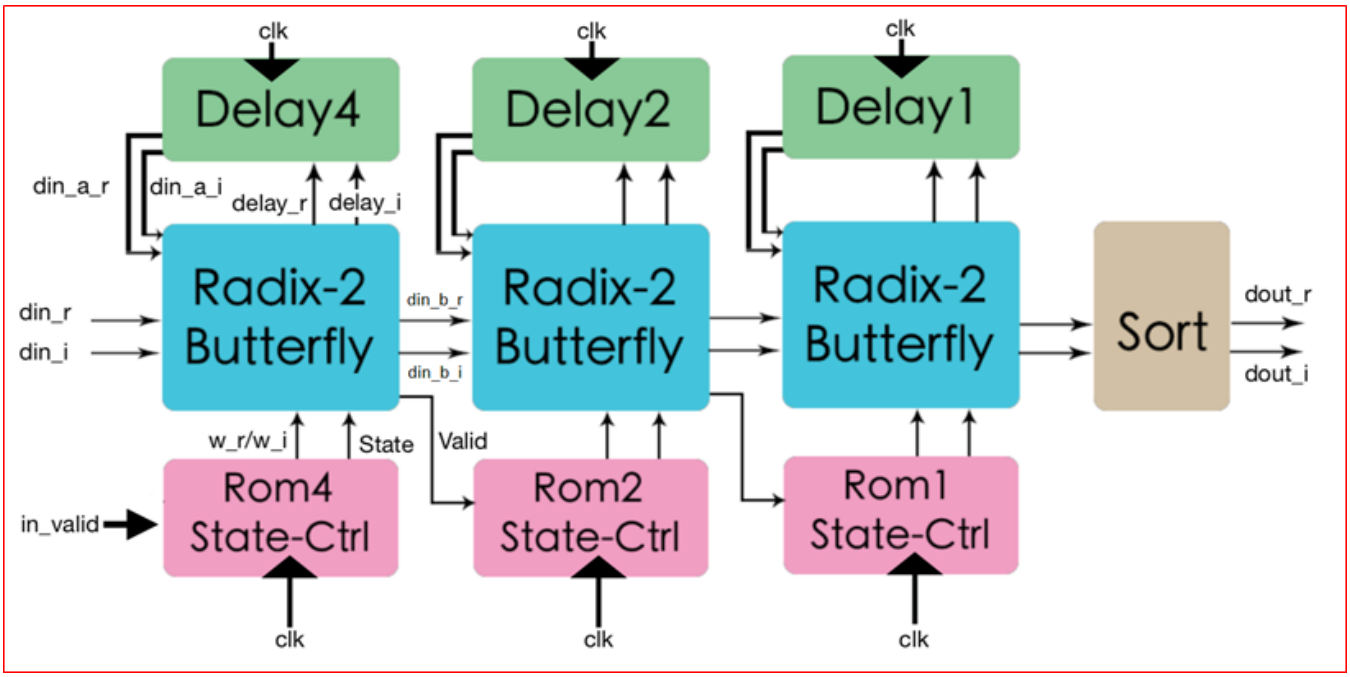
Finally, the throughput performance is analyzed in mathematical and compared with a test-bench result.

Following FFT HW module parameters will be used through the article.

- FFT length: 32.
- FFT algorithm: Decimation-in-frequency (DIF) Radix-2 Butterfly FFT.
- Processor architecture: Single-path delay-feed back (SDF) pipeline processor architecture.





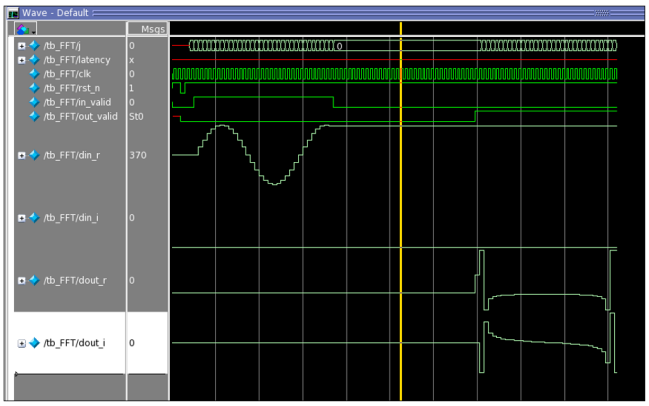


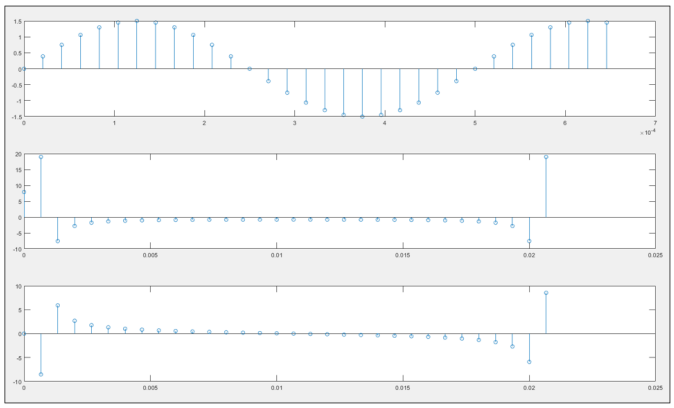
Outline:

The outline of attachment is as follows,

- The role and position of FFT HW module.
- Mathematical analysis of DFT FFT.
- Explanation of DIF radix-2 butterfly FFT algorithm.
- Explanation of a simple FFT processor architecture: specified for 8 points FFT.
- Explanation of SDF pipeline processor architecture: specified for 8 points FFT.
- Twiddle factors, Reordering modules are designed by attached MATLAB scripts.
- Sub modules:
  - Radix-2 butterfly: **radix2.v**.
  - ROM modules: **ROM_2.v, ROM_4.v, ROM_8.v, ROM_16.v**
  - Shift modules: **shift_1.v, shift_2.v, shift_4.v, shift_8.v, shift_16.v**.
  - Top module: **FFT.v**
  - Test bench: **FFT_tb.v.**

FFT_RTLviewer.pdf





G2touch_D2cente..._FPGA_v4.2.pptx


FFT_tb.v


FFT.v


radix2.v


ROM_2.v


ROM_4.v


ROM_8.v


ROM_16.v


shift_1.v


shift_2.v


shift_4.v


shift_8.v


shift_16.v


FFT_32_N...Order1.m


FFT_Numb...result.m


FFT-ROM_...esults.m

BRs,

SoC, mducng