

# Introduction of Chanung Lee

# Where am I From?

## ◆ FADU ( 1 Year 7 Months )

- Enterprise SSD Controller
  - PCIe Gen4
  - NVMe 1.4a

## ◆ RAON-TECH ( 3 Years 10 Months )

- Micro LCoS Display Panel
  - Various Size ( 0.36", 0.5", 0.55", 0.7" ~ ) and Resolution ( HD,FHD,QHD )
- Micro LCoS Display Controller
  - Support various input video interfaces (MIPI DSI, OpenLDI, and LVCMOS RGB) and formats
  - Stand-alone display (User-defined bitmap & text for OSD)
  - Low-power up-scaler
  - Various **DSP functions** (Histogram stretching, Content adaptive dynamic dimming, Digital gamma, etc.)
  - Ultra low power consumption with embedded frame buffer (SRAM)

## ◆ ETRI RTL(A-to-Z) 설계전문교육 ( 10 Weeks )

- RTL designer training course, From concept to FPGA verification
  - **IR communication module**
  - **WIFI FFT module**
- 우수 교육생 표창

## ◆ 청주대학교 전자공학과 ( 4 Years )

- 8bit CISC,RISC MCU design 과목 수료
- microprocessor 동호회 스마프 활동

# What I have done

Project	Description	Year	Job	Process	Where
EverXXX	Enterprise SSD Controller	2020	Digital Top과 RISCv Core의 설계 검증	12nm	FADU
RDP80XXX	0.8" Half-FHD OLED OS (1920 x 540)	2019	module RTL, FPGA 설계 및 검증	110nm	RAONTECH
Paper	Multi-Layer and Multi-function OSD for Microdisplay Systems	2018	<b>Chanung Lee</b> , Wook Hong, and Joon Goo Lee 1Research & Development Group of RAONTECH, Seongnam-si, Korea	IMID 2018 oral session (국제학회)	
RDC2XXX	LCoS Controller	2018	Sub module RTL, FPGA 설계 및 검증	55nm	
RDP3XXX	0.37" FHD LCoS Panel	2018	RTL, FPGA 설계 및 검증, Synthesis, STA	110nm	
RDP5XXX	0.5" HD LCoS Panel	2018	RTL 설계 및 검증	110nm	
RDP5XXX	0.55" FHD LCoS Panel	2018	RTL, FPGA 설계 및 검증	110nm	
RDP70XXX	0.7" SXGA uOLED Panel	2017	Synthesis, STA		
RDP7XXX	0.7" QHD LCoS Panel	2017	RTL 설계 및 검증	110nm	
RDP3XX	0.36" HD LCoS Panel	2017	RTL, FPGA 설계 및 검증	110nm	
RDP5XX	0.55" FHD LCoS Panel	2016	RTL, FPGA 설계 및 검증	110nm	
RB1XX	Force sensor	2016	Analog circuit emulation via FPGA		
RDC2XX	LCoS Controller	2015	RTL, FPGA 설계 및 검증	55nm	
<b>FFT</b>	<b>FFT module</b>	<b>2015</b>	<b>RTL 설계, simulation, FPGA 검증</b>		<b>ETRI</b>
<b>IR</b>	<b>IR communication</b>	2015	RTL 설계, simulation, FPGA 검증		
MCU	8bit RISC, CISC MCU	2014	RTL 설계, simulation		청주대학교

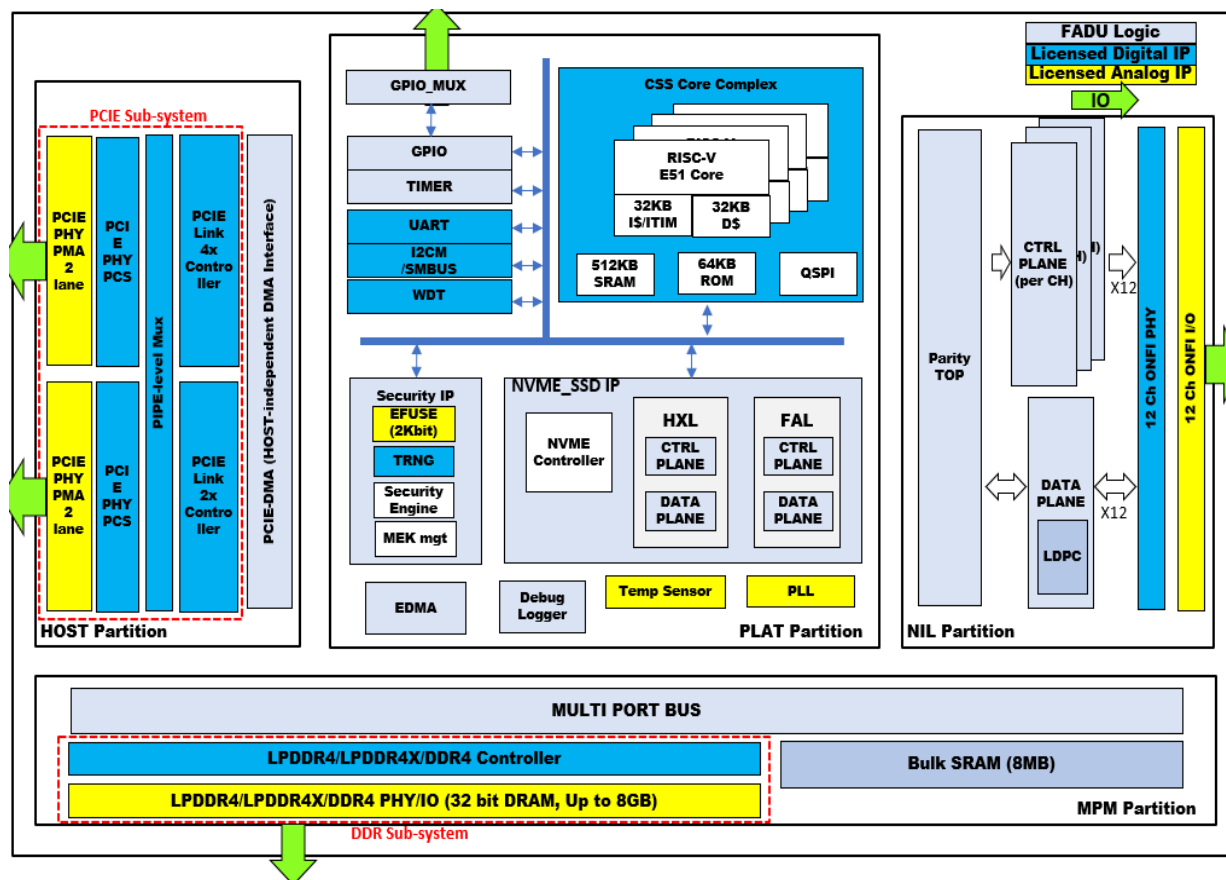
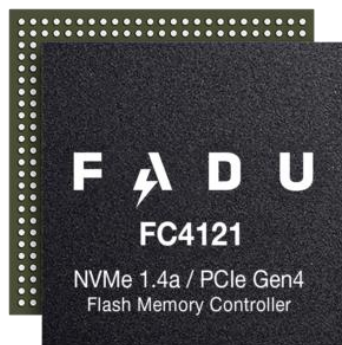
# Highlights - FADU

## Enterprise SSD Controller

- High Reliability
- Energy efficiency
- High clock speed

## Role :

- PLAT Partition



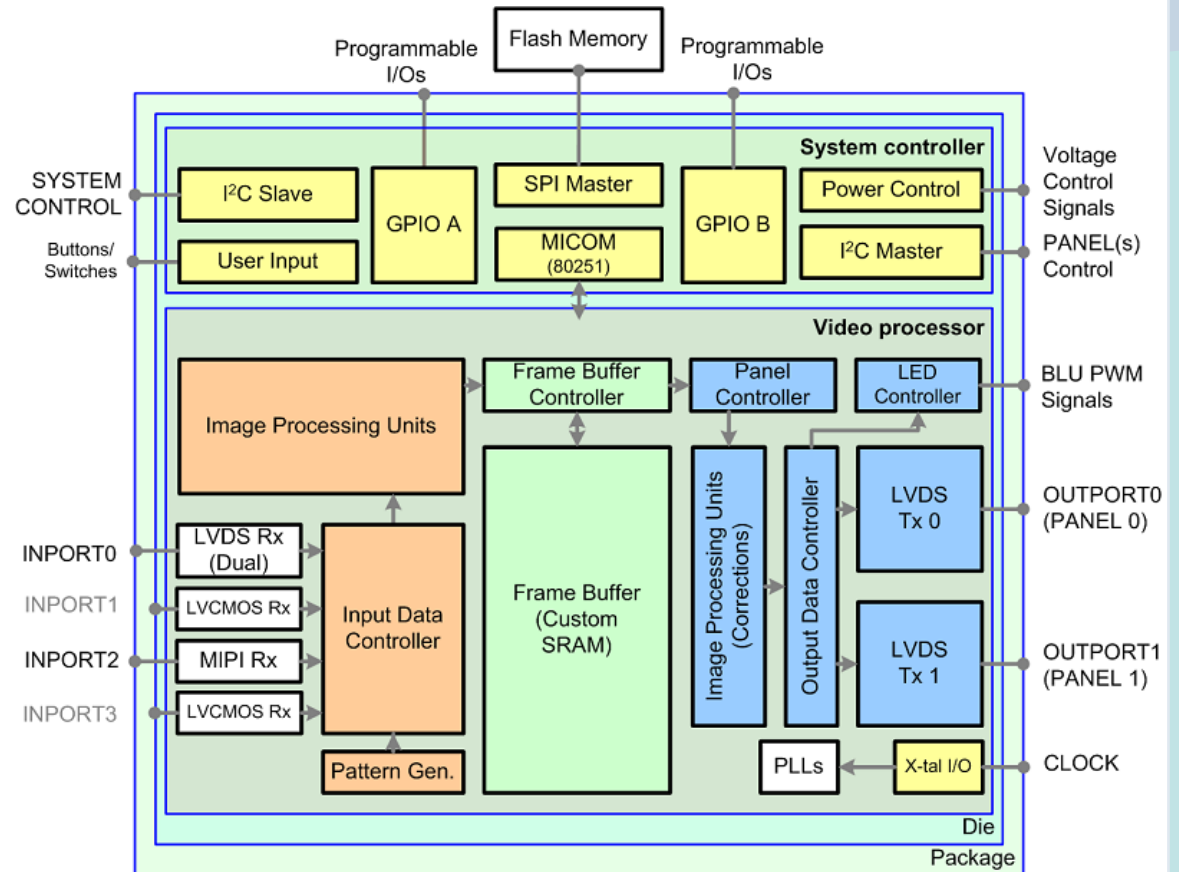
# Highlights - RAONTECH

## LCoS controller

- ASIC Display Driver IC
- **Image processing**
- High speed interface

## Role :

- OSD ( On Screen Display )
- **up-scaler**



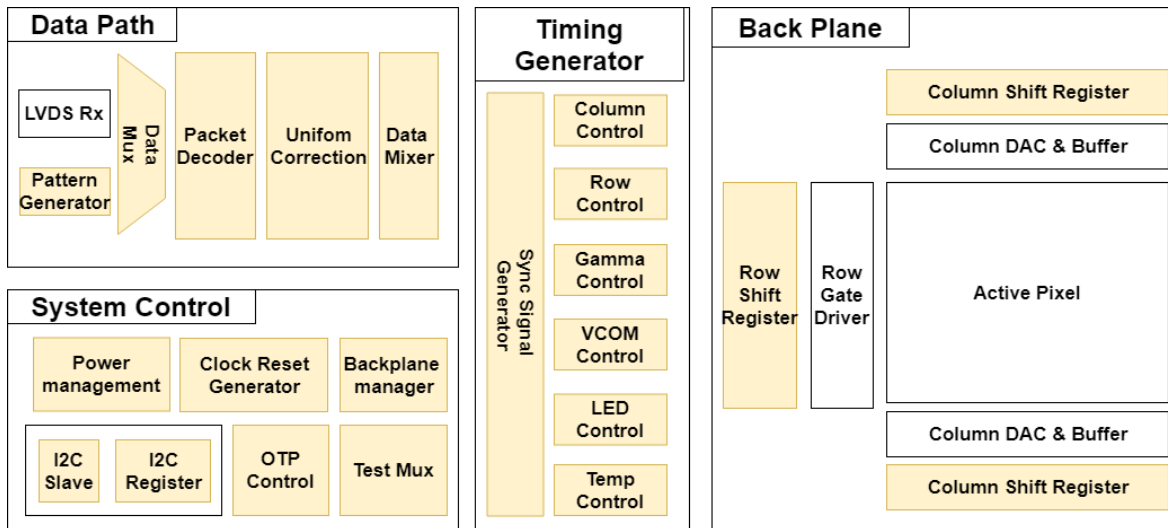
# Highlights - RAONTECH

## Microdisplay (LCoS) Panel

- Various size (0.36", 0.5", 0.55", 0.7") and resolution (HD, FHD, QHD)

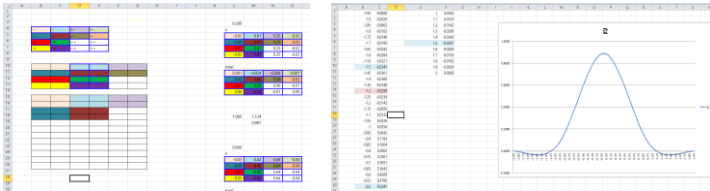
## Role :

- up-scaler

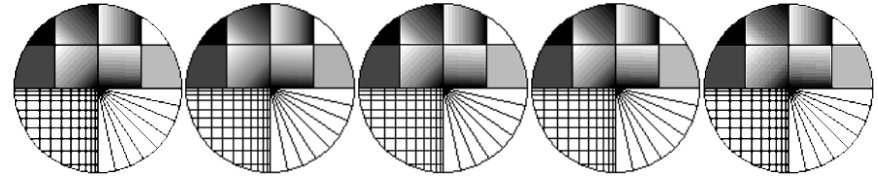


# Work Flow

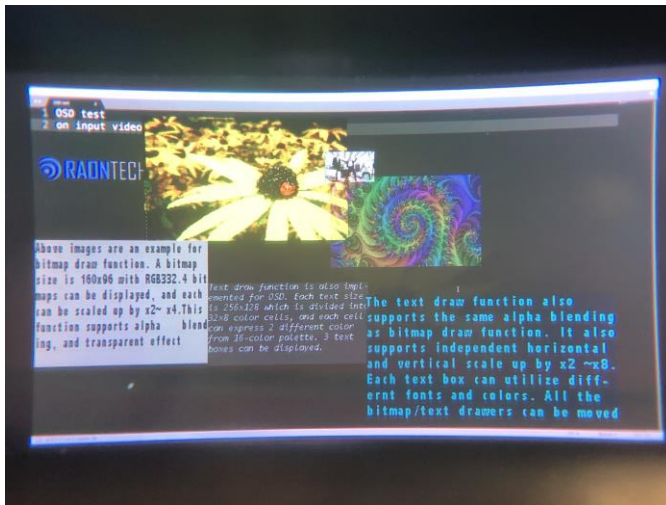
## Algorithm research & development



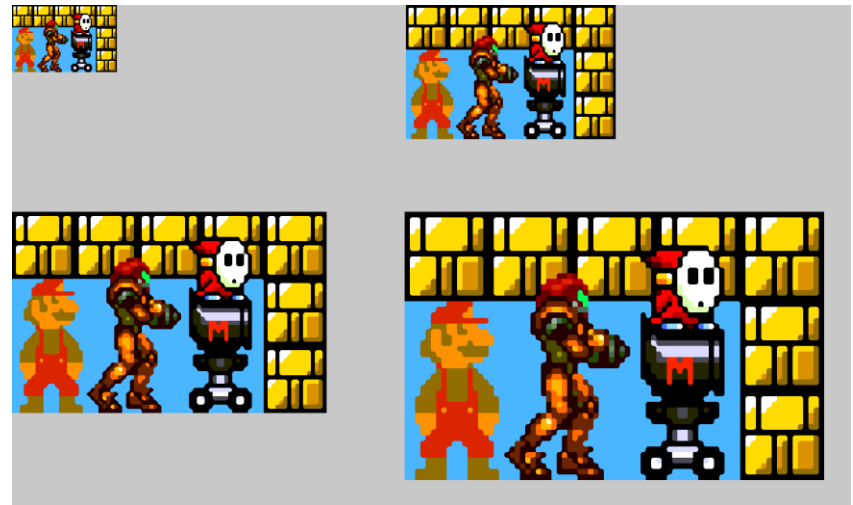
## High level language modeling ( Python or C )



## Synthesis, STA, Power-sim => Lab test



## RTL implementation , simulation



# ETRI

## IR Communication Module

통신 변조 방식 : OOK 변조

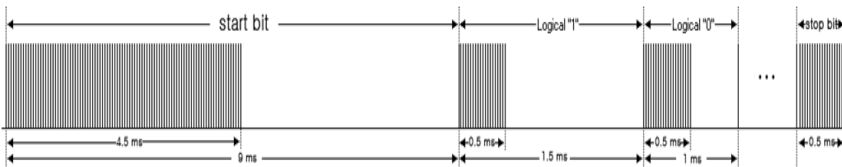
Operating Clock : 25Mhz

In / Out put bits : 8 bit / 8 bit

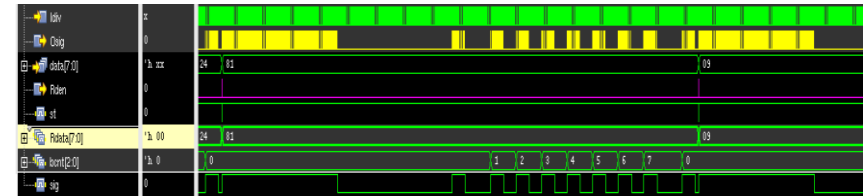
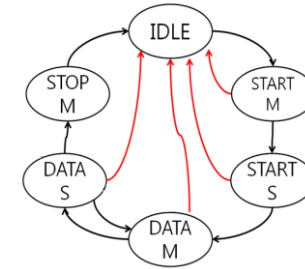
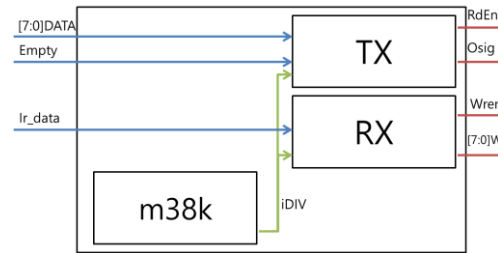
Carrier Frequency : 38Khz

Throughput : 0.5 Kbps

Data Format



IR TOP



## FFT WIFI Module

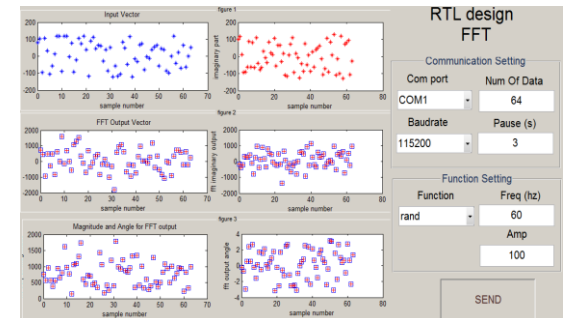
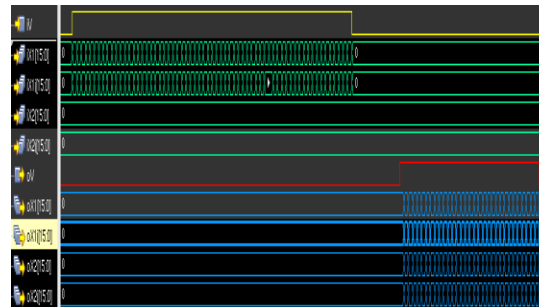
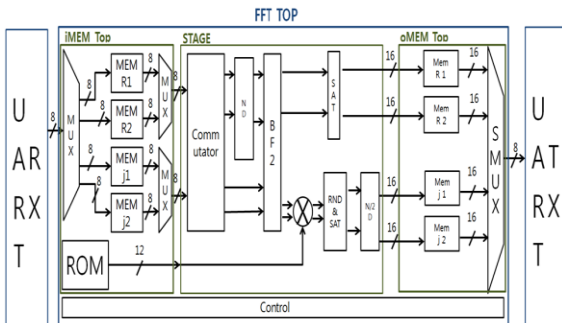
프로젝트 목표 : 64 Point DIF FFT

구현 알고리즘 : R2MDC

입/출력 비트 크기 : 8bit / 16 bit

Target Operating Clock : 25Mhz

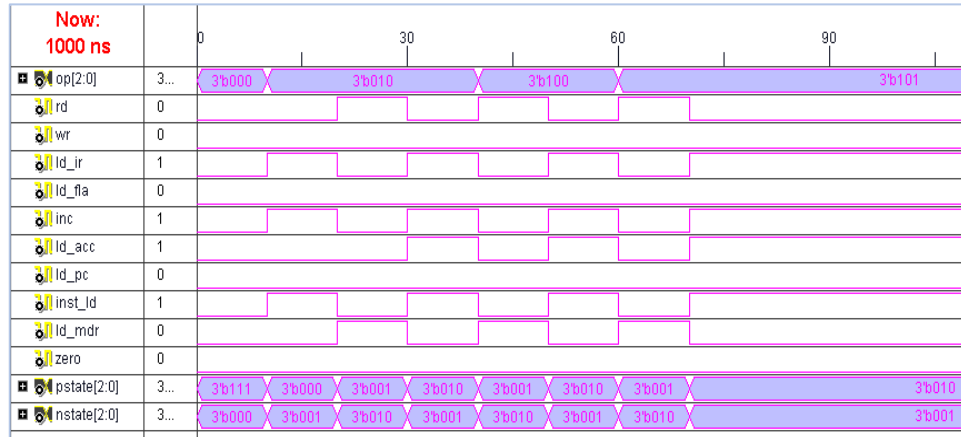
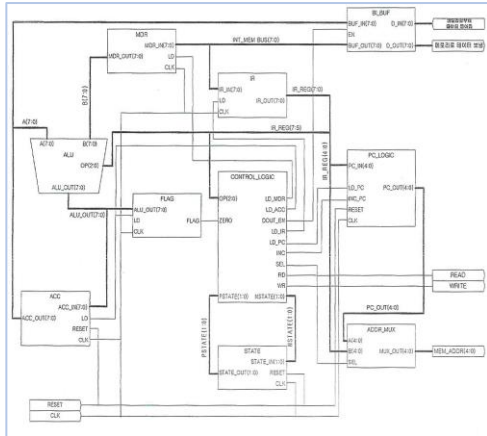
Throughput : 1 sample/clock





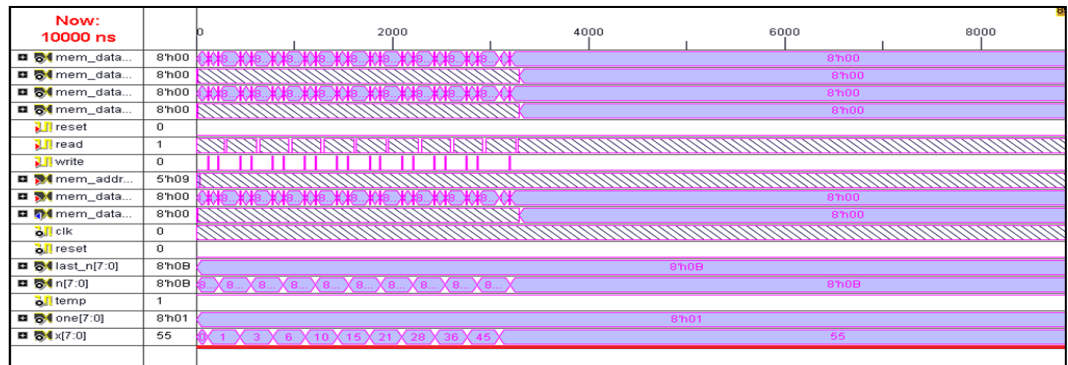
# University

## RISC block diagram & simulation wave



## RISC program run wave

메모리 주소	명령어	동작
00000	101	10000 Load X
00001	010	10001 Add N
00010	110	10000 Store X
00011	101	10001 Load N
00100	010	10011 Add one
00101	110	10001 Store N
00110	100	10010 Xor last_N
00111	001	00000 Skip if zero
01000	111	00000 Jump start
01001	000	00000 Halt
10000	000	00000 X
10001	000	00001 N
10010	000	01011 last_N
10011	000	00001 one



# IMID 2018

## Multi-Layer and Multi-function OSD for Microdisplay Systems

Chanung Lee, Wook Hong, and Joon Goo Lee

<sup>1</sup>Research & Development Group of RAONTECH, Seongnam-si, Korea

Tel.: 82-31-786-4621, E-mail: Joon.Lee@raon-tech.com

An on-screen display (OSD) is widely used by many display devices [1,2], since it is useful to display system information with and even without a video source. An OSD superimposes text and/or bitmap images on a screen, and thus a user can notice necessary details about system status. The most of display panels has offered OSD function by using its corresponding panel controller, however, they only provides simple limited functions. And it is rare to find the function in microdisplay systems in spite of usefulness. For better usability, we propose multi-layer OSD which has multitude additional features with limited resources. We design the OSD function in our panel controller to provide as many options as possible for various applications.

The OSD designed in the panel controller has two main modules. One is a bitmap renderer, and the other is a text renderer. The bitmap renderer can represent up to 4 different images, layer by layer, on an input video or a built-in test pattern image. Each bitmap is 160x96 size with RGB332 color depth, and the bitmap renderer supports individual x2 ~ x4 scaling up, 9-level alpha blending, and 3D mode for various applications. The text renderer is designed for overlaying characters, pictograms, or simple graphics on the top of the bitmap renderer's result, and it supports up to 3 individual text boxes. Each text box is 256x128 resolution which is divided into 32 columns by 8 rows of color cells, thus each cell size becomes 8x16, which is adequate for alphanumeric presentation. Fonts/pictograms can be extracted from a binary bitmap which size is the same as text box. Each of color cell can express up to two colors in a 16-color palette. Since each text box can use its own color palette and binary bitmap, and both of them are configurable, the text renderer provides a variety of options. The text renderer supports individual horizontal/vertical x2 ~ x8 scaling up, 9-level alpha blending for each of binary colors, and 3D mode as well. Both bitmap and text renderers are controllable via I<sup>2</sup>C communication path and embedded micro-computer, and each renderer can import bitmap images, or binary font data and color palettes from an SPI Flash memory to target look-up tables to use them.

Fig. 1 shows our proposal, multi-layer OSD, as a conceptual image, and its result view for an example. On the example, an FHD liquid crystal on silicon (LCoS) panel is used, and it displays 4 different bitmap images with various sizes and alpha blending modes, and 3 text boxes having different contents with various setting.



Fig. 1. A conceptual display manner for proposed OSD, and an example view on an FHD LCoS panel.

In this paper, we proposed multi-layer and multi-function OSD which can be used for various purposes, such as information display, multi-language subtitle, AR application, watermark, and so on. We implemented and fabricated the OSD as an application specific integrated circuits (ASIC), and verified all the functionalities we designed.

### Acknowledgment

### References

1. Y. Li, "Design of application layer in HD digital TV," *CSAE*, Zhangjiajie, pp. 301-305 (2012)
2. Himax Technologies, Inc., *HX8852-A LCoS Display Controller with Interface Compliant to MIPI datasheet*

