Ring Oscillators

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Abstract

This report presents an analysis of ring oscillators, circuits commonly employed to generate clock signals in integrated circuits. It starts with a concise overview of the conditions necessary for oscillation and the relevant circuitry. The report then proceeds with separate analyses for the two distinct sizing of the inverters used. Various parameters within the circuitry, including the number of stages, passive impedance values, and MOSFET dimensions, are adjusted to examine their effects on the outputs. Theoretical analyses are included wherever applicable.

Introduction

A ring oscillator is a type of electronic oscillator commonly used in integrated circuits for generating clock signals, testing, and measuring performance metrics such as propagation delay and frequency. It consists of an odd number of inverting logic gates (e.g., NOT gates) connected in a series loop. The basic principle of operation relies on the propagation delay through each gate and the feedback loop creating a continuous oscillating signal.
When power is applied to the ring oscillator, the circuit begins to oscillate due to the inherent delays in the gates. The output voltage at each stage will alternate between high and low states, resulting in a periodic waveform. The frequency of this waveform can be approximated by the formula:

$$f = \frac{1}{2n \cdot t_p}$$

where:

- f is the oscillation frequency,
- n is the number of stages,
- t_p is the propagation delay of a single gate.

1 Conditions for Oscillations:Barkhausen Criterion

1.1 Theory

The basic topology of a harmonic oscillator, shown in Figure 1 . The open-loop amplifier gain, $A(s)$, and feedback return ratio, $f(s)$, are frequency selective. An input signal, $X_i(s)$, is shown in Figure 1 for the sake of analysis: oscillators do not require an input signal to generate a sinusoidal output waveform. In oscillator circuits, $X_o(s)$ is non-zero for $X_i(s) = 0$.

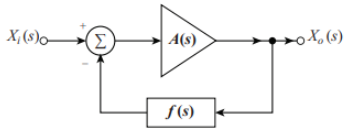


Figure 1: Basic topology of a harmonic oscillator.

The closed-loop gain of the circuit shown in Figure 1 is,

$$A_f(s) = \frac{A(s)}{1 + A(s)f(s)}, \quad (1)$$

where

$$A_f(s) = \frac{X_o(s)}{X_i(s)}.$$

The output signal is therefore,

$$X_o(s) = \frac{A(s)}{1 + A(s)f(s)} X_i(s). \quad (2)$$

In electronic oscillators, the circuit is not excited by an external time varying source: that is, the input signal $X_i(j\omega) = 0$. Therefore, for a non-zero output $X_o(s)$, Equation (2) must yield a loop gain $A(j\omega_0)f(j\omega_0) = -1$, at the frequency of oscillation, ω_0. This loop gain condition causes instability resulting in amplifier oscillation. The condition of unity loop gain with a 180° phase shift is called the Barkhausen criterion. The net phase shift considering the negative feedback is 360°. In order to achieve the requisite phase shift, reactive elements must be used in the feedback loop. Since the feedback element is reactive, the signal phase shift is invariably a function of frequency. This implies that there is only one frequency where the Barkhausen criterion is satisfied. Let us see the effect of the magnitude of the product $A\beta$ on the nature of the oscillations.

1. $|Af| > 1$: When the total phase shift around a loop is 0° or 360° and $|Af| > 1$, then the output oscillates but the oscillations are of growing type.

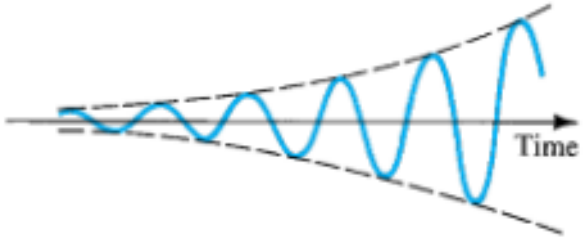


Figure 2: Growing type oscillation

2. $|Af| = 1$: When the total phase shift around a loop is 0° or 360° and $|Af| = 1$, then the oscillations are with constant frequency amplitude called sustained oscillations.

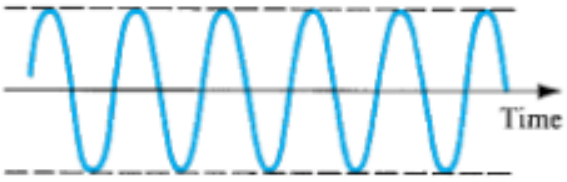


Figure 3: Sustained type oscillation

3. $|Af| < 1$: When the total phase shift around a loop is 0° or 360° and $|Af| < 1$, then the oscillations are with constant frequency amplitude called damped oscillations.

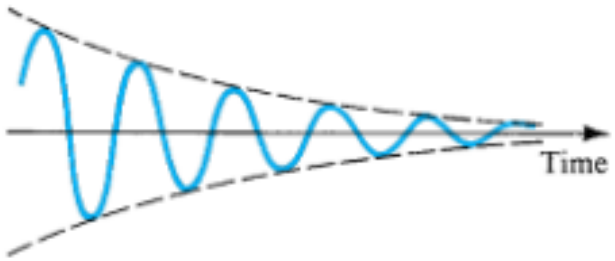


Figure 4: Damping type oscillation

2 CS-stage Ring Oscillator

2.1 1-Stage

2.1.1 Calculations

For a 1-stage ring oscillator, the general circuit is shown in the below figure:

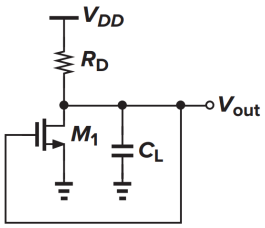


Figure 5: 1-stage CS ring oscillator.

The expressions for A and f are given by:

$$A = \frac{v_{ds}}{v_{gs}} = -g_m R_D \frac{1}{1 + j\omega C_L R_D}$$
$$f = 1$$
$$Af(j\omega) = -g_m R_D \frac{1}{1 + j\omega C_L R_D}$$

The natural frequency ω_0 is given by:

$$\omega_0 = \frac{1}{R_D \cdot C_L}$$

The phase angle ϕ is given by:

$$\phi = 180^\circ + \tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right)$$

The 180° comes from the negative sign of the gain.
The ϕ can go to a maximum value of 270° and a minimum value of 90°. So neither the 360° nor the 0° criteria can be met.Therefor, this system can't oscillate.

2.1.2 Implementation

Here is the implementation of the 1-stage ring oscillator on Cadence. Figure 6 show the inside contents of the symbol created, which is a CS amplifier design to have a gain of 2 at $V_{DD} = 3$.

The following figure shows the output for the simulation of the schematic in Figure 7.

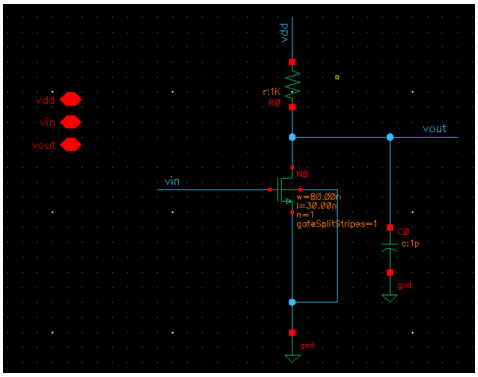


Figure 6: CS stage amplifier.

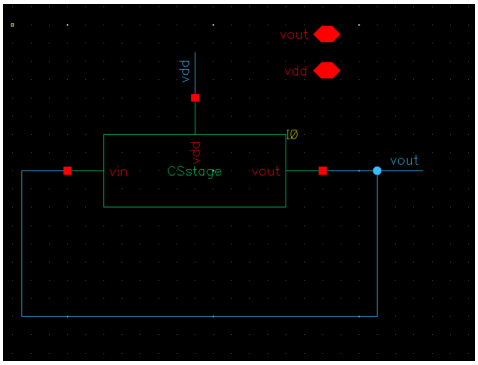


Figure 7: 1 stage oscillator.

Figure 8: Output waveform of 1 stage Oscillator.

As you can see there is no oscillation taking place.

2.2 2-Stage

2.2.1 Calculations

For a 2-stage ring oscillator, the general circuit is shown in the below figure:

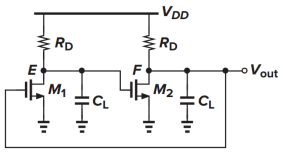


Figure 9: 2-stage CS ring oscillator.

The expressions for A and f are given by:

$$A = \frac{v_{ds}}{v_{gs}} = (g_m R_D)^2 \frac{1}{(1 + j\omega R_D C_L)^2}$$
$$f = 1$$
$$Af(j\omega) = (g_m R_D)^2 \frac{1}{(1 + j\omega R_D C_L)^2}$$

The natural frequency ω_0 is given by:

$$\omega_0 = \frac{1}{R_D \cdot C_L}$$

The phase angle ϕ is given by:

$$\phi = 2\tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right)$$

The ϕ can actually satisfy the $0°$ criteria . But, to have an oscillation frequency $\omega_{osc} \neq 0$, $\omega_0 \to \infty$ which means $R_D \to 0$, which would then affect the gain.Therefor this stage too won't give us any oscillations.

2.2.2 Implementation

Here is the implementation of the 2-stage ring oscillator on Cadence.

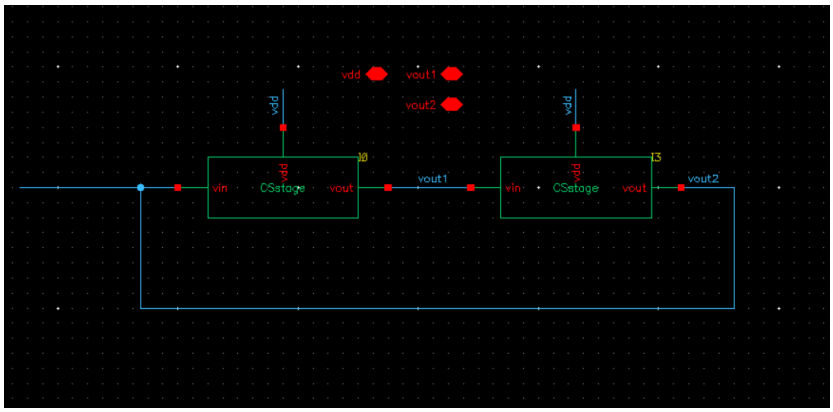


Figure 10: 2 stage oscillator.

Here is the following output for the above schematic

As you can see , there are no oscillations in the output.

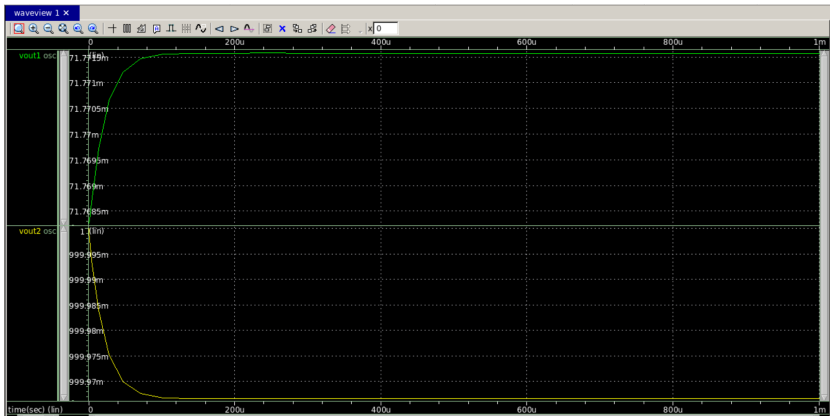


Figure 11: Output Waveform of 2-stage oscillator.

2.3 3-Stage

2.3.1 Calculations

For a 3-stage ring oscillator, the general circuit is shown in the below figure:

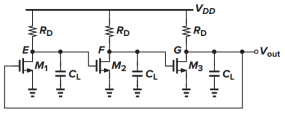


Figure 12: 3-stage CS ring oscillator.

The expressions for A and f are given by:

$$A = \frac{v_{ds}}{v_{gs}} = -\left(g_m R_D\right)^3 \frac{1}{\left(1 + j\omega R_D C_L\right)^3}$$

$$f = 1$$

$$Af(j\omega) = -\left(g_m R_D\right)^3 \frac{1}{\left(1 + j\omega R_D C_L\right)^3}$$

The natural frequency ω_0 is given by:

$$\omega_0 = \frac{1}{R_D \cdot C_L}$$

The phase angle ϕ is given by:

$$\phi = 180^\circ + 3\tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right)$$

The 180° comes from the negative sign of the gain.
The $3\tan^{-1}$ part has to be equal to 180° for the criteria to be satisfied , which means each stage needs to provide a phase shift of 60°, which is possible. This implies $\tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right) = 60^\circ$.Therefore $\omega_{osc} = \sqrt[2]{3}\omega_0$

Here, we can see that the start frequency is actually an achievable one. So, let's check for the magnitude criterion as well:

$$\frac{\left(g_m R_D\right)^3}{\left(\sqrt{1 + \left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right)^3} = 1 \implies g_m R_D = 2$$

This shows that the required DC gain of the CS amplifier must be 2, which I have already tuned it to . For a $V_{DD} = 3V$, corresponding values are $R_D = 20\text{k}\Omega$ and $C_L = 1\text{nF}$

2.3.2 Implementation

Here is the implementation of the 3-stage ring oscillator on Cadence.
Here is the following output for the above schematic

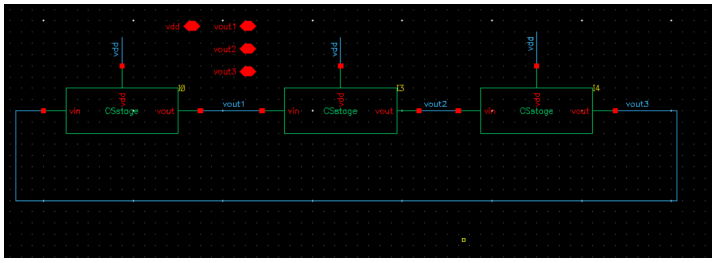


Figure 13: 3 stage oscillator.

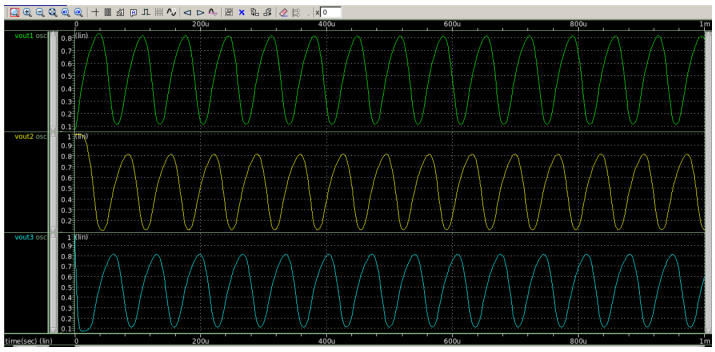


Figure 14: Output Waveform of 3-stage oscillator.

As we can see here, there are three different waves with the same frequency but have different phase at a particular point in time. I have calculated the frequency using a code in the input deck. The below figure consists the calculated data:

```
$DATA1 SOURCE='HSPICE' VERSION='O-2018.09-SP2 linux64' PARAM_COUNT=0
.TITLE ''
 time_period1     time_period2     time_period3     dly12_1
 dly12_2          dly12_3          dly13_1          dly13_2
 dly13_3          ph12_1           ph12_2           ph12_3
 ph13_1           ph13_2           ph13_3           freq1
 freq2            freq3            temper           alter#
  6.829e-05        6.843e-05        6.831e-05        4.802e-05
  4.548e-05        4.563e-05        2.494e-05        2.280e-05
  2.282e-05        2.532e+02        2.392e+02        2.405e+02
  1.315e+02        1.202e+02        1.203e+02        1.464e+04
  1.461e+04        1.464e+04        2.500e+01        1
~
~
```

Figure 15: Delays,Time Period and Frequency values.

As we can see the frequency f_{osc_p}=1.464 $\times$ 10^4.The theoretical oscillation frequency:

$$f_{osc} = \frac{1}{2\pi}\left(\frac{\sqrt{3}}{R_D C_L}\right)$$

f_{osc}=1.378 $\times$ 10^4. The frequency which I got appears to be more than the desired frequency. This might be due to the fact that, since oscillations are produced, the g_m values changes with time thereby varying the gain and causing non-idealities.

2.3.3 Input Deck

The input deck shows the sizing of the NFETs and the values of the components. It also shows how I have calulated certain values.

```
.TEMP 25.0
.OPTION
+    ARTIST=2
+    INGOLD=2
+    PARHIER=LOCAL
+    PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN
.include "osci_source"
.subckt CSstage vdd vin vout
xn0 vout vin 0 0 nfet w=1600e-9 l=500e-9 nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1
c0 vout 0 1e-9
r0 vout vdd 20e3
.ends CSstage

.param par_vdd=1

.tran 10p 1ms

.ic v(vout3)=par_vdd
*.ic v(vout2)=par_vdd
*.ic v(vout1)=par_vdd
v2 vdd 0 DC=par_vdd


**measuring the time period of the three signals
.meas tran time_period1
+trig v(vout1)='par_vdd*0.5' rise=2
+targ v(vout1)='par_vdd*0.5' rise=3

.meas tran time_period2
+trig v(vout2)='par_vdd*0.5' rise=2
+targ v(vout2)='par_vdd*0.5' rise=3

.meas tran time_period3
+trig v(vout3)='par_vdd*0.5' rise=2
+targ v(vout3)='par_vdd*0.5' rise=3
```

```
***measuring the time delay between vout1 and vout2
.meas tran dly12_1
+trig v(vout1)='par_vdd*0.5' rise=1
+targ v(vout2)='par_vdd*0.5' rise=1

.meas tran dly12_2
+trig v(vout1)='par_vdd*0.5' rise=2
+targ v(vout2)='par_vdd*0.5' rise=2

.meas tran dly12_3
+trig v(vout1)='par_vdd*0.5' rise=3
+targ v(vout2)='par_vdd*0.5' rise=3
****measuring the time delay between vout1 and vout3
.meas tran dly13_1
+trig v(vout1)='par_vdd*0.5' rise=1
+targ v(vout3)='par_vdd*0.5' rise=1

.meas tran dly13_2
+trig v(vout1)='par_vdd*0.5' rise=2
+targ v(vout3)='par_vdd*0.5' rise=2

.meas tran dly13_3
+trig v(vout1)='par_vdd*0.5' rise=3
+targ v(vout3)='par_vdd*0.5' rise=3

**calculating the phase difference between vout1 and vout2
.meas tran ph12_1 PARAM='360*freq1*dly12_1'
.meas tran ph12_2 PARAM='360*freq2*dly12_2'
.meas tran ph12_3 PARAM='360*freq1*dly12_3'
****calculating the phase difference between vout1 and vout3
.meas tran ph13_1 PARAM='360*freq3*dly13_1'
.meas tran ph13_2 PARAM='360*freq1*dly13_2'
.meas tran ph13_3 PARAM='360*freq3*dly13_3'
**calculating the frequency
.meas tran freq1 PARAM='1/time_period1'
.meas tran freq2 PARAM='1/time_period2'
.meas tran freq3 PARAM='1/time_period3'
.probe v(*)
.end
```

Figure 16: Input Deck

```
xi5 vdd vout1 vout2 CSstage
xi6 vdd vout2 vout3 CSstage
xi0 vdd vout3 vout1 CSstage
~
```

Figure 17: Source.

3 Inverter-Based Ring Oscillator

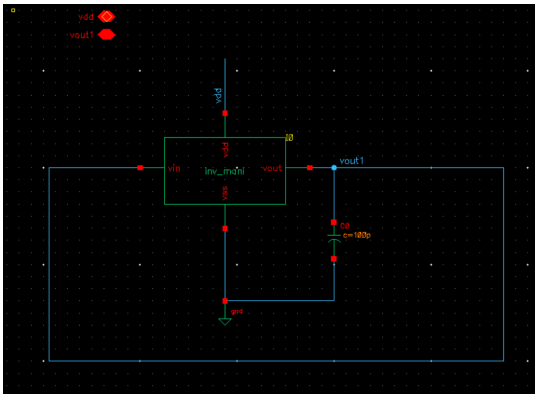
3.1 Input Deck

```
.meas tran time_period1
+trig v(vout1)='1' rise=1
+targ v(vout1)='1' rise=2

.meas tran time_period2
+trig v(vout1)='1' rise=3
+targ v(vout1)='1' rise=4

.meas tran time_period3
+trig v(vout1)='1' rise=5
+targ v(vout1)='1' rise=6

.meas tran dly11
+trig v(vout1)='ext_vdd*0.5' rise=1
+targ v(vout2)='ext_vdd*0.5' fall=1

.meas tran dly12
+trig v(vout1)='ext_vdd*0.5' fall=1
+targ v(vout2)='ext_vdd*0.5' rise=1

.meas tran dly21
+trig v(vout2)='ext_vdd*0.5' rise=1
+targ v(vout3)='ext_vdd*0.5' fall=1

.meas tran dly22
+trig v(vout2)='ext_vdd*0.5' fall=1
+targ v(vout3)='ext_vdd*0.5' rise=1
*.meas tran dly31
*+trig v(vout3)='ext_vdd*0.5' rise=1
*+targ v(vout4)='ext_vdd*0.5' fall=1

*.meas tran dly32
*+trig v(vout3)='ext_vdd*0.5' fall=1
*+targ v(vout4)='ext_vdd*0.5' rise=1

.meas tran freq1 PARAM='1/time_period1'
.meas tran freq2 PARAM='1/time_period2'
.meas tran freq3 PARAM='1/time_period3'

.probe v(*)
.end
```

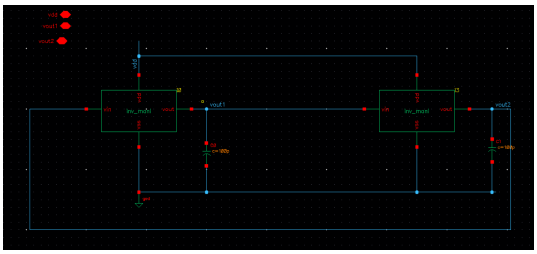
Figure 18: Input Deck

The input deck calculates the frequency , delays at each simulation.It also gives information of the sizings of the MOSFETs.
After conducting simulations across multiple stages, it's clear that the oscillator fails to operate with an even number of stages. Additionally, the oscillation frequency fluctuates with changes in the load capacitance. As the number of stages increases, the oscillations tend to resemble square waves more closely. This phenomenon arises because the signal delay accumulates with each additional inverter stage, requiring the signal to pass through N inverters for each update.**As the delay increases, the amplitude rises/falls until it is supposed to be inverted and it eventually reaches saturation/cut-off respectively. The frequency of the oscillation primarily depends on the achievable signal delay.**

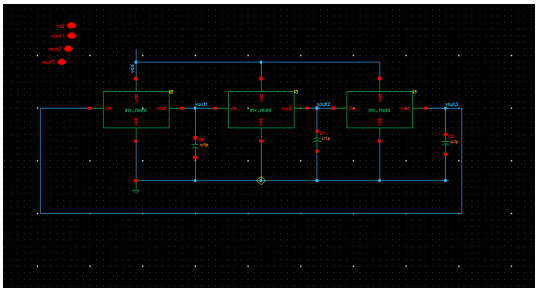
3.2 Some Oscillator Schematics



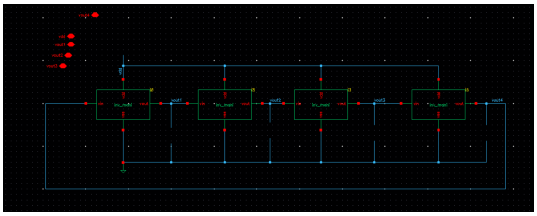
(a) 1-stage



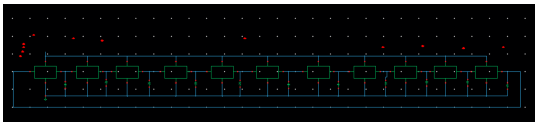
(b) 2-stage



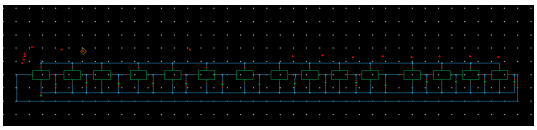
(a) 3-stage



(b) 4-stage



(a) 11-stage



(b) 15-stage

3.2.1 Output for even stage

Here is what the output waveform for an even stage oscillator looks like:

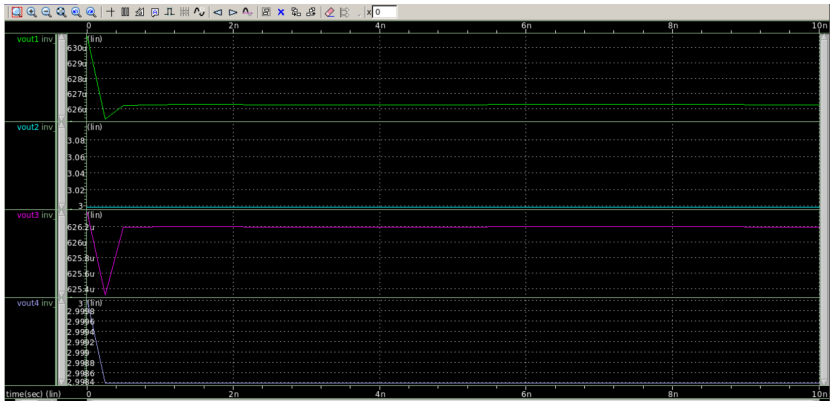


Figure 22: Output Waveform for even stage Ring Oscillator.

As we can see , it is apparent that the output of the inverters settle down near either 0V or V_{DD} alternatively.

Note:We don't get any oscillations for only 1 stage

3.2.2 Output for odd stages

Here is what the output waveform for an odd stage oscillator looks like:

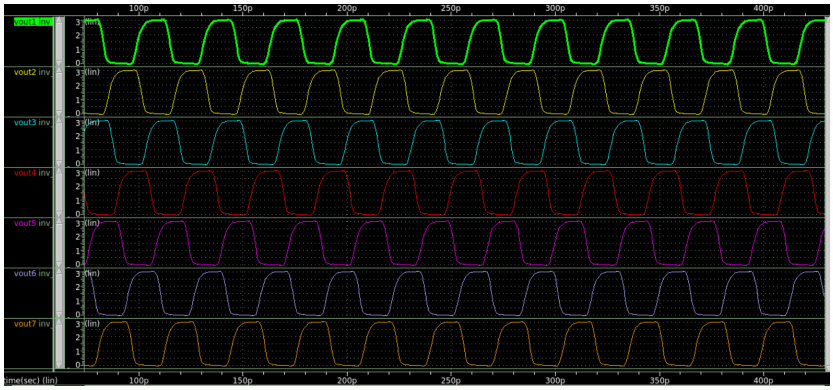


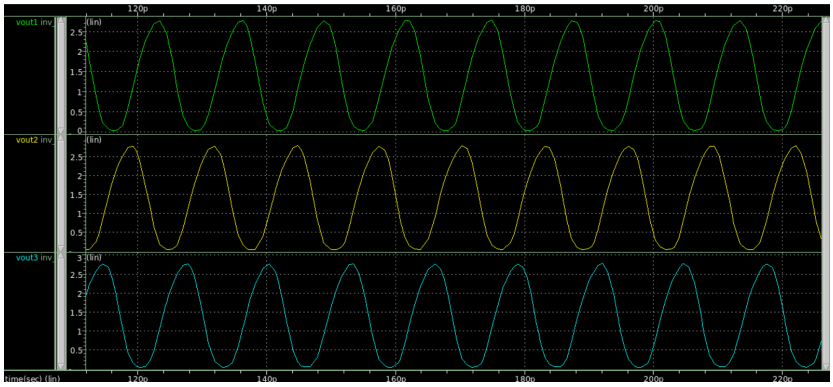
Figure 23: Output Waveform for an odd stage Ring Oscillator.

Here we can see oscillations of similar frequencies having different phases.

I have performed the simulations for two different sizings:
(i) W=80n , L=30n
(ii) W=160n , L=30n

3.3 W=80n,L=30n

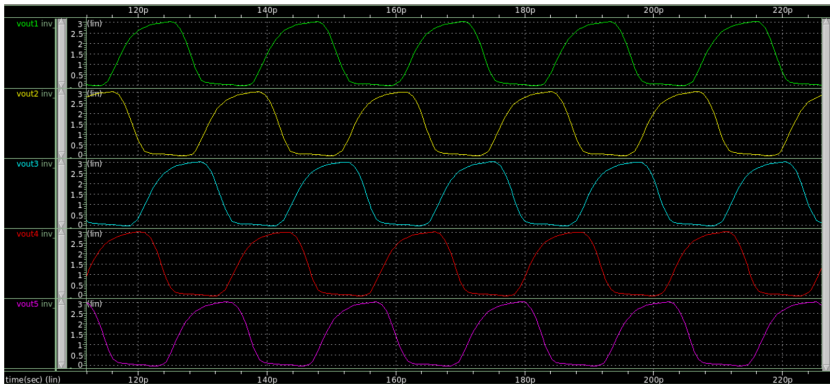
3.3.1 3-stage



.TITLE ''

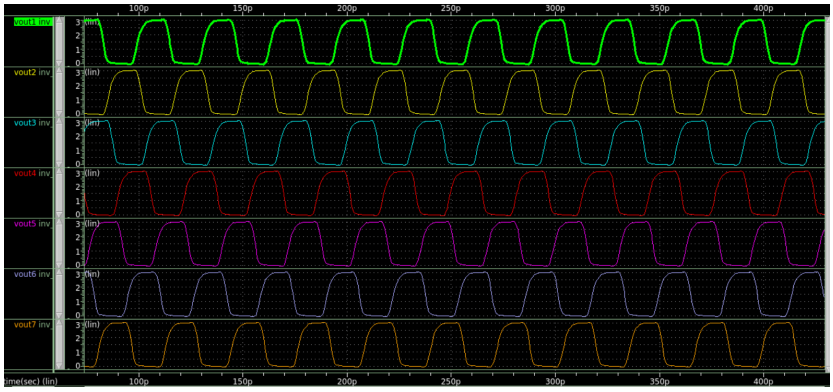
time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
1.298e-11	1.285e-11	1.295e-11	1.663e-12
2.700e-12	-1.137e-11	2.669e-12	7.702e+10
7.780e+10	7.722e+10	2.500e+01	1

3.3.2 5-stage



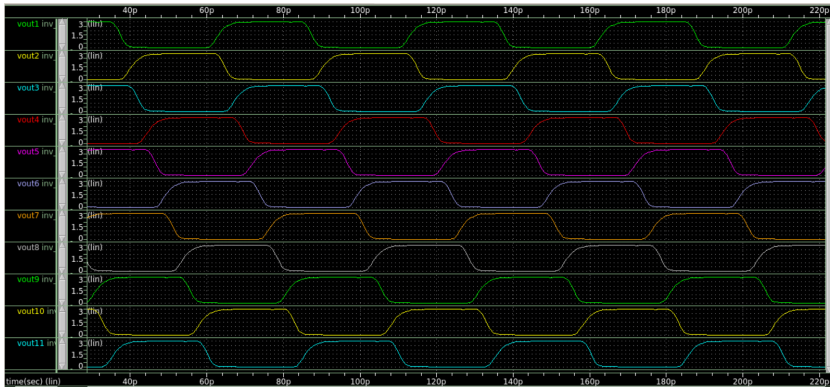
time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
2.275e-11	2.275e-11	2.266e-11	1.725e-12
2.821e-12	1.709e-12	2.777e-12	4.396e+10
4.396e+10	4.413e+10	2.500e+01	1

3.3.3 7-stage



time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
3.194e-11	3.183e-11	3.192e-11	1.725e-12
2.855e-12	1.737e-12	2.780e-12	3.131e+10
3.142e+10	3.133e+10	2.500e+01	1

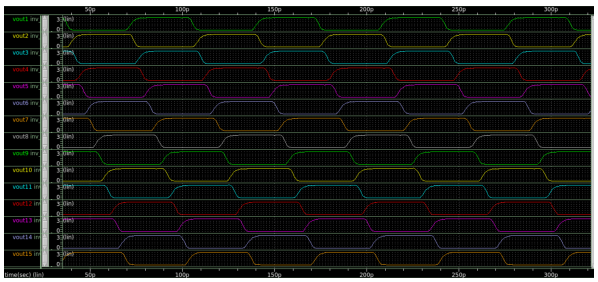
3.3.4 11-stage



TITLE ''

time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
5.015e-11	5.015e-11	4.999e-11	1.725e-12
2.855e-12	1.737e-12	2.780e-12	1.994e+10
1.994e+10	2.001e+10	2.500e+01	1

3.3.5 15-stage



time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
6.841e-11	6.829e-11	6.819e-11	1.725e-12
2.855e-12	1.737e-12	2.780e-12	1.462e+10
1.464e+10	1.467e+10	2.500e+01	1

3.3.6 Theoretical Calculations of frequency

Since the frequency of the oscillations depend on the delay , I have measured the delay across three inverters for accuracy .
The formula , $f = \frac{1}{2N \cdot t_d}$ states the frequency is dependent on twice(due to rise as well as fall) the delay of an inverter. But we know that the TPLH is more than the TPHL ,therefore, a better formula would be ,

$$f = \frac{1}{(T_{PLH} + T_{PHL})N}$$

I have calculated both these values in the simulation and applied them to the above formula. Here is the theoretical vs simulation data :

Stages	Simulation (Hz)	Theoretical (Hz)
3	7.722×10^{10}	7.27×10^{10}
5	4.396×10^{10}	4.36×10^{10}
7	3.131×10^{10}	3.11×10^{10}
11	1.993×10^{10}	1.98×10^{10}
15	1.462×10^{10}	1.45×10^{10}

Table 1: Comparison of Simulation and Theoretical Frequencies for Different Stages

The values are pretty similar.
I also calculated the frequency values by changing the load capacitance. Here is the data for collected:

Stages	No capacitance (Hz)	$C_L = 100$ pF (Hz)	$C_L = 100$ nF (Hz)	$C_L = 10$ µF (Hz)
3	7.722×10^{10}	2.08×10^{5}	2.087×10^{2}	2.08
5	4.396×10^{10}	1.226×10^{5}	1.228×10^{2}	1.225
7	3.131×10^{10}	0.8753×10^{5}	0.8766×10^{2}	0.8741
11	1.993×10^{10}	0.5574×10^{5}	0.5578×10^{2}	0.556
15	1.462×10^{10}	0.4084×10^{5}	0.4091×10^{2}	0.408

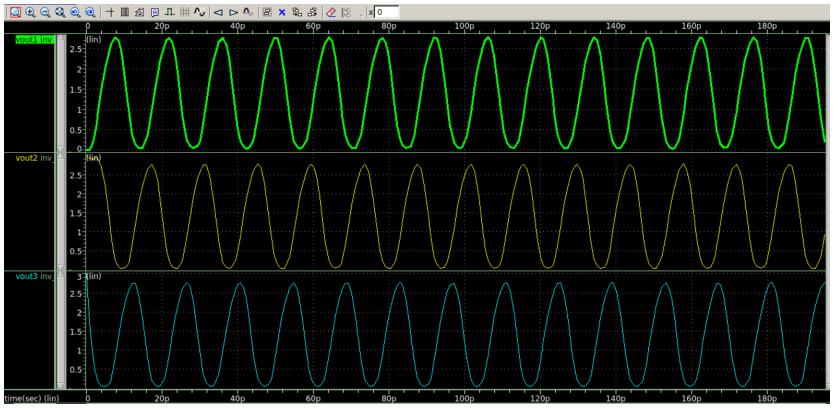
Table 2: Frequencies for Different Capacitance Values

From the above data it is very clear that the frequency is inversely proportional to the load capacitance value,(i.e.)

$$f \propto \frac{1}{C_L}$$

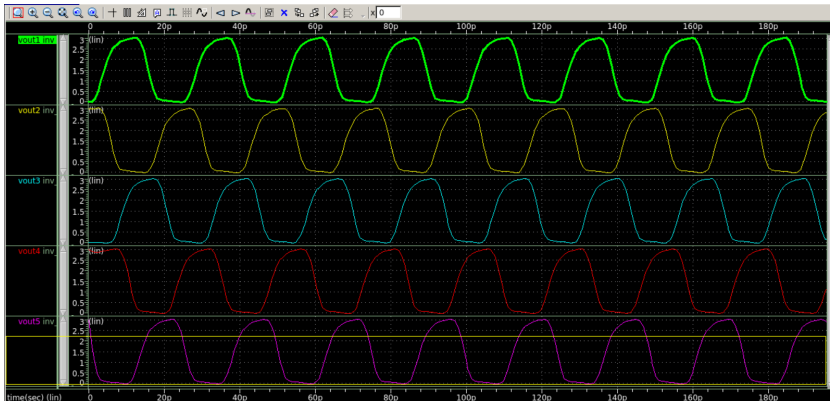
3.4 W=160n , L= 30n

3.4.1 3-stage



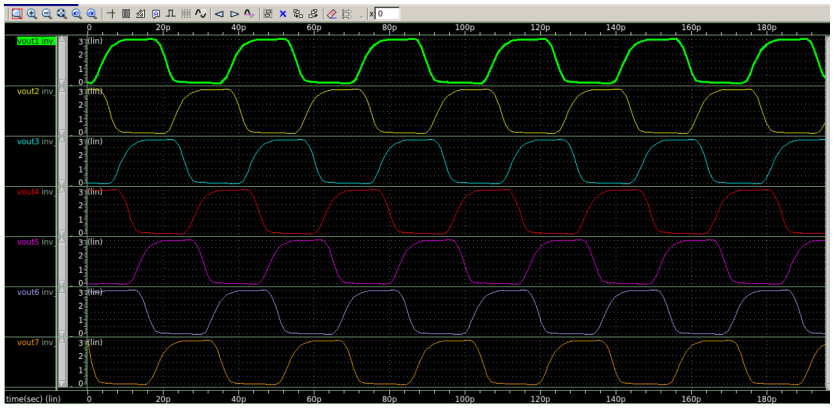
time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
1.414e-11	1.413e-11	1.404e-11	1.817e-12
2.910e-12	-1.236e-11	2.964e-12	7.071e+10
7.079e+10	7.125e+10	2.500e+01	1

3.4.2 5-stage



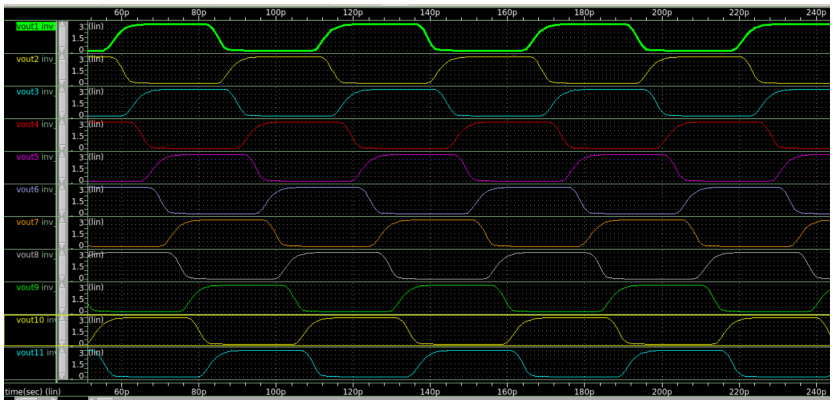
time_period1	time_period2	time_period3	dly11
dly12	dly21	dly22	freq1
freq2	freq3	temper	alter#
2.461e-11	2.458e-11	2.460e-11	1.876e-12
3.007e-12	1.868e-12	3.068e-12	4.064e+10
4.068e+10	4.064e+10	2.500e+01	1

3.4.3 7-stage



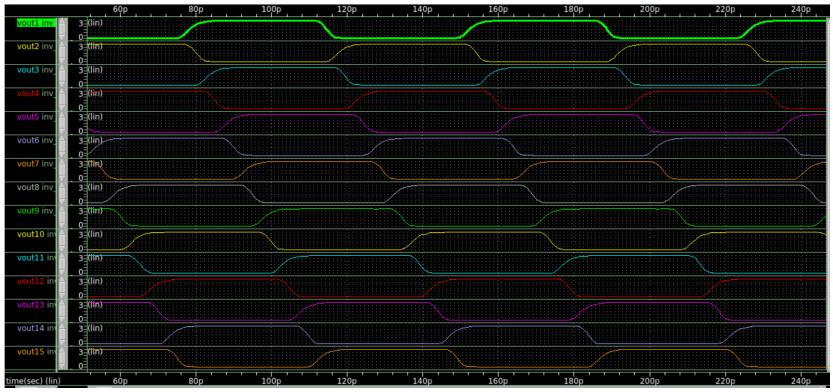

```
$DATA1 SOURCE='HSPICE' VERSION='O-2018.09-SP2 linux64' PARAM_COUNT=0
.TITLE ''
 time_period1     time_period2     time_period3     dly11
 dly12            dly21            dly22            freq1
 freq2            freq3            temper           alter#
  3.453e-11        3.447e-11        3.469e-11        1.876e-12
  3.074e-12        1.899e-12        3.071e-12        2.896e+10
  2.901e+10        2.883e+10        2.500e+01        1
~
~
```

3.4.4 11-stage




```
$DATA1 SOURCE='HSPICE' VERSION='O-2018.09-SP2 linux64' PARAM_COUNT=0
.TITLE ''
 time_period1     time_period2     time_period3     dly11
 dly12            dly21            dly22            freq1
 freq2            freq3            temper           alter#
  5.429e-11        5.438e-11        5.439e-11        1.876e-12
  3.082e-12        1.893e-12        3.071e-12        1.842e+10
  1.839e+10        1.839e+10        2.500e+01        1
~
```

3.4.5 15-stage



```
time_period1      time_period2      time_period3      dly11
dly12             dly21             dly22             freq1
freq2             freq3             temper            alter#
 7.401e-11         7.419e-11         7.418e-11         1.876e-12
 3.086e-12         1.892e-12         3.071e-12         1.351e+10
 1.348e+10         1.348e+10         2.500e+01         1
~
~
```

Here is the theoretical vs simulation data :

Stages	Simulation (Hz)	Theoretical (Hz)
3	7.071×10^{10}	6.66×10^{10}
5	4.06×10^{10}	4.0×10^{10}
7	2.9×10^{10}	2.8×10^{10}
11	1.84×10^{10}	1.82×10^{10}
15	1.348×10^{10}	1.33×10^{10}

Table 3: Comparison of Simulation and Theoretical Frequencies for Different Stages

The first value is way off but the rest are pretty similar.
Comparing the values of frequencies for the different sizing:

Stages	W=160n (Hz)	W=80n (Hz)
3	7.071×10^{10}	7.722×10^{10}
5	4.06×10^{10}	4.396×10^{10}
7	2.9×10^{10}	3.131×10^{10}
11	1.84×10^{10}	1.993×10^{10}
15	1.348×10^{10}	1.462×10^{10}

Table 4: Comparison of W=160n and W=80n sizing Frequencies for Different Stages with $C_L = 0$

Analysis: The frequencies are somewhat similar . This data is inconsistent with what we think we theoretically know which is that the frequency should increase as the size increases.**Where is the problem???**

From few sources, I have been made aware that the formula for the rise delay is ,

$$t_r = \frac{LC_L V_{DD}}{\mu_n C_{ox} W (V_{DD} - V_{th})^2} + 0.75 \frac{V_{DD}^2 C_L}{\mu_n \varepsilon_{ox} \varepsilon_0 W (V_{DD} - V_{th})^2}$$

Without external load capacitance: The effective capacitance C_L is primarily composed of parasitic capacitances. Since parasitic capacitances are proportional to $W \cdot C_{ox}$ (where W is transistor width and C_{ox} is oxide capacitance per unit area), both the numerator and denominator in the delay formula cancel out. Consequently, the propagation delay becomes independent of transistor width, resulting in an unchanged oscillation frequency.

However, when an external load capacitance C_L is added: which is significantly higher than the parasitic capacitance, the oscillation frequency of the ring oscillator follows the expected trend. This means that doubling the transistor width doubles the frequency, as the increased width reduces the propagation delay due to the lower resistance and improved driving capability of wider transistors.

Here is the data comparison of frequency with an external load capacitance $C_L = 100pF$:

Stages	W=160n (Hz)	W=80n (Hz)
3	3.815×10^5	2.08×10^5
5	2.22×10^5	1.226×10^5
7	1.587×10^5	0.8753×10^5
11	1.0×10^5	0.557×10^5
15	0.74×10^5	0.4084×10^5

Table 5: Comparison of W=160n and W=80n sizing Frequencies for Different Stages with $C_L = 100pF$

Here you can notice that , doubling the width almost doubles the frequency. So this data is consistent with the theory.