

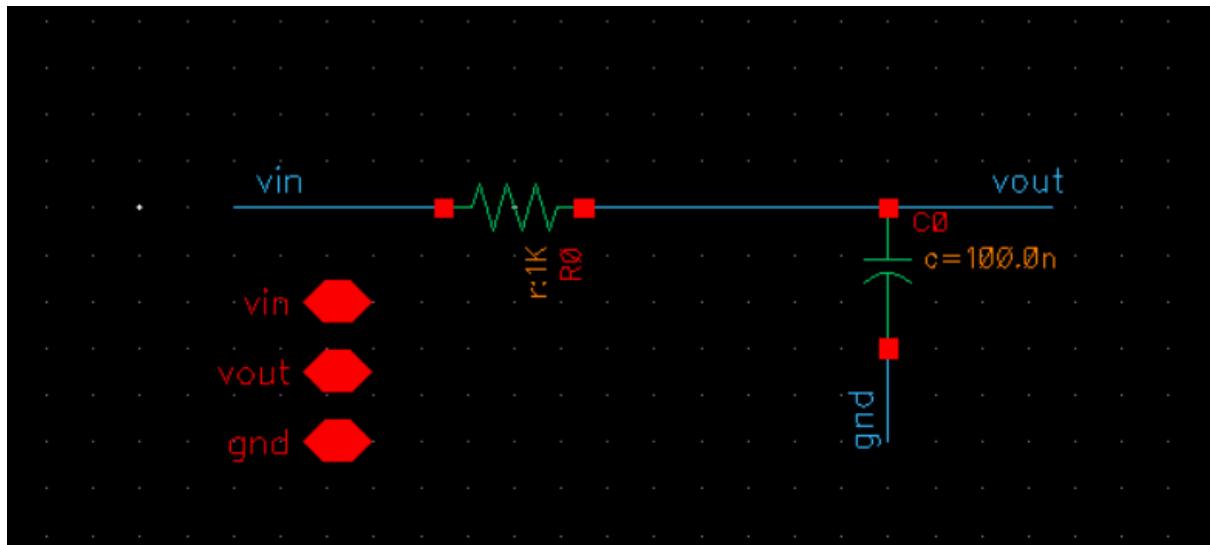
**MANIKANTA KRISHNAMURTHY**

# **INTERNSHIP REPORT**

## **WEEK 1**

# **1. RC CIRCUIT**

**SCHMATIC:**



VALUES: Resistance=1000 ohm ; Capacitance=1 micro farad

**NETLIST:**

```
|  
| c0 vout gnd 1e-6  
| r0 vout vin 1e3  
|  
|  
|
```

## INPUT DECK:

```
.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN

.include "rc_source"
|
*.tran 1n 10ms
**this for AC simulation
*vin vin 0 SIN(0 1 1k)
**bode plot
v1 vin 0 AC 1
.AC DEC 1000 1 1000000
.print ac v(vout)
**
.probe v(*)

.end
```

> For the AC simulation, we use ,

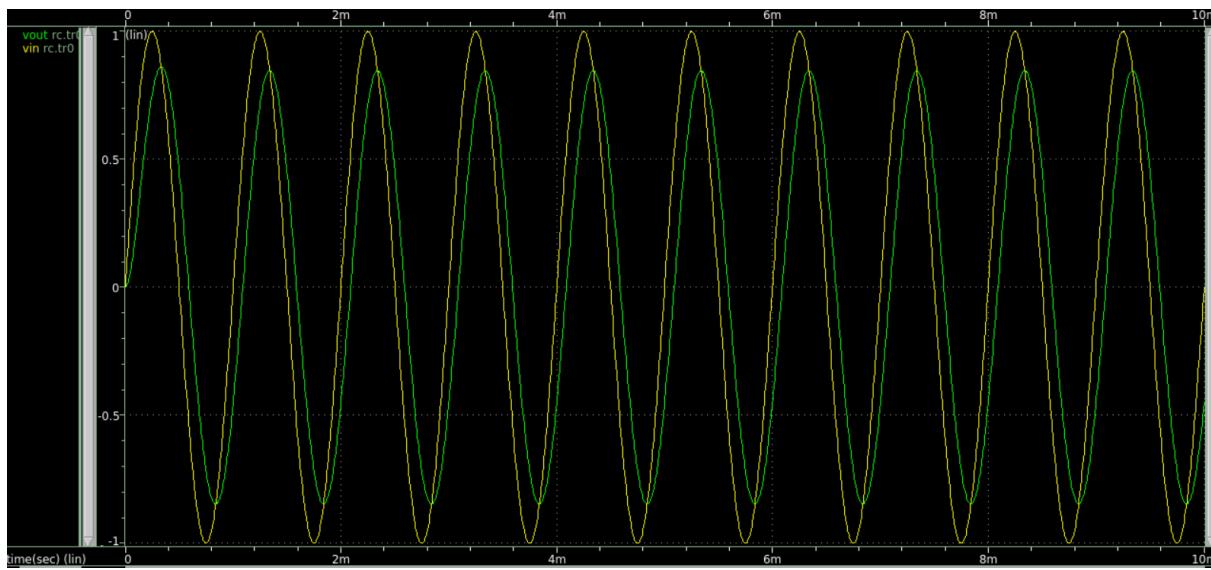
“**.tran 1n 10ms**  
**vin vin 0 SIN(0 1 1k)**” part only .

### **.tran 1n 10ms:**

- **.tran**: This command initiates a transient analysis.
- **1n**: The time step for the simulation, specified as 1 nanosecond (1e-9 seconds). This is the time interval at which the simulator calculates the circuit's behavior.
- **10ms**: The total simulation time, specified as 10 milliseconds (0.01 seconds). This is the duration over which the simulator will run the analysis.

### **vin vin 0 SIN(0 1 1k):**

- **vin**: This is the identifier (label) for the voltage source (same as in the previous line).
- **vin**: This is the positive terminal of the voltage source.
- **0**: This is the reference node (ground).
- **SIN(0 1 1k)**: This describes the voltage source as a sinusoidal (sine wave) source with specific parameters:
  - **0**: The DC offset of the sine wave (mean value).
  - **1**: The amplitude of the sine wave in volts (peak value).
  - **1k**: The frequency of the sine wave, specified as 1 kHz (1000 Hz).



## AC SIMULATION

>For the Bode Plot , we use ,

**" v1 vin 0 AC 1**

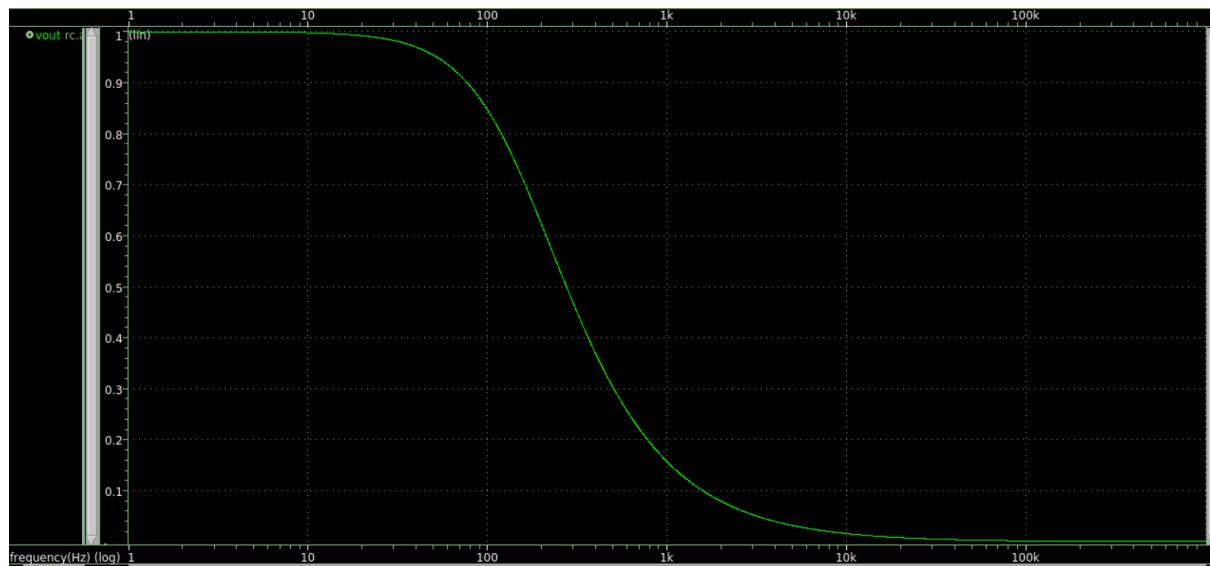
**.AC DEC 1000 1 1000000**" par only

**v1 vin 0 AC 1:**

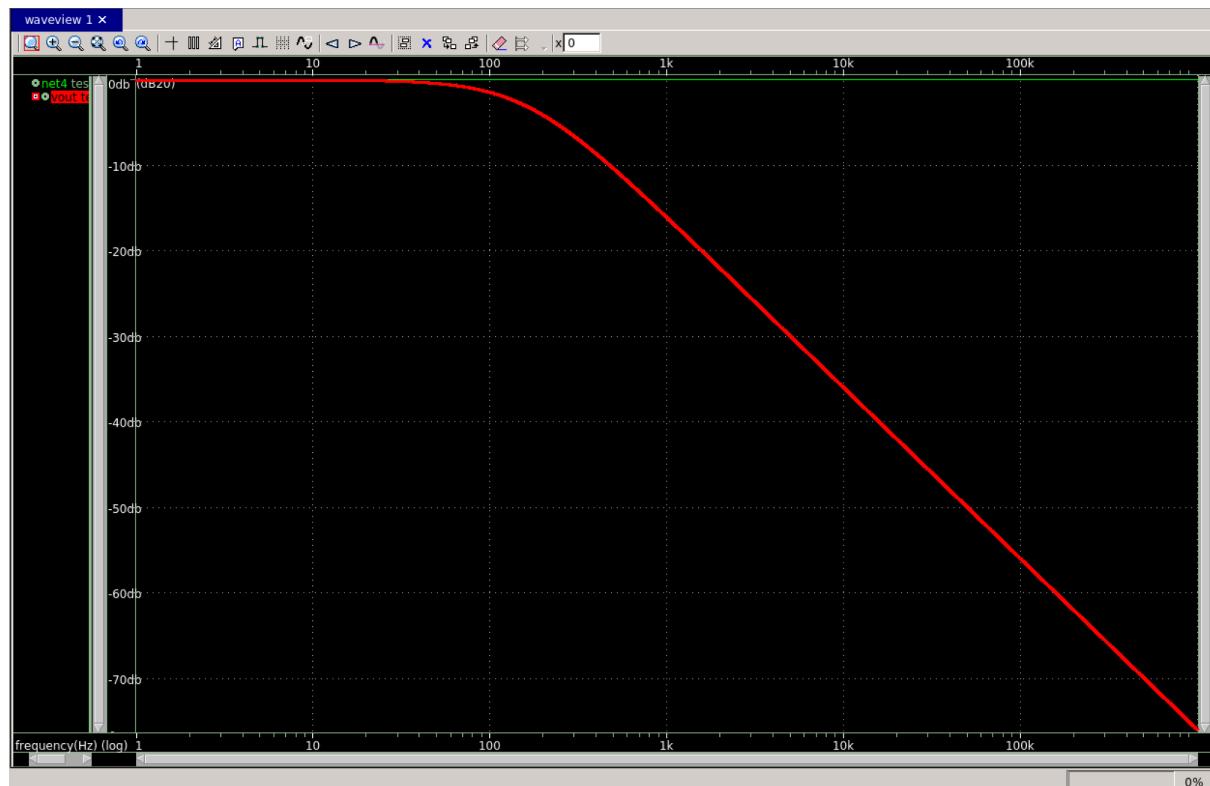
- **v1**: This is the identifier (label) for the voltage source.
- **vin**: This is the positive terminal of the voltage source.
- **0**: This is the reference node (ground).
- **AC**: Specifies that this voltage source is an AC source.
- **1**: This is the amplitude of the AC voltage in volts.

**.AC**: This is the command for an AC analysis.

- **DEC**: Specifies that the frequency range will be swept in a logarithmic (decade) scale.
- **1000**: The number of points per decade.
- **1**: The starting frequency of the sweep in Hz.
- **1000000**: The ending frequency of the sweep in Hz (1 MHz).

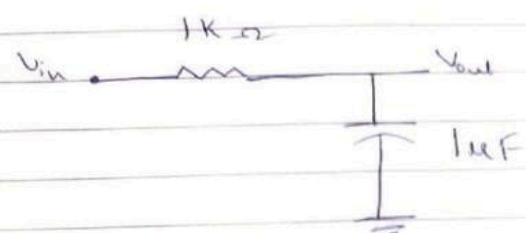


**V<sub>OUT</sub> vs log(w)**



**20log(V<sub>out</sub>/V<sub>in</sub>) vs log(w)**

## HAND CALCULATIONS:



Transfer function,

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = \frac{1}{1 + RCS}$$

$$R = 1\text{ k}\Omega ; C = 1\text{ }\mu\text{F}$$

$$\therefore H(j\omega) = \frac{1}{1 + RCj\omega}$$

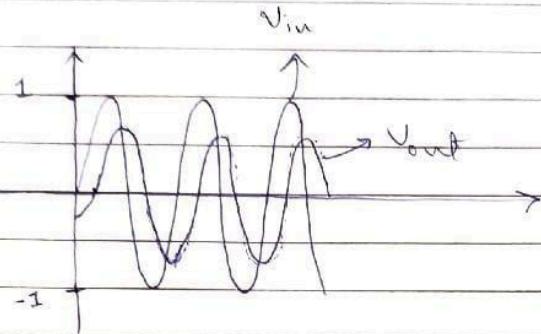
$$\therefore |H(j\omega)| = \frac{1}{\sqrt{1 + (RC\omega)^2}}$$

The  $-3\text{dB}$  line is where  $|H(j\omega)| = \frac{1}{\sqrt{2}}$

$$\Rightarrow \omega_{cut-off} = \frac{1}{RC} = \frac{1}{10^{-3}} = 10^3 \text{ rad/s}$$

$$\therefore f_{cut-off} = \frac{10^3}{2\pi} = 159.155 \text{ Hz}$$

AC simulation;



- Here the amplitude <sup>of V<sub>out</sub></sup> is less than amplitude of  $V_{in}$   
& the  $V_{out}$  sin wave has shifted to the right.
- ∴ Causing a delay

— / —

### Bode Plot

$$\begin{aligned} M &= 20 \log |H(j\omega)| = +20 \log \left( \frac{1}{(1+(RC\omega)^2)^{1/2}} \right) \\ &= -20 \log (1+(RC\omega)^2)^{1/2} \\ &= -10 \log (1+(RC\omega)^2) \end{aligned}$$

(1) For  $\omega \ll \frac{1}{RC}$

$$1+(RC\omega)^2 \approx 1$$

$$\therefore M = -10 \log (1) = 0$$

(2) For  $\omega \gg \frac{1}{RC}$

$$1+(RC\omega)^2 \approx (RC\omega)^2$$

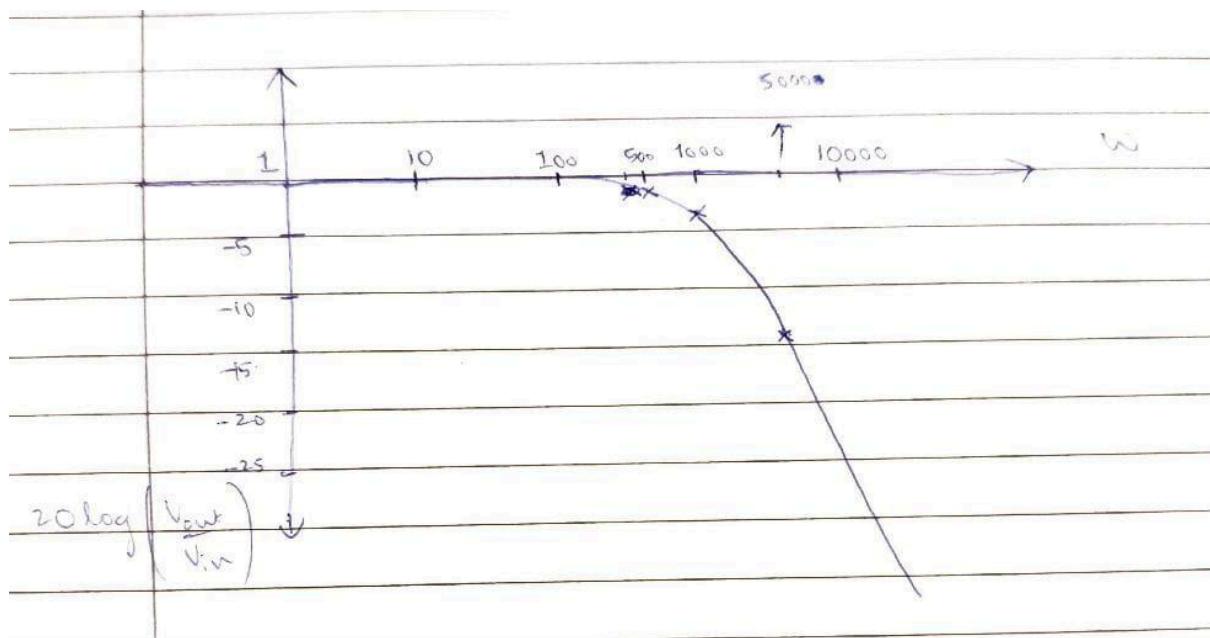
$$\therefore M = -10 \log (RC\omega)^2 = -20 \log (RC\omega)$$

$\Rightarrow -20 \text{ dB/dec}$  line

(3) For  $\omega = \frac{1}{RC}$   $M = -10 \log (2) = -3 \text{ dB}$

(4) For  $\omega = \frac{0.015}{RC}$   $M = -10 \log (1+0.015) \approx -1 \text{ dB}$

(5) For  $\omega = \frac{5}{RC}$   $M = -10 \log (26) = -14.15 \text{ dB}$



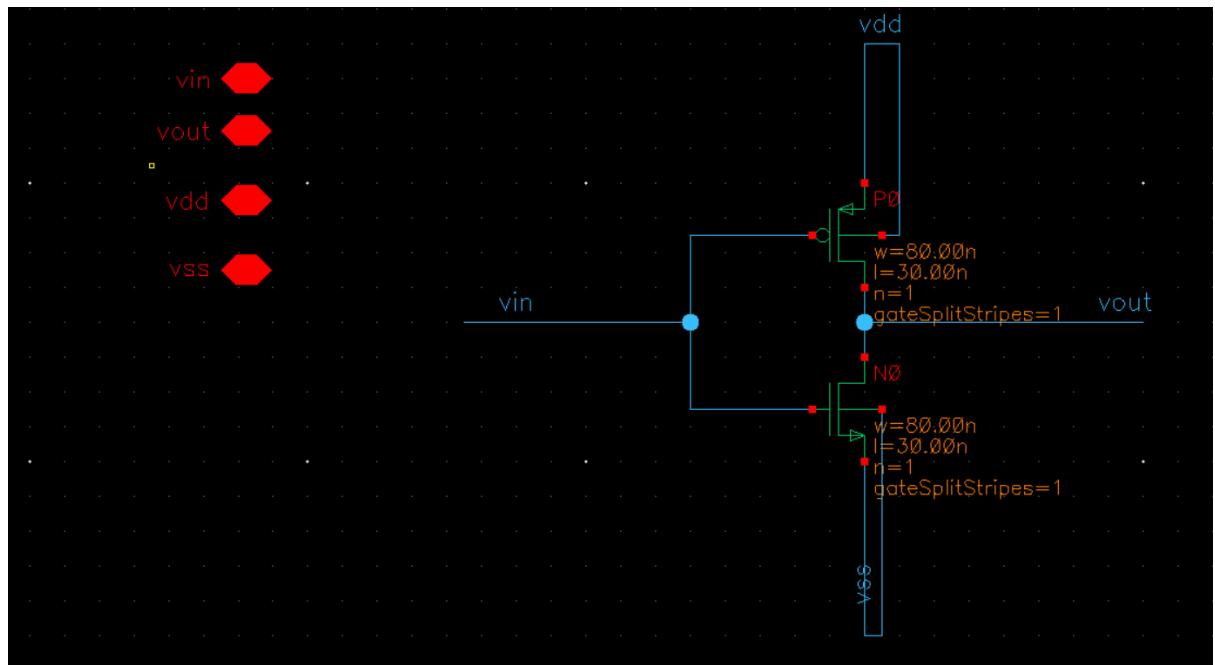
## QUESTIONS:

1. The frequencies are almost the same. The difference arises due to the fact that the cut-off is actually measured at  $w=1/RC$ . This implies  $20\log(V_{out}/V_{in}) = -3.01 \text{ dB}$ . Since we are measuring at  $-3 \text{ dB}$ , we are bound to get some difference.
2. The hand calculations and the actual plot are quite similar. The approximations which have been made seem to be quite accurate. For low frequencies the magnitude is almost 0 and for high frequencies the plot follows a  $-20 \text{ dB/dec}$  line.

2.

## 2.1. INVERTER

### SCHEMATIC:



## INPUT DECK:

```
.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.param par_vdd=1
.param wn=80e-9
.param wp=80e-9
.param ln=30e-9
.param lp=30e-9
.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN

*.include "inv_mani_source"
xn0 vout vin vss vss nfet w=wn l=ln nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1
xp0 vout vin vdd vdd pfet w=wp l=lp nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1

*****
.trans ln 10ms
*+sweep wn 5e-10 125e-9 50e-10
+sweep wp 5e-10 125e-9 50e-10
*+sweep ln 5e-9 125e-9 20e-9
|+sweep lp 5e-9 125e-9 20e-9
v1 vdd 0 DC=par_vdd
v2 vss 0 DC=0

vin vin 0 pulse( 0 1 2n 1n 1m 2m)
*vin vin 0 pwl 0 1 10ms 0
.meas tran tphl
+trig v(vin)='par_vdd*0.5' fall=1
+targ v(vout)='par_vdd*0.5' rise=1

.meas tran tplh
+trig v(vin)='par_vdd*0.5' rise=1
+targ v(vout)='par_vdd*0.5' fall=1
.probe v(*)
.end
```

\* Sweep the width of the pfet

```
.sweep wp 5e-10 125e-9 50e-10
```

\* Sweep the width of the nfet

```
.sweep wn 5e-10 125e-9 50e-10
```

\* Measure the high-to-low delay (tphl)

```
.meas tran tphl
+ trig v(vin) = 'par_vdd * 0.5' fall=1
+ targ v(vout) = 'par_vdd * 0.5' rise=1
```

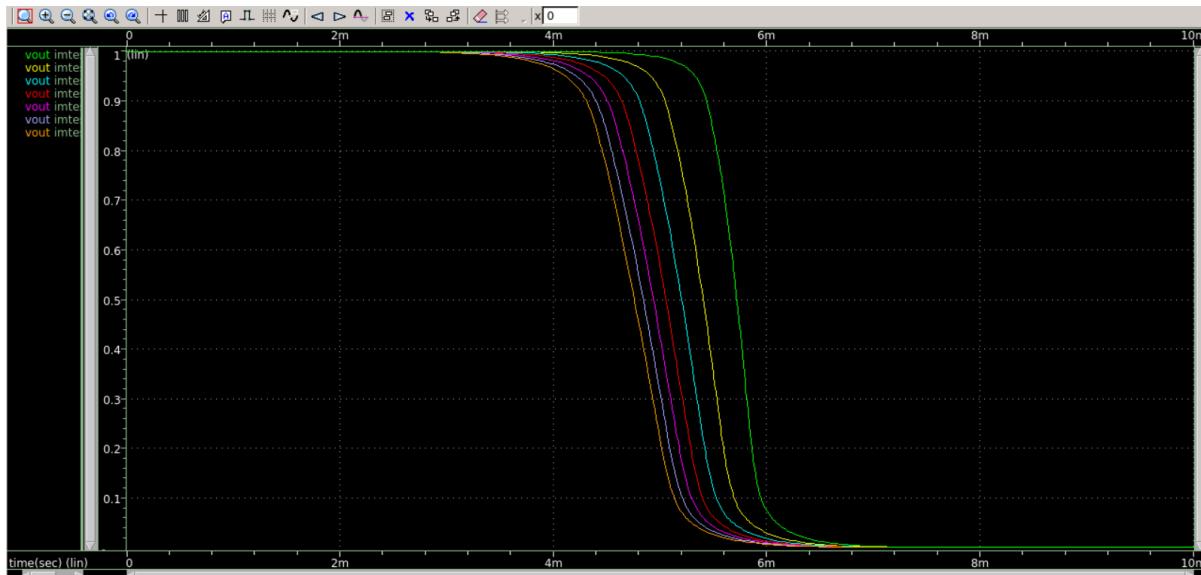
\* Measure the low-to-high delay (tplh)

```
.meas tran tplh
+ trig v(vin) = 'par_vdd * 0.5' rise=1
+ targ v(vout) = 'par_vdd * 0.5' fall=1
```

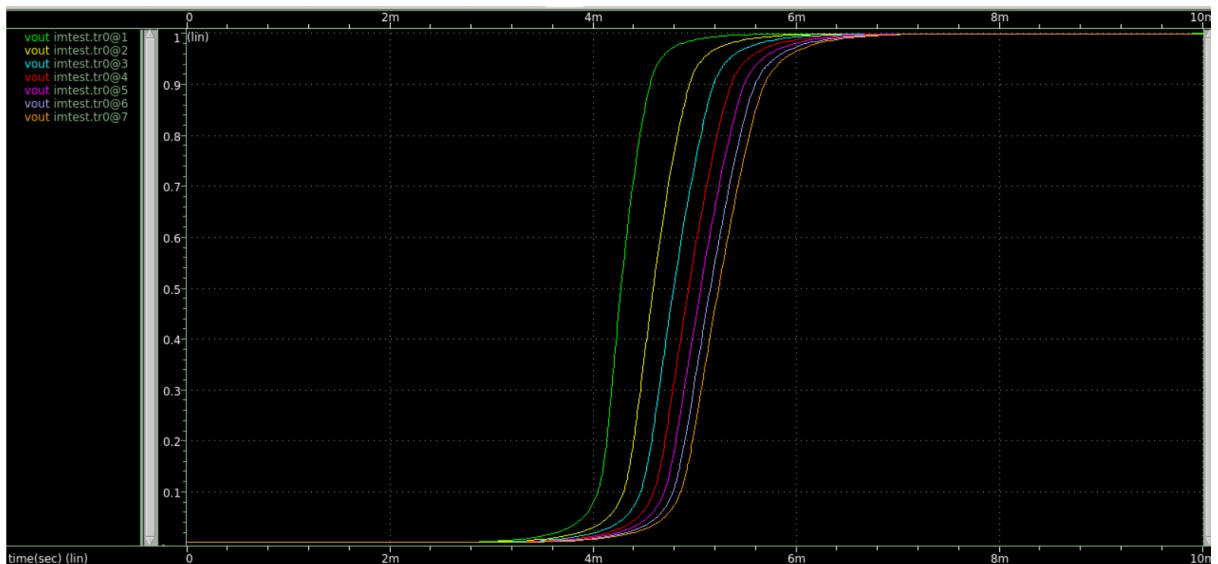
## DC SIMULATION

> Here are the simulation of the DC transfer curve for few of the widths of NFET & PFET

Gate Width Sweep of NFET

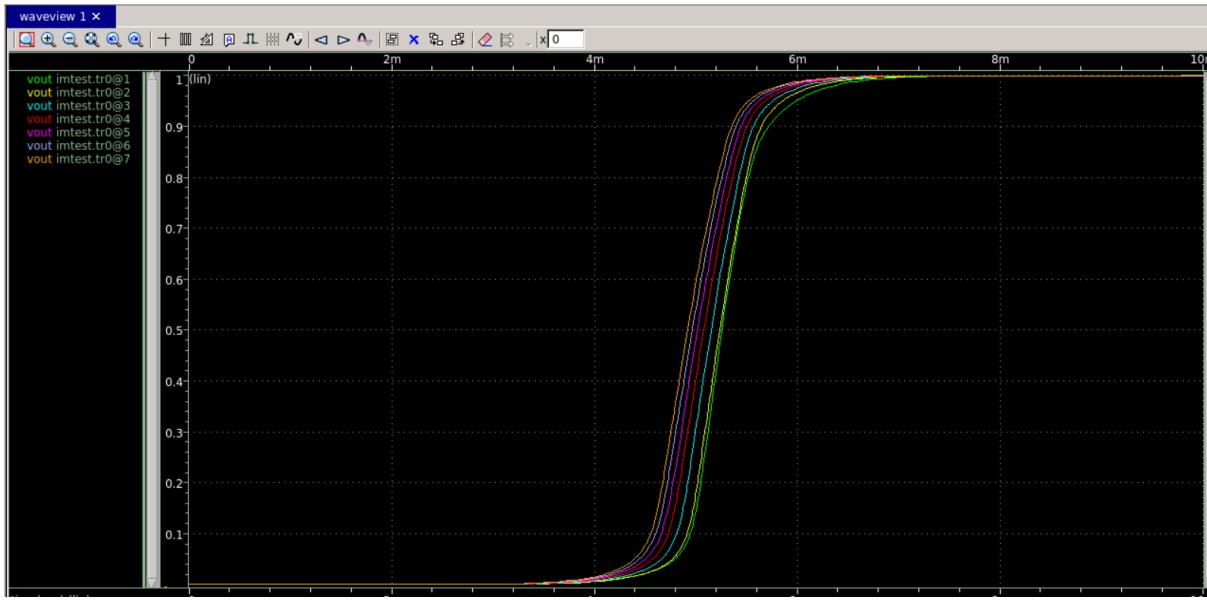


As the gate **width increases** (Width ratio decreases) the **curve shifts to the left**.

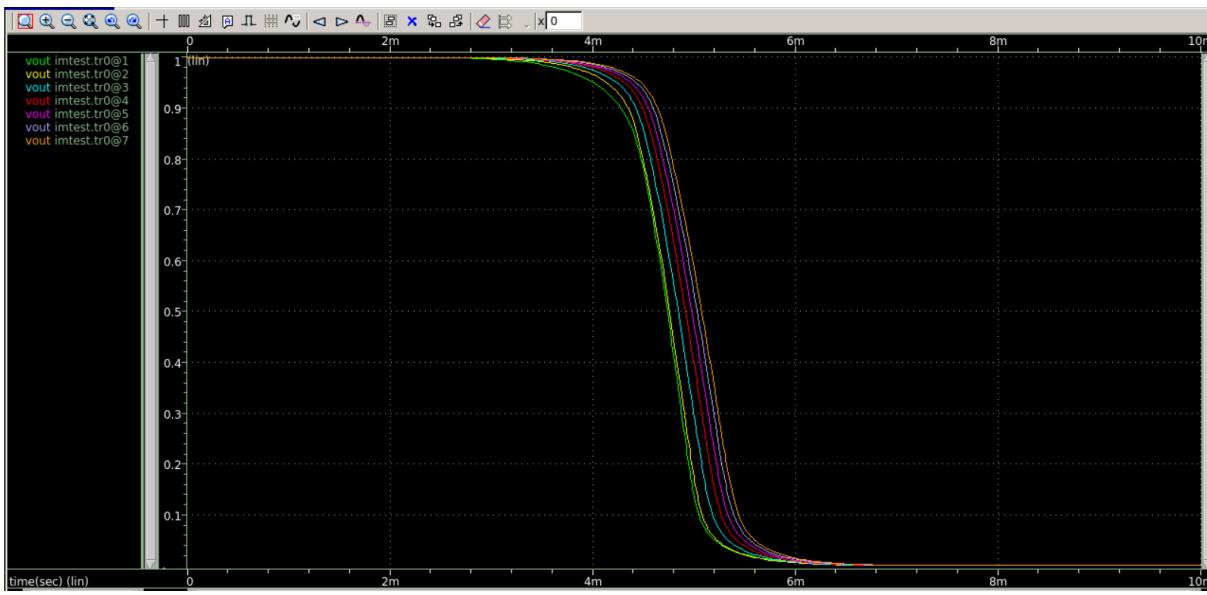


As the gate **width increases** (Width ratio decreases) the **curve shifts to the right**

## Gate Width Sweep of PFET



As the gate **width increases** (Width ratio increases) the **curve shifts to the left**.



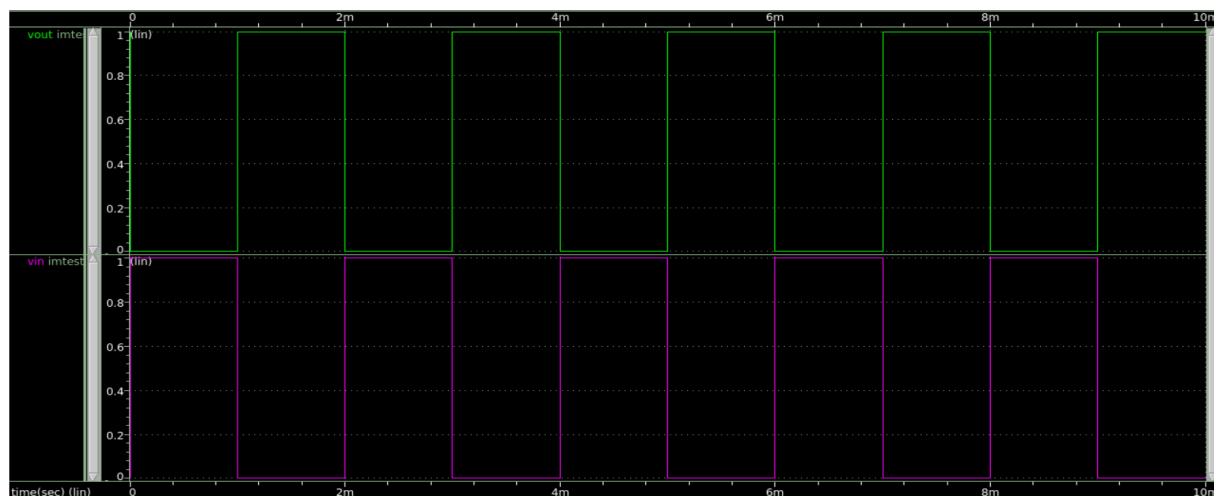
As the gate **width increases** (Width ratio increases) the **curve shifts to the right**.

- > When comparing the gate width sweeps of both PFET and NFET, it's evident that the NFET gate width sweep exhibits a significantly larger shift compared to the PFET gate width sweep.

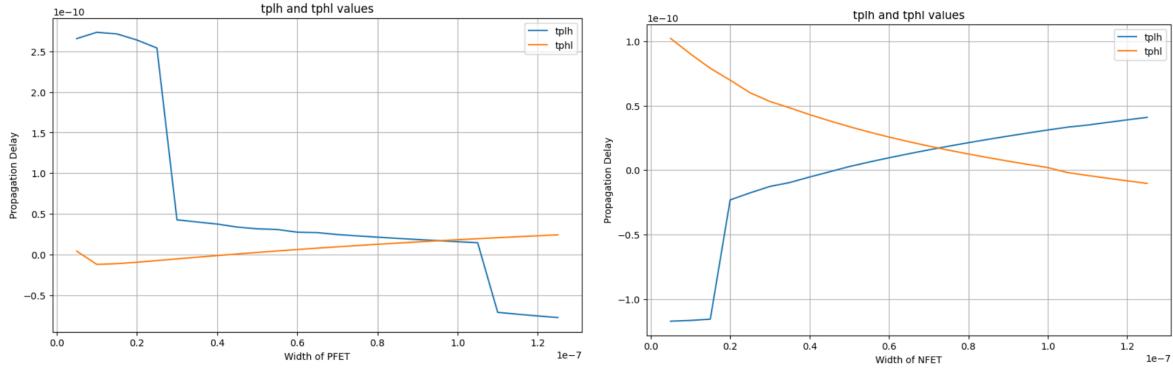
### From observations

- >The low to high signal data of both the NFET and PFET , indicates that the DC transfer curve **shifts towards the right as Width Ratio(wp/wn) decreases.**
- >Similarly , from the high to low signal of both NFET and PFET, it is evident that the DC transfer curve **shifts towards the left as Width Ratio(wp/wn) decreases.**
- >The drastic change in NFET gate sweep as compared to PFET gate sweep , is due to the fact that **wn is in the denominator** of the Width ratio , therefore, the value of the width ratio changes drastically .
- >Theoretically , the shift in the DC transfer curve depends on the **beta ratio.**( $\beta_p/\beta_n$ ) Where  $\beta_p=\mu_pCox(W/L)_p$ ;  $\beta_n=\mu_nCox(W/L)_n$
- >As the beta ratio increases, high-to-low shifts towards right and the low-to-high shifts towards left.

### TRANSIENT SIMULATION



Vout vs Vin



After noticing the delays from the two graphs it is evident that the two delays are different . (Why?)

### ##GENERALLY

- >In the low-to-high delay(tplh), it is required that the PFET goes to saturation .
- >In the high-to-low delay(tphl), it is required that the NFET goes to saturation .
- > **NFET** is dependent mainly on the **movement of the electrons** , whereas **PFET** depends on the **movement of holes**.
- >The **mobility of electrons is higher** than that of holes .
- >Hence it takes more time for a low to high transition compared to a high to low

### ##HERE

- >According to my observation , both the **delays depend on the Width Ratio(Wp/Wn)**.

- >In the first plot , increasing the Wp value => **increasing the Width ratio , increases the t<sub>PHL</sub> value and decreases the t<sub>PLH</sub> value.**
- >In the second plot , increasing the Wn value => **decreasing the Width ratio , increases the t<sub>PLH</sub> value and decreases the t<sub>PHL</sub> value.**

### THEORETICALLY,

$$t_{PHL} = \frac{\alpha_n C}{k'_n (W/L)_n V_{DD}}$$

where  $\alpha_n$  is a factor determined by the relative

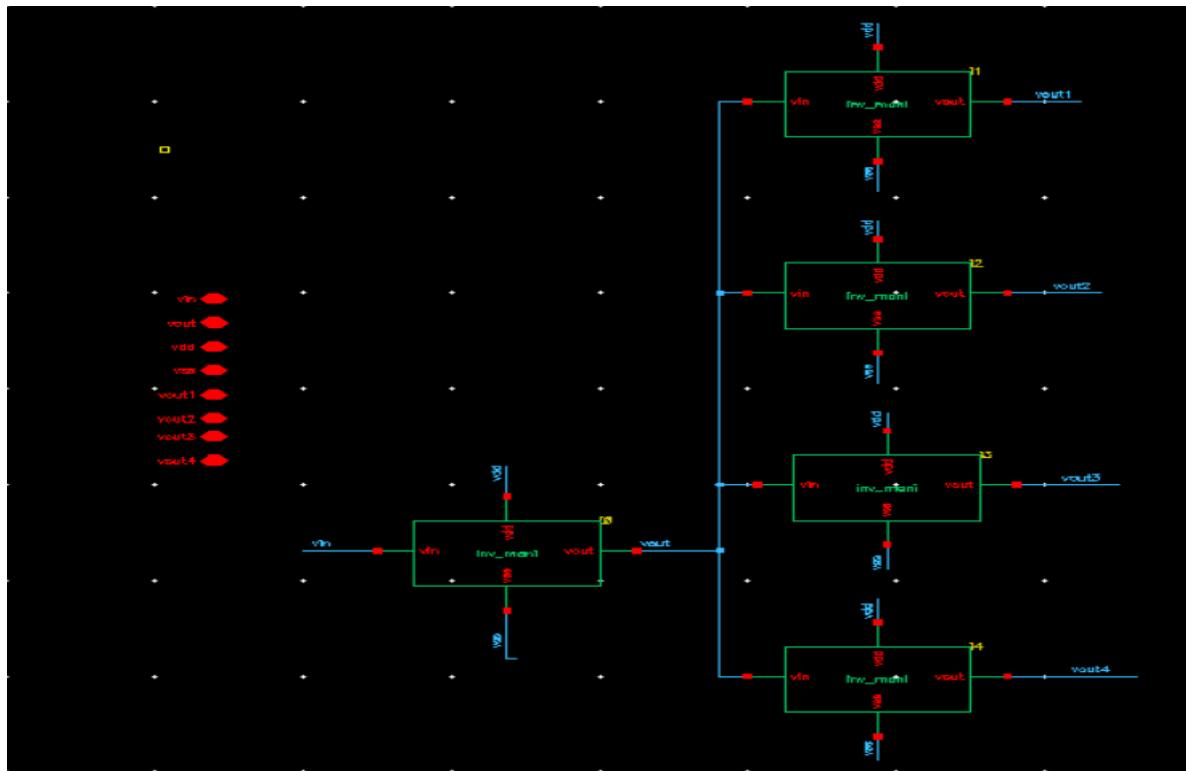
$$\alpha_n = 2 \sqrt{ \left[ \frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left( \frac{V_{tn}}{V_{DD}} \right)^2 \right] }$$

$$t_{PLH} = \frac{\alpha_p C}{k'_p (W/L)_p V_{DD}}$$

$$\text{where } \alpha_p = 2 \sqrt{ \left[ \frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left| \frac{V_{tp}}{V_{DD}} \right|^2 \right] }$$

## 2.2 FAN OUT

### SCHEMATIC:



### INPUT DECK:

```
.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN
.param input=0
.param par_vdd=0.9
.param par_temp=25
.param par_wn=80n
.param ratio=1
.param par_wp='par_wn*ratio'

.include "fan_source"

.subckt inv_mani vdd vin vout vss
xn0 vout vin vss vss nfet w=par_wn l=30e-9 nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1
xp0 vout vin vdd vdd pfet w=par_wp l=30e-9 nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1
.ends inv_mani

*****
**DC SIMULATION
*.dc input 0 1 0.01
```

```
*****
**DC SIMULATION
*.dc input 0 1 0.01

**TRANSIENT SIMULATION
.tran ln 10ms
+sweep ratio 0.7 2.5 0.1

v1 vdd 0 DC=par_vdd
v2 vss 0 DC=0

*vin vin 0 pulse( 0 1 2n 1n 1n 1m 2m)
vin vin 0 pwl 0 1 10ms 0
*vin vin 0 pwl 0 0 10ms 1
*.meas tran tphl
**+trig v(vin)='par_vdd*0.5' fall=2
**+targ v(vout1)='par_vdd*0.5' fall=2

*.meas tran tphh
**+trig v(vin)='par_vdd*0.5' rise=2
**+targ v(vout1)='par_vdd*0.5' rise=2

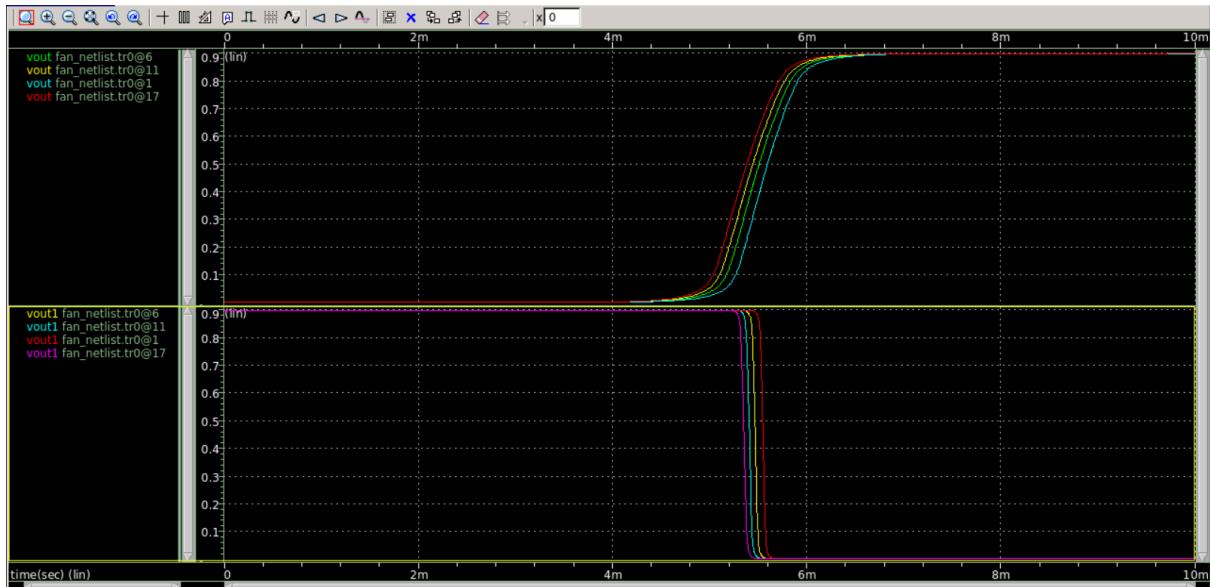
.probe v(*)
.end
```

## fan\_source

```
** Library name: manil
** Cell name: inv_mani
** View name: schematic
** End of subcircuit definition.

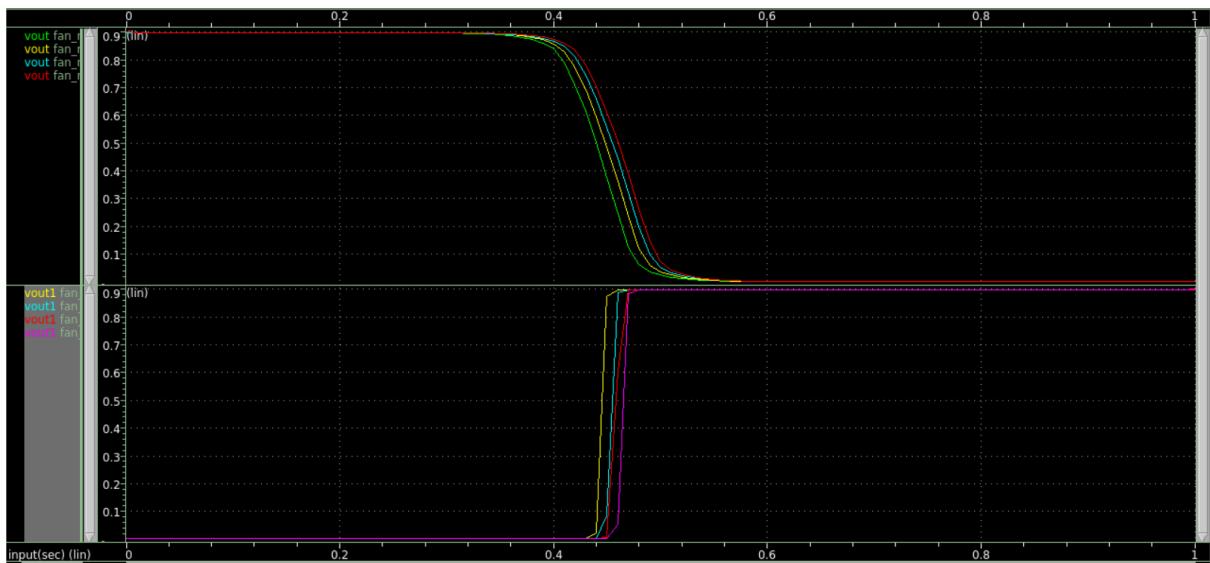
** Library name: manil
** Cell name: fan_out
** View name: schematic
xi4 vdd vout vout4 vss inv_mani
xi3 vdd vout vout3 vss inv_mani
xi2 vdd vout vout2 vss inv_mani
xi1 vdd vout vout1 vss inv_mani
xi0 vdd vin vout vss inv_mani
```

## DC SIMULATION



Input is going from 1V to 0V

As the width ratio increases the 2nd stage inverter output shifts towards the left



Input is going from 0V to 1V

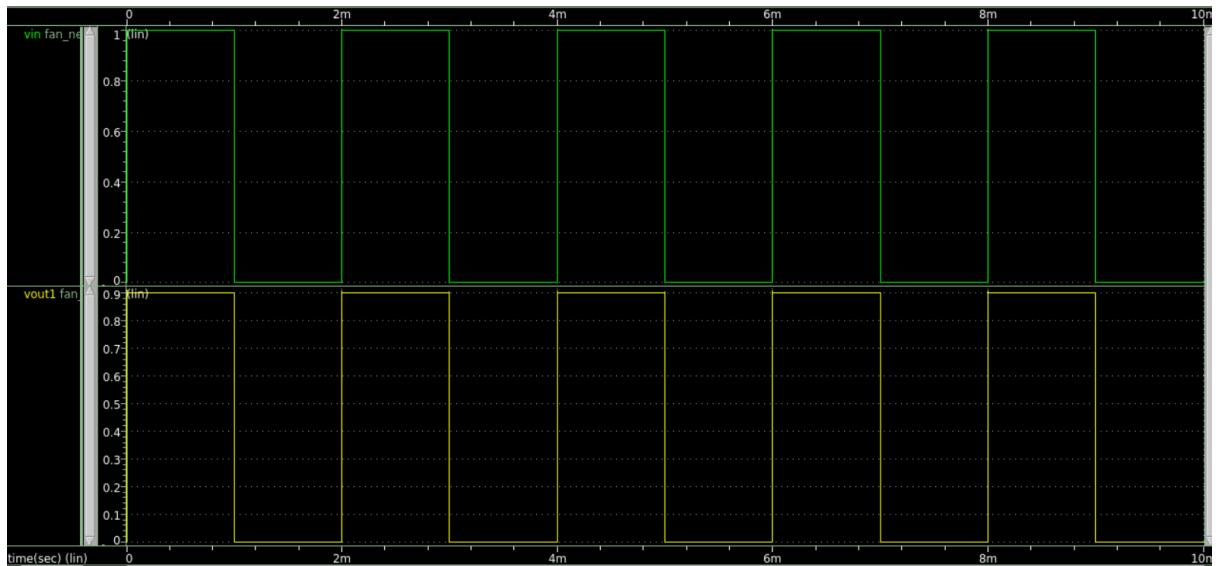
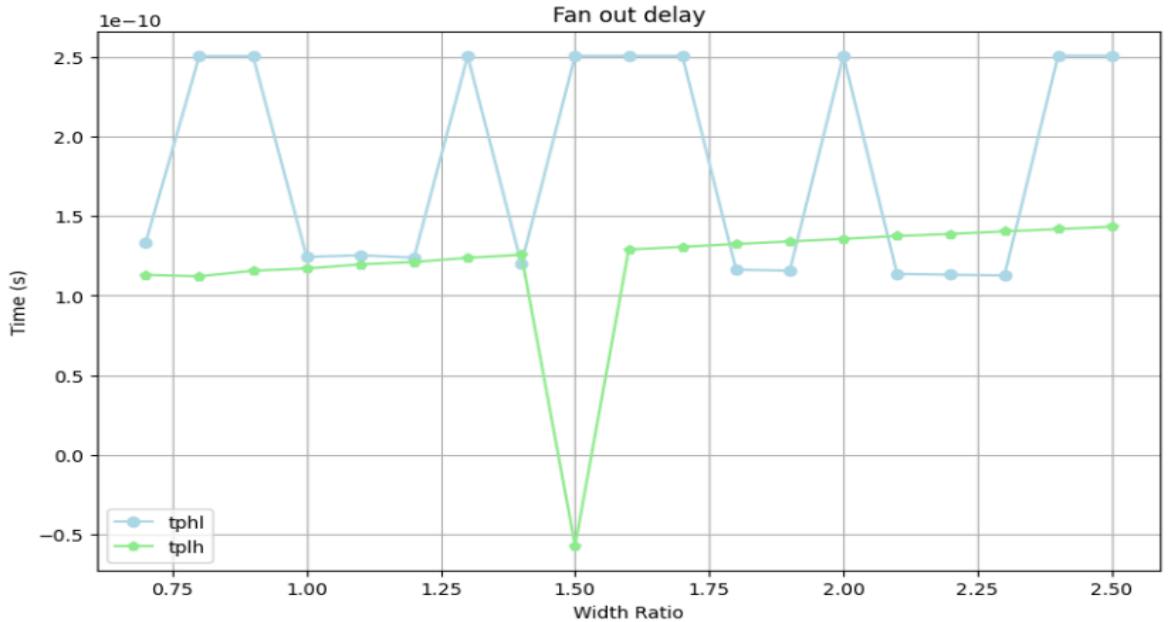
As the width ratio increases the 2nd stage inverter output shifts towards the right

>Here we also notice that the **rise time and fall time** of the output **has decreased**. (Why?)

>This is because the input to the first stage of fan-out is a ramp , this implies going from 1/0 V to 0/1 V takes 10ms . And the output of the first stage goes from 0/1 V to 1/0 V in much less than 10ms. And this goes to the second stage.

>The second stage being an inverter further reduces the time.

## TRANSIENT SIMULATION



vout1(2nd stage inverter output) vs vin

>Comparing this delay data with the delay data of a single inverter, we come to understand that there is more delay in the fan-out output(i.e **tphl and tplh has increased**) , which makes sense because there are two inverters in series thereby adding the delays.

>Here we notice that increasing the ratio , increases the tplh value which is opposite as seen in a single inverter , this is because ..... Increased width ratio increases the tphl of the first inverter (i.e. high to low signal), when this signal is passed through the second inverter , the output is a low to high signal. Therefore the net delay in tplh is increased(though greater width ratio decreases tplh of an inverter , the combined effect seems to increase the delay).

### 3. PVT SIMULATION

#### A. INPUT DECK

```
.OPTION post
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" FF
.include "fan_source"

.param var_temp=25
.param var_vdd=1
.param var_wn=80n
.param var_wp= 'var_wn*ratio'
.param ratio=2

.temp var_temp

.subckt inv_mani vdd vin vout vss
xn0 vout vin vss nfet w=var_wn l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1
xp0 vout vin vdd pfet w='2*var_wp' l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=1 pccrit=1 p_la=0 ngcon=1
.ends inv_mani

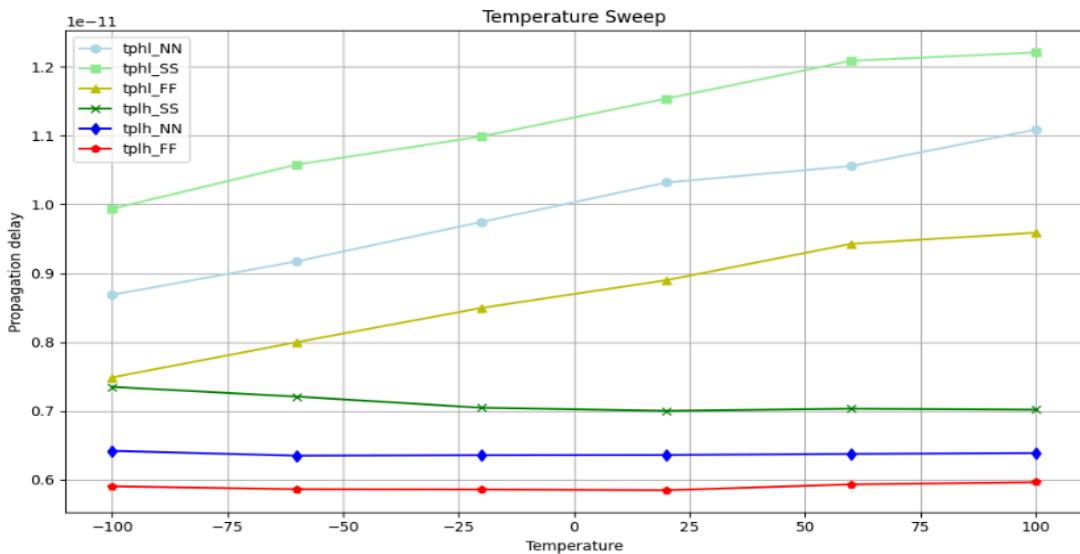
.tran lp ln
+sweep var_temp -100 100 40

.vdd vdd 0 DC=var_vdd
.vss vss 0 DC=0
.vin vin 0 pulse 0 var_vdd 0 lp lp 0.05n 0.ln

*.measure tran plhdly
*+trig v(vin)='var_vdd/2' fall=2
*+targ v(vout)='var_vdd/2' rise=2

*.measure tran phdly
*+trig v(vin)='var_vdd/2' rise=2
*+targ v(vout)='var_vdd/2' fall=2

.probe v(*)
.END
```



Here, we notice that , with increase in temperature , the tPHL increases and there is a slight decrease in the tPLH.

#### Affecting factors

- > carrier concentration: increases in temperature causes increase in carrier concentration leading to increased capacitance and hence longer propagation delays.
- > At higher temperatures, carriers have higher mobility, which can lead to faster propagation delays.

> as temperature increases, the threshold voltage of NMOS transistors typically decreases, while for PMOS transistors, it increases. This variation affects the turn-on and turn-off times of the transistors, thus impacting the propagation delay.

B.

```
.OPTION post
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN
.include "fan_source"

.param var_temp=25
.param var_vdd=1
.param var_wn=80n
.param var_wp= 'var_wn*ratio'
.param ratio=2

.temp var_temp

.sobckt inv_mani vdd vin vout vss
xn0 vout vin vss vss nfet w=var_wn l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1
xp0 vout vin vdd pfet w='2*var_wp' l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1
.ends inv_mani

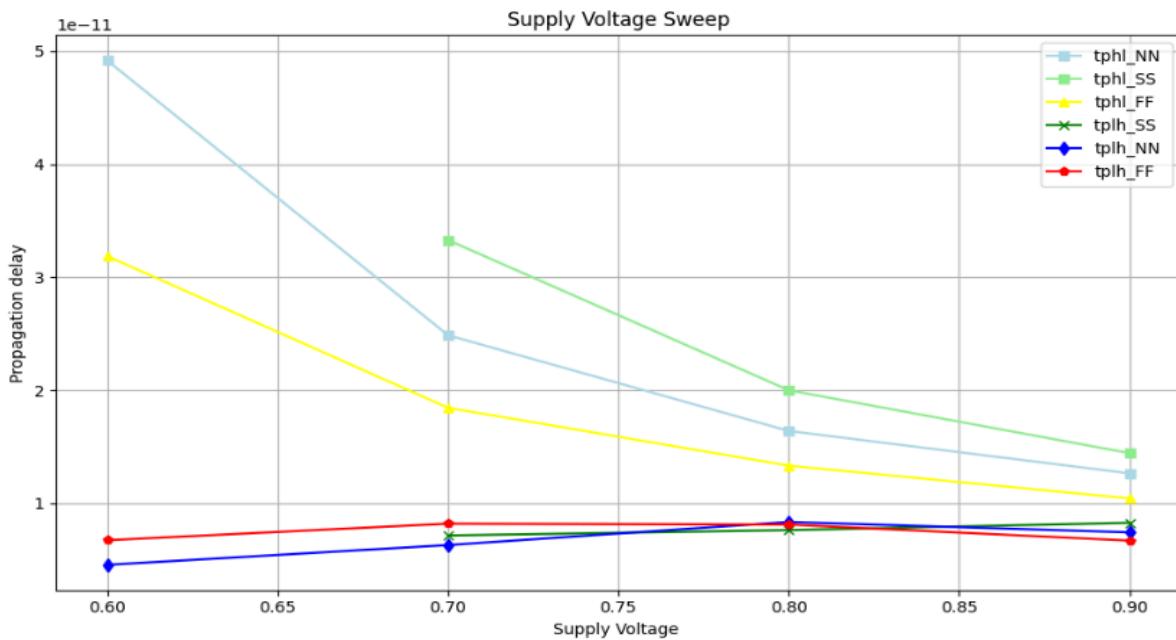
.tran 1p ln
+sweep var_vdd 0 0.9 0.1

vdd vdd 0 DC=var_vdd
vss vss 0 DC=0
vin vin 0 pulse 0 var_vdd 0 1p 1p 0.05n 0.1n

.measure tran phldly
+trig v(vin)='var_vdd/2' fall=2
+targ v(vout)='var_vdd/2' rise=2

*.measure tran phldly
*+trig v(vin)='var_vdd/2' rise=2
*+targ v(vout)='var_vdd/2' fall=2

.probe v(*)
.END
```



>Here we notice that few initial outputs couldn't be generated ,  
This is because the Vgs was lower than the threshold voltage . This results in no  
actual simulation of the inverters and hence no triggering and targeting.

However ,for the rest of the results increasing the supply voltage reduces tPHL and  
slightly increases tPLH.

### C.

```
.OPTION post
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" FF
.include "fan_source"

.param var_temp=25
.param var_vdd=1
.param var_vn=80n
.param var_wp=80n
*.param ratio=2

.temp var_temp

.subckt inv_mani vdd vin vout vss
xn0 vout vin vss vss nfet w=var_wn l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1
xp0 vout vin vdd pfet w='2*var_wp' l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1
.ends inv_mani

.tran 1p 1n
+sweep var_wn lin 6 40e-9 200e-9

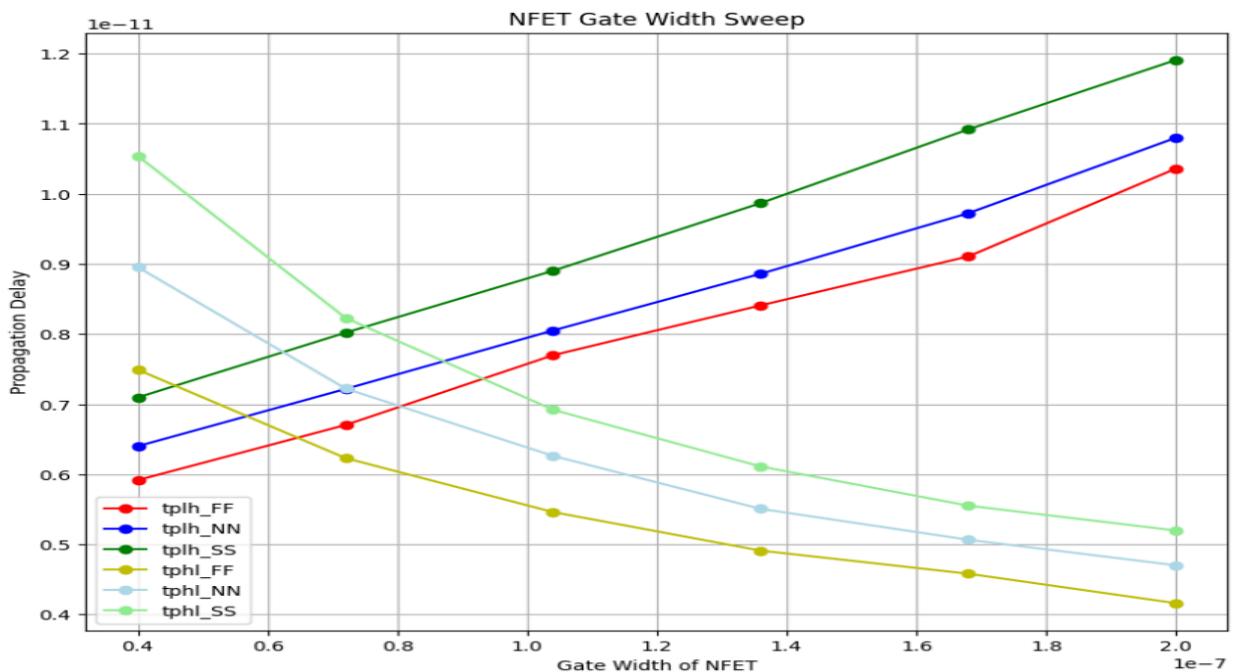
vdd vdd 0 DC=var_vdd
vss vss 0 DC=0
vin vin 0 pulse 0 var_vdd 0 1p 1p 0.05n 0.1n

*.measure tran phdly
*+trig v(vin)='var_vdd/2' fall=2
*+targ v(vout)='var_vdd/2' rise=2

.measure tran phfdly
*+trig v(vin)='var_vdd/2' rise=2
*+targ v(vout)='var_vdd/2' fall=2

.probe v(*)
.END
```

 Battery saver  
Battery saver is on



>Here as the width of the NFET is increasing , the width ratio decreases.

>This data is consistent with what we saw earlier , as the width ratio decreases, tPHL decreases and tPLH increases.

## D.

```
.OPTION post
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" FF
.include "fan_source"

.param var_temp=25
.param var_vdd=1
.param var_wn=80n
.param var_wp=80n
*.param ratio=2

.temp var_temp

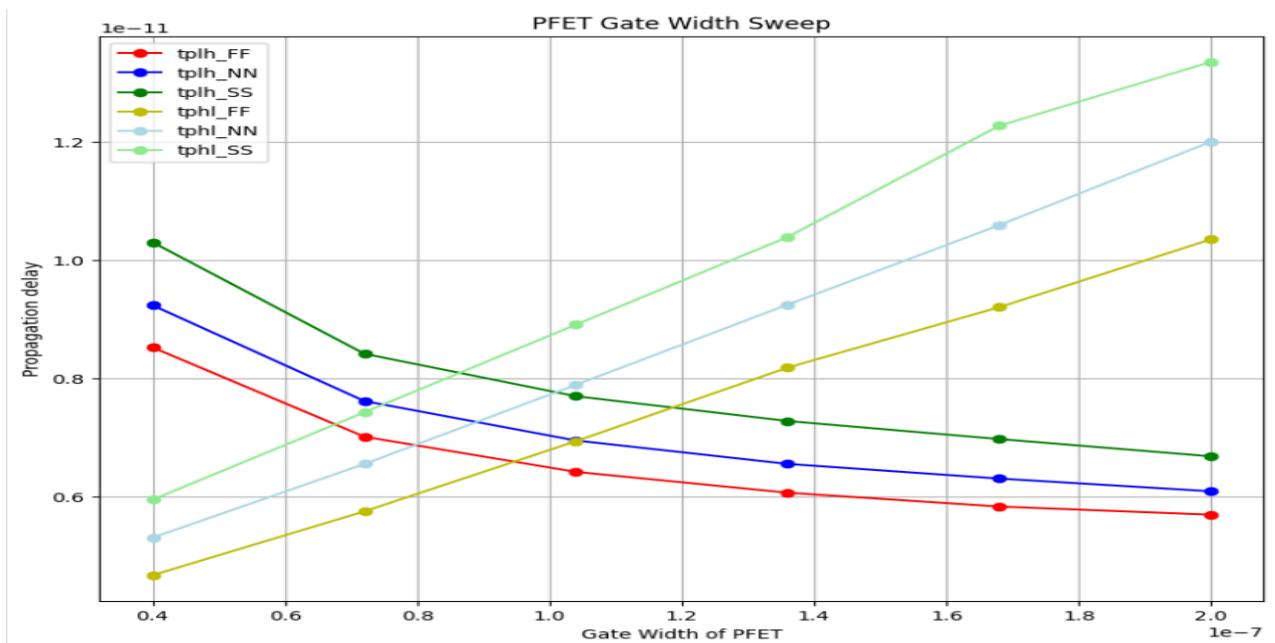
.subckt inv_mani vdd vin vout vss
x0 vout vin vss nfet w=var_wn l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1
x0 vout vdd vdd pfet w="2*var_wp" l=30e-9 nf=1 ps=312e-9 as=6.08e-15 ad=6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1
.ends inv_mani

.tran lp lin
+sweep var_wp|lin 6 40e-9 200e-9
vdd vdd 0 DC=var_vdd
vss vss 0 DC=0
vin vin 0 pulse 0 var_vdd 0 lp lp 0.05n 0.1n

*.measure tran phldly
*+trig v(vin)='var_vdd/2' fall=2
*+targ v(vout)='var_vdd/2' rise=2

.measure tran phldly
+trig v(vin)='var_vdd/2' rise=2
+targ v(vout)='var_vdd/2' fall=2

.probe v(*)
.END
```



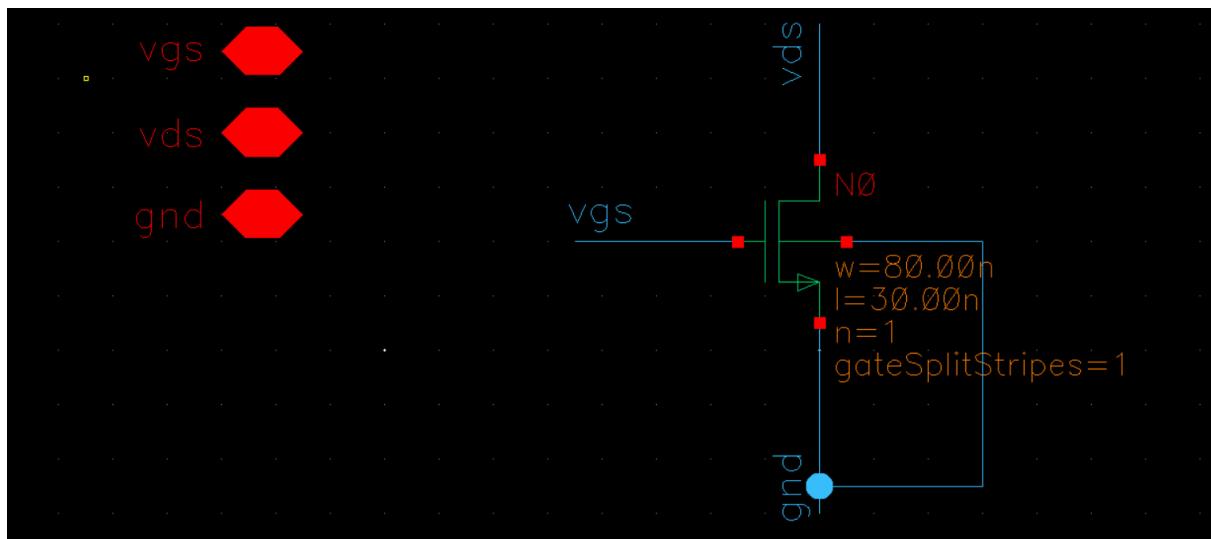
>Here as the width of the PFET is increasing , the width ratio increases.

>This data is consistent with what we saw earlier , as the width ratio increases, tPLH decreases and tPHL increases.

## 4.

### 4.1 NMOS

#### SCHEMATIC



#### INPUT DECK

```
*.TEMP 25.0
.OPTION post
+    ARTIST=2
+    INGOLD=2
+    PARHIER=LOCAL
+    PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN

.param par_temp=25
.param input=0
.param par_vgs=0.9
.param par_vds=0.9
.TEMP par_temp

*Id-Vds curve
v1 vds 0 DC=input
v2 vgs 0 DC=par_vgs
v0 gnd 0 DC=0

*Id_Vgs Curve
*v1 vds 0 DC=par_vds
*v2 vgs 0 DC=input
*v0 gnd 0 DC=0

.include "nmos_source"

.dc input 0 0.9 0.01
*+sweep par_vds 0.1 0.9 0.1
*+sweep par_vgs 0.1 0.9 0.1
+sweep par_temp -100 100 50
```

```

.meas dc slew1 DERIV(' -1*i(v1)' )AT=100m
*.meas dc vt1 PARAM='v(v2)-(i(v1)/slew1)' AT=100m

.meas dc slew2 DERIV(' -1*i(v1)' )AT=200m
*.meas dc vt2 PARAM='v(v2)-(i(v1)/slew2)' AT=200m

.meas dc slew3 DERIV(' -1*i(v1)' )AT=300m
*.meas dc vt3 PARAM='v(v2)-(i(v1)/slew3)' AT=300m

.meas dc slew4 DERIV(' -1*i(v1)' )AT=400m
*.meas dc vt4 PARAM='v(v2)-(i(v1)/slew4)' AT=400m

.meas dc slew5 DERIV(' -1*i(v1)' )AT=500m
*.meas dc vt5 PARAM='v(v2)-(i(v1)/slew5)' AT=500m

.meas dc slew6 DERIV(' -1*i(v1)' )AT=600m
*.meas dc vt6 PARAM='v(v2)-(i(v1)/slew6)' AT=600m

.meas dc slew7 DERIV(' -1*i(v1)' )AT=700m
*.meas dc vt7 PARAM='v(v2)-(i(v1)/slew7)' AT=700m

.meas dc slew8 DERIV(' -1*i(v1)' )AT=800m
*.meas dc vt8 PARAM='v(v2)-(i(v1)/slew8)' AT=800m

.meas dc slew9 DERIV(' -1*i(v1)' )AT=900m
*.meas dc vt9 PARAM='v(v2)-(i(v1)/slew9)' AT=900m

*.meas dc Id_Vg PARAM='I(v0)/v1'
.print DC i_out=par(' -1*I(v1)' )

.probe v(*)
.probe i(*)
.end

```

## NETLIST(nmos\_source)

```

xn0 vds vgs gnd vds nfet w=8e-9 l=30e-9 nf=1 ps=312e-9 pd=312e-9 as=6.08e-15 ad=
6.08e-15 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 plorient=l pccrit=1 p_la=0 ngcon=1

```

## CALCULATIONS:

>The code in the input deck allows you to calculate slope at 9 different points .  
 Look at the points where there is not much change in the value of the slope. This would mean that we are looking at points where the slope is almost constant. Take the aggregate of these values

>**Vt calculation**– Now that we know the slope at each point , the code lets you calculate the x-axis intercept for a line drawn ,at each point, whose slope is equal to the slope of the curve calculated at that point. We again look for the values which show constant value. Taking the aggregate of these intercepts gives a value approx. equal to the Vt(threshold voltage).

>**ro calculation**- The code in the input deck allows you to calculate slope at 9 different points .

To measure the 1/ro value , look at the points where there is not much change in the value of the slope. This would mean that we are looking at points where the slope is

almost constant. Take the aggregate of these values and this should be approximately equal to the  $1/ro$  value . Just invert the value which you get to get  $ro$ .

**>gm calculation-** It's value is just the slope of the  $Id$  vs  $Vgs$  curve at different points.

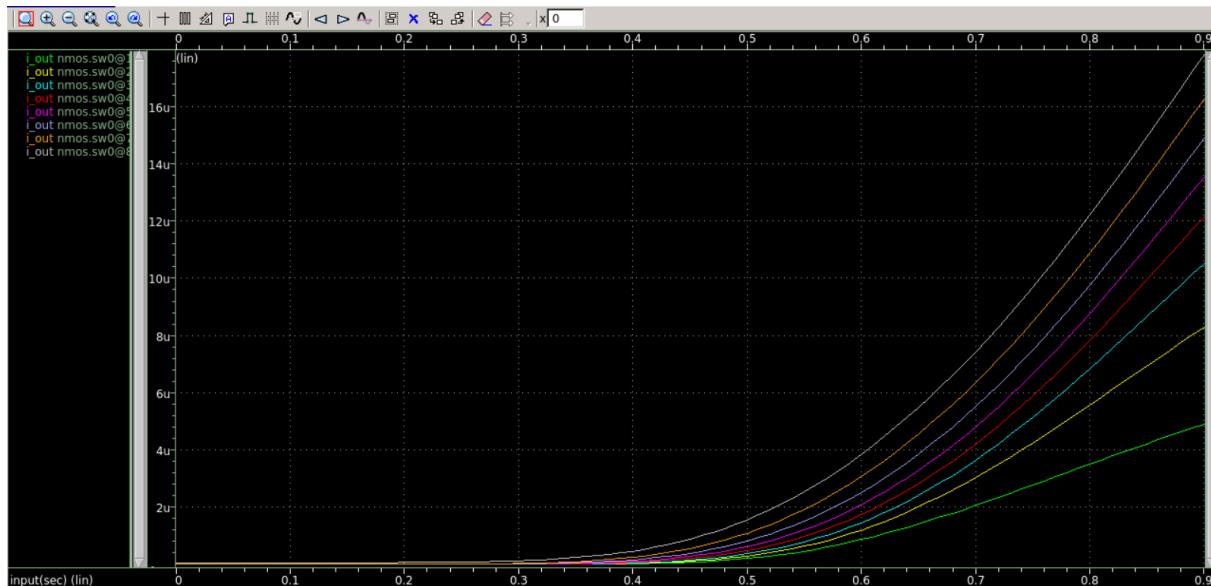
>I have simulated all the graphs for 3 different W/L ratios.

i)  $w=8n$  ,  $I=30n$

ii) $w=70n$  ,  $I=20n$

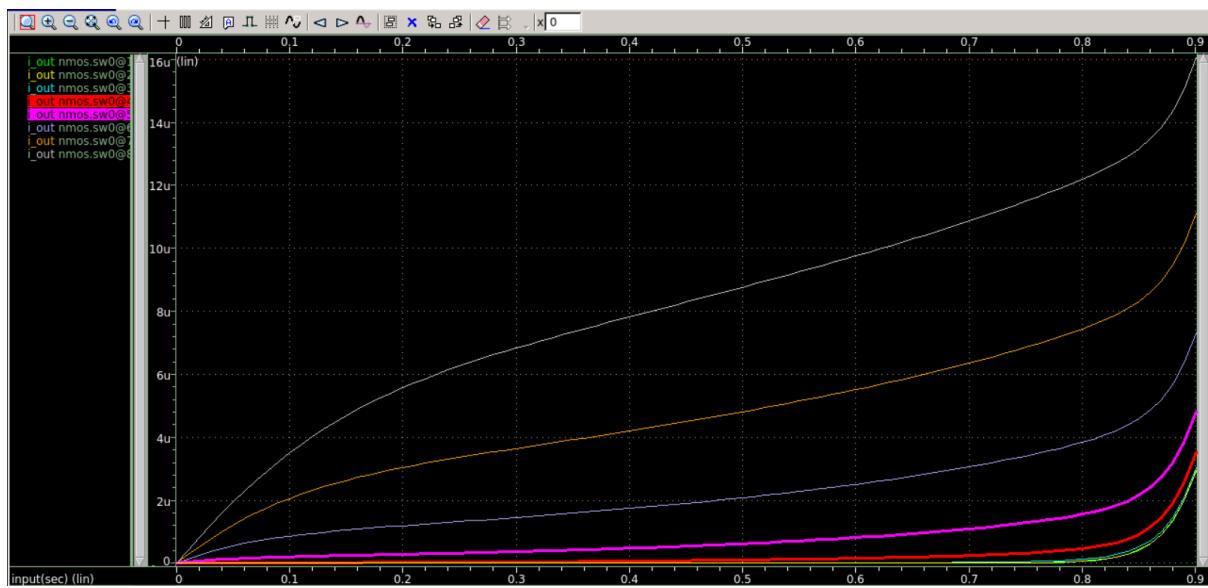
iii) $w=80n$  ,  $I=30n$

i)  $w=8n$  ,  $I=30n$



Id vs Vgs

	slew1	vt1	slew2				
	slew1	vt1	slew2				
	vt2	slew3	vt3				
	slew4	vt4	slew5				
	vt5	slew6	vt6				
	slew7	vt7	slew8				
	vt8	slew9	vt9				
	temper	alter#					
1.000e-01	1.295e-10	3.780e+04	2.111e-09				
	2.319e+03	3.504e-08	1.397e+02				
	5.103e-07	9.591e+00	3.479e-06				
	1.407e+00	9.289e-06	5.269e-01				
	1.367e-05	3.580e-01	1.455e-05				
	3.364e-01	1.317e-05	3.716e-01				
	2.500e+01	1					
2.000e-01	2.224e-10	3.719e+04	3.511e-09				
	2.356e+03	5.649e-08	1.464e+02				
	7.611e-07	1.087e+01	4.699e-06				
	1.760e+00	1.319e-05	6.272e-01				
	2.232e-05	3.707e-01	2.692e-05				
	3.073e-01	2.655e-05	3.116e-01				
	2.500e+01	1					
3.000e-01	3.756e-10	2.798e+04	5.675e-09	7.000e-01	6.894e-09	2.361e+03	6.584e-08
	1.852e+03	8.753e-08	1.201e+02		2.472e+02	6.558e-07	2.482e+01
	1.066e-06	9.860e+00	5.791e-06		4.085e-06	3.984e+00	1.285e-05
	1.815e+00	1.551e-05	6.776e-01		1.266e+00	2.559e-05	6.359e-01
	2.704e-05	3.887e-01	3.506e-05		3.888e-05	4.186e-01	4.978e-05
	2.997e-01	3.726e-05	2.821e-01		3.269e-01	5.675e-05	2.868e-01
	2.500e+01	1			2.500e+01	1	
4.000e-01	6.632e-10	1.832e+04	9.438e-09		5.241e-09	3.397e+03	1.594e-07
	1.287e+03	1.374e-07	8.841e+01		1.117e+02	1.228e-06	1.450e+01
	1.478e-06	8.219e+00	7.047e-06		5.899e-06	3.018e+00	1.579e-05
	1.724e+00	1.768e-05	6.871e-01		1.127e+00	2.877e-05	6.189e-01
	3.032e-05	4.007e-01	4.030e-05		4.160e-05	4.279e-01	5.200e-05
	3.014e-01	4.482e-05	2.711e-01	9.000e-01	3.423e-01	5.886e-05	3.024e-01
	2.500e+01	1			2.500e+01	1	
5.000e-01	1.264e-09	1.071e+04	1.651e-08		-2.542e-13	-8.572e+07	2.581e-07
	8.201e+02	2.217e-07	6.108e+01		8.440e+01	1.963e-06	1.110e+01
	2.052e-06	6.599e+00	8.571e-06		7.661e-06	2.844e+00	1.816e-05
	1.580e+00	2.002e-05	6.765e-05		1.200e+00	3.102e-05	7.024e-01
	2.500e+01	1			4.078e-01	5.021e-01	5.342e-05
						6.026e-05	3.615e-01
						2.500e+01	1



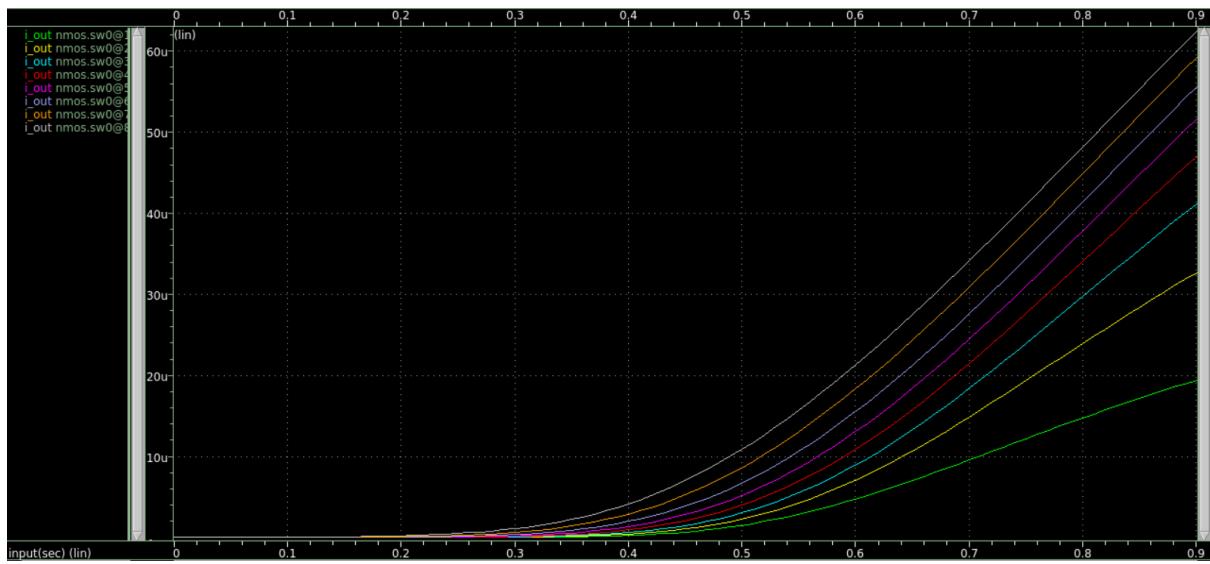
Id vs Vds

par_vgs	slew1	slew2	slew3
	slew4	slew5	slew6
	slew7	slew8	slew9
temper			
1.000e-01	3.622e-11	5.020e-11	8.983e-11
	1.819e-10	4.403e-10	1.942e-09
	4.151e-08	1.923e-06	9.442e-05
	2.500e+01	1	
2.000e-01	5.301e-10	6.953e-10	1.174e-09
	2.167e-09	4.416e-09	1.094e-08
	6.548e-08	1.970e-06	9.440e-05
	2.500e+01	1	
3.000e-01	8.398e-09	1.033e-08	1.638e-08
	2.779e-08	5.020e-08	9.880e-08
	2.506e-07	2.385e-06	9.461e-05
	2.500e+01	1	
4.000e-01	1.207e-07	1.294e-07	1.816e-07
	2.683e-07	4.105e-07	6.582e-07
	1.160e-06	3.869e-06	9.524e-05
	2.500e+01	1	
5.000e-01	2.500e+01	7.858e-07	9.380e-07
	1.018e-06	1.622e-06	2.253e-06
	1.211e-06	6.621e-06	9.622e-05
	3.300e-06		
	2.500e+01	1	
6.000e-01	4.934e-06	2.658e-06	2.625e-06
	3.063e-06	3.764e-06	4.775e-06
	6.259e-06	9.844e-06	9.724e-05
	2.500e+01	1	
7.000e-01	1.438e-05	7.227e-06	5.589e-06
	5.698e-06	6.444e-06	7.612e-06
	9.240e-06	1.271e-05	9.812e-05
	2.500e+01	1	
8.000e-01	2.787e-05	1.591e-05	1.083e-05
	9.406e-06	9.535e-06	1.043e-05
	1.185e-05	1.493e-05	9.893e-05
	2.500e+01	1	
9.000e-01	4.209e-05	2.767e-05	1.891e-05
	1.487e-05	1.348e-05	1.350e-05
	1.430e-05	1.676e-05	9.992e-05

Vds , Vt(avg of 3 values which are closest to eachother)  
0.1, 0.355  
0.2, 0.33  
0.3, 0.29  
0.4, 0.286  
0.5, 0.27  
0.6, 0.276  
0.7, 0.2686  
Vt(avg)=0.3V

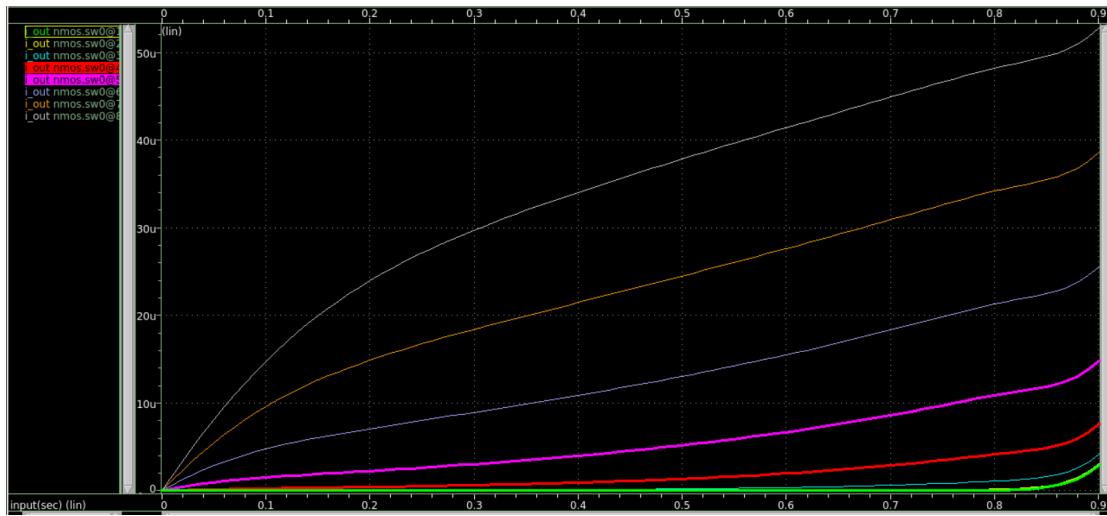
Vgs , ro(avg of 3 values which are closest to eachother)  
0.1, 1.7e10  
0.2, 3.86e8  
0.3, 2.93e7  
0.4, 5.71e6  
0.5, 6.67e5  
0.6, 3.6e5  
0.7, 1.6e5  
0.8, 8.55e4  
0.9, 6.58e4

$$\text{ii) } w=70n, l=20n$$



## Id vs Vgs

par_vds	slew1	vt1	slew2				
	vt2	slew3	vt3				
	slew4	vt4	slew5				
	vt5	slew6	vt6				
	slew7	vt7	slew8				
	vt8	slew9	vt9				
	temper	alter#					
1.000e-01	5.130e-09	3.782e+03	5.583e-08				
	3.475e+02	5.991e-07	3.238e+01				
	4.954e-06	3.916e+00	2.047e-05				
	9.476e-01	4.162e-05	4.662e-01				
	5.182e-05	3.744e-01	5.009e-05				
	3.873e-01	4.319e-05	4.492e-01				
	2.500e+01	1					
2.000e-01	9.391e-09	3.478e+03	9.954e-08				
	3.281e+02	1.027e-06	3.182e+01				
	7.679e-06	4.254e+00	2.971e-05				
	1.099e+00	6.356e-05	5.139e-01				
	8.695e-05	3.757e-01	9.090e-05				
	3.593e-01	8.332e-05	3.920e-01				
	2.500e+01	1		6.000e-01	1.145e-07	4.853e+02	9.181e-07
3.000e-01	1.662e-08	2.476e+03	1.697e-07		6.053e+01	6.431e-06	8.642e+00
	2.425e+02	1.651e-06	2.492e+01		2.705e-05	2.055e+00	6.539e-05
	1.088e-05	3.782e+00	3.764e-05		8.500e-01	1.055e-04	5.268e-01
	1.093e+00	7.675e-05	5.360e-01		1.313e-04	4.233e-01	1.412e-04
	1.064e-04	3.865e-01	1.159e-04		3.936e-01	1.410e-04	3.942e-01
	3.550e-01	1.113e-04	3.696e-01	7.000e-01	2.500e+01	1	
	2.500e+01	1			3.371e+01	1.019e-05	5.811e+00
4.000e-01	3.000e-08	1.567e+03	2.906e-07		3.571e-05	1.658e+00	7.580e-05
	1.618e+02	2.611e-06	1.801e+01		7.810e-01	1.127e-04	5.253e-01
	1.497e-05	3.140e+00	4.609e-05		1.345e-04	4.401e-01	1.426e-04
	1.020e+00	8.738e-05	5.380e-01	8.000e-01	4.152e-01	1.422e-04	4.163e-01
	1.181e-04	3.979e-01	1.298e-04		2.500e+01	1	
	3.623e-01	1.278e-04	3.678e-01		8.409e-08	7.424e+02	3.305e-06
	2.500e+01	1			1.889e+01	1.564e-05	3.991e+00
5.000e-01	5.655e-08	9.127e+02	5.074e-07		4.538e-05	1.376e+00	8.507e-05
	1.017e+02	4.097e-06	1.260e+01	9.000e-01	7.338e-01	1.177e-04	5.302e-01
	2.025e-05	2.549e+00	5.536e-05		1.358e-04	4.595e-01	1.423e-04
	9.323e-01	9.694e-05	5.324e-01		4.387e-01	1.418e-04	4.404e-01
	1.260e-04	4.097e-01	1.373e-04		2.500e+01	1	
	3.758e-01	1.367e-04	3.774e-01		1.958e-09	3.427e+04	4.175e-06

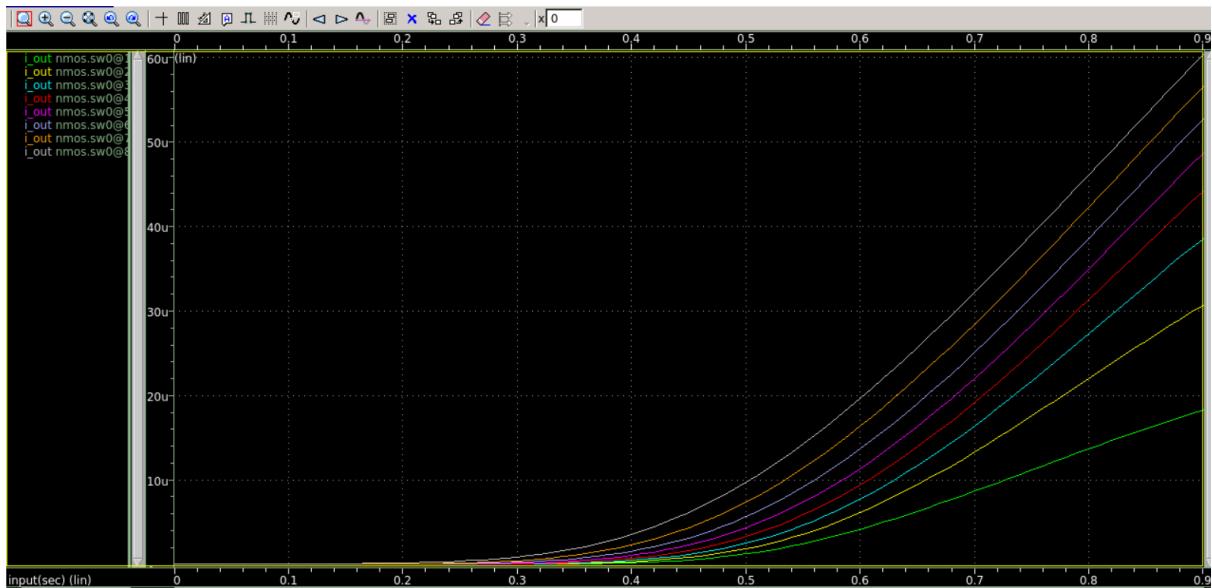


Id vs vds

par_vgs	slew1	slew2	slew3
	slew4	slew5	slew6
	slew7	slew8	slew9
temper	alter#		
1.000e-01	1.730e-09	2.574e-09	4.726e-09
	9.326e-09	1.978e-08	4.128e-08
	4.869e-08	1.860e-06	9.471e-05
	2.500e+01	1	
2.000e-01	1.805e-08	2.541e-08	4.377e-08
	7.924e-08	1.518e-07	3.111e-07
	6.426e-07	2.265e-06	9.502e-05
	2.500e+01	1	
3.000e-01	1.890e-07	2.479e-07	3.948e-07
	6.448e-07	1.080e-06	1.888e-06
	3.431e-06	5.720e-06	9.636e-05
	2.500e+01	1	
4.000e-01	1.639e-06	1.788e-06	2.463e-06
	3.470e-06	4.963e-06	7.272e-06
	1.085e-05	1.292e-05	9.917e-05
	2.500e+01	1	
5.000e-01	9.007e-06	7.249e-06	8.482e-06
	1.049e-05	1.317e-05	1.675e-05
	2.131e-05	2.108e-05	1.025e-04
	2.500e+01	1	
6.000e-01	3.167e-05	1.947e-05	1.858e-05
	2.029e-05	2.290e-05	2.614e-05
	2.969e-05	2.650e-05	1.052e-04
	2.500e+01	1	
7.000e-01	7.230e-05	4.150e-05	3.195e-05
	3.005e-05	3.061e-05	3.208e-05
	3.365e-05	2.854e-05	1.069e-04
	2.500e+01	1	
8.000e-01	1.206e-04	7.229e-05	4.913e-05
	3.996e-05	3.649e-05	3.529e-05
	3.472e-05	2.874e-05	1.082e-04
	2.500e+01	1	
9.000e-01	1.670e-04	1.071e-04	7.000e-05
	5.147e-05	4.248e-05	3.784e-05
	3.490e-05	2.844e-05	1.095e-04

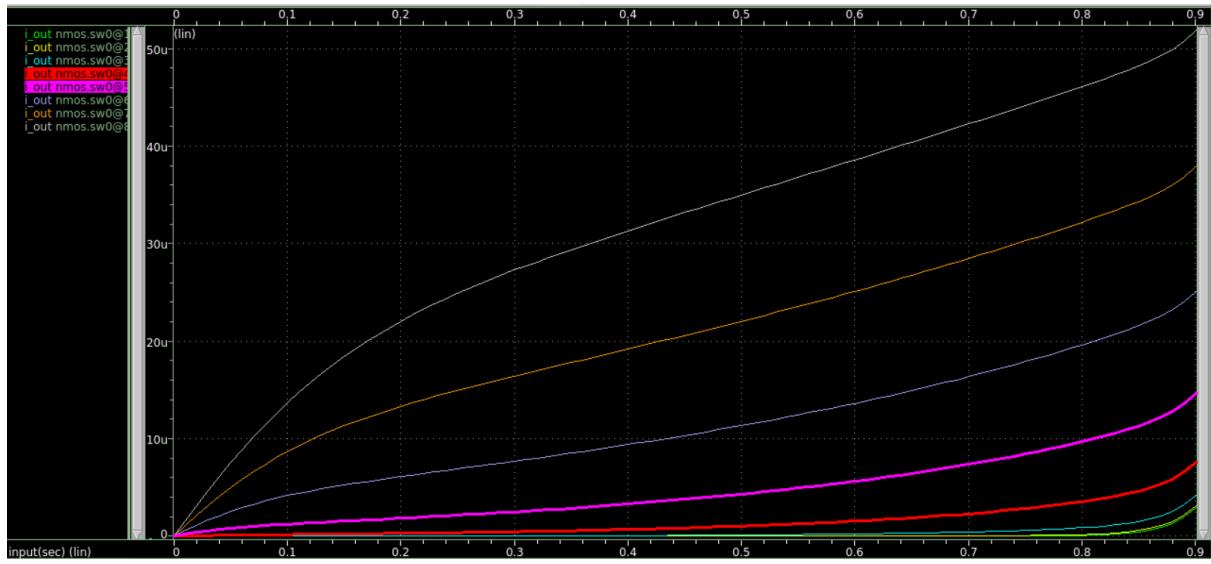
<u>Vds</u> , <u>vt</u> (avg of 3 values which are closest to eachother)	<u>Vgs</u> , <u>ro</u> (avg of 3 values which are closest to eachother)
0.1,0.4039	0.1,3.3e8
0.2,0.376	0.2,3.45e7
0.3,0.37	0.3,2.32e6
0.4,0.376	0.4,3.15e5
0.5,0.3875	0.5,6.48e4
0.6,0.394	0.6,3.8e4
0.7,0.4155	0.7,3.2e4
	0.8,2.817e4
Vt(avg)=0.389V	0.9,2.96e4

iii)  $w=80n$  ,  $l=30n$



Id vs Vgs

par_vds	slew1	vt1	slew2			
	vt2	slew3	vt3			
	slew4	vt4	slew5			
	vt5	slew6	vt6			
	slew7	vt7	slew8			
	vt8	slew9	vt9			
	temper	alter#				
1.000e-01	1.674e-09	1.094e+04	2.421e-08	6.000e-01	4.913e-08	1.073e+03
	7.568e+02	3.492e-07	5.246e+01		1.003e+02	4.757e-06
	3.844e-06	4.765e+00	1.796e-05		2.265e-05	1.108e+01
	1.020e+00	3.792e-05	4.831e-01		2.328e+00	5.773e-05
	4.917e-05	3.726e-01	4.932e-05		9.133e-01	9.752e-05
	3.714e-01	4.365e-05	4.196e-01		1.264e-04	5.406e-01
	2.500e+01	1			4.170e-01	1.396e-04
2.000e-01	3.198e-09	9.599e-03	4.494e-08		3.775e-01	1.413e-04
	6.830e+02	6.223e-07	4.932e+01		2.500e+01	3.732e-01
	6.026e-06	5.093e+00	2.567e-05	7.000e-01	1.183e-07	4.781e+02
	1.196e+00	5.708e-05	5.377e-01		5.271e+01	7.829e-06
	8.173e-05	3.755e-01	8.896e-05		3.048e-05	7.226e+00
	3.450e-01	8.373e-05	3.666e-01		8.286e-01	6.827e-05
	2.500e+01	1			1.062e-04	5.326e-01
3.000e-01	5.963e-09	6.473e+03	8.064e-08		1.312e-04	4.311e-01
	4.786e+02	1.052e-06	3.669e+01		3.989e-01	1.426e-04
	8.692e-06	4.440e+00	3.245e-05		2.500e+01	3.966e-01
	1.189e+00	6.876e-05	5.613e-01		3.061e-07	1.971e+02
	9.988e-05	3.864e-01	1.132e-04		2.580e+01	2.338e-06
	3.410e-01	1.115e-04	3.463e-01		1.294e-05	4.664e+00
	2.500e+01	1			4.053e-05	7.928e-05
4.000e-01	1.140e-08	3.875e+03	1.463e-07		7.610e-01	1.135e-04
	3.019e+02	1.753e-06	2.519e+01		1.339e-04	5.316e-01
	1.216e-05	3.632e+00	3.986e-05		4.505e-01	1.418e-04
	1.108e+00	7.871e-05	5.612e-01		4.255e-01	4.258e-01
	1.114e-04	3.965e-01	1.270e-04		2.500e+01	1
	3.479e-01	1.278e-04	3.455e-01	9.000e-01	1.969e-07	3.350e+02
	2.500e+01	1			1.583e+01	4.168e-06
5.000e-01	2.281e-08	2.134e+03	2.721e-07		1.852e-05	3.562e+00
	1.789e+02	2.896e-06	1.681e+01		4.917e-05	8.708e-05
	1.670e-05	2.915e+00	4.824e-05		7.575e-01	1.177e-04
	1.009e+00	8.825e-05	5.516e-01		1.348e-04	5.606e-01
	1.199e-04	4.061e-01	1.350e-04		4.677e-01	1.410e-04
	3.605e-01	1.368e-04	3.557e-01		2.500e+01	4.695e-01



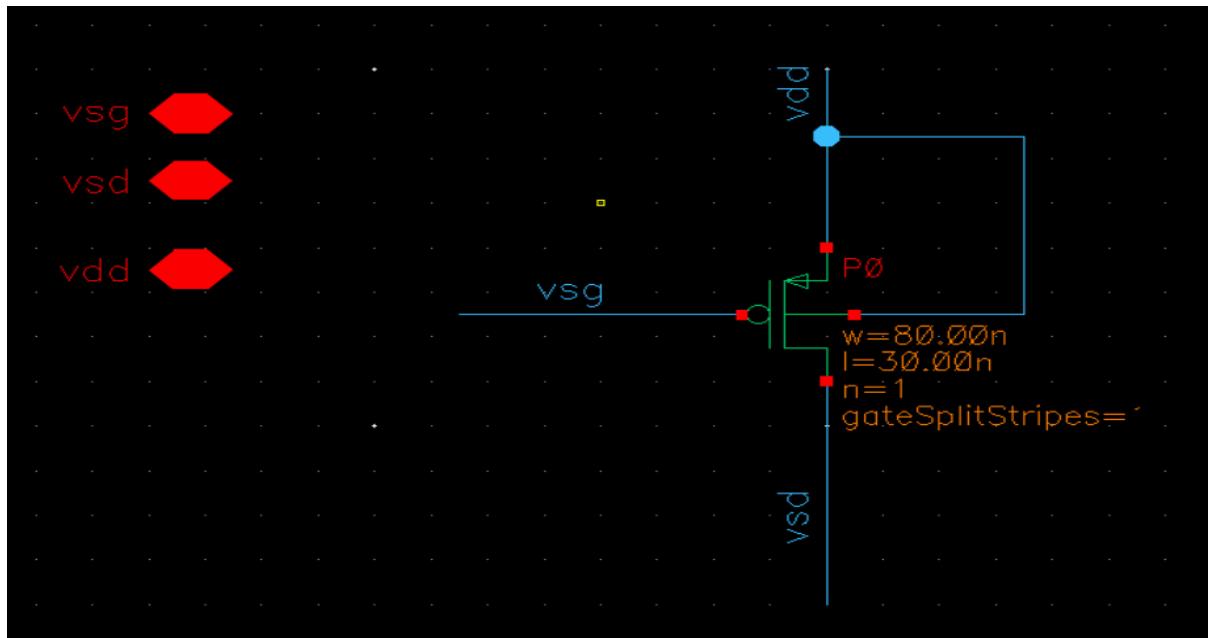
Id vs Vds

par_vgs	slew1	slew2	slew3
	slew4	slew5	slew6
	slew7	slew8	slew9
temper	alter#		
1.000e-01	5.282e-10	8.562e-10	1.660e-09
	3.451e-09	7.856e-09	2.067e-08
	8.972e-08	1.938e-06	9.472e-05
	2.500e+01	1	
2.000e-01	7.295e-09	1.123e-08	2.053e-08
	3.940e-08	7.998e-08	1.763e-07
	4.604e-07	2.860e-06	9.516e-05
	2.500e+01	1	
3.000e-01	1.020e-07	1.469e-07	2.486e-07
	4.295e-07	7.548e-07	1.367e-06
	2.639e-06	6.854e-06	9.740e-05
	2.500e+01	1	
4.000e-01	1.149e-06	1.351e-06	1.921e-06
	2.770e-06	4.032e-06	5.992e-06
	9.237e-06	1.588e-05	1.016e-04
	2.500e+01	1	
5.000e-01	7.158e-06	5.932e-06	7.077e-06
	8.892e-06	1.137e-05	1.478e-05
	1.963e-05	2.716e-05	1.061e-04
	2.500e+01	1	
6.000e-01	2.688e-05	1.639e-05	1.604e-05
	1.796e-05	2.086e-05	2.463e-05
	2.940e-05	3.564e-05	1.093e-04
	2.500e+01	1	
7.000e-01	6.416e-05	3.619e-05	2.849e-05
	2.775e-05	2.932e-05	3.193e-05
	3.522e-05	3.924e-05	1.107e-04
	2.500e+01	1	
8.000e-01	1.106e-04	6.539e-05	4.509e-05
	3.793e-05	3.603e-05	3.627e-05
	3.743e-05	3.931e-05	1.112e-04
	2.500e+01	1	
9.000e-01	1.567e-04	9.959e-05	6.564e-05
	4.953e-05	4.236e-05	3.927e-05
	3.794e-05	3.784e-05	1.115e-04

$V_{ds}$ , $V_t$ (avg of 3 values which are closest to eachother)	$V_{gs}$ , $V_o$ (avg of 3 values which are closest to eachother)
0.1, 0.387	0.1, 5e8
0.2, 0.3621	0.2, 3.66e7
0.3, 0.358	0.3, 3.63e6
0.4, 0.3633	0.4, 2.356e5
0.5, 0.3741	0.5, 6.55e4
0.6, 0.389	0.6, 4e4
0.7, 0.41	0.7, 3.125e4
	0.8, 2.74e4
	0.9, 2.6e4
$V_t$ (avg)=0.377	

## 4.2. PMOS

### SCHEMATIC:



### INPUT DECK:

```

.OPTION post
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

.LIB "/tools/pdk/samsung/LN28LPP_HSPICE_S00-V2.1.0.1/HSPICE/LN28LPP_Hspice.lib" NN

.param par_temp=25
.param input=0.9
.param par_vsg=0
.param par_vsd=0

.TEMP par_temp

*Id-Vsd curve
v1 vsd 0 DC=input
v2 vsg 0 DC=par_vsg
v0 vdd 0 DC=0.9

*Id-Vsg curve
*v1 vsd 0 DC=par_vsd
*v2 vsg 0 DC=input
*v0 vdd 0 DC=0.9

.include "pmos_source"

.dc input 0.9 0.01
+sweep par_vsd 0.1 0.9 0.1
+sweep par_vsg 0.1 0.9 0.1
+sweep par_temp -200 200 100
*.meas dc slew1 DERIV('-1*i(v1)')AT=100m
*.meas dc slew2 DERIV('-1*i(v1)')AT=200m
*.meas dc slew3 DERIV('-1*i(v1)')AT=300m
*.meas dc slew4 DERIV('-1*i(v1)')AT=400m
*.meas dc slew5 DERIV('-1*i(v1)')AT=500m
*.meas dc slew6 DERIV('-1*i(v1)')AT=600m
*.meas dc slew7 DERIV('-1*i(v1)')AT=700m
*.meas dc slew8 DERIV('-1*i(v1)')AT=800m
*.meas dc slew9 DERIV('-1*i(v1)')AT=900m

*.meas dc vt1 PARAM='v(v2)-(i(v1)/slew1)'AT=100m
*.meas dc vt2 PARAM='v(v2)-(i(v1)/slew2)'AT=200m
*.meas dc vt3 PARAM='v(v2)-(i(v1)/slew3)'AT=300m
*.meas dc vt4 PARAM='v(v2)-(i(v1)/slew4)'AT=400m
*.meas dc vt5 PARAM='v(v2)-(i(v1)/slew5)'AT=500m
*.meas dc vt6 PARAM='v(v2)-(i(v1)/slew6)'AT=600m
*.meas dc vt7 PARAM='v(v2)-(i(v1)/slew7)'AT=700m
*.meas dc vt8 PARAM='v(v2)-(i(v1)/slew8)'AT=800m
*.meas dc vt9 PARAM='v(v2)-(i(v1)/slew9)'AT=900m

*.meas dc Id_Vg PARAM='I(v0)/v1'
.print DC i_out=par('I(v1)')

.probe v(*)
.probe i(*)
.end

```

NETLIST(pmios\_source)

```
xp0 vsd vsg vdd vdd pfet w=10e-9 l=70e-9 nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwel  
l=0 plorient=1 pccrit=1 p_la=0 ngcon=1
```

>CALCULATIONS : are similar to how it is for nmos.

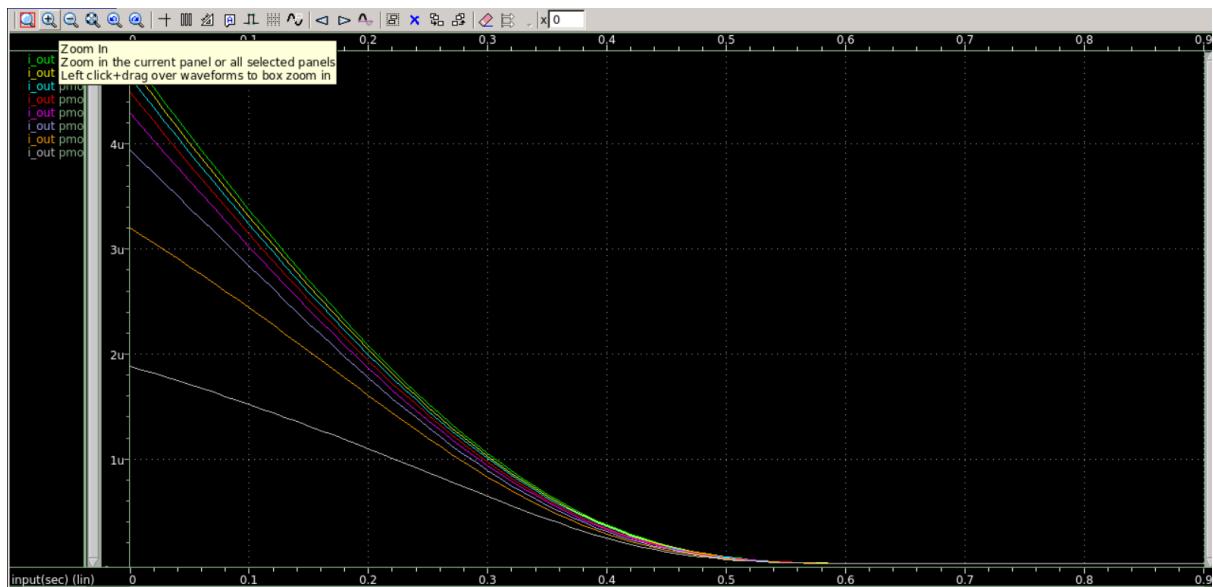
>I have simulated all the graphs for 3 different W/L ratios.

i)  $w=10n$ ,  $l=70n$

ii)  $w=80n$ ,  $l=30n$

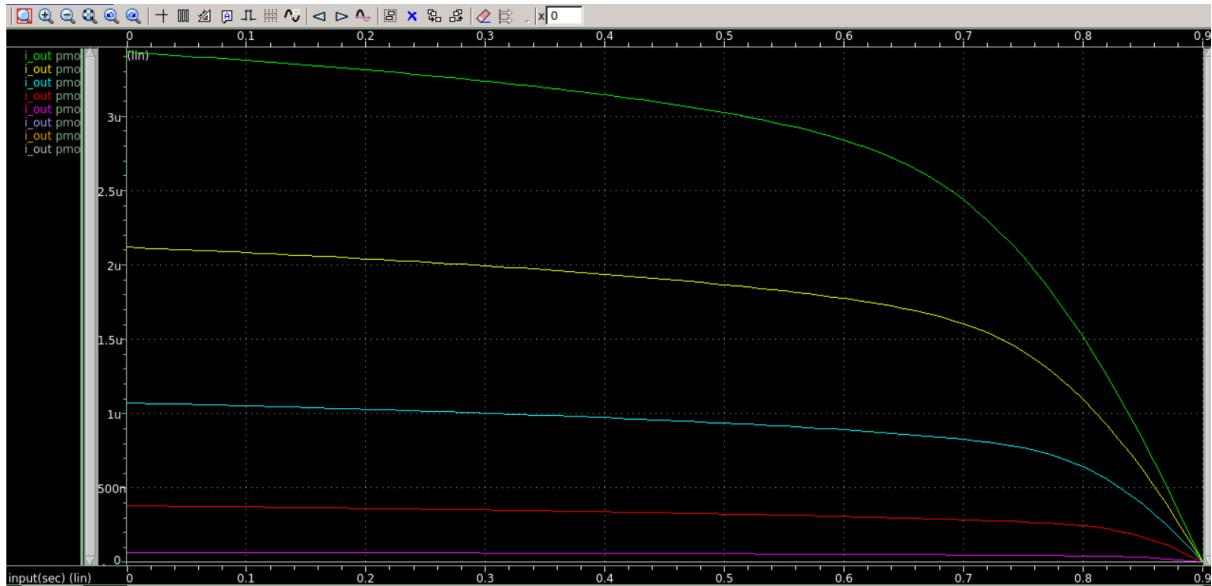
iii)  $w=300n$ ,  $l=30n$

i)  $w=10n$ ,  $l=70n$



Id vs vgs

par_vsd	slew1	slew2	slew3			
	slew4	slew5	slew6			
	slew7	slew8	slew9			
	vt1	vt2	vt3			
	vt4	vt5	vt6			
	vt7	vt8	vt9			
	temper	alter#				
1.000e-01	1.383e-05	1.164e-05	8.499e-06			
	4.661e-06	1.342e-06	1.326e-07			
	8.457e-09	5.412e-10	4.698e-11			
	-3.498e-01	-4.156e-01	-5.695e-01			
	-1.038e+00	-3.606e+00	-3.649e+01			
	-5.722e+02	-8.943e+03	-1.030e+05			
	2.500e+01	1				
2.000e-01	1.359e-05	1.144e-05	8.341e-06	6.000e-01	1.106e-05	9.885e-06
	4.557e-06	1.304e-06	1.287e-07		3.946e-06	1.089e-06
	8.213e-09	5.266e-10	4.661e-11		6.812e-09	4.411e-10
	-3.495e-01	-4.150e-01	-5.693e-01		-3.561e-01	-3.986e-01
	-1.042e+00	-3.641e+00	-3.691e+01		-9.985e-01	-3.619e+00
	-5.782e+02	-9.018e+03	-1.019e+05		-5.784e+02	-8.933e+03
	2.500e+01	1			2.500e+01	1
3.000e-01	1.328e-05	1.120e-05	8.158e-06	7.000e-01	8.132e-06	8.337e-06
	4.440e-06	1.261e-06	1.242e-07		3.683e-06	1.003e-06
	7.939e-09	5.099e-10	4.540e-11		6.244e-09	4.062e-10
	-3.492e-01	-4.141e-01	-5.685e-01		-3.939e-01	-3.842e-01
	-1.044e+00	-3.677e+00	-3.734e+01		-8.698e-01	-3.194e+00
	-5.842e+02	-9.095e+03	-1.022e+05		-5.130e+02	-7.887e+03
	2.500e+01	1			2.500e+01	1
4.000e-01	1.287e-05	1.090e-05	7.940e-06	8.000e-01	3.978e-06	4.470e-06
	4.305e-06	1.213e-06	1.191e-07		3.059e-06	8.774e-07
	7.625e-09	4.908e-10	4.381e-11		5.428e-09	3.553e-10
	-3.493e-01	-4.125e-01	-5.661e-01		-4.738e-01	-4.217e-01
	-1.044e+00	-3.706e+00	-3.775e+01		-6.163e-01	-2.148e+00
	-5.895e+02	-9.160e+03	-1.026e+05		-3.473e+02	-5.305e+03
	2.500e+01	1			2.500e+01	1
5.000e-01	1.226e-05	1.050e-05	7.669e-06	9.000e-01	-1.114e-13	-7.607e-14
	4.145e-06	1.157e-06	1.131e-07		-2.147e-14	-9.240e-15
	7.257e-09	4.683e-10	4.191e-11		-1.149e-15	-3.465e-16
	-3.503e-01	-4.090e-01	-5.597e-01		-3.021e-01	-4.424e-01
	-1.036e+00	-3.712e+00	-3.794e+01		-1.568e+00	-3.642e+00
	-5.915e+02	-9.166e+03	-1.024e+05		-2.929e+01	-9.713e+01
	2.500e+01	1			2.500e+01	1



Id vs Vds

par_vsg	slew1	slew2	slew3
	slew4	slew5	slew6
	slew7	slew8	slew9
	temper	alter#	
1.000e-01	5.960e-07	6.937e-07	8.337e-07
	1.053e-06	1.453e-06	2.554e-06
	6.483e-06	1.260e-05	1.760e-05
	2.500e+01	1	
2.000e-01	3.875e-07	4.431e-07	5.192e-07
	6.300e-07	8.073e-07	1.161e-06
	2.863e-06	8.260e-06	1.359e-05
	2.500e+01	1	
3.000e-01	2.167e-07	2.443e-07	2.807e-07
	3.314e-07	4.068e-07	5.303e-07
	8.662e-07	3.918e-06	9.032e-06
	2.500e+01	1	
4.000e-01	8.967e-08	1.000e-07	1.134e-07
	1.313e-07	1.569e-07	1.960e-07
	2.629e-07	9.310e-07	4.406e-06
	2.500e+01	1	
5.000e-01	1.904e-08	2.117e-08	2.389e-08
	2.751e-08	3.256e-08	4.010e-08
	5.236e-08	1.082e-07	1.066e-06
	2.500e+01	1	
6.000e-01	1.572e-09	1.751e-09	1.982e-09
	2.289e-09	2.720e-09	3.367e-09
	4.422e-09	8.392e-09	9.631e-08
	2.500e+01	1	
7.000e-01	9.734e-11	1.082e-10	1.224e-10
	1.413e-10	1.679e-10	2.081e-10
	2.744e-10	5.303e-10	6.314e-09
	2.500e+01	1	
8.000e-01	8.276e-12	8.653e-12	9.483e-12
	1.066e-11	1.232e-11	1.485e-11
	1.909e-11	3.620e-11	4.256e-10
	2.500e+01	1	
9.000e-01	3.734e-12	2.726e-12	2.550e-12
	2.591e-12	2.695e-12	2.861e-12
	3.148e-12	4.376e-12	3.252e-11
	2.500e+01	1	

|Vds| , Vt(avg of 3 values which are closest to eachother)

```

0.1, -0.445
0.2, -0.4446
0.3, -0.439
0.4, -0.4426
0.5, -0.4395
0.6, -0.4310
0.7, -0.418
0.8, -0.439
Vt(avg)=-0.437 V

```

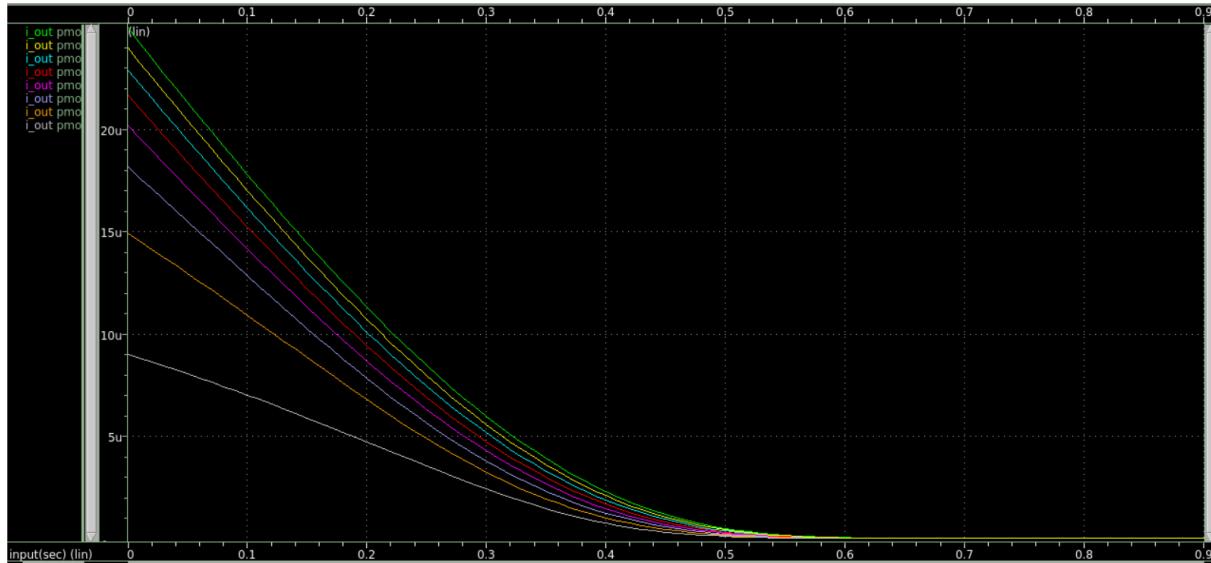
|Vgs| ,  $\text{f}_0$

```

0.1, 1.41e6
0.2, 2.22e6
0.3, 4e6
0.4, 1e7
0.5, 4.68e7
0.6, 5.66e8
0.7, 9.165e9
0.8, 1.136e4

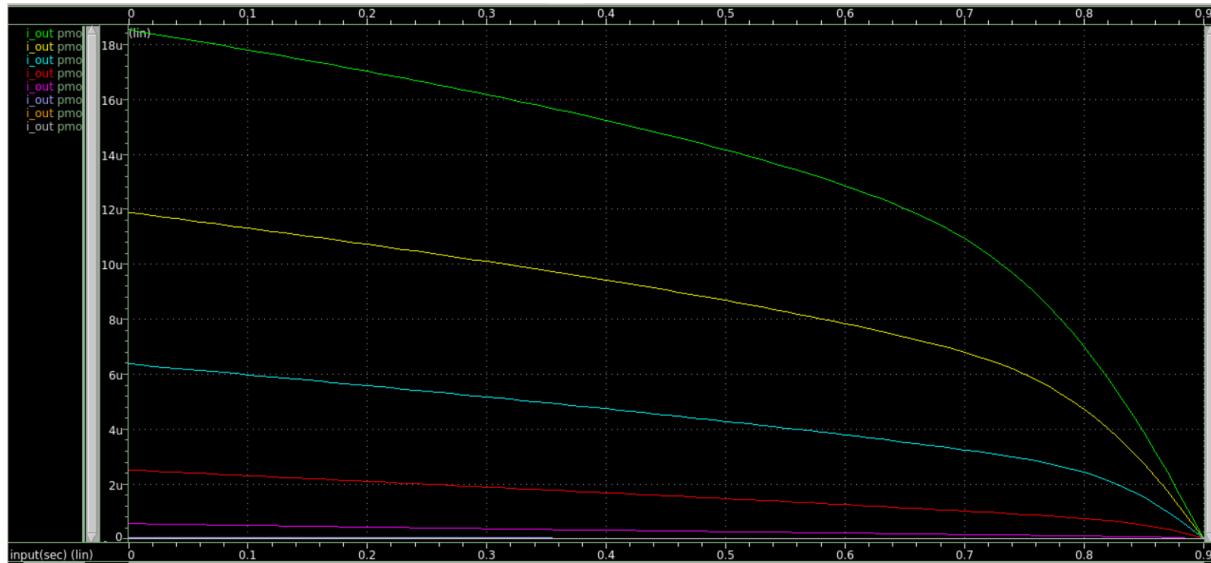
```

ii) w=80n, l=30n



Id vs Vgs

	slew4	slew5	slew6	slew7	slew8	slew9	
1.000e-01	6.850e-05	5.943e-05	4.495e-05				
	2.630e-05	8.958e-06	1.128e-06				
	9.434e-08	7.854e-09	8.752e-10				
	-3.641e-01	-4.197e-01	-5.550e-01				
	-9.485e-01	-2.784e+00	-2.211e+01				
	-2.644e+02	-3.176e+03	-2.850e+04				
	2.500e+01	1					
2.000e-01	6.663e-05	5.751e-05	4.298e-05	6.000e-01	5.257e-05	4.595e-05	3.275e-05
	2.454e-05	7.981e-06	9.715e-07		1.646e-05	4.234e-06	4.550e-07
	8.110e-08	6.782e-09	7.626e-10		3.822e-08	3.285e-09	3.814e-10
	-3.598e-01	-4.168e-01	-5.577e-01		-3.454e-01	-3.952e-01	-5.544e-01
	-9.767e-01	-3.003e+00	-2.467e+01		-1.103e+00	-4.289e+00	-3.992e+01
	-2.955e+02	-3.535e+03	-3.143e+04		-4.752e+02	-5.528e+03	-4.761e+04
	2.500e+01	1			2.500e+01	1	
3.000e-01	6.440e-05	5.534e-05	4.084e-05	7.000e-01	4.152e-05	3.963e-05	2.901e-05
	2.271e-05	7.026e-06	8.278e-07		1.398e-05	3.289e-06	3.424e-07
	6.906e-08	5.803e-09	6.570e-10		2.899e-08	2.527e-09	2.977e-10
	-3.554e-01	-4.136e-01	-5.605e-01		-3.588e-01	-3.760e-01	-5.136e-01
	-1.008e+00	-3.258e+00	-2.765e+01		-1.066e+00	-4.530e+00	-4.352e+01
	-3.314e+02	-3.944e+03	-3.484e+04		-5.141e+02	-5.897e+03	-5.006e+04
	2.500e+01	1			2.500e+01	1	
4.000e-01	6.165e-05	5.282e-05	3.848e-05	8.000e-01	2.174e-05	2.373e-05	2.086e-05
	2.078e-05	6.089e-06	6.952e-07		1.082e-05	2.305e-06	2.308e-07
	5.803e-08	4.905e-09	5.590e-10		1.982e-08	1.766e-09	2.125e-10
	-3.512e-01	-4.099e-01	-5.626e-01		-4.147e-01	-3.800e-01	-4.321e-01
	-1.042e+00	-3.556e+00	-3.114e+01		-8.334e-01	-3.912e+00	-3.906e+01
	-3.731e+02	-4.414e+03	-3.873e+04		-4.549e+02	-5.107e+03	-4.242e+04
	2.500e+01	1			2.500e+01	1	
5.000e-01	5.804e-05	4.980e-05	3.582e-05	9.000e-01	-2.503e-13	-1.965e-13	-1.343e-13
	1.871e-05	5.162e-06	5.717e-07		-7.770e-14	-3.735e-14	-1.488e-14
	4.782e-08	4.071e-09	4.678e-10		-4.952e-15	-1.495e-15	-3.010e-16
	-3.473e-01	-4.048e-01	-5.626e-01		-3.475e-01	-4.428e-01	-6.479e-01
	-1.077e+00	-3.905e+00	-3.526e+01		-1.120e+00	-2.329e+00	-5.846e+00
	-4.215e+02	-4.951e+03	-4.309e+04		-1.757e+01	-5.819e+01	-2.891e+02
	2.500e+01	1					

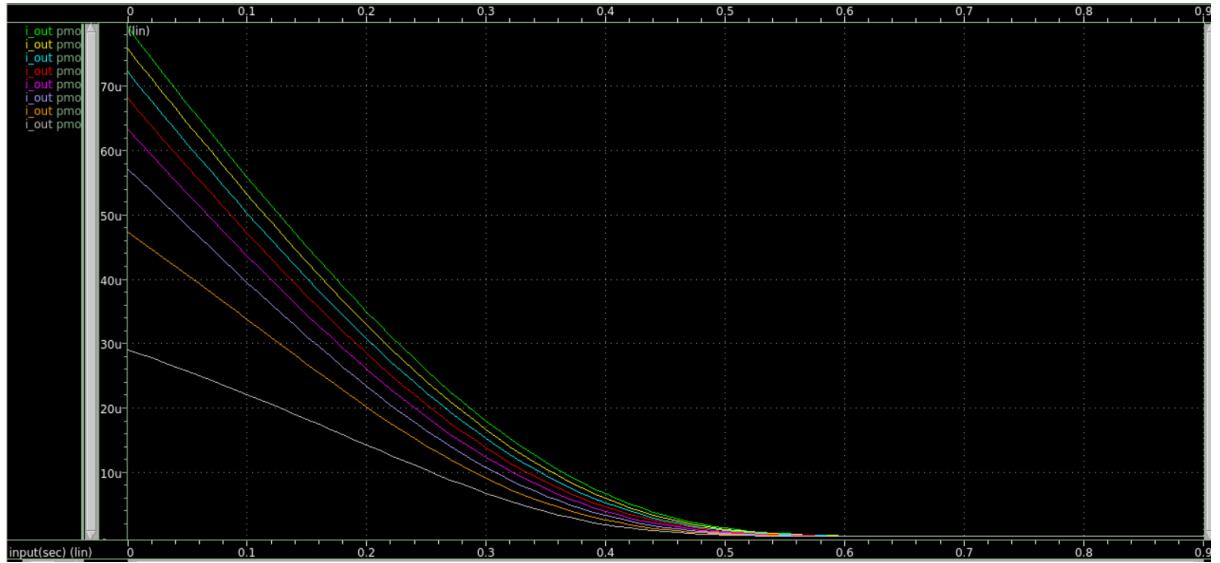


Id vs Vds

par_vsg	slew1	slew2	slew3
	slew4	slew5	slew6
	slew7	slew8	slew9
	temper	alter#	
1.000e-01	7.573e-06	8.139e-06	8.911e-06
	1.002e-05	1.175e-05	1.520e-05
	2.712e-05	5.599e-05	8.353e-05
	2.500e+01	1	
2.000e-01	5.796e-06	6.100e-06	6.508e-06
	7.074e-06	7.890e-06	9.168e-06
	1.328e-05	3.355e-05	6.114e-05
	2.500e+01	1	
3.000e-01	3.931e-06	4.043e-06	4.199e-06
	4.421e-06	4.743e-06	5.205e-06
	5.998e-06	1.386e-05	3.632e-05
	2.500e+01	1	
4.000e-01	2.074e-06	2.068e-06	2.077e-06
	2.105e-06	2.165e-06	2.269e-06
	2.411e-06	3.510e-06	1.392e-05
	2.500e+01	1	
5.000e-01	6.263e-07	5.930e-07	5.635e-07
	5.391e-07	5.216e-07	5.132e-07
	5.140e-07	5.753e-07	2.403e-06
	2.500e+01	1	
6.000e-01	7.532e-08	6.868e-08	6.294e-08
	5.813e-08	5.436e-08	5.180e-08
	5.047e-08	5.449e-08	2.299e-07
	2.500e+01	1	
7.000e-01	6.219e-09	5.651e-09	5.162e-09
	4.756e-09	4.439e-09	4.226e-09
	4.123e-09	4.542e-09	2.033e-08
	2.500e+01	1	
8.000e-01	5.153e-10	4.684e-10	4.290e-10
	3.964e-10	3.713e-10	3.548e-10
	3.484e-10	3.954e-10	1.895e-09
	2.500e+01	1	
9.000e-01	5.232e-11	4.396e-11	3.967e-11
	3.680e-11	3.470e-11	3.339e-11
	3.306e-11	3.865e-11	1.933e-10
	2.500e+01	1	

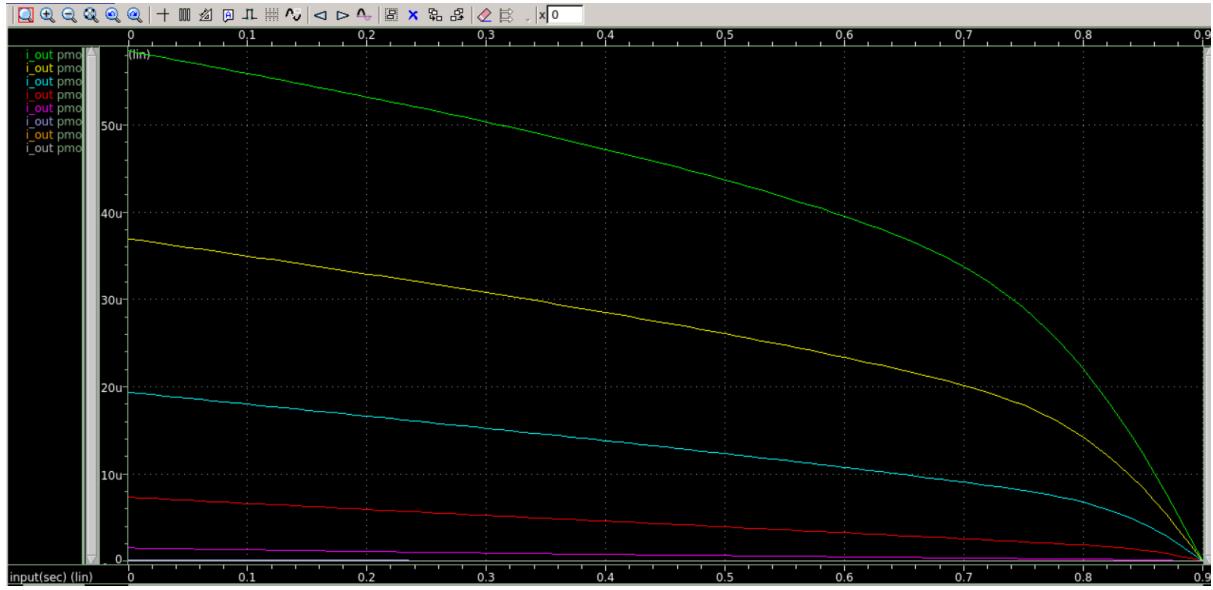
$ V_{gs} $ , $r_0$	
80/30 $ V_{ds} , v_t$ 0.1, -0.446 0.2, -0.447 0.3, -0.4431 0.4, -0.441 0.5, -0.438 0.6, -0.4135 0.7, -0.4161 $v_t(\text{avg}) = -0.434 \text{ V}$	0.1, 1.22e5 0.2, 1.63e5 0.3, 2.46e5 0.4, 4.824e5 0.5, 1.68e6 0.6, 1.45e7 0.7, 1.755e8 0.8, 2.12e9

iii)  $w=300n$ ,  $l=30n$



Id vs Vgs

par_vsd	slew1	slew2	slew3				
	slew4	slew5	slew6				
	slew7	slew8	slew9				
	vt1	vt2	vt3				
	vt4	vt5	vt6				
	vt7	vt8	vt9				
	temper	alter#					
1.000e-01	2.220e-04	1.904e-04	1.410e-04				
	7.939e-05	2.461e-05	2.963e-06				
	2.616e-07	2.333e-08	2.768e-09				
	-3.565e-01	-4.155e-01	-5.612e-01				
	-9.967e-01	-3.215e+00	-2.671e+01				
	-3.024e+02	-3.392e+03	-2.859e+04				
	2.500e+01	1					
2.000e-01	2.158e-04	1.838e-04	1.340e-04				
	7.321e-05	2.145e-05	2.498e-06	6.000e-01	1.718e-04	1.456e-04	9.913e-05
	2.204e-07	1.975e-08	2.367e-09		4.601e-05	1.030e-05	1.076e-06
	-3.514e-01	-4.124e-01	-5.657e-01		9.604e-08	8.873e-09	1.102e-09
	-1.036e+00	-3.535e+00	-3.035e+01		-3.326e-01	-3.922e-01	-5.762e-01
	-3.439e+02	-3.839e+03	-3.202e+04		-1.242e+00	-5.543e+00	-5.309e+01
	2.500e+01	1			-5.947e+02	-6.437e+03	-5.184e+04
3.000e-01	2.084e-04	1.764e-04	1.265e-04		2.500e+01	1	
	6.685e-05	1.845e-05	2.084e-06	7.000e-01	1.393e-04	1.270e-04	8.718e-05
	1.840e-07	1.658e-08	2.002e-09		3.811e-05	7.775e-06	7.937e-07
	-3.463e-01	-4.092e-01	-5.705e-01		7.155e-08	6.711e-09	8.463e-10
	-1.080e+00	-3.913e+00	-3.465e+01		-3.396e-01	-3.723e-01	-5.425e-01
	-3.924e+02	-4.355e+03	-3.606e+04		-1.241e+00	-6.083e+00	-5.959e+01
	2.500e+01	1			-6.610e+02	-7.048e+03	-5.589e+04
4.000e-01	1.996e-04	1.679e-04	1.184e-04	8.000e-01	2.500e+01	1	
	6.025e-05	1.561e-05	1.713e-06		7.542e-05	7.951e-05	6.440e-05
	1.516e-07	1.374e-08	1.673e-09		2.881e-05	5.264e-06	5.249e-07
	-3.413e-01	-4.056e-01	-5.754e-01		4.812e-08	4.617e-09	5.956e-10
	-1.130e+00	-4.363e+00	-3.975e+01		-3.854e-01	-3.656e-01	-4.514e-01
	-4.494e+02	-4.956e+03	-4.072e+04		-1.009e+00	-5.522e+00	-5.538e+01
	2.500e+01	1			-6.041e+02	-6.296e+03	-4.880e+04
5.000e-01	1.882e-04	1.579e-04	1.093e-04	9.000e-01	2.500e+01	1	
	5.334e-05	1.290e-05	1.380e-06		-8.352e-13	-6.500e-13	-4.480e-13
	1.225e-07	1.120e-08	1.375e-09		-2.620e-13	-1.270e-13	-5.077e-14
	-3.364e-01	-4.009e-01	-5.790e-01		-1.691e-14	-5.105e-15	-1.028e-15
	-1.187e+00	-4.906e+00	-4.588e+01		-3.499e-01	-4.497e-01	-6.524e-01
	-5.169e+02	-5.654e+03	-4.605e+04		-1.116e+00	-2.301e+00	-5.756e+00
					-1.729e+01	-5.725e+01	-2.844e+02
					2.500e+01	1	



Id vs vds

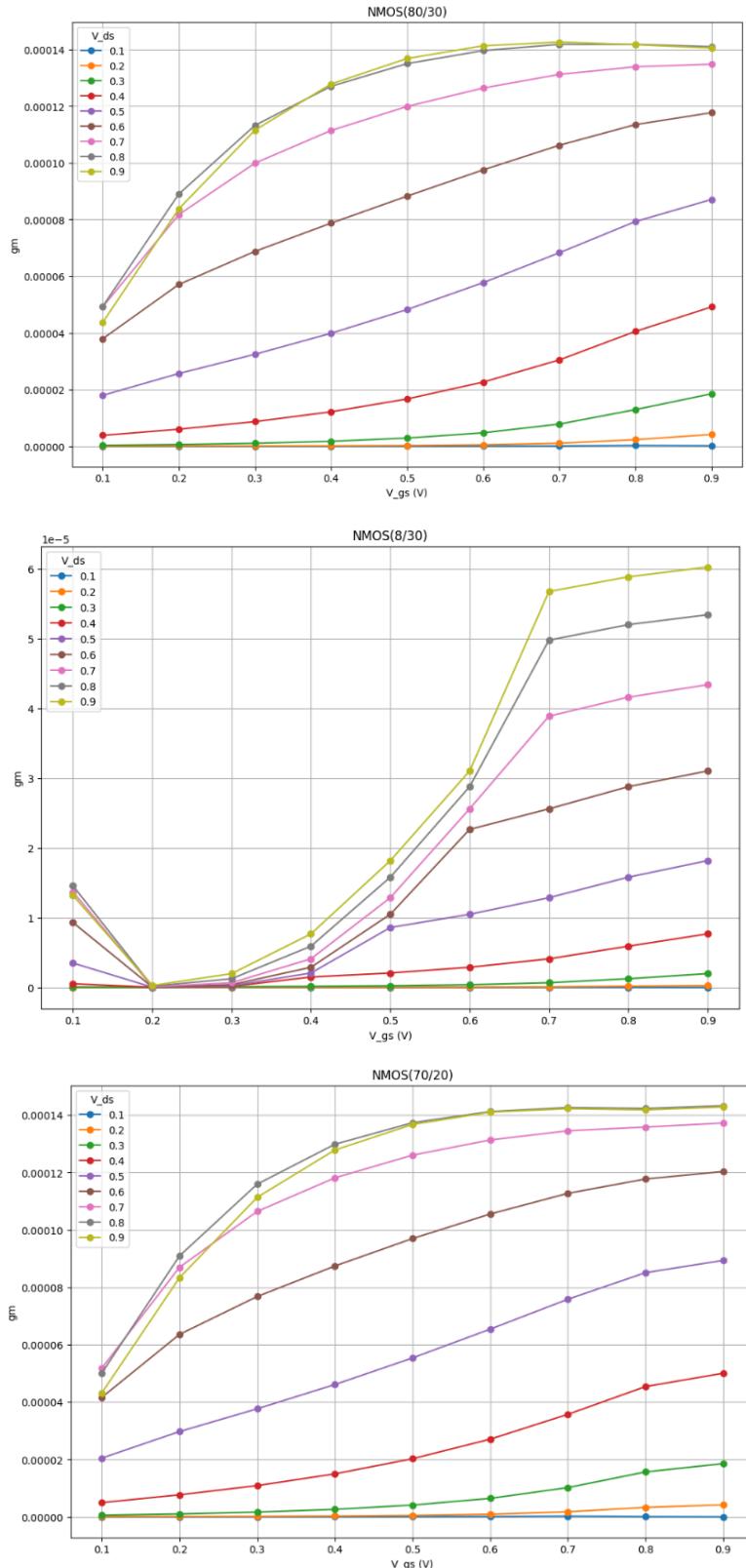
par_vsg	slew1	slew2	slew3
	slew4	slew5	slew6
	slew7	slew8	slew9
	temper	alter#	
1.000e-01	2.621e-05	2.781e-05	3.001e-05
	3.314e-05	3.791e-05	4.699e-05
	7.962e-05	1.720e-04	2.673e-04
	2.500e+01	1	
2.000e-01	2.017e-05	2.096e-05	2.203e-05
	2.354e-05	2.571e-05	2.900e-05
	3.886e-05	9.748e-05	1.890e-04
	2.500e+01	1	
3.000e-01	1.361e-05	1.379e-05	1.409e-05
	1.456e-05	1.528e-05	1.635e-05
	1.806e-05	3.720e-05	1.049e-04
	2.500e+01	1	
4.000e-01	6.991e-06	6.834e-06	6.709e-06
	6.632e-06	6.627e-06	6.726e-06
	6.907e-06	9.064e-06	3.527e-05
	2.500e+01	1	
5.000e-01	1.964e-06	1.805e-06	1.661e-06
	1.535e-06	1.429e-06	1.350e-06
	1.293e-06	1.380e-06	5.355e-06
	2.500e+01	1	
6.000e-01	2.297e-07	2.036e-07	1.811e-07
	1.620e-07	1.464e-07	1.345e-07
	1.260e-07	1.316e-07	5.232e-07
	2.500e+01	1	
7.000e-01	2.007e-08	1.775e-08	1.576e-08
	1.409e-08	1.273e-08	1.170e-08
	1.099e-08	1.174e-08	4.963e-08
	2.500e+01	1	
8.000e-01	1.778e-09	1.574e-09	1.402e-09
	1.258e-09	1.141e-09	1.054e-09
	9.968e-10	1.099e-09	4.993e-09
	2.500e+01	1	
9.000e-01	1.873e-10	1.538e-10	1.349e-10
	1.214e-10	1.108e-10	1.030e-10
	9.840e-11	1.127e-10	5.493e-10
	2.500e+01	1	

Vds  , Vt	Vgs  , ro
0.1,-0.444	0.1,3.57e4
0.2,-0.443	0.2,4.762e4
0.3,-0.442	0.3,7.23e4
0.4,-0.44	0.4,1.46e5
0.5,-0.4387	0.5,5.55e5
0.6,-0.4336	0.6,4.88e6
0.7,-0.4	0.7,5.6e7
Vt(avg)=-0.4325V	0.8,6.3e8

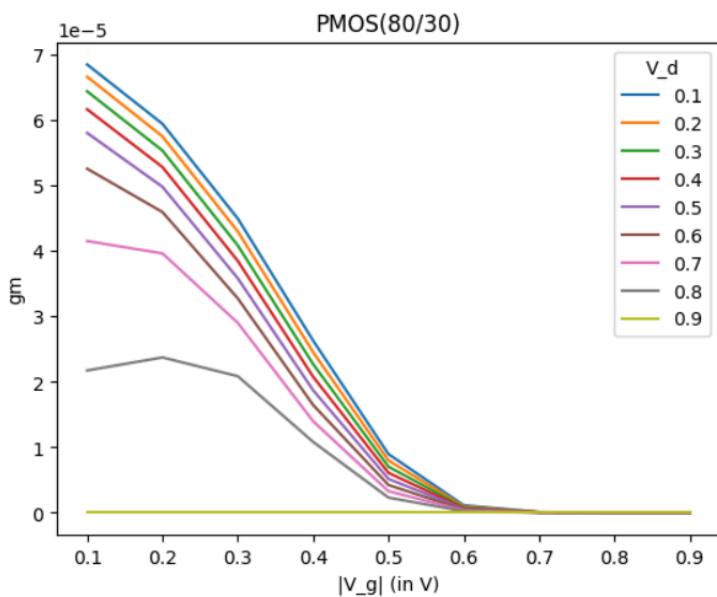
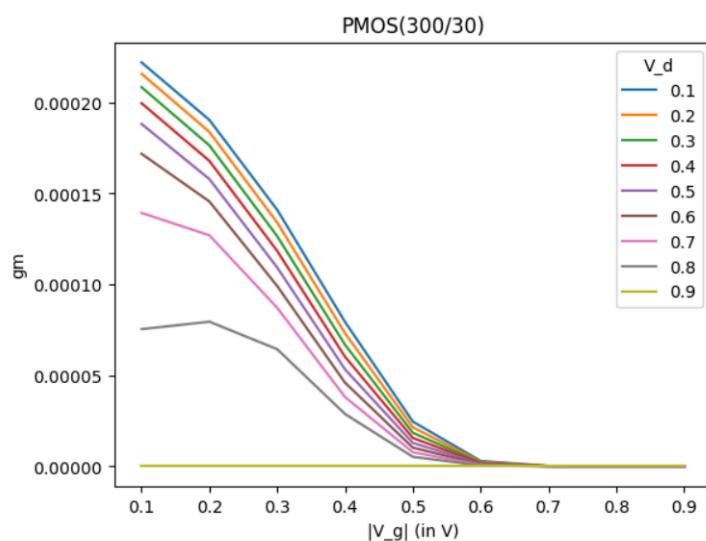
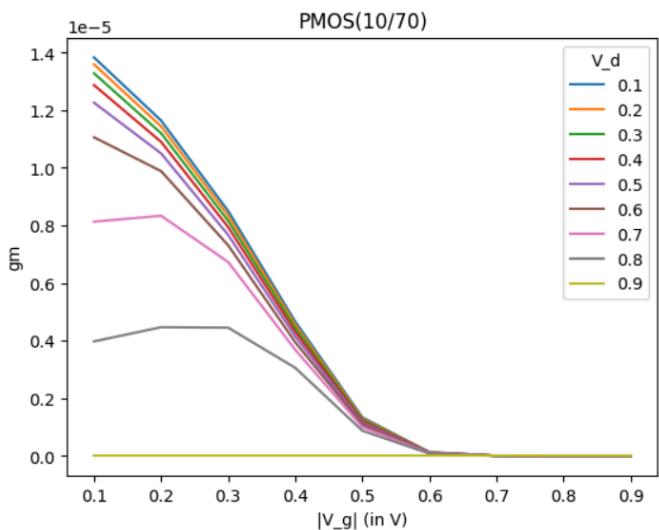
## 5. PYTHON PLOTS

## A. Gm

### NMOS

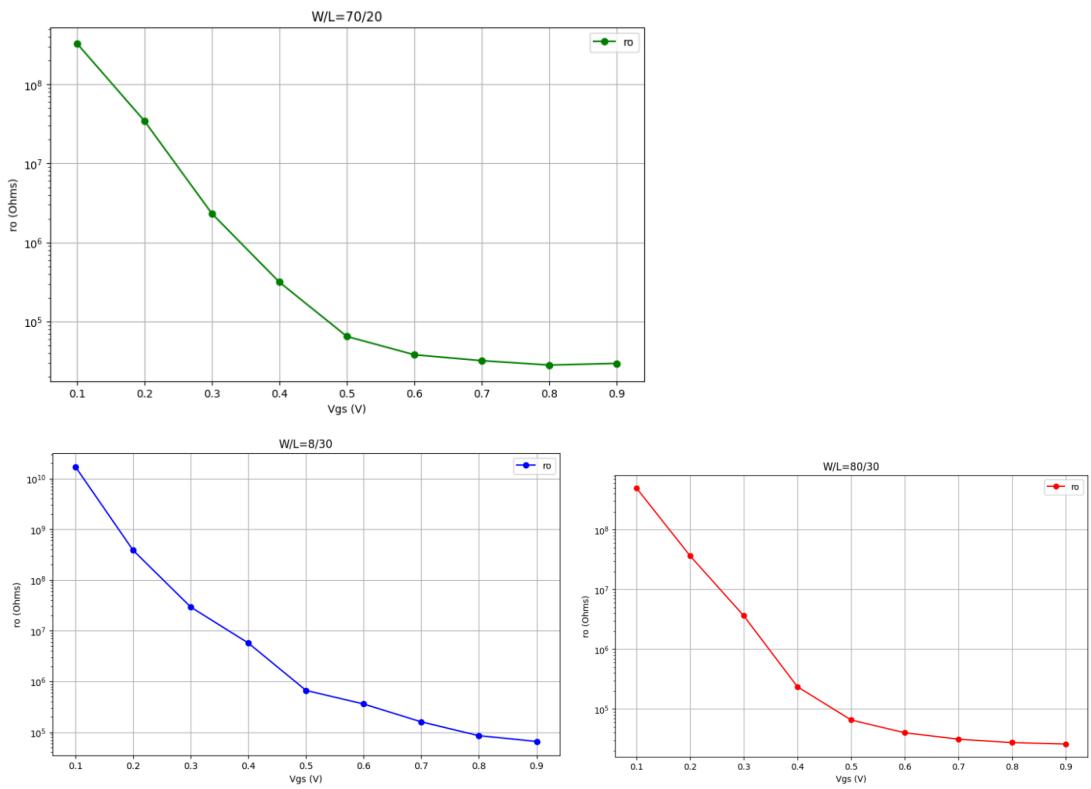


## PMOS

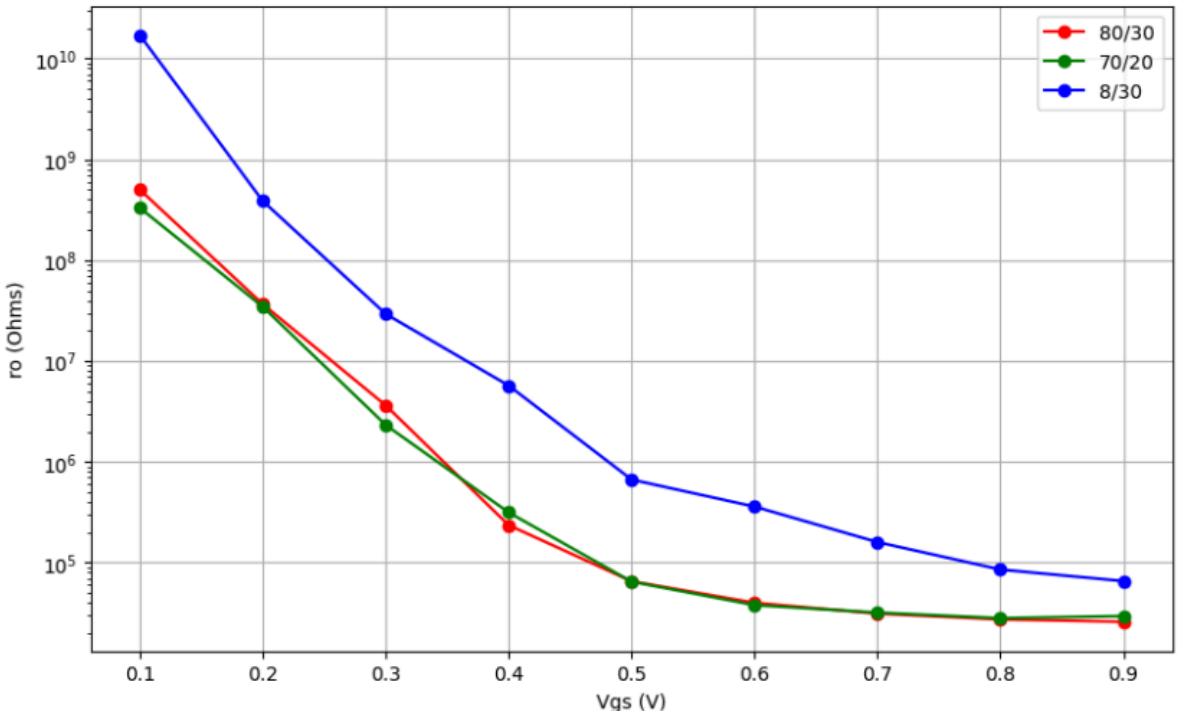


**B. Ro**

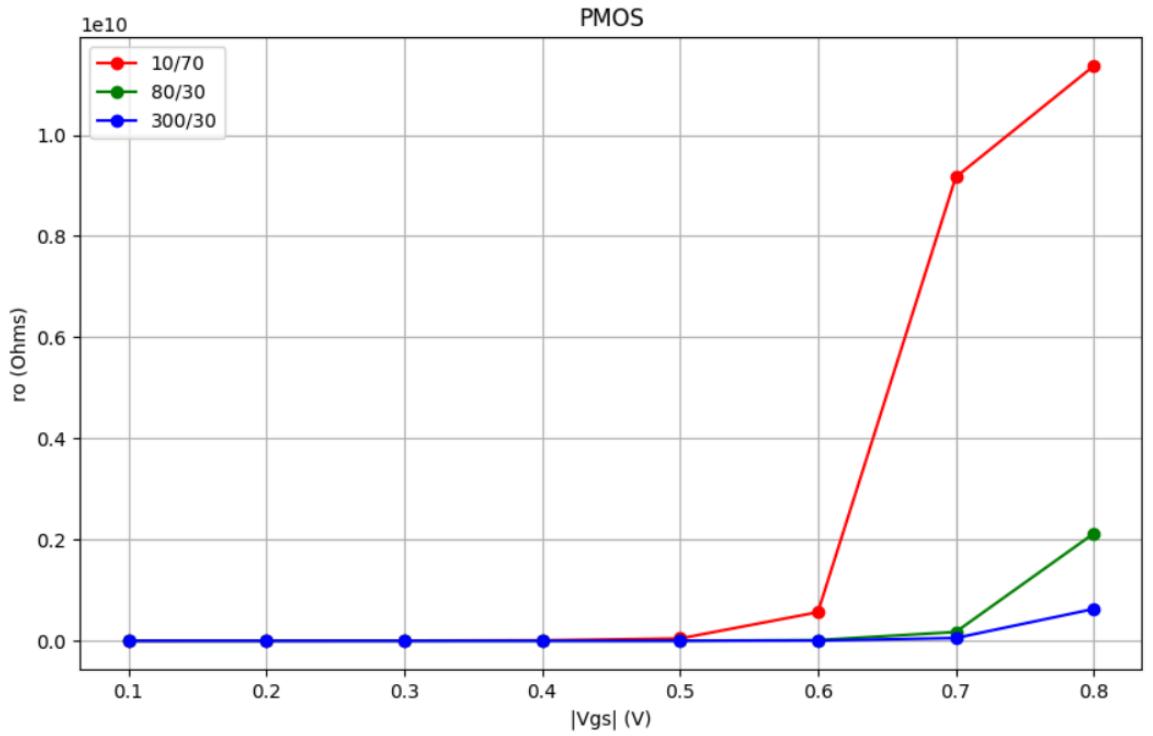
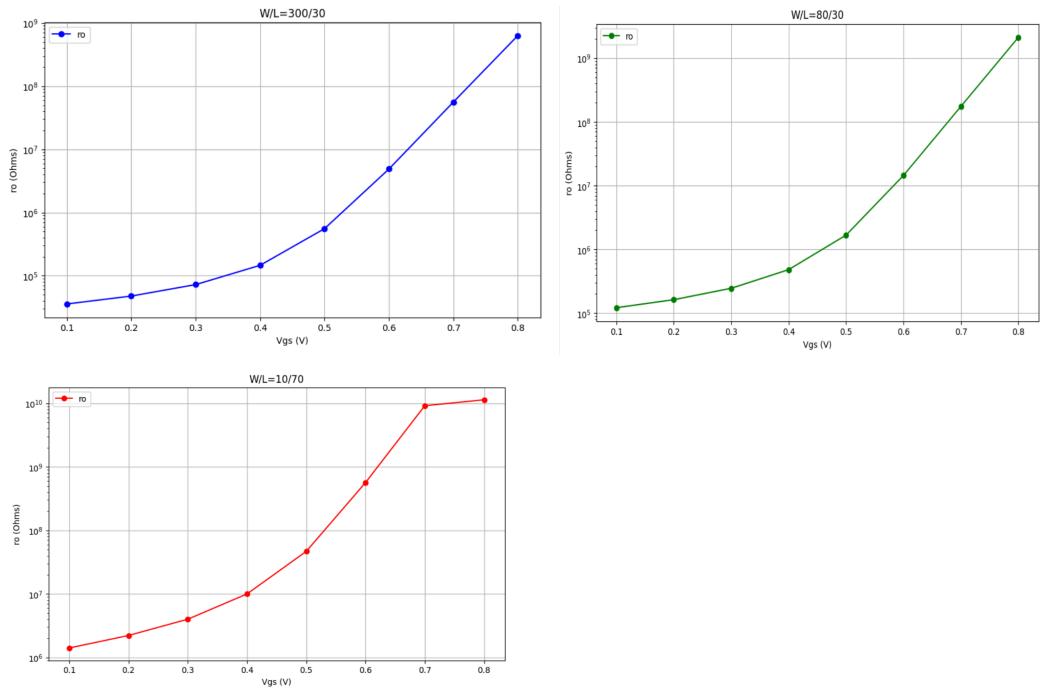
## NMOS



## NMOS



## PMOS



### 3. Threshold voltage

