Code No: 153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, April/May - 2023
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering – Artificial Intelligence and Machine Learning)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What is meant by an instruction?	[2]
b)	Write the difference between Arithmetic Micro instructions and Logic Micro instructions.	[3]
c)	What is control memory?	[2]
d)	What is meant by hardwired control?	[3]
e)	Explain how floating point number is represented.	[2]
f)	What are techniques to represent signed integer number?	[3]
g)	Define DMA.	[2]
h)	What is an associate memory? What is its need?	[3]
i)	What is meant by delayed branching?	[2]
j)	What is branch prediction?	[3]

PART – B

(50 Marks)

2.a) With a neat schematic, explain the steps involved in fetch and decode phases using register transfer instructions.
b) Explain the phases of Interrupt Cycle with a neat flowchart. [5+5]

OR

3.a) Using the register transfer notations, explain the Memory-Reference instructions with examples.
b) Explain register transfer language. Show how to achieve Inter Register Transfer with examples and block diagram. [5+5]

4. Discuss about different types of addressing modes. [10]

OR

5. Draw and explain about micro program control unit. [10]

6.a) What is meant by normalization? Explain the IEEE standards to represent floating point number.
b) Describe the hardware implementation for addition and subtraction in detail. [4+6]

OR

7. With a neat flow chart, explain the rules to perform floating point multiplication. [10]

8.a) Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.
b) Explain in detail about strobe control method of asynchronous data transfer. [5+5]

OR

9.a) Discuss memory mapped I/O in computer organization.
b) What is I/O interface and explain it with block diagram. [5+5]

10.a) Explain about arithmetic pipelining.
b) Explain time-shared common bus Organization. [5+5]

OR

11.a) Explain interprocessor communication and synchronization.
b) Differentiate tightly coupled and loosely coupled multiprocessors. [5+5]

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