**Floating Point Adder Implementation in Verilog**

*Detailed explanation of each code module has been commented in the code files

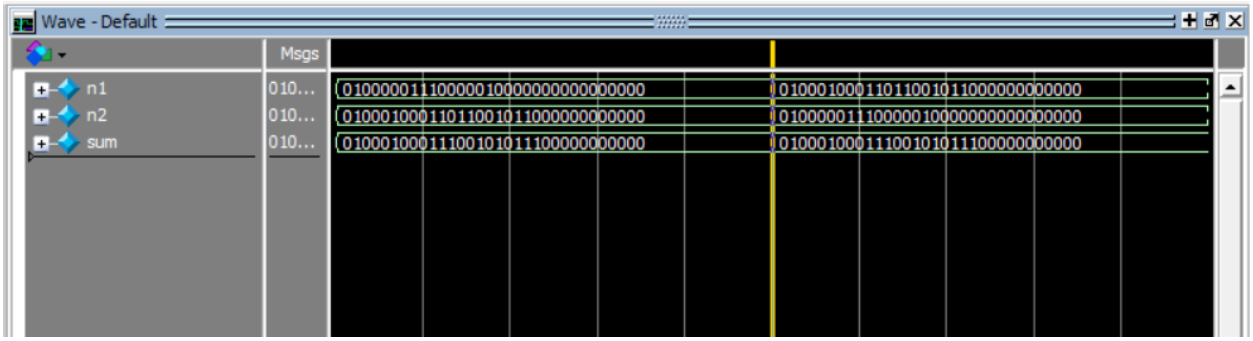
To test this circuit, one must simulate the fpAdderTb module.

Detailed comments are given in the code file. The testbench has a few distinct test cases which I felt would show the extent of the capabilities of the adder while handling negative numbers or overflow.

**The first two cases** are shown as follows

First, n1 is taken as 24.125 and n2 as 946.75. In the second half, n1 and n2 are exchanged.

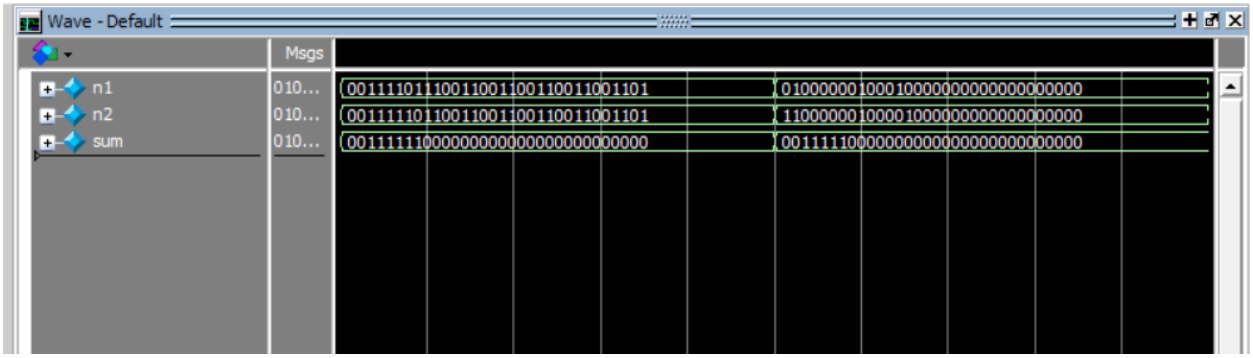
In both cases, we obtain the correct result – 01000100011100101011100000000000. That is : 970.875




**The next two test cases** are :-

First, n1 = 0.1, n2 = 0.4

Then, n1 = 4.25, n2 = - 4.125



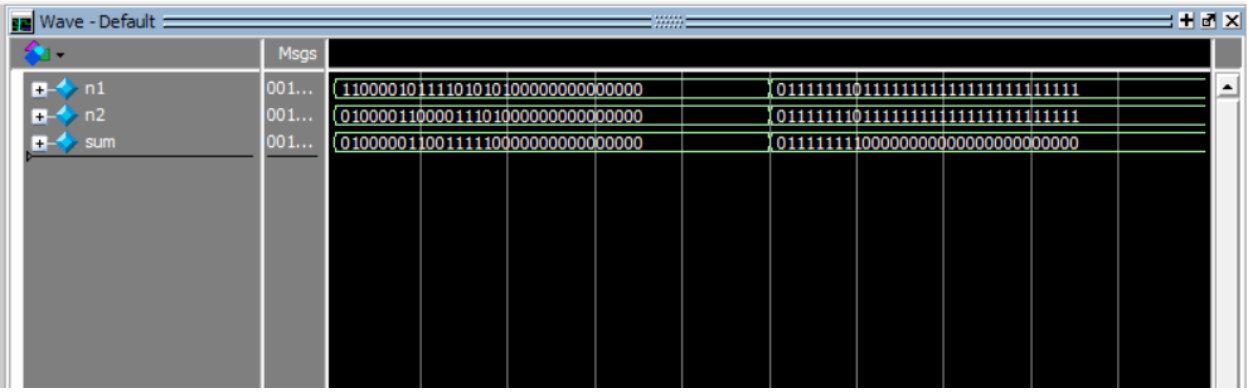

The correct result is obtained in both cases (0.5 and 0.125 respectively)

**The fifth test case** has n1 = -4.125 and n2 = 4.25, This (and the previous test case) show that the normalization function works for subtracting numbers that are very close.

**The sixth test cas**e has the same n2 = 4.25 while n1 = -8.125. The output is shown here :


Correct results are obtained in both cases (0.125 and -3.875 respectively)

**The seventh test case** has n1 = -122.625 and n2 = 142.5, while **the last test case** has n1 and n2 as close to infinity as possible (exponent = 254 and fraction = all ones). Their addition enters the overflow condition and returns infinity. These outputs are shown as follows :-




Sum is 19.875 in the second last case, and for the last one, sum gets represented as **Infinity.**