

# Manikandan Gunaseelan

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## EDUCATION

### **BITS Pilani, K K Birla Goa Campus**

*BE (hons) Electronics and Communication Engineering*

Current GPA : **8.05/10**

*Aug. 2018 – July 2022*

### **DAV Public School, Pune**

*Grade XII*

Score : **92.8%**

*May 2018*

### **DAV Public School, Pune**

*Grade X*

GPA : **10/10**

*May 2016*

## SKILLS AND COURSEWORK

**Relevant Coursework:** Computer Programming, Computer Architecture, Digital Design, Microprocessor Programming and Interfacing, Cryptography, Communication Networks

**Technical Skills:** C, C++, Python (Flask, pytest), Cisco IOS XR, MySQL, GNU/Linux, Bash Scripting

## EXPERIENCE

### **Cisco Systems India**

*Software Engineer*

Aug 2022 - Present

*Bangalore, KA*

- Contributing in the design and maintenance of the Manageability Models Sneak-Peek dashboard, which provides data about model adoption in the different Automation packages across teams in Cisco's Mass-Scale Infrastructure Group

### **Cisco Systems India**

*Technical Undergraduate Intern*

Jan 2022 - July 2022

*Bangalore, KA*

- Contributed to CAFY Automation Packages used for automating testcases to exercise features of Cisco's Network Operating System IOS XR
- As a part of the Manageability team, automated multiple testcases for NETCONF and NACM protocols using Python library functions to communicate with IOS XR
- As a part of LPTS-AAA team, assisted in the migration of Traffic Generator platform from Spirent to IXIA for the LPTS packages - including run failure analysis and debugging

## PROJECTS

### **Implementation of MIPS Processor in Verilog** | *Computer Architecture*

Mar 2021 – Apr 2021

- Verilog implementation of pipelined and single-cycle (modified) MIPS processors
- Single cycle processor had a floating point addition instruction which used a separate IEEE754 Floating point adder module
- Pipelined processor with a forwarding unit, hazard detection unit and basic branch prediction to tackle data and control hazards
- Understood the basics of processor working and design, the differences between single-cycle and pipelined processors, and the handling of various hazards that arise when working with a pipelined processor

### **Spirit Level Reaction Time Tester** | *Microprocessor Programming*

Mar 2020 – Apr 2020

- Implemented a reaction time tester on the Intel 8086 Microprocessor which checks a person's sobriety based on their reaction time in pressing a button upon seeing a sequence of LEDs
- Also included a simulation on Proteus 7 using the x86 Assembly language

## CERTIFICATIONS

### **Google IT Support Professional Certificate** | *Coursera*

July 2020

- Included courses on Networking Fundamentals, Operating Systems, System Administration and IT security
- Verilog implementation of pipelined and single-cycle (modified) MIPS processors
- Hands-on experience in the form of virtual labs conducted on Qwiklabs

### **Introduction to Data Analytics for Business** | *Coursera*

June 2020

- Learnt about the data analytics practices executed in the business world - how data is created, stored, accessed and then later analysed
- Involved a module on the basics of SQL