

Manikandan Gunaseelan

+91-7448090869 | [E-Mail](#) | [LinkedIn](#) | [GitHub](#)

EDUCATION

BITS Pilani, K K Birla Goa Campus <i>BE (hons) Electronics and Communication Engineering</i>	GPA : 8.05/10 <i>Aug. 2018 – July 2022</i>
DAV Public School, Pune <i>Grade XII</i>	Score : 92.8% <i>May 2018</i>
DAV Public School, Pune <i>Grade X</i>	GPA : 10/10 <i>May 2016</i>

SKILLS AND COURSEWORK

Relevant Coursework: Computer Programming, Computer Architecture, Digital Design, Microprocessor Programming and Interfacing, Cryptography, Communication Networks

Technical Skills: C, C++, Python (Flask, pytest), Cisco IOS XR, MySQL, GNU/Linux, Bash Scripting

EXPERIENCE

Cisco Systems India <i>Software Engineer</i>	Aug 2022 - Present <i>Bangalore, KA</i>
<ul style="list-style-type: none">Contributing in the design and maintenance of the Manageability Models Sneak-Peek dashboard, which provides data about model adoption in the different Automation packages across teams in Cisco's Mass-Scale Infrastructure Group	
Cisco Systems India <i>Technical Undergraduate Intern</i>	Jan 2022 - July 2022 <i>Bangalore, KA</i>
<ul style="list-style-type: none">Contributed to CAFY Automation Packages used for automating testcases to exercise features of Cisco's Network Operating System IOS XRAs a part of the Manageability team, automated multiple testcases for NETCONF and NACM protocols using Python library functions and APIs to communicate with IOS XRAs a part of LPTS-AAA team, assisted in the migration of Traffic Generator platform from Spirent to IXIA for the LPTS packages - including run failure analysis and debugging	

PROJECTS

Implementation of MIPS Processor in Verilog <i>Computer Architecture</i>	Mar 2021 – Apr 2021
<ul style="list-style-type: none">Verilog implementation of pipelined and single-cycle (modified) MIPS processorsSingle cycle processor had a floating point addition instruction which used a separate IEEE754 Floating point adder modulePipelined processor with a forwarding unit, hazard detection unit and basic branch prediction to tackle data and control hazardsUnderstood the basics of processor working and design, the differences between single-cycle and pipelined processors, and the handling of various hazards that arise when working with a pipelined processor	
Spirit Level Reaction Time Tester <i>Microprocessor Programming</i>	Mar 2020 – Apr 2020
<ul style="list-style-type: none">Implemented a reaction time tester on the Intel 8086 Microprocessor which checks a person's sobriety based on their reaction time in pressing a button upon seeing a sequence of LEDsAlso included a simulation on Proteus 7 using the x86 Assembly language	

CERTIFICATIONS

Google IT Support Professional Certificate <i>Coursera</i>	July 2020
<ul style="list-style-type: none">Included courses on Networking Fundamentals, Operating Systems, System Administration and IT securityHands-on experience in the form of virtual labs conducted on Qwiklabs	
Introduction to Data Analytics for Business <i>Coursera</i>	June 2020
<ul style="list-style-type: none">Learnt about the data analytics practices executed in the business world - how data is created, stored, accessed and then later analysedInvolved a module on the basics of SQL	