Computer Organization

Assignment 1

Section CB

Date of Submission – 20/9/2024

(Roll No. 1-22)

1	An 8-bit processor is fed by two 8-bit inputs using registers R1 and R2. The inputs are $(-23)_{10}$ and $(-19)_{10}$. A binary addition should be performed by the processor. Calculate the binary addition result. The result must be in 8-bit format.
2	Imagine you are building a simple computer system for educational purpose. The computer will be used to perform basic calculations and store simple data. Then, explain necessary building blocks that are required to build a computer that can perform basic calculations and store simple data.
3	There are a few dynamic situations where IEEE floating-point representation is required. For example, when dealing with the spacecraft's velocity, you come across a value like (-39.125) m/s. Use IEEE 32-bit and 64-bit floating-point representations to represent this number.
4	Explain the organization of Von Neumann computer with schematic diagram.
5	Considering a 2's complement-based 8-bit processor, perform the following arithmetic operations. Also, check the existence of overflow in each operation. (a) (-100) + (15) (b) (-32) + (-97)

(Roll No. 23-44)

1	Perform (-36) – (+23) arithmetic operation using 2's compliment. Also check the existence of overflow in each operation. Assume 8-bit representation.
2	Implement the following Boolean function with a suitable multiplexer. $F(x, y, z) = \Sigma (0, 3, 6, 7)$
3	There are a few dynamic situations where IEEE floating-point representation is required. For example, when dealing with the spacecraft's velocity, you come across a value like (-85.125) m/s. Use IEEE 32-bit and 64-bit floating-point representations to represent this number.
4	In an arithmetic logic unit, two half subtractors are connected to form a full subtractor. Show the connections between half subtractors. Also, determine the required Boolean logic for the outputs.
5	Determine the minimum number of bits needed to represent -32 in 2's compliment representation.

Assignment (Roll No. 45-66)

1	Perform the following arithmetic operations using Two's complement 8- bit representation. Also check the existence of overflow in each operation. (a) (– 70) – (+80) (b) –70 – 32
2	In an arithmetic logic unit, two half adders are connected to form a full adder. Show the connections between half adders. Also, determine the required Boolean logic for the outputs.
3	Determine the minimum number of bits needed to represent -32 in 2's compliment representation.
4	Express $(101101.101101)_2$ as a floating-point number using IEEE double precision.
5	Implement the following Boolean function with a suitable multiplexer. $F(x, y, z) = \Sigma (0, 2, 5, 7)$