EE-312L Power Electronics

Laboratory Project (CLO3)

Session 2018, 6th Semester

June 20, 2021

University of Engineering and Technology
Lahore, Pakistan

1 Introduction

Multilevel inverters are playing a dominant role in modern smart grids. High power is obtained by using multiple medium power sources at the input of a multilevel inverter. Some of the medium voltage sources are batteries, solar panels or super capacitors etc. Therefore, a multilevel inverter is an inescapable component of modern grid.
The main advantage of using multilevel inverters in modern power systems is to get a nearly approaching sinusoidal output voltage without a load side filter or with a very small size filter as compared to a conventional H-bridge inverter whose filter size is very large. Other advantages of multilevel inverters include low dv/dt stress across the switches, low voltage rating for switches and low switching losses. A typical output voltage waveform of a 7-level inverter is shown in Figure 1.

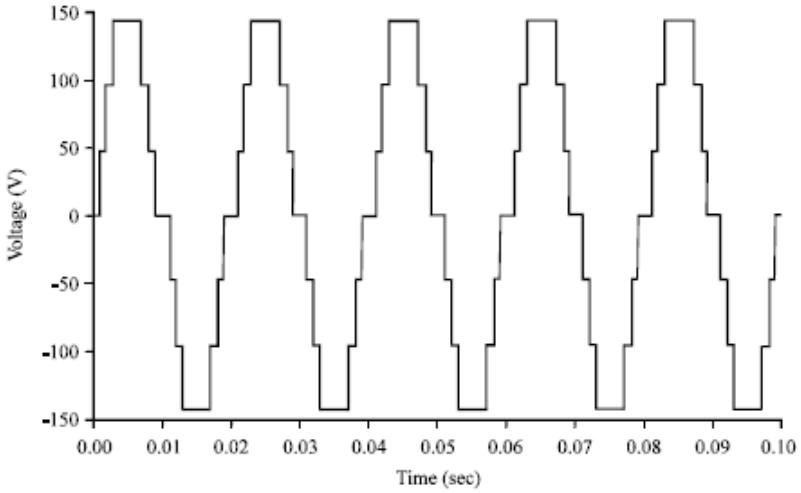


Figure 1: Output voltage waveform of a multilevel inverter (*Ref: Nandhini Gayathri et-al*)

2 Project Description

Consider a single phase cascaded H-bridge multilevel inverter shown in Figure 2. The inverter is being fed by two independent DC voltage sources V_1 and V_2. The output of first stage is v_{H1} whereas the output of second stage is v_{H2}. The total voltage between terminal A and N is $v_{H1} + v_{H2}$. The PWM for each MOSFET (Switch) is decided by tracking the path of voltage sources to the output terminals for desired voltage level. A two stage cascaded H-

bridge multilevel inverter shown in Figure 2 can have 5-level, 7-level or 9-level output voltage depending on the magnitude of both voltage sources (keep in mind that those three different output voltage waveforms can be obtained using the same hardware).

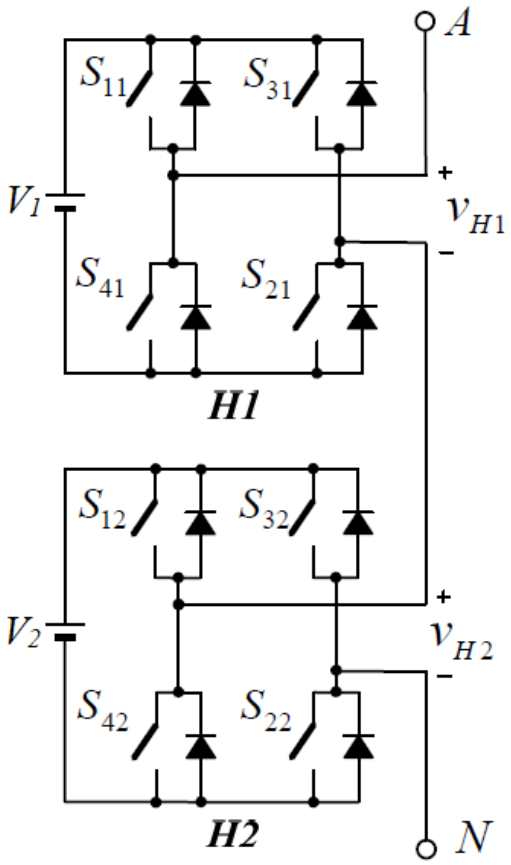


Figure 2: Circuit diagram of a cascaded H-bridge inverter

Important Note

You are required to simulate the circuit of Figure 2 on MATLAB/Simulink as well as perform its hardware implementation on Printed Circuit Board (PCB). You are free to choose the values of input DC voltage sources as well as the load power rating as long as you remain within the current rating of copper tracks of PCB (1.5mm track width for power side). You are not required to design the PCB as a schematic diagram of the circuit of Figure 2 is provided at the last page of this document whose PCB design (gerber

files) are also available in the zip folder that you can freely use to fabricate the PCB. A suggested way to fabricate the PCB is to use https://jlcpcb.com/ or https://www.pcbway.com/ who can fabricate 10 PCBs for 2-5USD (excluding shipping). Therefore, one order of 10 PCBs is sufficient for 10 groups. You are free to choose other available options to fabricate the PCB.

2.1 Task 1

Based on your chosen values of both input voltage sources and load power, determine the electrical ratings of all the switches and show them in tabular form.

2.2 Task 2

Implement Phase Shifted Carrier Based PWM (PSCPWM) for the 5-level, 7-level and 9-level inverter, obtain the output voltage waveform at each stage and then resultant voltage waveform. Do not forget to include the waveforms of each gate pulse. Perform FFT analysis on the Simulink and determine Total Harmonic Distortion (THD) of the voltage.

2.3 Task 3

Implement Level Shifted Carrier Based PWM (LSCPWM) for the 5-level, 7-level and 9-level inverter, obtain the output voltage waveform at each stage and then resultant voltage waveform. Do not forget to include the waveforms of each gate pulse. Perform FFT analysis on the Simulink and determine Total Harmonic Distortion (THD) of the voltage.

2.4 Task 4

Connect a resistive load and obtain the waveforms of output voltage and output current.

2.5 Task 5

Connect an RL load and obtain the waveforms of output voltage and output current.

3 Deliverables

You are required to submit a detailed report (LaTeXbased) and simulation files in a zip folder. Report should include the following contents.

- Title Page
- Abstract (Motivation, What has been done, What has been achieved, etc.)
- Table of Contents
- List of Figures and Tables
- List of Tables
- Introduction (Motivation, Problem Statement and Organization, about one paragraph each, maximum 3 pages, 1 and half page is enough)
- Literature Review (About 3-5 pages with references ranging from basic/classical to latest)
- Software Implementation
- Hardware Implementation
- Results and Discussion
- Conclusions and Future Works (max one page, one paragraph for each point)
- References (IEEE style)
- Appendices (if any)

Please use the FYP template of the department for this report. It should be clear that which simulation belongs to which task/sub-task. Please mention the name and path of the file for each result (figure, table or graph) in the respective caption/title. Failure to follow this instruction will result zero points in that portion of simulations. The zip folder should have two sub-folders named as "Report" (containing pdf file of the report) and "Simulations" (containing the simulations according to the path and name as specified in their corresponding result caption or title). Please import the data into the MATLAB workspace and plot the results with good resolution. Screen shots will not be accepted.

Submission Deadline

July 30, 2021

Project Groups

You can work on this project in a group with a maximum of four (4) students

3-D View of Fabricated PCB

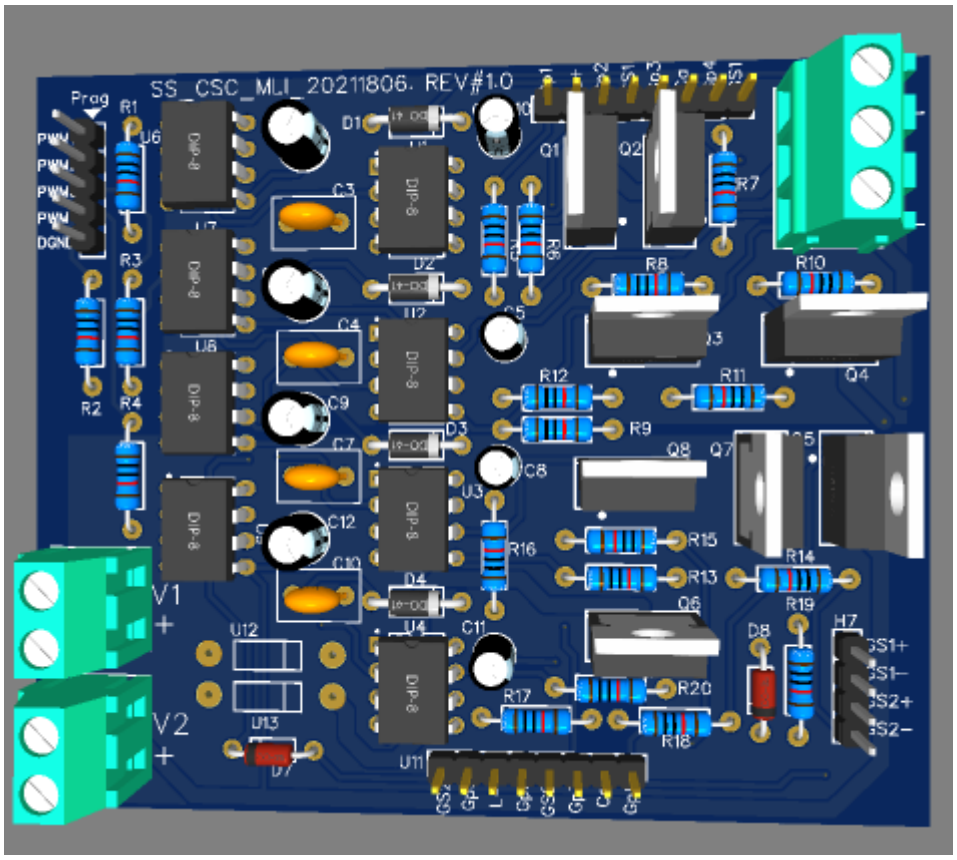
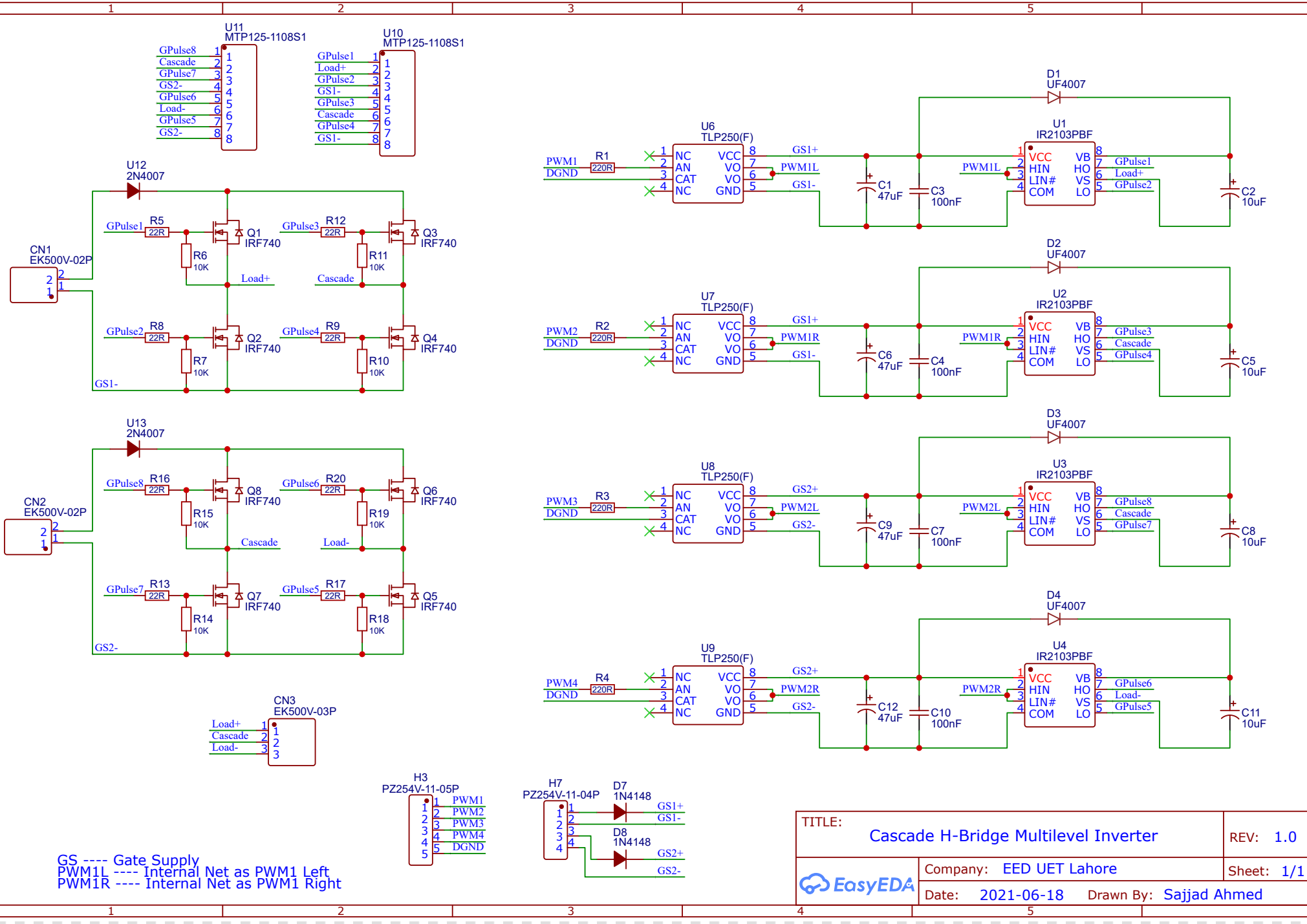


Figure 3: 3-D View of Fabricated PCB


U11
MTP125-1108S1
GPulse8
Cascade
GPulse7
GS2-
GPulse6
Load-
GPulse5
GS2-
U10
MTP125-1108S1
GPulse1
Load+
GPulse2
GS1-
GPulse3
Cascade
GPulse4
GS1-
U12
2N4007
CN1
EK500V-02P
GPulse1
R5
22R
Q1
IRF740
GPulse3
R12
Q3
IRF740
R6
10K
R11
10K
Load+
Cascade
GPulse2
R8
Q2
IRF740
GPulse4
R9
Q4
IRF740
R7
10K
R10
10K
GS1-
U13
2N4007
CN2
EK500V-02P
GPulse8
R16
Q8
IRF740
GPulse6
R20
Q6
IRF740
R15
10K
R19
10K
Cascade
Load-
GPulse7
R13
Q7
IRF740
GPulse5
R17
Q5
IRF740
R14
10K
R18
10K
GS2-
CN3
EK500V-03P
Load+
Cascade
Load-
H3
PZ254V-11-05P
PWM1
PWM2
PWM3
PWM4
DGND
H7
PZ254V-11-04P
D7
1N4148
GS1+
GS1-
D8
1N4148
GS2+
GS2-
GS ---- Gate Supply
PWM1L ---- Internal Net as PWM1 Left
PWM1R ---- Internal Net as PWM1 Right
U6
TLP250(F)
PWM1
DGND
R1
220R
NC
AN
CAT
NC
VCC
VO
VO
GND
GS1+
PWM1L
GS1-
C1
47uF
C3
100nF
D1
UF4007
U1
IR2103PBF
PWM1L
VCC
HIN
LIN#
COM
VB
HO
VS
LO
GPulse1
Load+
GPulse2
C2
10uF
U7
TLP250(F)
PWM2
DGND
R2
220R
GS1+
PWM1R
GS1-
C6
47uF
C4
100nF
D2
UF4007
U2
IR2103PBF
PWM1R
GPulse3
Cascade
GPulse4
C5
10uF
U8
TLP250(F)
PWM3
DGND
R3
220R
GS2+
PWM2L
GS2-
C9
47uF
C7
100nF
D3
UF4007
U3
IR2103PBF
PWM2L
GPulse8
Cascade
GPulse7
C8
10uF
U9
TLP250(F)
PWM4
DGND
R4
220R
GS2+
PWM2R
GS2-
C12
47uF
C10
100nF
D4
UF4007
U4
IR2103PBF
PWM2R
GPulse6
Load-
GPulse5
C11
10uF
TITLE:
Cascade H-Bridge Multilevel Inverter
REV: 1.0
EasyEDA
Company: EED UET Lahore
Sheet: 1/1
Date: 2021-06-18
Drawn By: Sajjad Ahmed