TE | comp | V | 2016
microprocessor
7/1/2024
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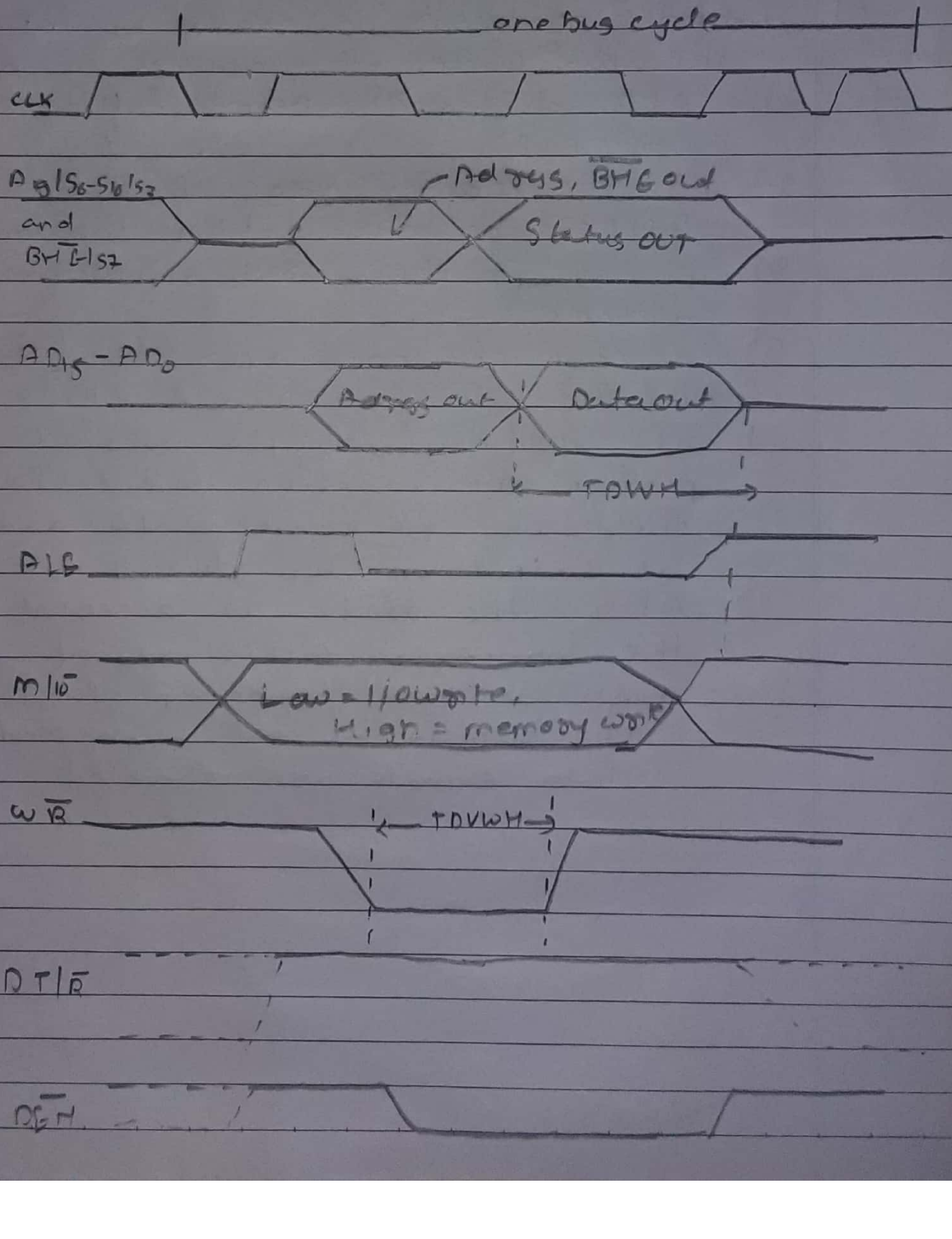
5057

Camlin Page 1

Q.3 A]



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Microprocessor
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Camlin Page 2

Q.3]
A]

1) When processor is ready to initiate the bus cycle, it applies a pulse to ALE during T1, Before falling edge of ALE
2) At the trailing edge of ALE, ICs 74LS373 or 8282 latches the adress
3) During T2 the address signal are disable
4) in case of input operation, RD is activated during T2 and AD° to AD15
5) if memory or I/O interface can perform the transfer immediately there are no wait states and data is output on bus during T3
6) After the data is accepted by the processor, RD is raised high at the beginning of T4 T4, WR is raised high and data signals are disabled

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Camlin Page 93

Q.3] B]

- model small
- stack 100H
- data

String db 'abba', '$'
String1 db 'String is palindrome', '$'
String2 db 'string is not palindrome', '$'

- code

main proc far
mov AX, @DATA
Mov DS, AX
CALL Palindrome
mov AH, 4CH
INT 21H
Palindrom proc
mov SI, offset string
loop1:
mov AX, [SI]
cmp AL, '$'
JE Label 1
INC SI
JMP LOOP1
label 1:
mov DI, offset string
DEC SI
loop2:
CMP SI, DI
JL Output1
mov AX, [SI]

Q.3]

B]

```
MOV BX, [DI]
CMP AL, BL
JNE output2
DEC SI
INC DI
JMP Loop2

output1:
    MOV AH, 09H
    INT 21H
    RET

output2:
    LEA DX, string2
    MOV AH, 09H
    INT 21H
    RET

Palindrome ENDP
END main
```