0701_R16_COMP_V_CSC501_MP/ PART-I-MCQ / University of Mumbai Online Examination 2021

*Required

0701_R16_COMP_V_CSC501_MP/ PART-I-MCQ / University of Mumbai Online Examination 2021

University of Mumbai Online Examinations 2021
Scheme: R2016/CBCGS
Year and Branch: TE/COMPUTER
Semester: V
Subject Code and Name : CSC501 Microprocessor
Time: 2 hour
Max Marks: 40
Please Note before you attempt the Examination:
1.The question paper will be of total 80 Marks and Two hours duration
2. Out of which 40 marks will be of 20 MCQs carrying two marks each
4.Students are supposed to submit MCQ responses with in 40 minutes, this link will be deactivated after 40 minutes
5.Remaining two questions carrying 20 marks each(Total 40 marks) will be of subjective/descriptive in nature
6. Use only registered mail id to attempt the examination
7. Keep your Hall ticket or College ID with you while appearing for the examination

---

For single step execution ..... flag is used. *   2 points

○ DF

○ OF

◉ TF

○ IF

Size of every location in instruction queue of 8086 microprocessor is .... bits *   2 points

○ 20

○ 32

○ 8

◉ 16

ALE signal from microprocessor 8086 in minimum mode is connected to ..... *   2 points

○ Clock generator

○ Transceivers

◉ Address Latches

○ Bus controller

Duty cycle of the clock required for microprocessor 8086 is ... *   2 points

○ 20 percent

○ 50 percent

○ 66 percent

◉ 33 percent

In maximum mode of 8086 DT/ R̅ signal is generated by ...... *   2 points

○ Transceivers

○ Address latches

◉ Bus controller

○ Microprocessor

In 8086 instruction DIV CL stores quotient at ..... * 2 points

○ CH

◉ AL

○ AH

○ CL

Addressing mode of SUB AL, BL is .... * 2 points

○ Direct

○ Register Indirect

○ Immediate

◉ Register

Which of the following is assembler directive? * 2 points

◉ SEGMENT

○ ADD

○ DIV

○ MUL

8086 Instruction CMP AL, BL uses ....operation * 2 points

○ Division

◉ Subtraction

○ Addition

○ Complement

How many hardware interrupt inputs are available on 8086 2 points
microprocessor? *

◉ 2

○ 1

○ 16

○ 8

Which of the following ICWs are compulsory in any situation while 2 points
programming 8259? *

○ ICW2 and ICW4

○ ICW1 and ICW3

◉ ICW1 and ICW2

○ ICW2 and ICW3

Address of last location of EPROM in 8086 based memory system is .... * 2 points

○ FFFFEH

○ 00000H

◉ FFFFFH

○ 0000H

Size of counters in 8253/8254 is .... *   2 points

- ⚪ 8 bits
- 🔘 16 bits
- ⚪ 20 bits
- ⚪ 32 bits

How many I/O modes can be programmed using 8255? *   2 points

- ⚪ 4
- ⚪ 3
- 🔘 2
- ⚪ 1

IC 8257 is .... *   2 points

- ⚪ Bus Controller
- 🔘 DMA Controller
- ⚪ Clock generator
- ⚪ Programmable Peripheral Interface

BSR mode of 8255 is applicable to *   2 points

- ⚪ Port A
- ⚪ Not applicable to ports
- 🔘 Port C
- ⚪ Port B

PE bit in Control Register of 80836 DX is used to enable .... *   2 points

- ⚪ Real address mode
- 🔘 Protected address mode
- ⚪ Paging
- ⚪ Not applicable to 80386 DX

How many segment registers are present in 80386 DX *   2 points

- ⚪ 8
- ⚪ 4
- 🔘 6
- ⚪ 5

Branch prediction is done in .... Stage of Integer pipeline of Pentium processor. *   2 points

- ⚪ PF
- ⚪ D2
- 🔘 D1
- ⚪ EX

In MESI protocol "M" stands for *   2 points

- ⚪ Modern

○ Modern

○ Main

◉ Modified

○ Master

Back   Submit