

Now we will start to calculate the dimensions of our transistors using hand calculation and the prior information given to us and we will also be using look up tables from matLab.

T₁ : First stage : Differential Amplifier

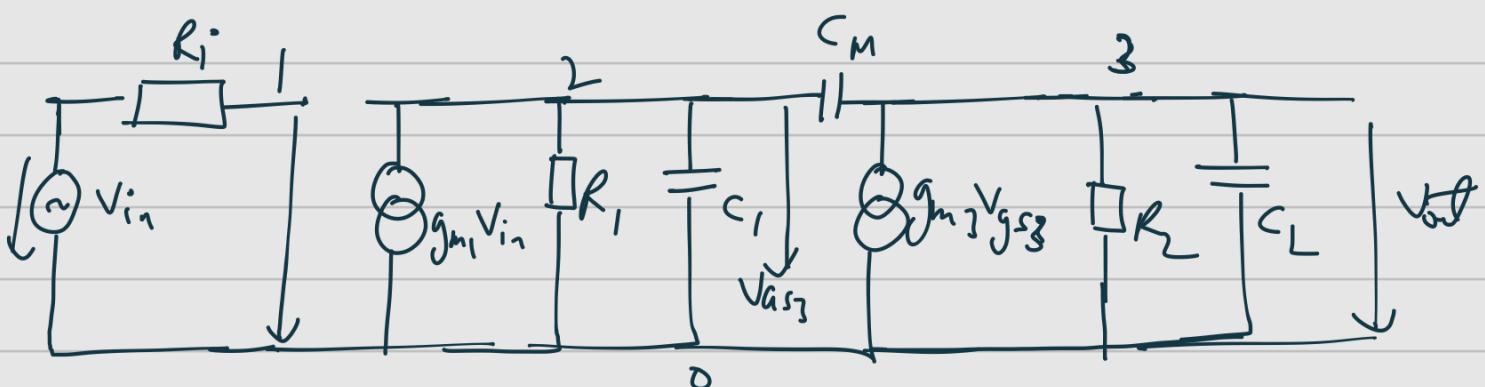
a) conditions given to us $Z_i > 10W_0$ & $|P_L| > 2.2W_0$

Hint

$$\frac{C_1}{C_M} \approx 0.3$$

The formula to calculate P_2 can be found by calculating poles and zeros of transfer function of our 2-stage amplifier which can either be calculated using mathematica or using hand calculation.

To begin with we need to draw small signal model of our 2-stage amplifier



R_1 & R_2 \rightarrow output resistance of the differential amplifier (first stage) and the output resistance of the inverter with current source load (second stage) respectively.
 C_1 & C_2 \rightarrow total parasitic capacitance at node N₁ & N₂

To get the gain per junction we need to calculate node voltages and use nodal analysis \rightarrow

At node 1

$$V_{in} = V_1 \quad \text{--- (1)}$$

At node 2

$$-g_{m1}V_{in} - \frac{V_2}{R_1} - V_2 sC_1 - (V_2 - V_3) sC_M = 0$$

At node 3

$$-g_{m3}V_{in} - \frac{V_3}{R_2} - V_3 sC_L - (V_3 - V_2) sC_M = 0$$

Solving these equations in mathematica and using dominant pole approximation we can get P_2 as

$$P_2 \approx \frac{-g_{m3}}{C_2 \left(1 + \frac{C_1}{C_M}\right)}$$

$$P_2 \approx \frac{-g_{m3}}{C_2 (1.3)}$$

Taking 5% margin as a safety design considerations

$$Z_1 \approx 5 \cdot 1.10\omega_0$$

$$P_2 \approx 5\% \cdot 2.2\omega_0$$

$$Z_1 = 0.5\omega_0$$

$$P_2 = 0.11\omega_0$$

$$\omega_0 = 2\pi \times 15\text{MHz}$$

$$\omega_0 = 30\pi\text{MHz}$$

$$Z_1 = 0.5 \times 30\pi \text{ MHz} \\ = 15\pi \text{ MHz}$$

$$Z_2 = 0.11 \times 30\pi \text{ MHz} \\ = 3.3\pi \text{ MHz}$$

$$\Rightarrow P_2 = \frac{-g_{mb}}{C_2(1.3)}$$

$$3.3\pi \text{ MHz} = \frac{-g_{mb}}{C_2(1.3)} \quad \text{--- (1)}$$

$$Z_1 = \frac{g_{mb}}{C_M}$$

$$15\pi \text{ MHz} = \frac{g_{mb}}{C_M} \quad \text{--- (2)}$$

$$\text{From eq } (1) = \text{eq } (2)$$

$$15\pi \text{ MHz } C_M = -4.296 C_2 \pi \text{ MHz}$$

$$C_M = -0.286 C_2$$

$$I_5 = C_M \times \text{slowRate}$$

$$C_M = -0.286 C_2$$

C_2 is the dominant contributor so,

$$C_2 = 3 \text{ pF}$$

$$C_M = 0.286 \times C_2 \\ = 0.286 \times 3 \text{ pF} \\ \boxed{C_M = 0.858 \text{ pF}}$$

$$I_5 = 0.858 \text{ pF} \times \frac{15 \text{ V}}{\text{ms}}$$

$$\boxed{\text{SR} = \frac{15 \text{ V}}{\text{ms}}}$$

$$\boxed{I_5 = 12.87 \mu\text{A}}$$

given in specification

$$\omega_V = A_{DC} \times \rho_1 \\ = A_{DC} \times \frac{1}{R_1 R_L g_{mb} C_M}$$

$$\boxed{\rho_1 = \frac{1}{R_1 R_L g_{mb} C_M}}$$

$$= \frac{g_{m1} g_{m2} R_1 R_2}{R_1 R_2 g_{m1} C_M}$$

$$\boxed{\omega_v = \frac{g_{m1}}{C_M}}$$

$$g_{m1} = \omega_v C_M$$

$$g_{m1} = 30\pi \text{MHz} \times 0.858 \mu\text{F}$$

$$g_{m1} = 80.8236 \times 10^{-6} \text{s}$$

$$I_D = \frac{I_S}{2}$$

$$\frac{g_m}{I_D} = \frac{80.8236 \times 10^{-6}}{6.435 \times 10^{-6}}$$

$$= 12.87 \text{mA}$$

$$= 6.435 \text{mA}$$

$$\boxed{\frac{g_m}{I_D} = 12.56}$$

Now with this $\frac{g_m}{I_D}$ we can use look up table

from matlab to get I_D (normalized) for our NMOS.

which comes out to be -

$$I_D (\text{normalized}) = 1.5672$$

$$\omega = \frac{I_D}{I_D (\text{normalized})} = \frac{6.435 \times 10^{-6}}{1.5672}$$

$$\boxed{\omega_{1,2} = 4.106 \mu\text{m}}$$

So width of each transistor T_1 and T_2 is approximately

4.106 μm

with length of 1μm

$$V_{CM,min} = V_{SS} + 1V \leq ICMR \leq V_{CM,max} = V_{DD} - 1V$$

$$V_{SS} + V_{CM} - V_{GS} - V_{DS5} = 0$$

$$V_{CM,min} = V_{SS} + 1V \quad V_{SS} = 0V$$

$$V_{CM,min} - 1V = 0$$

$$V_{CM,min} = 1V$$

$$0 + 1 - V_{GS} = V_{DS5}$$

$$V_{DS5} = 1 - V_{GS} \rightarrow \text{needs to be taken from Look-up table}$$

$$V_{DS5} = 1 - (0.64106 + 0.1)$$

$$\boxed{V_{DS5} = 0.25894V}$$

$$V_{DS} \geq \frac{2}{\frac{g_m}{I_D}}$$

$$\left(\frac{g_m}{I_{D5}} \right) = \frac{2}{0.25894}$$

$$\boxed{\left(\frac{g_m}{I_{D5}} \right) = 7.723}$$

$$(I_D)_{normalised} = 2.4045$$

$$\boxed{W_5 = \frac{12.87 \mu A}{2.4045} = 5.352 \mu m}$$

$$\boxed{(W) = 5.352 \mu m = 2.67}$$

$$L' = 2 \times 10^{-6} \text{ m}$$

$$V_{CM, max} = V_{DD} - 1V$$

Given $V_{D1} = V_{D3} = V_{GS}$

$$\begin{aligned} V_{CM, max} &= 3.3 - 1 \\ &= 2.3V \end{aligned}$$

$$V_{DD} - V_{GS3} - V_{DS1} - V_{DS5} = 0$$

$$\begin{aligned} V_{DS5} &= V_{CMmax} - V_{GS1} \\ &= 2.3 - (0.6410 + 0.1) \\ V_{DS5} &= 1.559V \end{aligned}$$

$$V_{DS1} \geq \frac{2}{\left(\frac{g_m}{I_D}\right)_1}$$

$$V_{DS1} = \frac{2}{12.56}$$

$$V_{DS1} = 0.159V$$

Then,

$$\begin{aligned} V_{GS} &= V_{DS1} + V_{DS5} \\ &= 0.159 + 1.559 \\ &= 1.718V \end{aligned}$$

$$\begin{aligned} V_{GS3} &= V_{DD} - V_{GS} \\ &= 3.3 - 1.718 \\ &= 1.582V \end{aligned}$$

$$V_{DS1} = V_{GS3} \geq \frac{2}{\left(\frac{g_m}{I_D}\right)_1} \Rightarrow \left(\frac{g_m}{I_D}\right)_1 = 1.317$$

as this $\frac{g_m}{I_D}$ is left for our transistor

to be deleted in saturation

region hence we will take
 approx $\left(\frac{g_m}{I_D}\right)_s = 4$

$$I_D (\text{normalised}) = 1.9253$$

$$\omega_j = \frac{6.435 \times 10^{-6}}{1.9253} = 3.34 \text{ rad/s}$$

$$\left(\frac{\omega}{L}\right)_s = \left(\frac{3.34}{2}\right) = 1.67$$

Now we need to find the widths of our second stage transistors

$$P_2 = \frac{-g_{m6}}{C_2 \left(1 + \frac{C_1}{C_M}\right)}$$

$$\text{Phase margin} = 60^\circ$$

$$P_2 = 2.2 \omega_0$$

$$\omega_0 = \frac{g_{m1} g_{m6} R_L R_C}{R_C R_L g_{m6} C_M}$$

$$P_2 = 2.2 \frac{g_{m1}}{C_M}$$

$$\frac{g_{m6}}{C_2 \left(1 + \frac{C_1}{C_M}\right)} = \frac{2.2 g_{m1}}{0.286 \times 10^{-12} \times C_L}$$

$$g_{m6} = \frac{2.2 g_{m1} \times 1.3}{0.286}$$

$$\boxed{g_{m6} = 10 g_{m1}}$$

$$V_{GS3} = V_{DS3} = V_{DS4} = V_{GS6}$$

$$g_m = \frac{2I_{ref}}{V_{Aref}}$$

since V_{Aref} is same so

$$\left(\frac{g_m}{I_D}\right)_S = \left(\frac{g_m}{I_D}\right)_6$$

$$g_{m6} = 10 \times g_{m1}$$

$$= 10 \times 80.82 \times 10^{-5}$$

$$= 80.82 \times 10^{-5} \text{ S}$$

$$\left(\frac{g_m}{I_D}\right)_S = 4$$

$$I_{D6} = \frac{1}{\left(\frac{g_m}{I_D}\right)_S} g_{m6}$$

$$= 202 \mu A$$

$$\left(\frac{g_m}{I_D}\right)_6 = \left(\frac{g_m}{I_D}\right)_S = 4 \quad L = 1 \mu m$$

$$I_D = 202 \mu A$$

$$I_D (\text{normalised}) \text{ from look up table} = 3.812 \frac{\mu A}{\mu m}$$

$$W = \frac{202 \times 10^{-6}}{3.8122} = 52.9 \mu m$$

$$\left(\frac{W}{L}\right)_6 = 52.9$$

$$I_{D_1} = I_{D_4} = \frac{I_{D_5}}{2} \quad \text{and} \quad I_6 = I_7$$

Since M_5 & M_7 have same gate source voltages

$$\frac{T}{T} = (\omega)$$

$$\frac{I_{D5}}{I_{D7}} = \frac{\left(\frac{w}{L}\right)_5}{\left(\frac{w}{L}\right)_7}$$

$$\left(\frac{w}{L}\right)_7 = \left(\frac{w}{L}\right)_5 \times \frac{I_{D7}}{I_{D5}}$$

$$= 2.67 \times \frac{20L}{2 \times 6.435}$$

$$\left(\frac{w}{L}\right)_7 = 41$$

$$W_7 = 41 \times 2 = 82 \mu m$$

In a 2-stage amplifier the input referred offset voltage is determined by 2 transistor pairs

(i) Input Differential pair (T_1 & T_2)

(ii) Current mirror pairs (T_3 & T_4)

It is due to the mismatches between 2 CMOS identical transistors could be characterized by the random variations of difference in

a) threshold voltage (V_{T0})

b) Body factor (γ)

Standard deviation of the offset voltage

$$\sigma^2(V_{DS}) = \sigma^2(T_{D1}) + \sigma\left(\frac{T_{D2}}{A_{in}}\right)^2 - (1)$$

$$A_{in} = \frac{g_{m1}}{g_{m2}} = \sqrt{\frac{W_1 \times L_1}{W_2}}$$

Given in specs

$$= \sqrt{\frac{4.106 \times 2}{3.34}} \\ = 1.568$$

$A_{V_{T01}} = 6.18$
 $A_{V_{T02}} = 4.632$

$$\sigma^2(V_{T01}) = A_{V_{T01}}^2 = (6.18)^2 = 37.74$$

$$\sigma^L(V_{T_{02}}) = \frac{A_V^L T_{on}}{W_2 L_2} = \frac{(6.18)^2}{4.106 \times 1} = 9.301$$

putting these values in eqn(1)

$$\sigma(V_{os}) = \sqrt{9.301 + \frac{9.301}{1.568}} \\ = 3.617 \text{ mV}$$

which is not within the specifications so we need to change the dimensions of L_1 & L_2

$$W_1 = 2 \text{ mm} \quad W_2 = 6 \text{ mm}, L_2 = 3 \text{ mm} \\ W_1 = 10 \text{ mm}$$

$$A_{in} = \sqrt{\left(\frac{W_1}{L_1}\right) \times \left(\frac{L_2}{W_2}\right)} \\ = \sqrt{\frac{10}{2} \times \frac{3}{6}} = 1.730$$

$$\sigma^L(V_{T_{01}}) = \frac{(6.18)^2}{20} = 1.90$$

$$\sigma^L(V_{T_{02}}) = \frac{(6.18)^2}{18} = 2.121$$

$$\sqrt{1.90 + \frac{2.121}{(1.730)^2}}$$

$\sigma(V_{os}) = 1.615 \text{ mV} \leq 1.66 \text{ mV}$ as given in specification sheet
and Now we will add more margin to our transistors dimensions to reduce offsets or to reduce issues due to process variations

so the new dimensions will be

		W (μm)	L (μm)
M ₁	-	1.68	1
M ₂	-	1.68	1
M ₃	-	9.79	2.82
M ₄	-	9.79	2.82
M ₅	-	5.35	2
M ₆	-	7.24	2
M ₇	-	52.9	1
M ₈	-	84	2

Putting these values in Cadence and running simulations to get the values as per specifications will show us that we have issues with offset, phase margin and slew rate so to deal with issue steps mentioned needs to be followed -